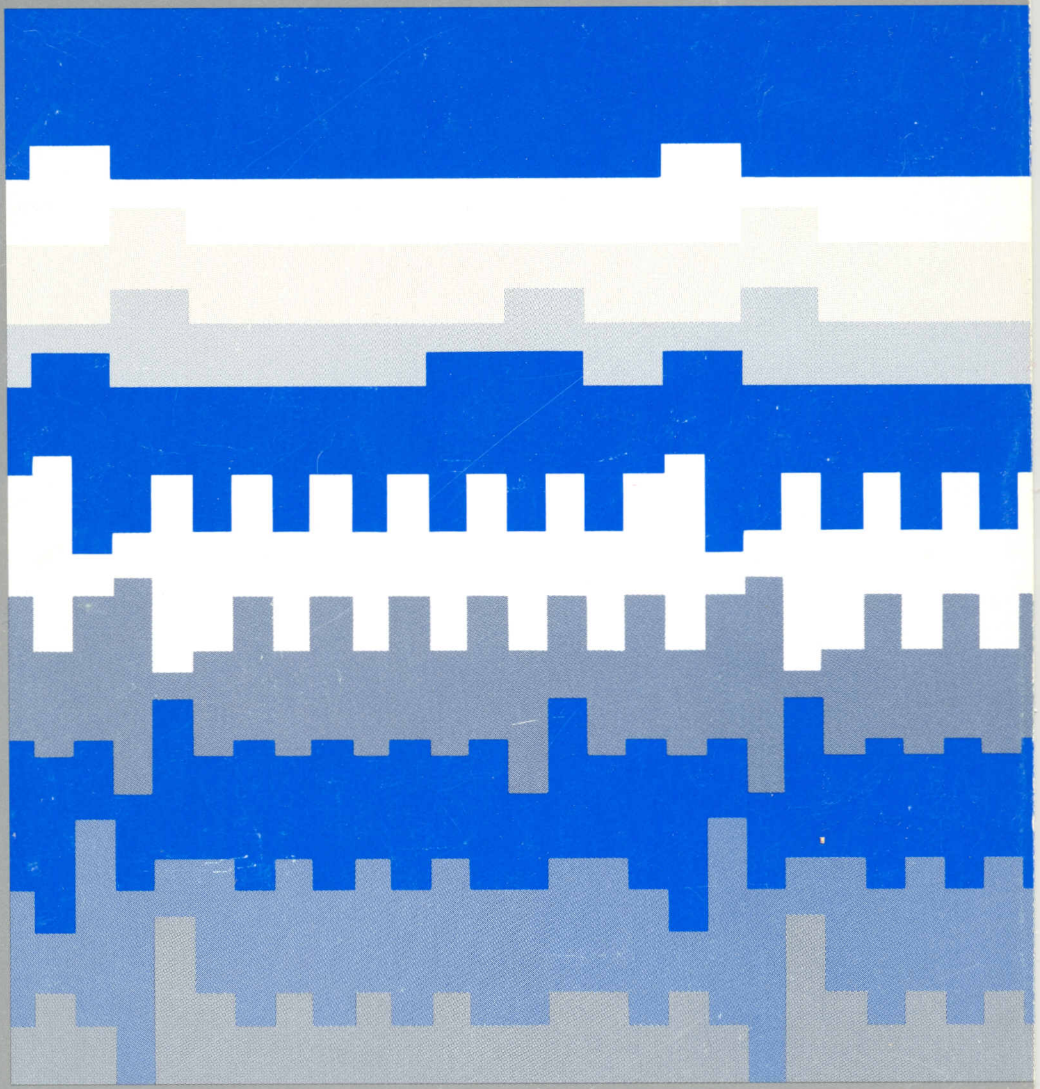
HITACHI®

LCD CONTROLLER/DRIVER LSI DATA BOOK



LCD CONTROLLER/DRIVER LSI DATA BOOK

HITACHI®

M24T026

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Contents

General Information

Quick Reference Guide

Type		Extension Driver			
Type Number		HD44100R	HD66100F	HD61100A	HD61200
Power supply for internal circuits (V)		2.7 to 5.5	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5
Power supply for LCD driver circuits (V)		13	6	17	17
Power dissipation (mW)		5	5	5	5
Operating temperature (°C)		–20 to +75*1	–20 to +75*1	–20 to +75*1	–20 to +75
Memory	ROM (bit)	—	—	—	—
	RAM (bit)	—	—	—	—
LCD driver	Common	20	—	—	—
	Column	40 (20)	80	80	80
Instruction set		—	—	—	—
Operation frequency (MHz)		0.4	1	2.5	2.5
Duty		Static–1/33	Static–1/16	Static–1/100	1/32–1/128
Package		FP-60A Chip	FP-100	FP-100	FP-100

Type		Column Driver					
Type Number		HD66204	HD66214T	HD66224T	HD66106	HD66107T	HD66110RT
Power supply for internal circuits (V)		2.7 to 5.5	2.7 to 5.5	2.5 to 5.5	4.5 to 5.5	4.5 to 5.5	2.7 to 5.5
Power supply for LCD driver circuits (V)		28	28	28	37	37	40
Power dissipation (mW)		15	15	15	15	25	25
Operating temperature (°C)		–20 to +75*1	–20 to +75	–20 to +75	–20 to +75	–20 to +75	–20 to +75
Memory	ROM (bit)	—	—	—	—	—	—
	RAM (bit)	—	—	—	—	—	—
LCD driver	Common	—	—	—	—	—	—
	Column	80	80	80	80	160	160
Instruction set		—	—	—	—	—	—
Operation frequency (MHz)		8	8	8 MHz at 5 V 6.5 MHz at 3 V	6	8	12 MHz at 5 V 10 MHz at 3 V
Duty		1/64–1/240	1/64–1/240	1/64–1/240	1/100–1/480	1/100–1/480	1/100–1/480
Package		FP-100 TFP100 Chip	TCP	SLIM-TCP	FP-100 TFP100 Chip	TCP	SLIM-TCP

*1 –40 to +80°C (special request). Please contact Hitachi agents.
*2 Under development

Quick Reference Guide

Type		Column Drive (within RAM)				TFT Column Driver		
Type Number		**HD44102CH**	**HD61102**	**HD61202**	**HD66108T**	**HD66300T**	**HD66310T**	**HD66330T**
Power supply for internal circuits (V)		4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	2.7 to 5.5	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5
Power supply for LCD driver circuits (V)		11	15.5	17	15	15	23	5
Power dissipation (mW)		5	5	5	5	160	100	100
Operating temperature (°C)		–20 to +75*1	–20 to +75	–20 to +75*1	–20 to +75	–20 to +75	–20 to +75*3 (–20 to +60)	–20 to +75
Memory	ROM (bit)	—	—	—	—	—	—	—
	RAM (bit)	200 × 8	512 × 8	512 × 8	165 × 65	—	—	—
LCD driver	Common	—	—	—	0–65	—	—	—
	Column	50	64	64	100–165	120	160	192
Instruction set		6	7	7	7	—	—	—
Operation frequency (MHz)		0.28	0.4	0.4	4	4.8	12/15	28
Duty		Static–1/32	Static–1/64	1/32–1/128	1/32, 1/34, 1/36, 1/48, 1/50, 1/64, 1/66	—	—	—
Package		FP-80 Chip	FP-100	FP-100 TFP-100 Chip	TCP	TCP	TCP	SLIM-TCP

Type		Segment Display			
Type Number		**HD61602**	**HD61603**	**HD61604**	**HD61605**
Power supply for internal circuits (V)		2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5
Power supply for LCD driver circuits (V)		5	5	5	5
Power dissipation (mW)		0.5	0.5	0.5	0.5
Operating temperature (°C)		–20 to +75*1	–20 to +75*1	–20 to +75*1	–20 to +75*1
Memory	ROM (bit)	—	—	—	—
	RAM (bit)	204	64	204	64
LCD driver	Common	4	1	4	1
	Column	51	64	51	64
Instruction set		4	4	4	4
Operation frequency (MHz)		0.52	0.52	0.52	0.52
Duty		Static, 1/2, 1/3, 1/4	Static	Static, 1/2, 1/3, 1/4	Static
Package		FP-80 FP80A	FP-80	FP-80	FP-80

*1 –40 to +80°C (special request). Please contact Hitachi agents.
*2 Under development
*3 –20 to +75°C in 12 MHz version, –20 to +65°C in 15 MHz version

Type		Common Driver						
Type Number		HD44103CH	HD44105H	HD61103A	HD61203	HD66205	HD66215T	HD66115T
Power supply for internal circuits (V)		4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	2.7 to 5.5	2.5 to 5.5	2.5 to 5.5
Power supply for LCD driver circuits (V)		11	11	17	17	28	28	40
Power dissipation (mW)		4.4	4.4	5	5	5	5	5
Operating temperature (°C)		–20 to +75*1	–20 to +75*1	–20 to +75*1	–20 to +75*1	–20 to +75*1	–20 to +75	–20 to +75
Memory	ROM (bit)	—	—	—	—	—	—	—
	RAM (bit)	—	—	—	—	—	—	—
LCD driver	Common	20	32	64	64	80	100/101	160 (80 + 80)
	Column	—	—	—	—	—	—	—
Instruction set		—	—	—	—	—	—	—
Operation frequency (MHz)		1	1	2.5	2.5	0.1	0.1	2.5
Duty		1/8, 1/12, 1/16, 1/24, 1/32	1/8, 1/12, 1/32, 1/48	Static–1/10, 1/64	1/32–1/64	1/64–1/240	1/64–1/240	1/100–1/480
Package		FP-60	FP-60 Chip	FP-100	FP-100 TFP100 Chip	FP-100 TFP100 Chip	SLIM-TCP	SLIM-TCP

Type		Character Display Controller				
Type Number		HD43160AH	HD44780U (LCD-II)	HD66702R (LCD-II/E20)	HD66710 (LCD-II/F8)	HD66712*2 (LCD-II/F12)
Power supply for internal circuits (V)		4.5 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5
Power supply for LCD driver circuits (V)		—	11	7	13	13
Power dissipation (mW)		10	2	2	2	2
Operating temperature (°C)		–20 to +75	–20 to +75*1	–20 to +75*1	–20 to +75*1	–20 to +75
Memory	ROM (bit)	6420	9920	7200	9600	9600
	RAM (bit)	80 × 8	80 × 8, 64 × 8	80 × 8, 64 × 8	80 × 8, 64 × 8, 8 × 8	80 × 8, 64 × 8 8 × 8
LCD driver	Common	—	16	16	33	33
	Column	—	40	100	40	60
Instruction set		6	11	11	11	11
Operation frequency (MHz)		0.25/0.375	0.25	0.25	0.25	0.25
Duty		1/8, 1/12, 1/16	1/8, 1/11, 1/16	1/8, 1/11, 1/16	1/17, 1/33	1/17, 1/33B
Package		FP-54	FP-80B TFP-80 Chip	FP-144A Chip	FP-100A TFP-100 Chip	TCP

*1 –40 to +80°C (special request). Please contact Hitachi agents.
*2 Under development

Quick Reference Guide

Type		Graphic Display Controller		
Type Number		HD61830 LCDC	HD61830B LCDC	HD63645F HD64645F HD64646FS LCTC
Power supply for internal circuits (V)		4.5 to 5.5	4.5 to 5.5	4.5 to 5.5
Power supply for LCD driver circuits (V)		—	—	—
Power dissipation (mW)		30	50	50
Operating temperature (°C)		–20 to +75	–20 to +75*1	–20 to +75
Memory	ROM (bit)	7360	7360	—
	RAM (bit)	—	—	—
LCD driver	Common	—	—	—
	Column	—	—	—
Instruction set		12	12	15
Operation frequency (MHz)		1.1	2.4	10
Duty		Static–1/128	Static–1/128	Static–1/512
Package		FP-60	FP-60	FP-80 FP-80B

*1 –40 to +80°C (special request). Please contact Hitachi agents.
*2 Under development

Type		Low-Power LCD Chipset	
Type Number		HD66503	HD66520
Power supply for internal circuits (V)		2.7–5.5	2.7–5.5
LCD driver circuits (V)		28	28
Power dissipation (mW)		0.5	0.5
Operating temperature (°C)		–20° to +75°	–20° to +75°
Memory	ROM (bit)		
	RAM (bit)		76800
LCD driver	Common	240	—
	Column	—	160
Operation frequency (MHz)		65 KHz	65 KHz
Duty		1/120, 1/240	1/120, 1/240
Package		TCP	TCP

Type Number Order

Sorted by Type Name

Type	Function	Reference Page
HD43160AH	LCD controller	199
HD44100RFS	40-channel LCD driver	151
HD44102CH	50-channel column driver within RAM	489
HD44103CH	20-channel common driver	511
HD44105H	32-channel common driver	519
HD44780UA00FS/00TF/01FS/ 02FS/UB**FS/TF LCD-II	LCD controller/driver (8 × 2 character)	214
HD61100A	80-channel column driver	174
HD61102RH	64-channel column driver within RAM	528
HD61103A	64-channel common driver	556
HD61200	80-channel column driver	186
HD61202/TFIA	64-channel column driver within RAM	580
HD61203/TFIA	64-channel common driver	612
HD61602R/RH	Segment display type LCD driver	841
HD61603R	Segment display type LCD driver	841
HD61604R	Segment display type LCD driver	871
HD61605R	Segment display type LCD driver	871
HD61830A00H LCDC	LCD controller	898
HD61830B00H LCDC	LCD controller	898
HD63645F LCTC	LCD timing controller (68 family)	934
HD64645F LCTC	LCD timing controller (80 family)	934
HD64646FS LCTC	LCD timing controller (80 family)	934
HD66100F/FH	80-channel LCD driver	161
HD66106FS	80-channel column/common driver	772
HD66107T00/01/11/12/24/25	160-channel column/common driver	787
HD66108T00	165-channel graphic LCD controller/driver	638
HD66110RTA8/RTB0/RTB1/TA4	160-channel column driver	807
HD66115TA0/1	160-channel common driver	824
HD66204F/FL/TF/TFL	80-channel column driver	691
HD66205F/FL/TF/TFL/TA1/TA2/ TA3/TA6/TA7/TA9L	80-channel common driver	706
HD66214TA1/2/3/6/9L	80-channel column driver	722
HD66215TA0/1/2	100-channel common driver	751
HD66224TA1/TA2/TB0	80-channel column driver	737
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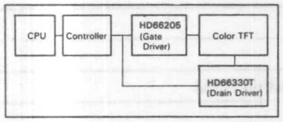
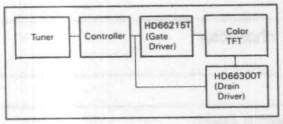
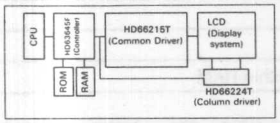
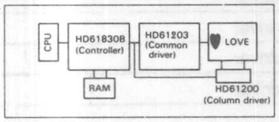
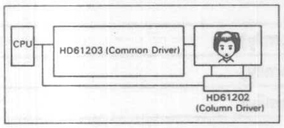
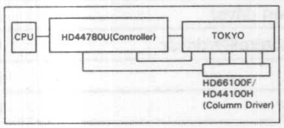
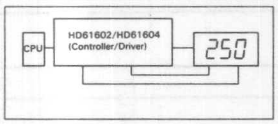
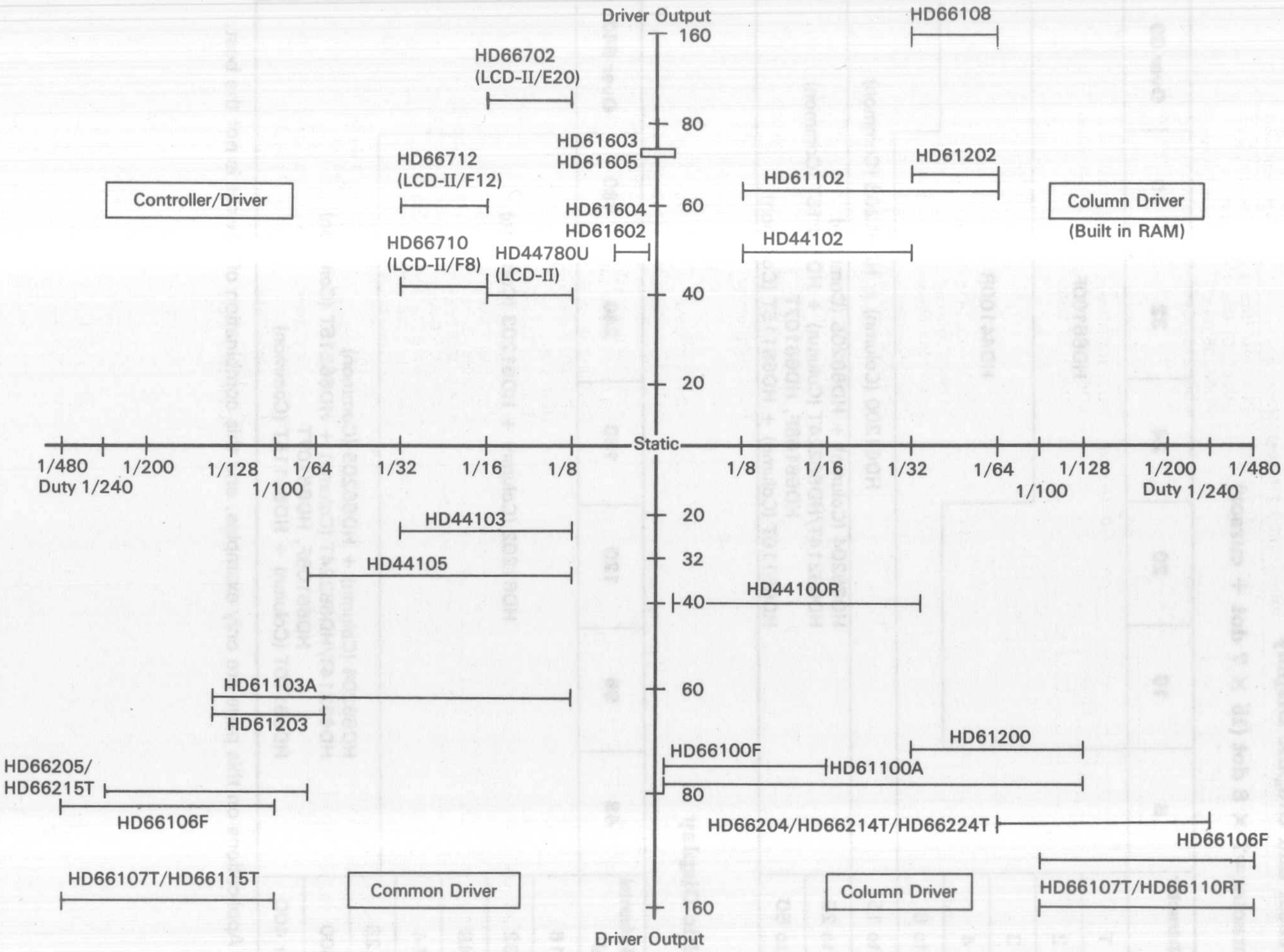
HD66310T00/T0015	160-channel TFT digital column driver (8 gray scale)	1088
HD66330TA0	192-channel TFT digital column driver (64 gray scale)	1108
HD66503	240-channel row driver with internal LCD timing circuit	979
HD66520	160-channel 4-level grayscale display column with internal bit-map RAM	996
HD66702RA00F/00FL/01F/02F/ RB**F/FL LCD-II/E20	LCD controller/driver (20 × 2 character)	273
HD66710***F8 LCD-II/F8	LCD controller/driver (8 × 4 character)	334
HD66712 LCD-II/F12	LCD controller/driver (12 × 4 character)	411

Selection Guide

Hitachi LCD Driver System

Type	Reference Figure	Screen Size (max)	Lineup	Application
TFT Full Color System		(800×3)×520 dots	HD66310T(Drain) HD66330T(Drain) HD66205(Gate) HD66215T(Gate)	Personal Computer Terminal Workstation Navigation System
Color LCD-TV System		720×480 dots	HD66300T(Drain) HD66205(Gate) HD66215T(Gate)	LCD-TV Portable Video
Display System for CRT Compatible		640×400 dots	HD63645/64645/64646(Controller) HD66204(Column)/66205(Common) HD66224T(Column)/HD66215T(Common) HD66106F(Driver)	Personal Computer, Wordprocessor, Terminal
Graphic Display System		Character 80×16 Graphic 480×128 dots	HD61100A(Column), HD61830B(Controller) HD61200(Column) HD61103A(Common), HD61203(Common)	Laptop Computer, Facsimile, Telex, Copy machine
Graphic Display System (Bitmap)		480×128 dots	HD44102(Column)/61102(Column) HD44103(Common) HD61202(Column) HD44105(Common)/61103A(Common) HD61203(Common) HD66108 (Column)/Common)	Laptop Computer, Handy Wordprocessor, Toy
Character Display System		40 Characters ×2 Columns 80 Characters ×1 Column	HD44780U(LCD-II) (Controller/Driver) (Controller/Driver) HD44100R(Column) HD66100F(Column) HD66702(LCD-II/E20) HD66710(LCD-II/F8) HD66712(LCD-II/F12)	Electrical Typewriter, Multifunction Telephone, Handy Terminal
Segment Display System		25 Digits ×1 Column	HD61602 (Controller/Driver) HD61604 (Controller/Driver) HD61603 (Controller/Driver) HD61605 (Controller/Driver)	ECR, Measurement System, Telephone Industrial Measurement System


Driver Output
160
80
60
40
20
Static
20
32
40
60
80
160
Driver Output
1/480
Duty 1/240
1/200
1/128
1/100
1/64
1/32
1/16
1/8
1/8
1/16
1/32
1/64
1/128
1/100
1/200
Duty 1/240
1/480
Controller/Driver
HD66702
(LCD-II/E20)
HD61603
HD61605
HD66712
(LCD-II/F12)
HD61604
HD61602
HD66710
(LCD-II/F8)
HD44780U
(LCD-II)
Column Driver
(Built in RAM)
HD66108
HD61202
HD61102
HD44102
HD44103
HD44105
HD44100R
HD61103A
HD61203
HD66205/
HD66215T
HD66106F
HD66107T/HD66115T
Common Driver
HD61200
HD66100F
HD61100A
HD66204/HD66214T/HD66224T
HD66106F
HD66107T/HD66110RT
Column Driver

Application

Character and Graphic Display

1 character=7 × 8 dot (15 × 7 dot + cursor)

Line \ Character	8	16	20	24	32	40	Over 80
1					HD66100F		
2							
3					HD44100R		
4							
6 to 8							
12 to 15					HD61200 (Column) + HD61203 (Common)		
16 to 25					HD66204 (Column) + HD66205 (Common) HD66214T/HD66224T (Column) + HD66215T (Common) HD66106F, HD66107T HD66110T (Column) + HD66115T (Common)		
26 to 50							

Graphic Display

Vertical \ Horizontal	48	96	120	180	240	480	Over 640
16							
32				HD61202 (Column) + HD61203 (Common)			
48							
64							
128							
400			HD66204 (Column) + HD66205 (Common) HD66214T/HD66224T (Column) + HD66215T (Common) HD66106F, HD66107T HD66110T (Column) + HD66115T (Common)				
Over 400							

Note: Applications on this page are only examples, and this combination of devices is not the best.

Differences Between Products

1. HD66100F and HD44100R

	HD66100F	HD44100H
LCD drive circuits	80	20×2
Power supply for internal logic (V)	3 to 6	3 to 13
Display duty	Static to 1/16	Static to 1/33
Package	100 pin plastic QFP	60 pin plastic QFP

2. HD61100A and HD61200

		HD61100A	HD61200
LCD drive circuits	common	–	–
	column	80	80
Display duty		static to 1/128	1/32 to 1/128
Power supply for LCD drive circuits (V)		0 to 17	8 to 17
Power supply limits of LCD driver circuit voltage		V_{CC} to V_{EE} (no limit)	shown in figures below

Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L, and V4R) when load current flows through one of the terminals Y_1 to Y_{80} is specified under the following conditions:
$V_{CC}-V_{EE}=17V$
$V1L=V1R$, $V3L=V3R=V_{CC}-2/7\ (V_{CC}-V_{EE})$
$V2L=V2R$, $V4L=V4R=V_{EE}+2/7\ (V_{CC}-V_{EE})$

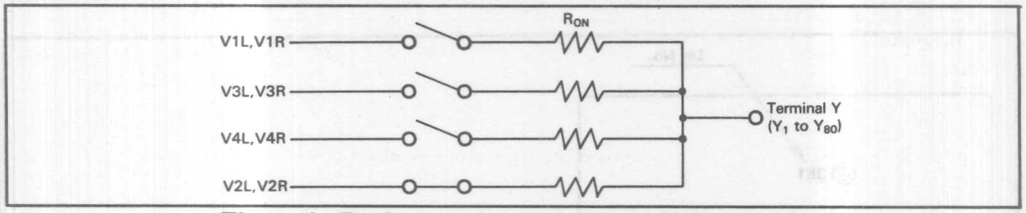


Figure 1 Resistance between Y ard V Terminals

The following is a description of the range of power supply voltage for liquid crystal display drives. Apply positive voltage to V1L=V1R and V3L=V3R and negative voltage to V2L=V2R and V4L=V4R within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice the ΔV depends on power supply voltage $V_{CC}-V_{EE}$.

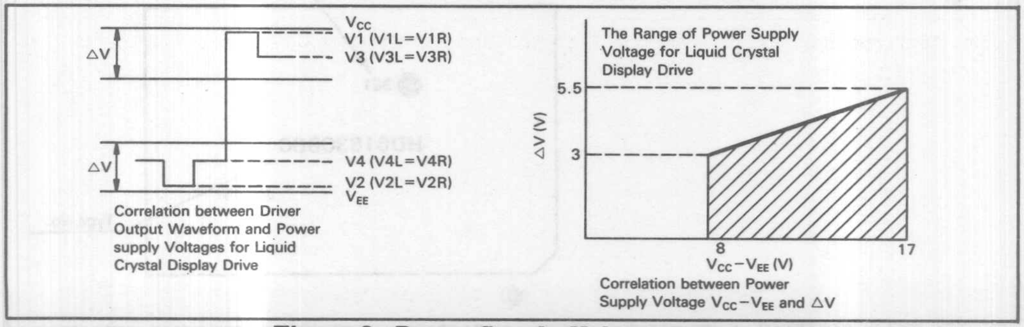


Figure 2 Power Supply Voltage Range

3. HD66100F and HD61100A

		HD66100F	HD61100A
LCD driver circuits	common	–	–
	column	80	80
Power supply for LCD drive circuits (V)		3 to 6	5.5 to 17.0
Display duty		static to 1/16	static to 1/128
Operating frequency (MHz)		1.0 MHz (max)	2.5 MHz (max)
Data fetch method		Shift	Latch
Package		100 pin Plastic QFP (FP-100)	100 pin plastic QFP (FP-100)

4. HD61830 and HD61830B

	HD61830	HD61830B
Oscillator	Internal	External
Operating frequency (MHz)	1.1 MHz	2.4 MHz
Display duty	static to 1/128	static to 1/128
Programmable screen size (Max)	64×240 dots (1/64 duty)	128×480 dots (1/64 duty)
Other	pin 6:C pin 7:R pin 9:CPO	pin 6:$\overline{CE}$ pin 7:$\overline{OE}$ pin 9:NC
Package Marking	Ⓐ	Ⓑ

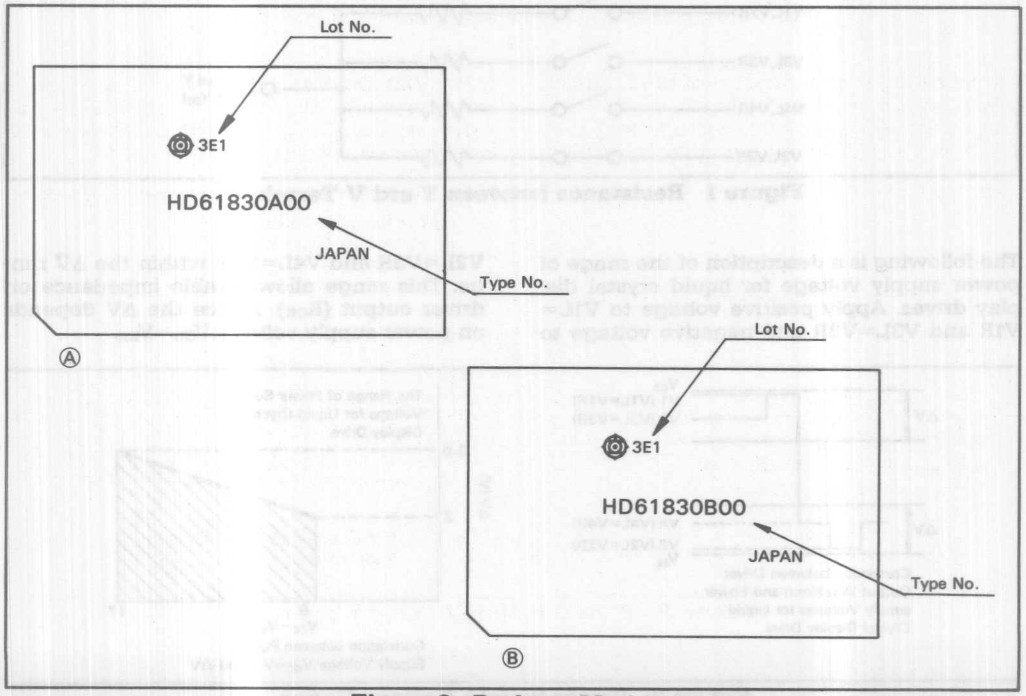


Figure 3 Package Marking

5. HD61102 and HD61202

	HD61102	HD61202
Display duty	static to 1/64	1/32 to 1/64
Recommended voltage between V_{CC} and V_{EE} (V)	4.5 to 15.5	8 to 17
Power supply limits of LCD driver circuits voltage	V_{CC} to V_{EE} (no limit)	shown in following figures
Pin 88	DY (output)	NC (no connection)
Absolute maximum rating of V_{EE} (V)	$V_{CC}-17.0$ to $V_{CC}+0.3$	$V_{CC}-19.0$ to $V_{CC}+0.3$

Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L and V4R) when load current flows through one of the terminals Y_1 to Y_{64} is specified under the following conditions:

$V_{CC}-V_{EE}=15V$
$V1L=V1R,\ V3L=V3R=V_{CC}-2/7\ (V_{CC}-V_{EE})$
$V2L=V2R,\ V4L=V4R=V_{EE}+2/7\ (V_{CC}-V_{EE})$

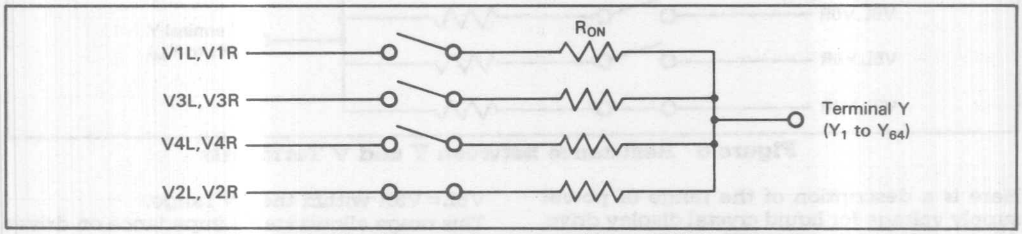


Figure 4 Resistance between Y and V Terminals

The following is a description of the range of power supply voltage for liquid crystal display drives. Apply positive voltage to V1L=V1R and V3L=V3R and negative voltage to V2L=V2R and V4L=V4R within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC}-V_{EE}$.

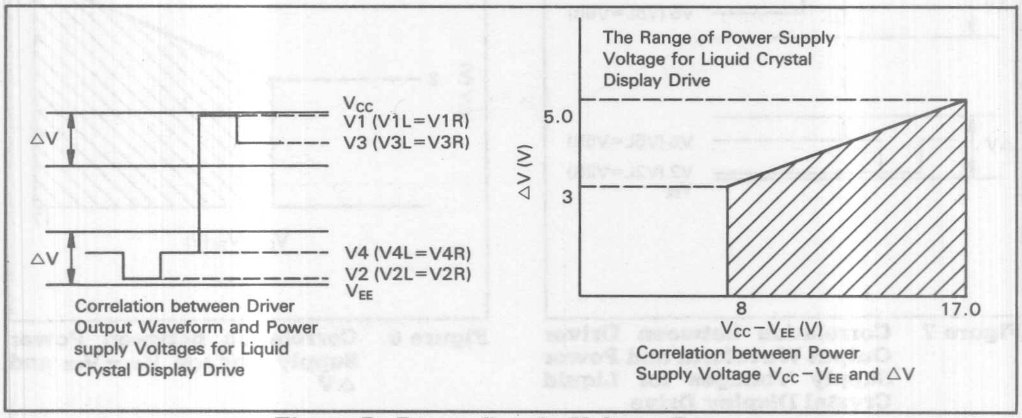


Figure 5 Power Supply Voltage Range

6. HD61103A and HD61203

	HD61103A	HD61203
Recommended voltage between V_{CC} and V_{EE} (V)	4.5 to 17	8 to 17
Power supply limits of LCD drive circuits voltage	V_{CC} to V_{EE} (no limit)	shown in figures below
Output terminal	shown in following figure 4	shown in following figure 5

Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R) when load current flows through one of the terminals X1 to X64. This value is specified under the following conditions:

$V_{CC}-V_{EE}=17V$
$V1L=V1R$, $V6L=V6R=V_{CC}-1/7\ (V_{CC}-V_{EE})$
$V2L=V2R$, $V5L=V5R=V_{EE}+1/7\ (V_{CC}-V_{EE})$

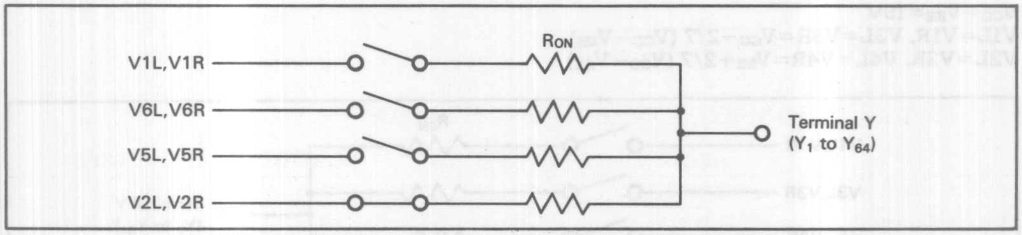


Figure 6 Resistance between Y and V Terminals

Here is a description of the range of power supply voltage for liquid crystal display drive. Apply postive voltage to V1L=V1R and V6L=V6R and negative voltage to V2L=V2R and V5L=V5R within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC}-V_{EE}$.

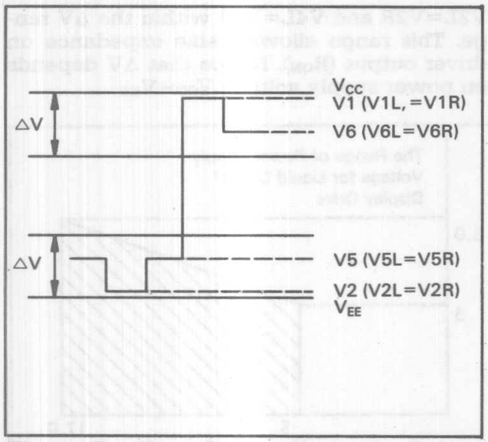


Figure 7 Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive

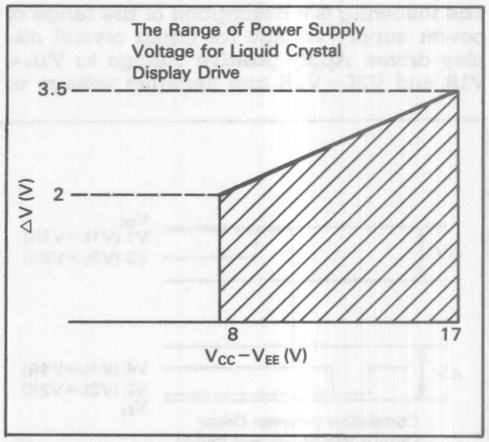


Figure 8 Correlation between Power Supply Voltage $V_{CC}-V_{EE}$ and ΔV

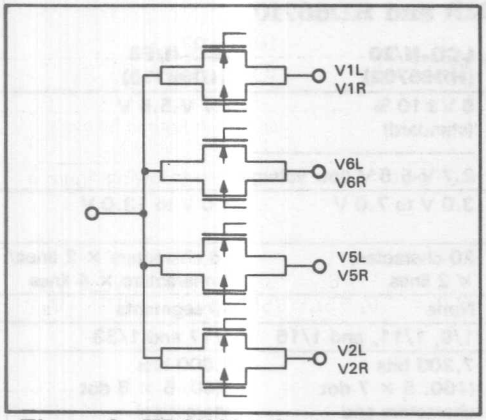


Figure 9 HD61103A Output Terminal

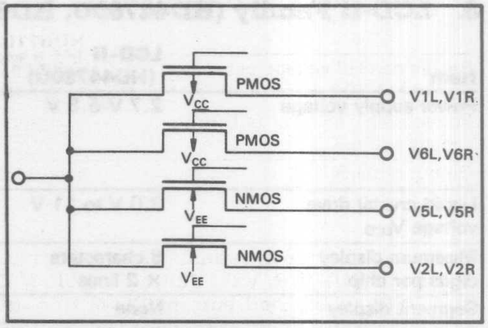


Figure 10 HD61203 Output Termiral

7. HD61602, HD61603, HD61604, and HD61605

		HD61602	HD61603	HD61604	HD61605
Power supply (V_{DD})		2.2~5.5V	2.2~5.5V	4.5~5.5V	4.5~5.5V
Instruction word		8 bits × 2	4 bits × 4	8 bits × 2	4 bits × 4
LCD power supply circuit		Yes	–	–	–
Segment terminals		51	64	51	64
Display size frame frequency (fosc = 100 kHz)	Static	6 digits + 3 marks 33Hz	8 digits 33Hz	6 digits + 3 marks 98Hz	8 digits 98Hz
	1/2 duty	12 digits + 6 marks 65Hz	–	12 digits + 6 marks 195Hz	–
	1/3 duty	17 digits 208Hz	–	17 digits 521Hz	–
	1/4 duty	25 digits + 4 marks 223Hz	–	25 digits + 4 marks 781Hz	–

8. LCD-II Family (HD44780U, HD66702R and HD66710)

Item	LCD-II (HD44780U)	LCD-II/20 (HD66702)	LCD-II/F8 (HD66710)
Power supply voltage	2.7 V-5.5 V	5 V±10 % (standard) 2.7 V-5.5 V (low voltage)	2.7 V-5.5 V
Liquid crystal drive voltage V_{LCD}	3.0 V to 11 V	3.0 V to 7.0 V	3.0 V to 13.0 V
Maximum display digits per chip	8 characters × 2 lines	20 characters × 2 lines	16 characters × 2 lines/ 8 characters × 4 lines
Segment display	None	None	40 segments
Displaye duty cycle	1/8, 1/11, and 1/16	1/8, 1/11, and 1/16	1/17 and 1/33
CGROM	9,920 bits (208: 5 × 8 dot characters and 32: 5 × 10 dot characters)	7,200 bits (160: 5 × 7 dot characters and 32: 5 × 10 dot characters)	9,600 bits (240: 5 × 8 dot characters)
CGRAM	64 bytes	64 bytes	64 bytes
DDRAM	80 bytes	80 bytes	80 bytes
SEGRAM	None	None	8 bytes
Segment signals	40	100	40
Common signals	16	16	33
Liquid crystal drive waveform	A	B	B
Number of displayed lines	1 or 2	1 or 2	1,2, or 4
Low power mode	None	None	Available
Horizontal scroll	Character unit	Character unit	Dot unit
CPU bus timing	2 MHz (5-V operation) 1 MHz (3-V operation)	1 MHz	2 MHz (5-V operation) 1 MHz (3-V operation)
Package	QFP1420-80 80-pin bare chip	LQFP2020-144 144-pin bare chip	QFP1420-100 100-pin bare chip

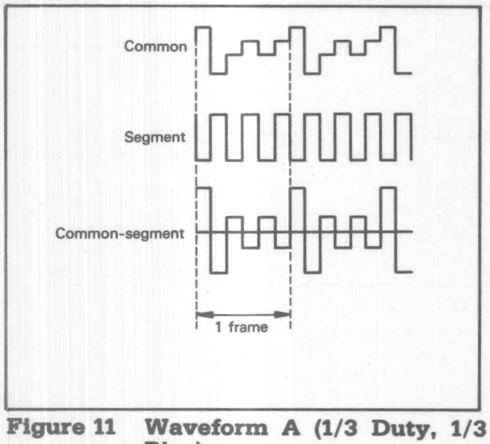


Figure 11 Waveform A (1/3 Duty, 1/3 Bias)

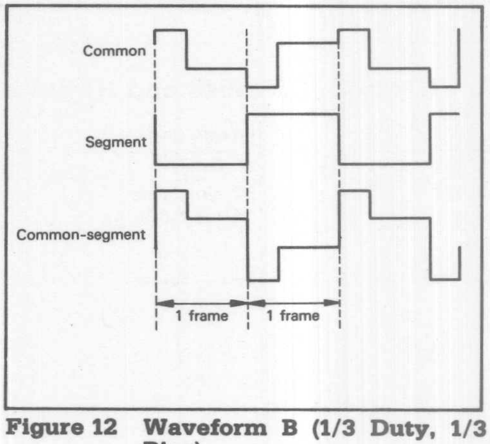


Figure 12 Waveform B (1/3 Duty, 1/3 Bias)

9. HD66204, HD66214T and HD66224T

	HD66204	HD66214T	HD66224T
Datainput (bit)	4	4	4/8
Packge	100-pin plaslic QFP FP-100, TFP-100 Die	TCP	TCP (8mm)

10. HD66205, HD66215T and HD66115T

	HD666205	HD66215T	HD66115T
LCD drive circuits	80	100/101	160
Power supply for LCD drive circuits (V)	-10 to -28 (V_{CC} -V_{EE})	-10 to -28 (V_{CC} -V_{EE})	+14 to +40 (V_{LCD}-GND)

11. HD66106F and HD66204

	HD66106F	HD66204
LCD drive circuits voltage	+14 to +35 (V_{LCD}-GND)	-10 to -28 (V_{CC}-V_{EE})
Display Duty	1/100 to 1/400	1/64 to 1/200
Operating frequency (MHz)	6.0 MHz	8 MHz
Function	column and common driver	column driver

12. HD66106F, HD66107T and HD66110RT

	HD66106F	HD66107T	HD66110RT
LCD drive circuits	80	160	160
Data transfer	4-bits	4/8-bits	4-bits/8-bits
Operating frequency (MHz)	6	8	12
Power supply for LCD drive circuits	14 to 37	14 to 37	28 to 40
Packge	100-pin plastic QFP (FP-100A)	TCP	TCP (9mm)

13. HD63645, HD64645 and HD64646

	HD63645F	HD64645F	HD64646FS
CPU interface	68 family	80 family	80 family
Package	80-pin plastic QFP (FP-80)	80-pin plastic QFP (FP-80)	80-pin plastic QFP (FP-80A)
Other	–	–	HD64646 has another LCD drive interface in HD64645

Package Information

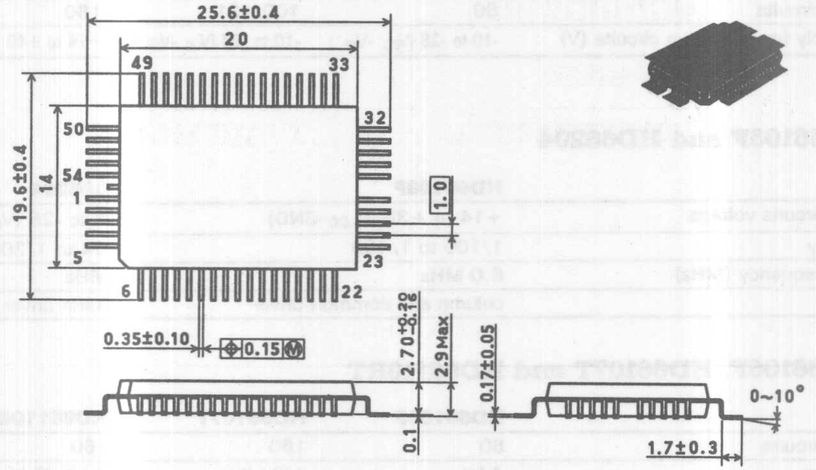
Package Information

The Hitachi LCD driver devices use plastic flat packages to reduce the size of the equipment in which they are incorporated and provide higher density mounting by utilizing the features of thin liquid crystal display elements.

Package Dimensions

Scale: 3/2

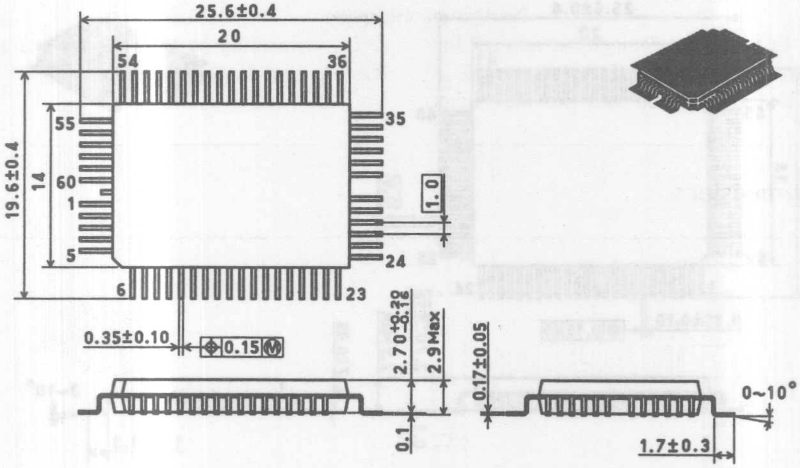
FP-54



Code	FP-54
EIAJ	—
JEDEC	—

Applicable LSI	HD43160AH

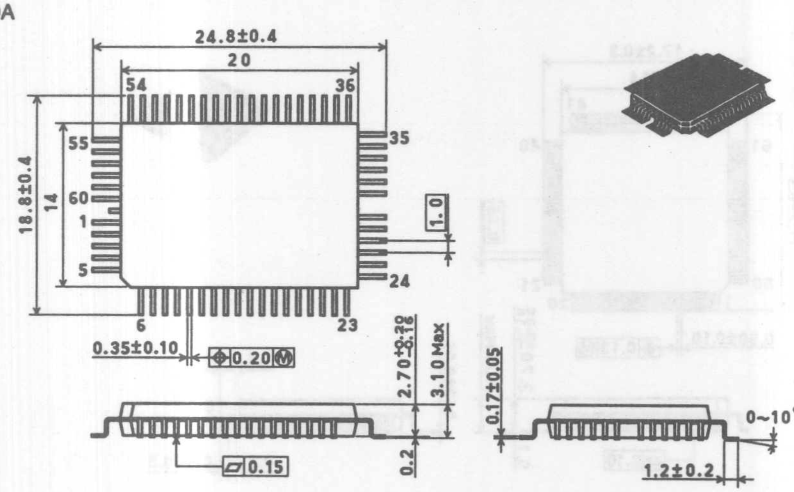
FP-60



Code	FP-60
EIAJ	—
JEDEC	—

Applicable LSI	HD44103, HD44105, HD61830, HD61830B

FP-60A

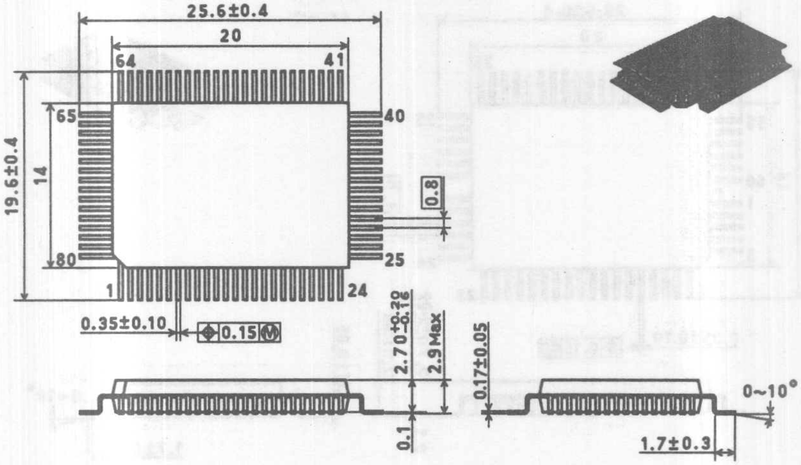


Code	FP-60A
EIAJ	SC-582-F
JEDEC	—

Applicable LSI	HD44100R

Package Information

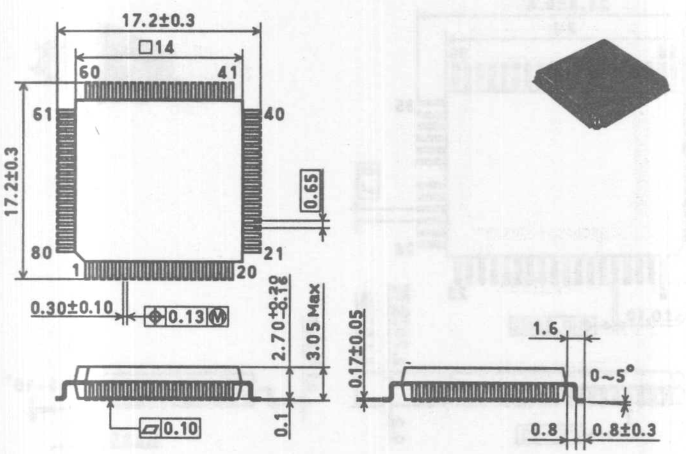
FP-80



Code	FP-80A
EIAJ	—
JEDEC	—

Applicable LSI	HD61602, HD61603, HD61604, HD61605, HD63645, HD64645, HD44102

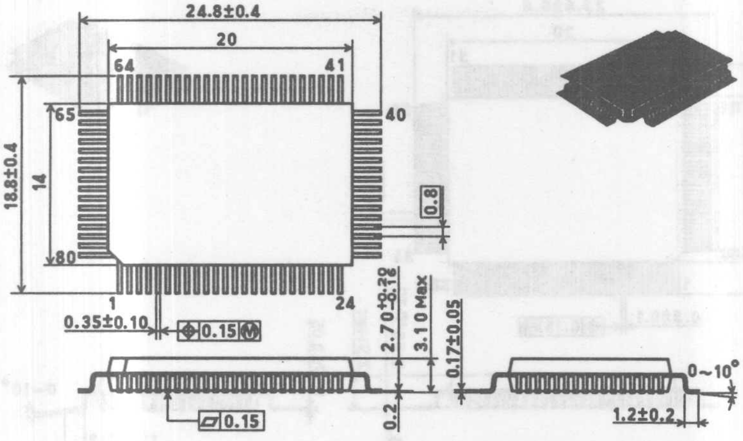
FP-80A



Code	FP-80A
EIAJ	—
JEDEC	—

Applicable LSI	HD61602

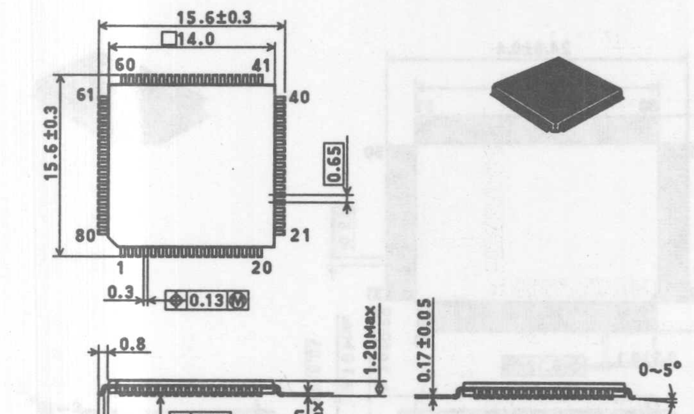
FP-80B



Code	FP-80B
EIAJ	—
JEDEC	—

Applicable LSI	HD64646, HD44780U

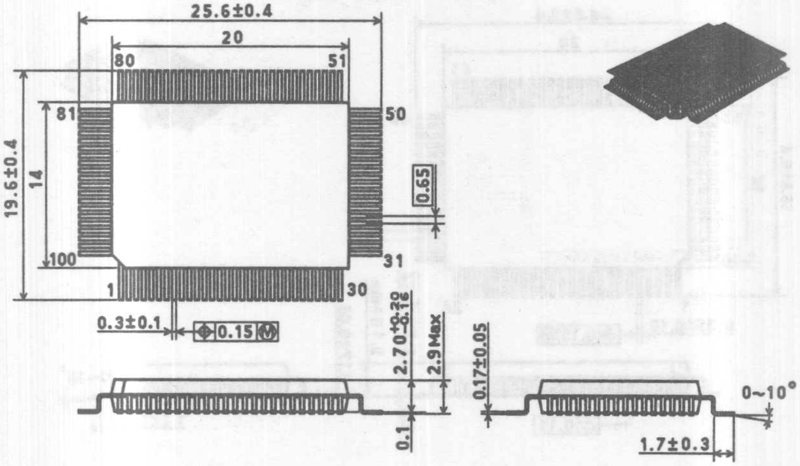
TFP-80



Code	TFP-80
EIAJ	—
JEDEC	—

Applicable LSI	HD44780U

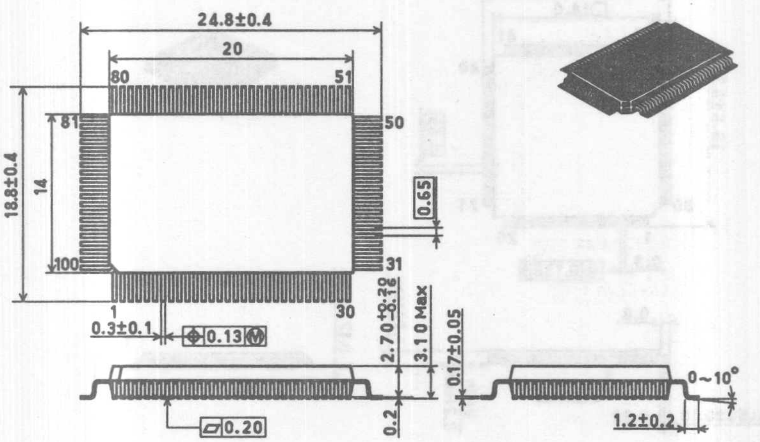
FP-100



Code	FP-100
EIAJ	—
JEDEC	—

Applicable LSI	HD61100A, HD61102, HD61103A, HD66204, HD66205, HD61200, HD61202, HD61203, HD66100F

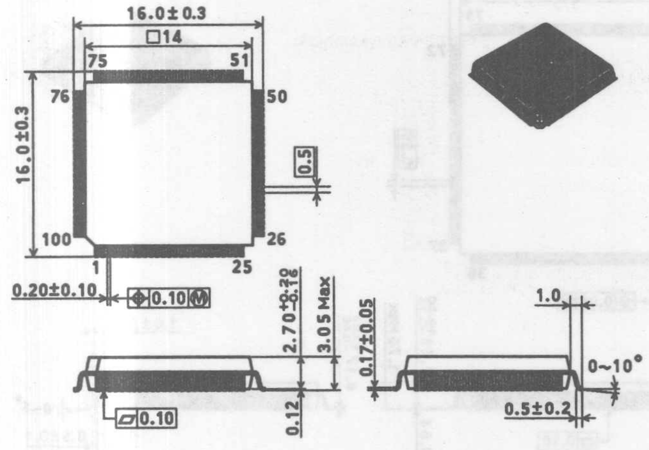
FP-100A



Code	FP-100A
EIAJ	—
JEDEC	—

Applicable LSI	HD66106F, HD66710

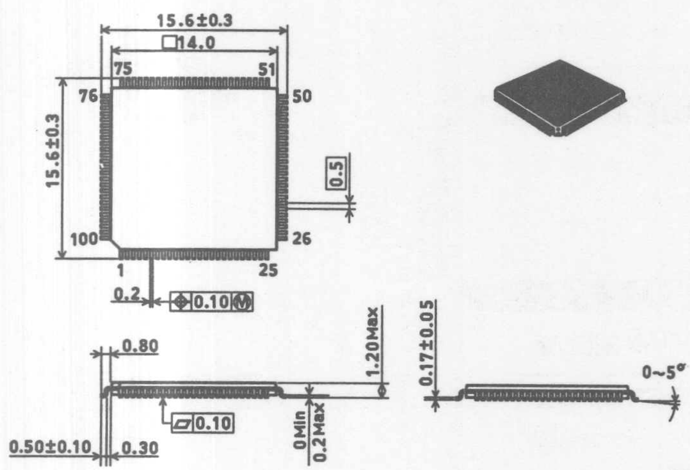
FP-100B



Code	FP-100B
EIAJ	—
JEDEC	—

Applicable LSI	HD66100F

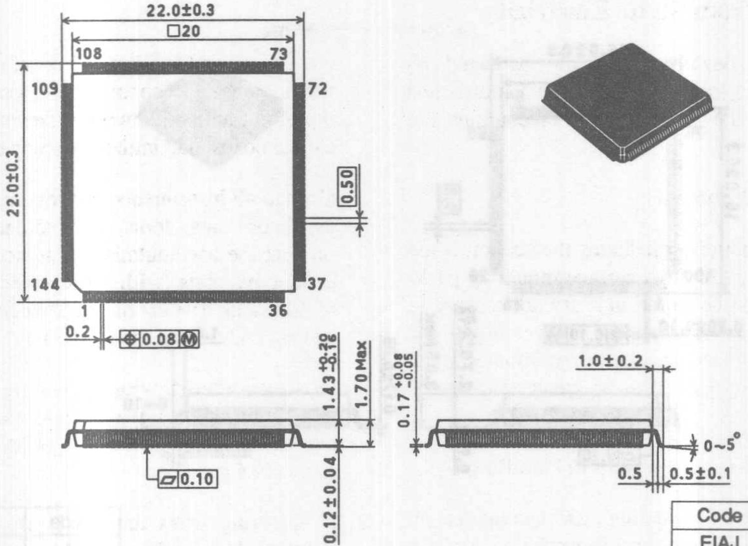
TFP-100



Code	TFP-100
EIAJ	—
JEDEC	—

Applicable LSI	HD66204, HD66205, HD61202, HD61203

FP-144A



Code	FP-144A
EIAJ	SC-596-A
JEDEC	—

Applicable LSI	HD66702

Notes on Mounting

1. Damage from Static Electricity

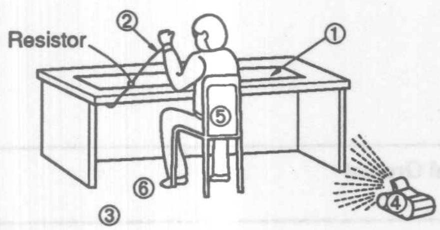
Semiconductor devices are easily damaged by static discharges, so they should be handled and mounted with the utmost care. Precautions are discussed below.

1.1 Work Environment

Low relative humidity facilitates the accumulation of static charge. Although surface mounting package devices must be stored in a dry atmosphere to prevent moisture absorption, they should be handled and mounted in a work environment with a relative humidity of 50% or greater to prevent static buildup.

1.2 Preventing Static Buildup in Handling

1. Avoid the use of insulating materials that easily accumulate a static charge in workplaces where mounting operations are performed. In particular, charged objects can induce charges in semiconductors and finished PC boards even without direct contact. Recommended measures include the use of anti-static work garments, conductive carrier boxes, and ionized air blowers.
2. Ground all instruments, conveyors, work benches, floor mats, tools, and soldering irons to prevent the accumulation of static charges. Lay conductive mats (with a resistance on the order of 10^9 Ω to 10^{11} Ω) on workbenches and floors and ground them. (See figure 1.)
3. Personnel should wear grounding bracelets on their arms or legs. To prevent electric shocks, insert a resistor of 1 MΩ or greater in series as shown in figure 2.
4. If soldering irons are used, use low voltage (12 V to 24 V) soldering irons designed for use with semiconductors. Ground soldering iron tips as shown in figure 3.



① High resistance conductive mat (grounded)
② Personal ground (bracelet)
③ High resistance conductive mat (grounded)
④ Humidifier
⑤ Anti-static work clothes
⑥ Anti-static shoes

Figure 1 Static Electricity Countermeasures for Semiconductor Handling

1.3 Preventing Semiconductor Discharges

Semiconductors are not damaged by static charges on the package or chip itself. However, damage will occur if the lead frame contacts a metal object and the charge dissipates. Grounding the metal object does not help in this situation.

The following measures should be taken.

1. Avoid contact or friction between semiconductors and easily charged insulators.
2. Avoid handling or working with semiconductors on metal surfaces. Semiconductors should be handled on grounded high resistance mats.
3. If a semiconductor may be charged, do not allow that device to contact any metal objects.

1.4 Precautions during Mounting

1. Grounded high resistance mats must be used when mounting semiconductors on PC boards. Ground mats before handling semiconductors. Particular caution is required following conductivity testing, since capacitors on the PC board may retain a charge.
2. PC boards can also acquire a static charge by contact, friction, or induction. Take precautions to prevent discharge through contact with transport boxes or other metal objects during transportation. Such precautions include the use of anti-static bags or other techniques for isolating the PC boards.

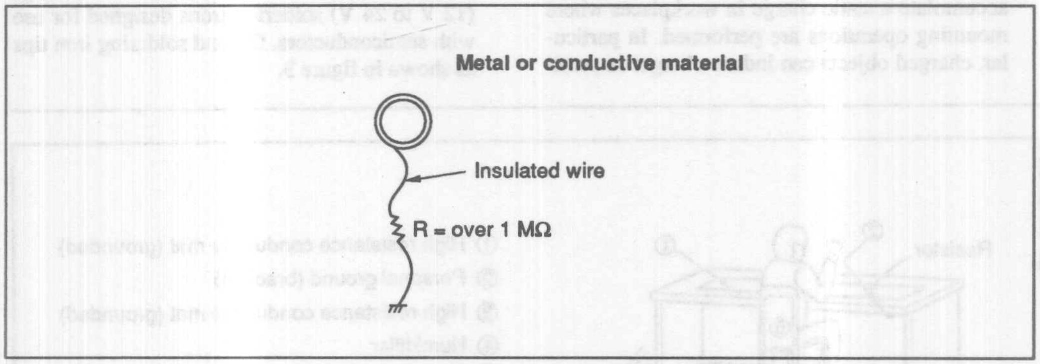


Figure 2 Personal Ground

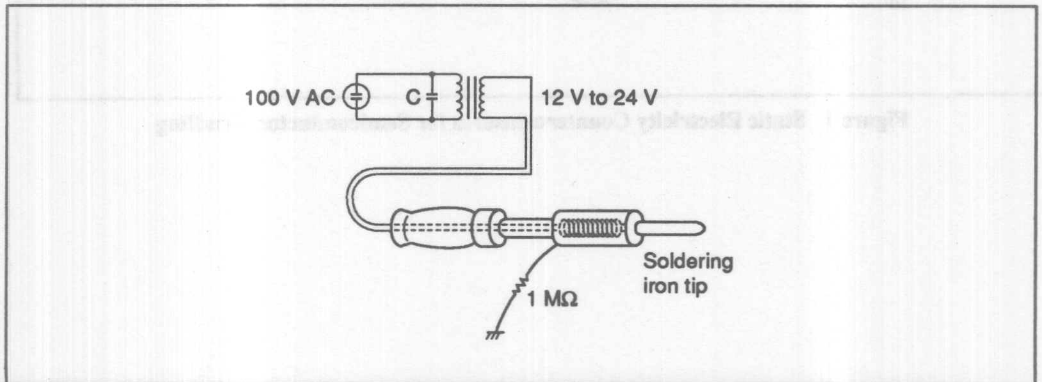


Figure 3 Soldering Iron Grounding Example

2. Precautions Prior to Reflow Soldering

Surface mount packages that hold large chips are weaker than insertion mount packages. Since the whole package is heated during the reflow operation, the characteristics described below should be considered when determining the handling used prior to reflow soldering and the conditions used in the reflow operation.

2.1 Package Cracking Mechanism in Reflow Soldering

Packages that have absorbed moisture are thought to crack due to the mechanism shown in figure 4. Moisture absorbed during storage diffuses through the interior of the package. When a package in this state is passed through the reflow furnace, that moisture rediffuses. Some of it escapes along the boundary between the resin and the frame. This can lead to boundary separation. As the pressure in this space increases the resin warps, finally resulting in a crack.

The Fick diffusion model can be used to calculate the diffusion of moisture in resin:

$$\frac{\partial C\,(x,\,t)}{\partial_t} = D\,(t)\,\frac{\partial^2 C\,(x,\,t)}{\partial^2\,x^2}$$

The volume of moisture absorbed by the package can be expressed as follows:

$$Q\,(t) = \int C\,(x,\,t)\,dx$$

The increase in internal pressure can be calculated from the moisture diffusion during reflow heating by using the C (x, t) function.

Figure 5 shows the relationships between the maximum stresses when packages of various moisture absorption states are heated, the adhesion strength between the resin and frame at various temperatures, and the strength of the resin itself. While this model indicates that cracks will result in this example when the moisture absorption ratio exceeds 0.2 wt% in a VPS (vapor phase soldering at 215°C) process, actual tests show that cracks result in packages with a moisture absorption ratio of 0.25 wt%. This indicates that the model is valid.

Therefore moisture management should focus on the moisture content in the vicinity of the frame.

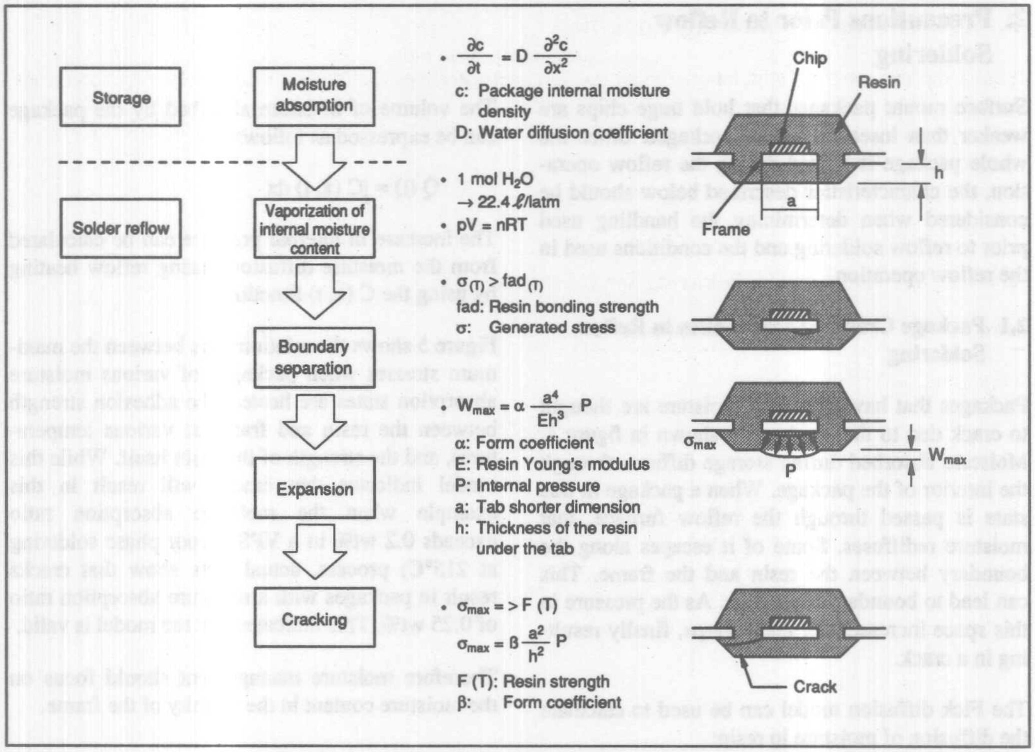


Figure 4 Package Crack Generation Mechanism

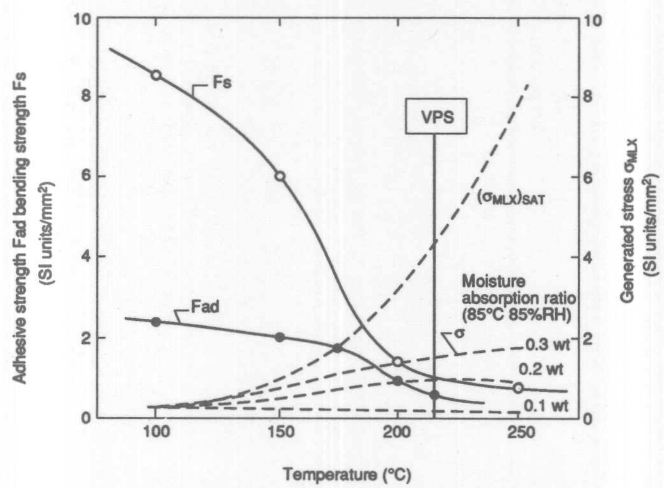


Figure 5 Temperature Dependence of Resin Adhesive Strength, Mechanical Strength, and Generated Stress

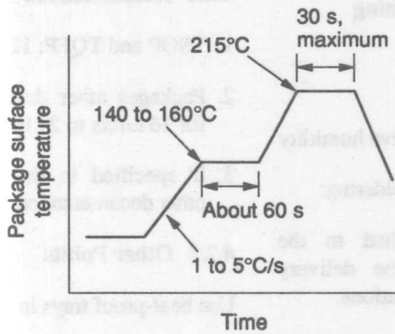
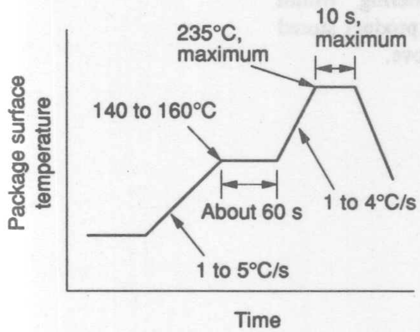
3. Recommended Soldering Conditions

Soldering temperature stipulations must be followed and the moisture absorption states of plastic packages must be carefully monitored to prevent degradation of the reliability of surface mount packages due to thermal shock. This section presents Hitachi's recommended soldering conditions.

3.1 Recommended Soldering Temperatures

See table 1.

Table 1 Recommended IC Soldering Temperatures

Method	Recommended Conditions	Notes
Vapor-phase reflow		
Infrared reflow Hot-air reflow		Since TSOP, TQFP, and packages whose body thickness is less than 1.5 mm are especially vulnerable to thermal shock, we recommend limiting the soldering conditions to a maximum temperature of 230°C for a maximum time of 10 seconds for these packages.

4. Moisture Absorption Prevention Conditions

Plastic packages absorb moisture when stored in a high humidity. If devices are mounted using solder reflow techniques when they have absorbed moisture they are susceptible to reflow cracking. Products that are particularly susceptible to the influence of absorbed moisture are packed in moisture-proof packing. These products should be handled under the following conditions after opening the moisture-proof packing.

4.1 Storage and Handling after Opening Moisture-Proof Packing

Storage temperature: 5°C to 30°C

Storage humidity: Under 60% relative humidity

Time between unpacking and reflow soldering:

1. If specified on the label attached to the moisture-proof packing, or in the delivery specifications: follow those specifications.

2. If not specified on the label attached to the moisture-proof packing or in the delivery specifications: perform reflow soldering within 168 hours (one week) with the product stored under the conditions specified above.

4.2 Baking

4.2.1 Baking is Required in the Following Situations

1. If the desiccant indicator has turned pink.

2. If the storage period following unpacking exceeds the specifications for that period.

4.2.2 Recommended Baking Conditions

1. TSOP and TQFP: 125°C for 4 hours

2. Packages other than TSOP and TQFP: 125°C for 16 hours to 24 hours

3. If specified in the delivery specifications or other documentation, follow those specifications.

4.2.3 Other Points

Use heat-proof trays in the baking operation.

Surface Mounting Package Handling Precautions

1. Package temperature distribution

The most common method used for mounting a surface mounting device is infrared reflow. Since the package is made of a black epoxy resin, the portion of the package directly exposed to the infrared heat source will absorb heat faster and thus rise in temperature more quickly than other parts of the package unless precautions are taken. As shown in the example in figure 6, the surface directly facing the infrared heat source is 20° to 30°C higher than the leads being soldered and 40° to 50°C higher than the bottom of the package. If soldering is performed under these conditions, package cracks may occur.

To avoid this type of problem, it is recommended that an aluminum infrared heat shield be placed over the resin surface of the package. By using a 2-mm thick aluminum heat shield, the top and bottom surfaces of the resin can be held to 175°C when the peak temperature of the leads is 240°C.

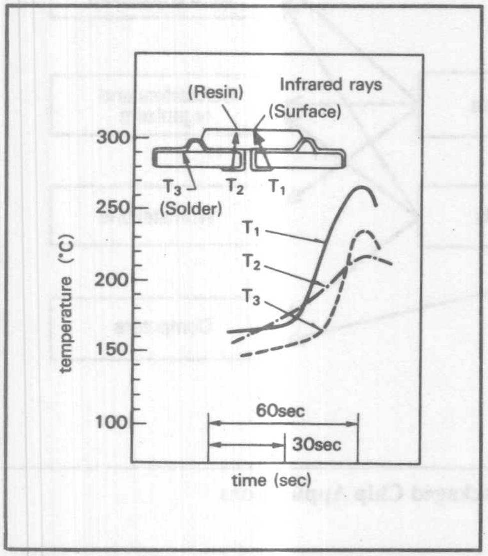


Figure 6 Temperature Profile During Infrared Heat Soldering (Example)

2. Package moisture absorption

The epoxy resin used in plastic packages will absorb moisture if stored in a high-humidity environment. If this moisture absorption becomes excessive, there will be sudden vaporization during soldering, causing the interface of the resin and lead frame to spread apart. In extreme cases, package cracks will occur. Therefore, especially for thin packages, it is important that moisture-proof storage be used.
To remove any moisture absorbed during transportation, storage, or handling, it is recommended that the package be baked at 125°C for 16 to 24 hours before soldering.

3. Heating and cooling

One method of soldering electrical parts is the solder dip method, but compared to the reflow method, the rate of heat transmission is an order of magnitude higher. When this method is used with plastic items, there is thermal shock resulting in package cracks and a deterioration of moisture-resistant characteristics. Thus, it is recommended that the solder dip method not be used.
Even with the reflow method, an excessive rate of heating or cooling is undesirable. A rate in temperature change of less than 4°C/sec is recommended.

4. Package contaminants

It is recommended that a resin-based flux be used during soldering. Acid-based fluxes have a tendency of leaving an acid residue which adversely affects product reliability. Thus, acid-based fluxes should not be used.
With resin-based fluxes as well, if a residue is left behind, the leads and other package parts will begin to corrode. Thus, the flux must be thoroughly washed away. If cleansing solvents used to wash away the flux are left on the package for an extended period of time, package markings may fade, so care must be taken.

The precautions mentioned above are general points to be observed for reflow. However, specific reflow conditions will depend on such factors as the package shape, printed circuit board type, reflow method, and device type.

For details on surface mounting small thin packages, please consult the separate manual available on mounting. If there are any additional questions, please contact Hitachi, Ltd.

The Information of TCP

Features of TCP (TAB Technology)

The structure and materials used by Tape Carrier Package (TCP) give it the following features as compared with conventional packages:

Thin, Lightweight, and Fine Pitch

With thickness less than 1 mm and fine-pitch leads, a reduced pad pitch on the device enables more functionality in a package of equivalent size. Specifically, these features enable:

- Thin and high definition LCM (Liquid Crystal display Module)
- Lightweight and ultra-high pin count systems

Flexible Design

The following can be tailored to the design of the system (e.g. mother board design):

- Pattern layout
- TCP design

TCP Applications

Thinness, ultra-high pin count, and fine pitch open up new possibilities of TCP applications for compact and highly functional systems. Figure 1 shows some applications of TCP-packaged chips.

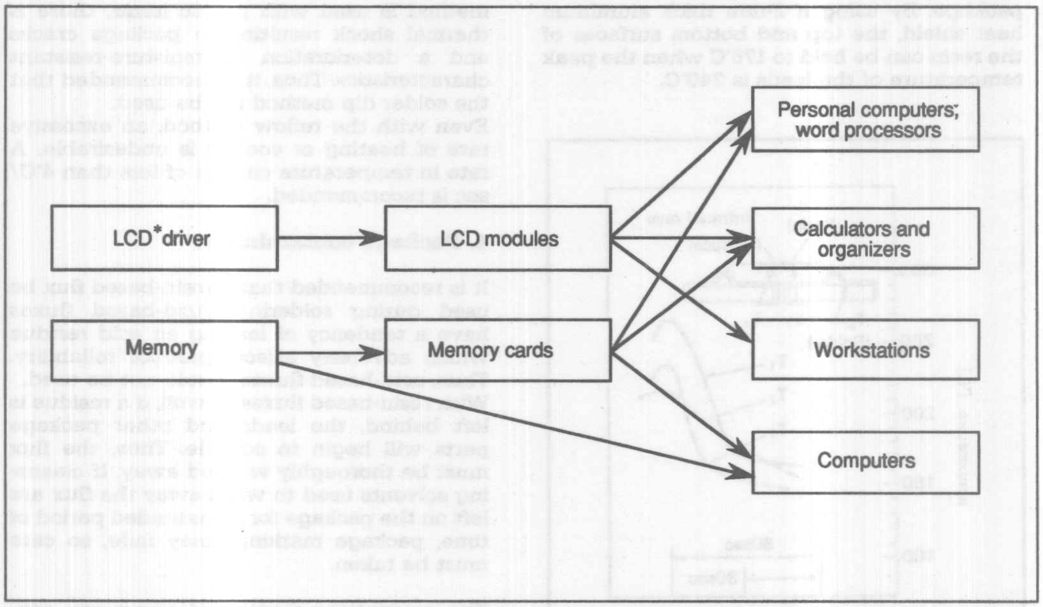


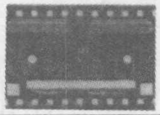
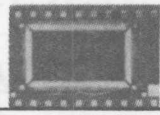
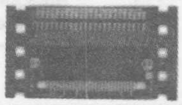
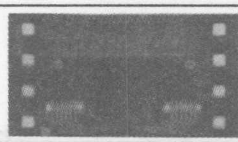
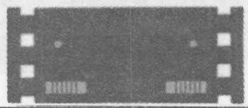
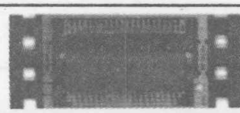
Figure 1 Examples of TCP-Packaged Chip Applications

Hitachi TCP Products

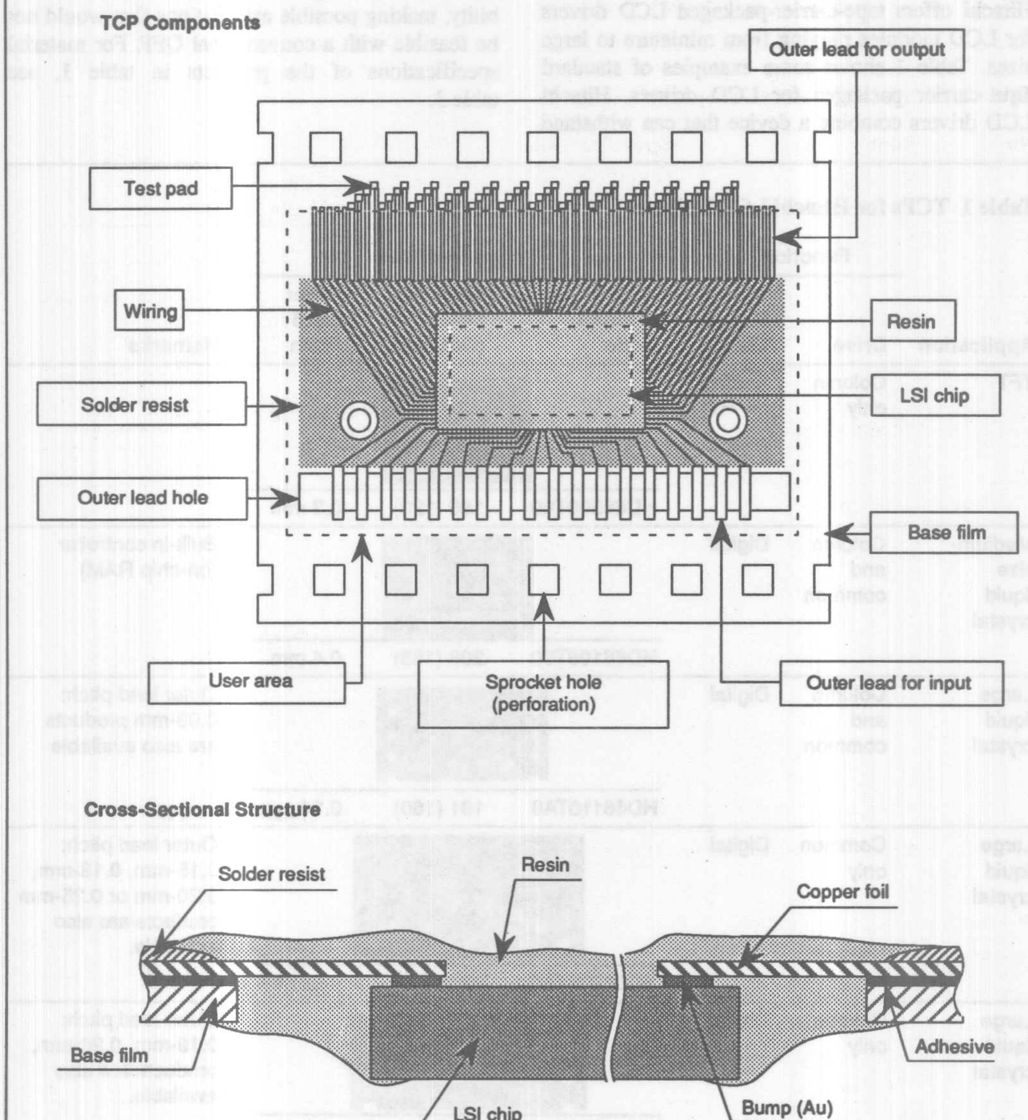
TCP for Hitachi LCD Driver

Hitachi offers tape-carrier-packaged LCD drivers for LCD modules ranging from miniature to large sizes. Table 1 shows some examples of standard tape carrier packages for LCD drivers. Hitachi LCD drivers combine a device that can withstand high voltages and provide high definition with a tape carrier package that promises excellent reliability, making possible applications that would not be feasible with a conventional QFP. For material specifications of the products in table 1, see table 3.

Table 1 TCPs for Hitachi LCD Drivers

	Function		Appearance			
Application	Drive	Signal Output	Product Code	Total Pin Count (Output)	Outer Lead Pitch	Remarks
TFT	Column only	Analog	 HD66300T00	156 (120)	0.3 mm	
Medium-size liquid crystal	Column and common	Digital	 HD66108T00	208 (165)	0.4 mm	Built-in controller (on-chip RAM)
Large liquid crystal	Column and common	Digital	 HD66110TA8	191 (160)	0.14 mm	Outer lead pitch: 0.08-mm products are also available
Large liquid crystal	Common only	Digital	 HD66205TA9L	92 (80)	0.22 mm	Outer lead pitch: 0.15-mm, 0.18-mm, 0.20-mm or 0.25-mm products are also available.
Large liquid crystal	Column only	Digital	 HD66214TA9L	98 (80)	0.22 mm	Outer lead pitch: 0.18-mm, 0.20-mm, products are also available.
Large liquid crystal	Column only	Digital	 HD66224TA1	108 (80)	0.21 mm	Outer lead pitch: 0.20-mm products are also available.

TCP External View and Cross-Sectional Structure



TCP Materials and Features

TCP Material Specifications: Table 2 lists Hitachi TCP material specifications. Ask us if you require other materials. In this case, use TCP ordering manual [ADE-801-001 (O)].

Table 3 lists current material specifications for various Hitachi products.

Table 2 Hitachi TCP Material Specifications

No.	Item	Specifications
1	Base film	UPILEX® S-type: thickness 75 μm ±5 μm KAPTON® V-type: thickness 125 or 75 μm ±5 μm
2	Adhesive	Toray #5900
		TOMOEGAWA E-type
3	Copper foil	Rolled copper: thickness 35 or 25 μm ±5 μm
		Electro-deposited copper: thickness 35 or 25 μm ±5 μm
4	Resin	Epoxy resin
5	Outer lead plating	Tin
6	Solder resist	Epoxy solder resist

Cross-sectional view

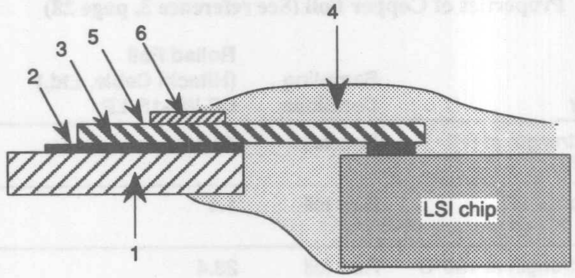


Table 3 Material Specifications for Hitachi Products

Product Code	Application	Base Film	Adhesive	Copper Foil	Outer Lead Plating
HD66300T00	TFT	KAPTON® V	Toray #5900	Rolled copper	Tin
HD66108T00	Large liquid crystal	KAPTON® V	Toray #5900	Rolled copper	Tin
HD66110TA8	Large liquid crystal	UPILEX® S	TOMOEGAWA E-type	Electro-deposited copper	Tin
HD66205TA9L	Large liquid crystal	UPILEX® S	Toray #5900	Rolled copper	Tin
HD66214TA9L	Large liquid crystal	UPILEX® S	Toray #5900	Rolled copper	Tin
HD66224TA1	Large liquid crystal	UPILEX® S	TOMOEGAWA E-type	Electro-deposited copper	Tin

Properties of Materials: Properties of Hitachi TCP materials are as follows.

1. Base film

The properties of base film are shown in table 4. Hitachi currently adopts UPILEX® S, which exhibits high rigidity and super dimensional stability with respect to temperature changes compared with conventional KAPTON® V.

2. Copper foil (copper wiring)

The properties of rolled foil and electro-deposited foil are shown in table 5. Hitachi plans to adopt electro-deposited foil due to its excellent elongation properties at room temperature (RT) compared with conventional rolled foil.

Table 4 Properties of Base Film (See references 1 and 2, page 28)

Property		UPILEX® S (Ube Industries, Ltd.)	KAPTON® V (Du Pont-Toray Co., Ltd.)
Coefficient of linear expansion $\times 10^{-5}$/°C	To 100°C	0.8	—
	To 200°C	1.0	2.6
Tensile modules (kgf/mm^2)		900	355

Table 5 Properties of Copper Foil (See reference 3, page 28)

Property	Sampling Condition	Rolled Foil (Hitachi Cable, Ltd.) CF-W5-1S-LP	Electro-Deposited Foil (Mitsui Mining & Smelting Co., Ltd.) 3EC-VLP
Tensile strength at RT (kgf/mm^2)	Raw foil	43.0	54.9
Elongation at RT (%)	Raw foil	1.0	10.1
Tensile strength at 180°C (kgf/mm^2)	Raw foil	23.4	25.4
Elongation at 180°C (%)	Raw foil	7.7	7.0

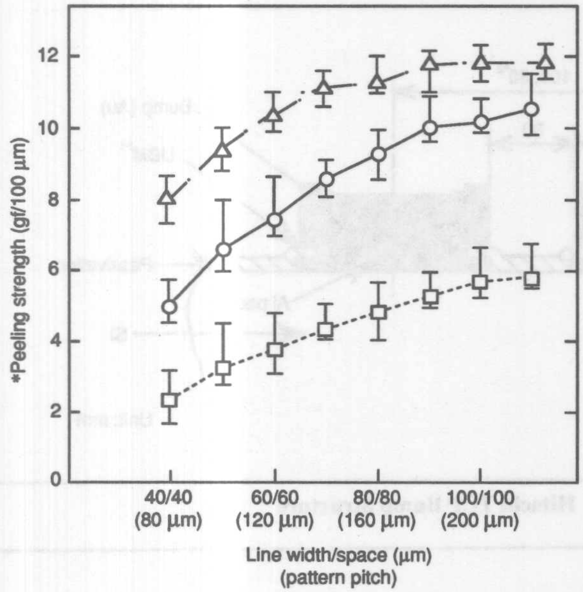
Note: Data from film suppliers.
Number of measured samples: 2 pieces each
1 kgf/mm^2 = 9.80665 MPa

3. Adhesive

The relationship between peeling strength (adhesive/electro-deposited foil) and lead width is shown in figure 2. Hitachi adopts the following two combinations because of their higher peeling strength.

— Adhesive TOMOEGAWA E-type/electro-deposited foil

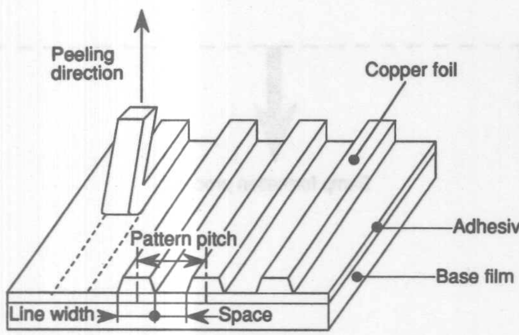
— Adhesive Toray #5900/rolled foil



	Adhesive	Copper foil
△	TOMOEGAWA E-type	Electro-deposited foil
○	Toray #5900	Rolled foil
□	TOMOEGAWA E-type	Rolled foil

*Peeling strength

— How to measure —



Measuring method: 90° peel

Measuring condition: 25°C

Number of measured samples:

Five pieces are measured for each specification, and two leads are measured for each piece.

Figure 2 Relationship between Peeling Strength and Lead Width

Fine-Pitch Bump Formation

Bumps are essential in TCP products; they are the foundation of TAB technology and have excellent corrosion resistance in their structure. When the current trend toward high-performance chips with ultra-large pin-out began driving pad counts upward (and reducing pad pitch), Hitachi was quick to develop a volume production process for forming fine-pitch bumps.

Figure 3 shows the Hitachi TCP bump structure. Figure 4 shows a flowchart of the bump formation process.

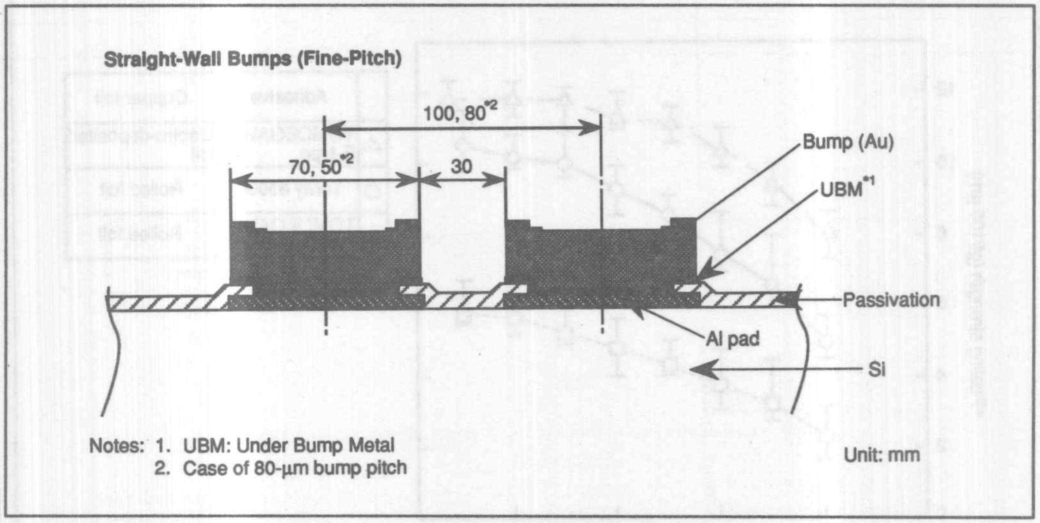


Figure 3 Hitachi TCP Bump Structure

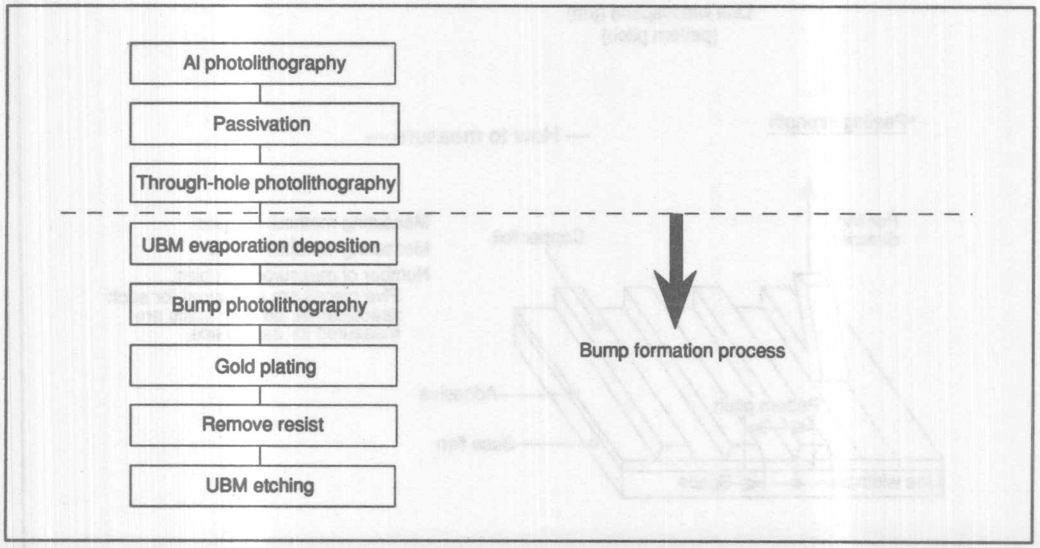


Figure 4 Bump Formation Flowchart

TCP Fabrication Flow

TCP Tape: TCP tapes are purchased from tape manufacturers. In many cases, the quality of TCP products depends critically on the quality of the tape, so in addition to evaluating constituent materials, Hitachi strictly controls the stability of the tape fabrication process.

TCP Fabrication Process: The TCP fabrication process starts from wafers (or chips) with bumps, and a patterned tape. After being bonded by a high-precision inner lead bonder, the chips are sealed in resin. Figure 5 shows the standard fabrication process for TCPs used in Hitachi LCDs.

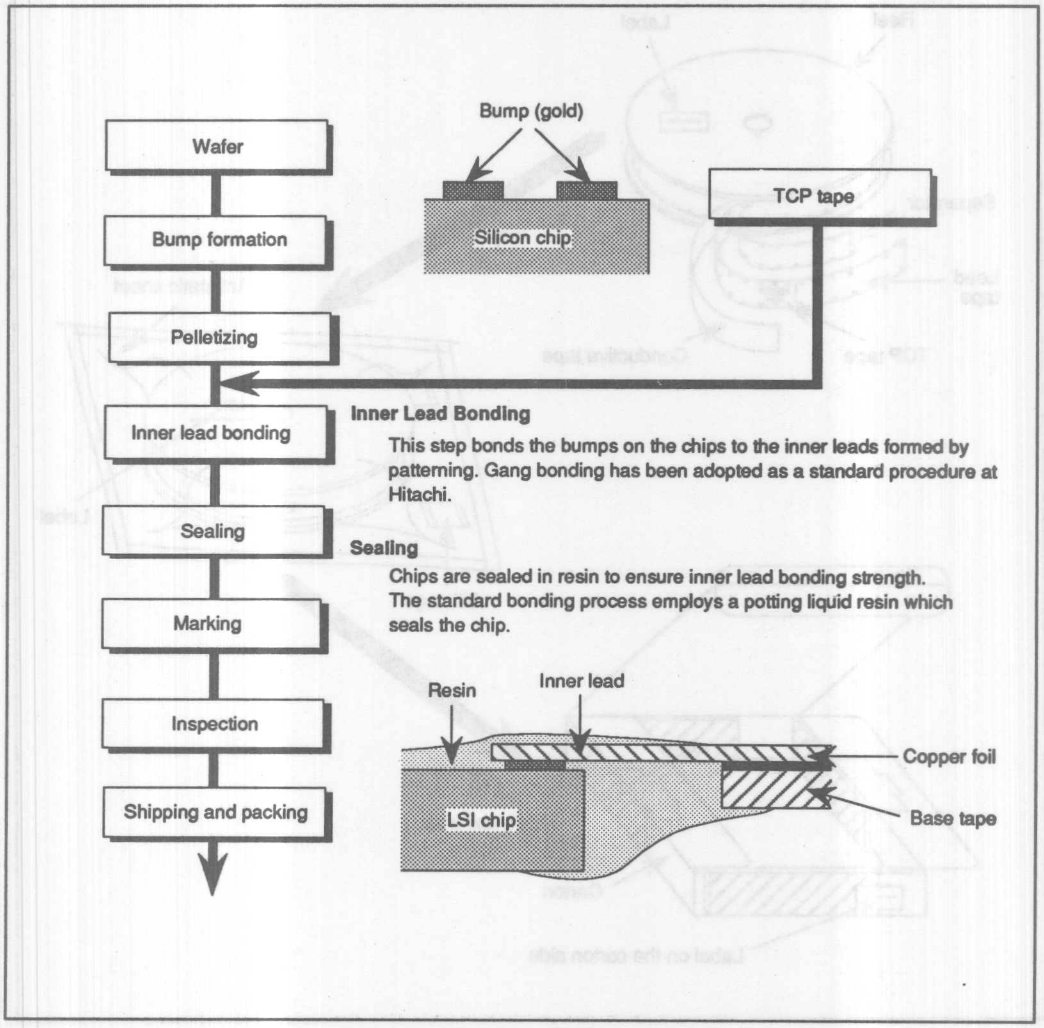


Figure 5 Standard Fabrication Process for TCPs Used in Hitachi LCDs

Packing

Packing Format: TCP products are packed in moisture-proof packages. A reel wound with TCP tape is sealed in an opaque antistatic sheet with N_2 to protect the product from mechanical shock and then packed into a carton before delivery to ensure the solderability of lead plating.

Labels which indicate the product name, quantity, and so on are placed on the reel, antistatic sheet, and carton. Figure 6 shows the TCP packing format.

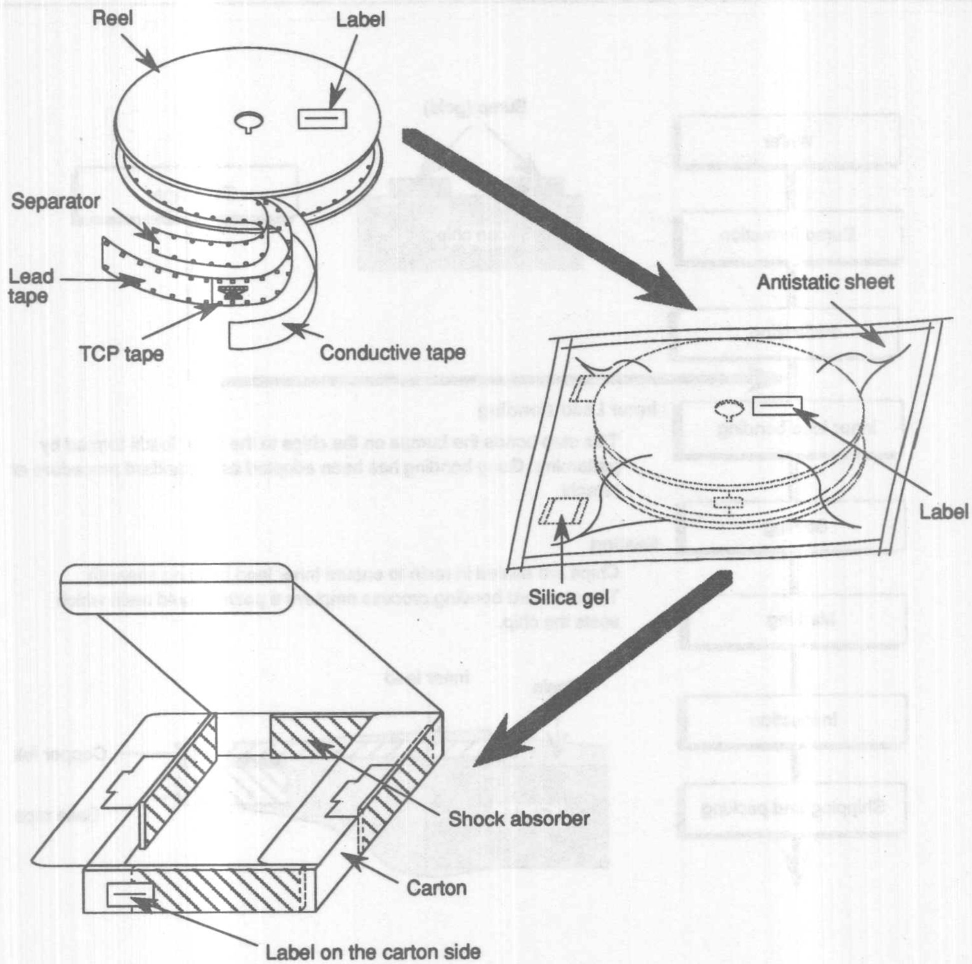


Figure 6 Packing Format

Tape Specification:

1. TCP tape — 40 m
2. Lead tape — 2 +1/–0.5 m added to both ends of the TCP
3. Conductive tape — 40 m
4. Separator — 40 m
5. Width of tape — 35 mm

Note: The lengths of the TCP tape, conductive tape, and separator may vary slightly depending on the quantity of the product on the tape.

Reel Specification: Figure 7 shows reel dimensions.

For recycling purpose, we would appreciate it if you return the reel and separator to us after use.

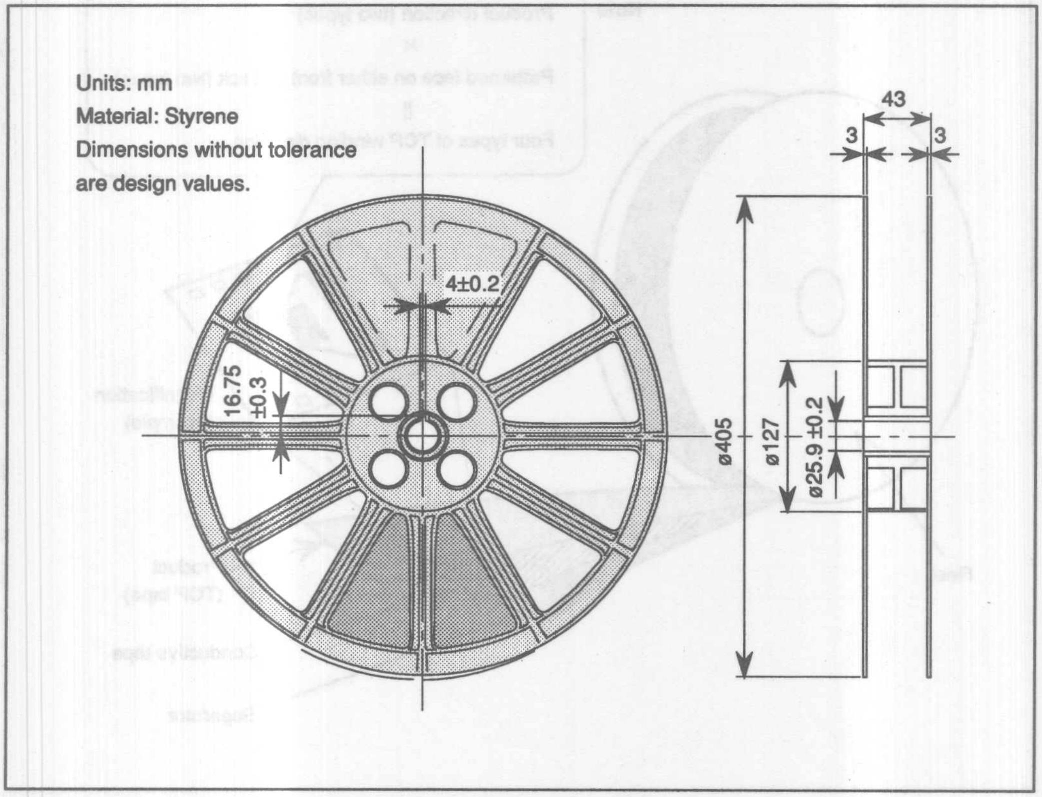


Figure 7 Reel Dimensions

TCP Winding Direction: Figure 8 shows one way of winding TCPs. The combination of two product directions when pulling it out from the reel and placement of the patterned face on either the front or back of the tape makes for four types of TCP winding directions.

The winding direction is an essential specification which affects the chip punching machine and assembly equipment during the packaging process. As the wind direction differs according to the product, please check the delivery specification before using TCP.

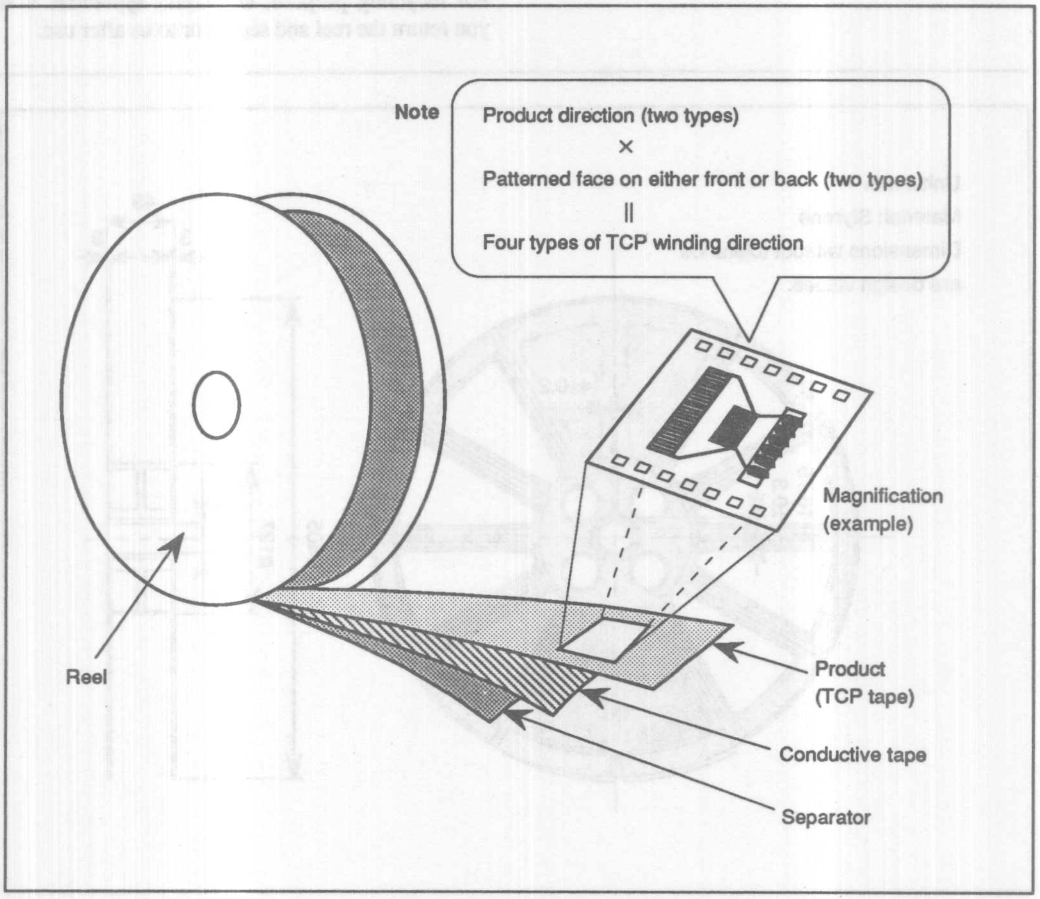


Figure 8 Example of TCP Winding Direction

TCP Mounting Methods

TCP Mounting Structure

Typical example of an LCM structure using TCPs is illustrated in figure 9.

Basic Mounting Process

See figure 10.

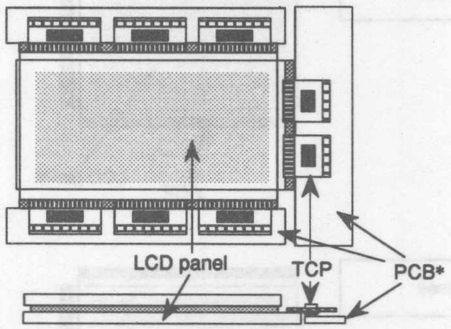


Figure 9 LCM Structure

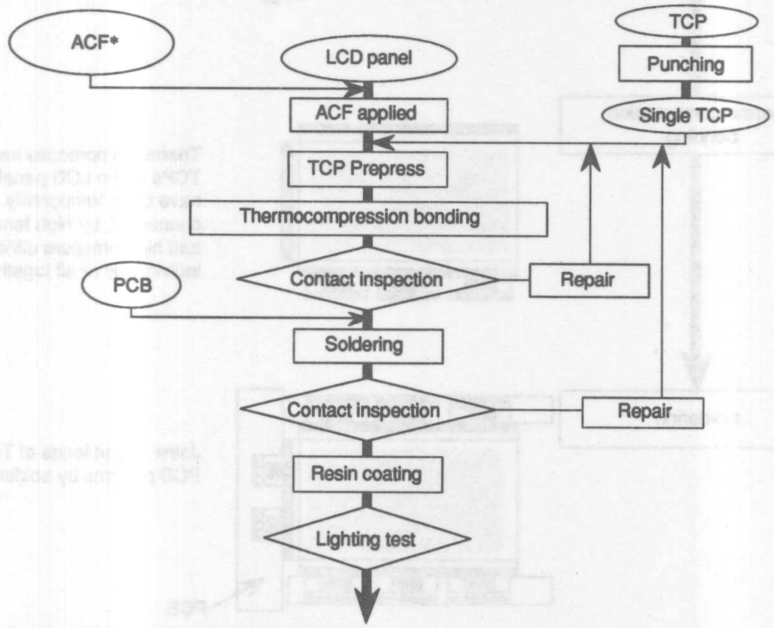


Figure 10 TCP OLB (Outer Lead Bonding) Basic Flowchart

Process Outline

An outline of LCM assembly process using TCPs is given in figure 11.

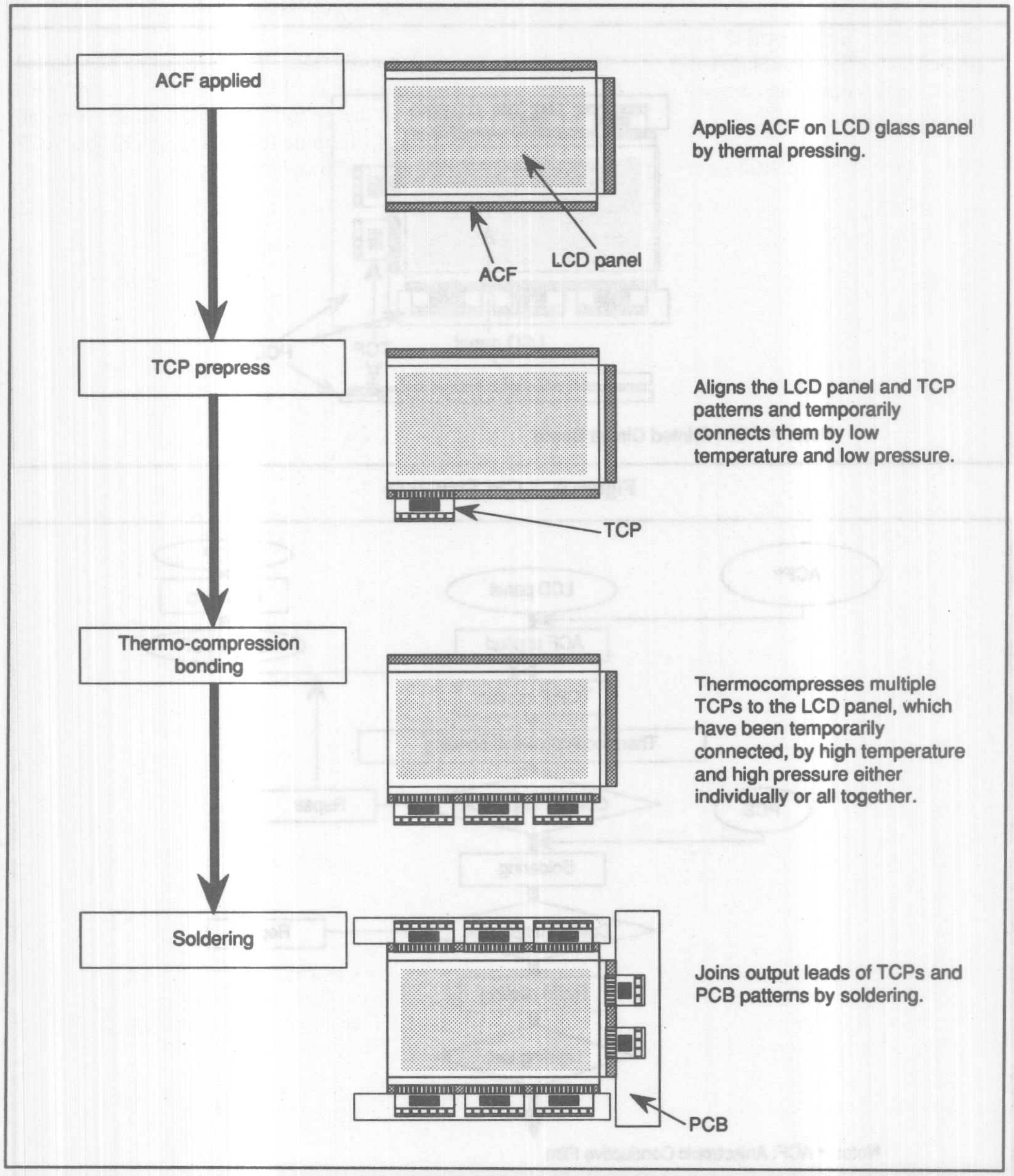


Figure 11 Outline of LCM Assembly Process

TCP Mounting Conditions

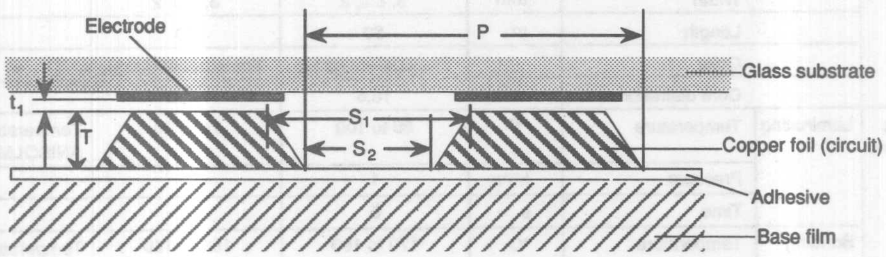
Mounting TCPs on LCD Panels (See reference 4, page 28): ACF is an adhesive film that can connect electrodes on an LCD glass panel with output leads of TCPs. There are two types of ACFs:

- One whose thermosetting and thermoplastic properties make handling easier (such as in repair) and reduces the stresses caused by temperature changes.
- One whose thermosetting properties provide low connection resistance and high thermostability.

Please select ACF depending on the type of application.

1. Selection of ACF thickness

   An appropriate ACF thickness must be selected depending on the height, line width and space width of the circuit to be connected; a rough calculation formula for obtaining a proper ACF thickness is shown below.



$$\text{ACF thickness before connection } t_0 = \frac{\frac{S_1 + S_2}{2}}{P} \times T + t_1 + \alpha$$

t_1: ACF thickness after connection (2 µm)
T: Circuit height
P: Pitch
S_1: Space width (top)
S_2: Space width (bottom)
α: Correction value
AC-6073, AC-6103 — 0.15T
AC-7104, AC-7144 — 0.25T

Incomplete filling can occur in the space if ACF thickness is too thin, while if too thick, connection reliability becomes poor since conductive particles are not flattened out. It is necessary to select an appropriate ACF thickness. Some adjustment of ACF thickness can be controlled by bonding conditions (especially pressure).

2. Laminating and bonding conditions

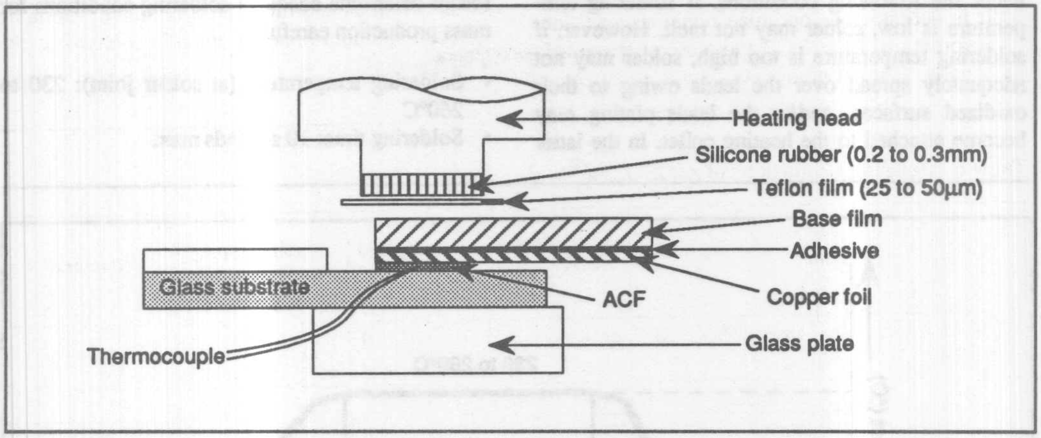
It is necessary to optimize bonding conditions according to ACF, TCP and glass panel specifications. The bonding conditions adopted by ANISOLM® (Hitachi Chemical Co., Ltd.) are shown in table 6 for reference. Please determine your optimum bonding conditions based on the following.

Table 6 Bonding Conditions of ANISOLM®

Item			Unit	Mixture of Thermosetting and Thermoplastic		Thermosetting		Remarks
				AC-6073	AC-6103	AC-7104	AC-7144	
Standard specifications	Min. pitch	Line	µm	70	50	50	35	
		Space	µm	70	50	50	35	
		Resolution	Line/mm	7	10	10	14	
		Thickness	µm	22	22, 18	25	16	
		Width	mm	3, 2.5, 2		3, 2.5, 2		
		Length	m	50		50		
		Color		Transparent (gray)		Transparent (gray)		
		Core diameter	mm	18.5		18.5		
Bonding conditions	Laminating	Temperature	°C	80 to 100		70 to 90		Temperature on ANISOLM®
		Pressure	MPa	1		1		
		Time	s	5		5		
	Bonding	Temperature	°C	170 to 190		160 to 180		Temperature on ANISOLM®
		Pressure	MPa*	2		2	3	
		Time	s	20		20		

Note: * 1 MPa = 1.01972×10^{-1} kgf/mm²

Measuring Method of ACF Temperature Profile (example)



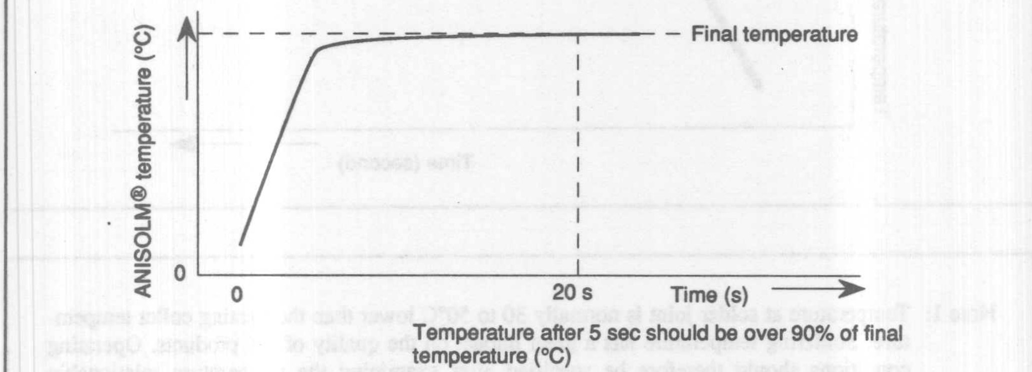
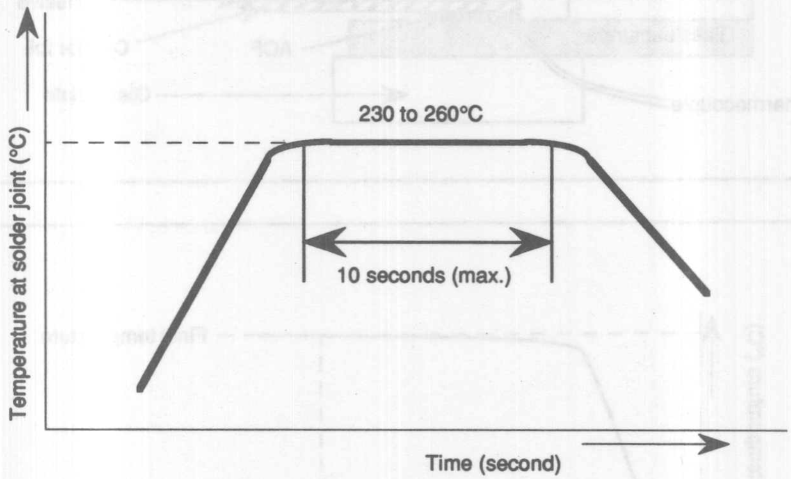


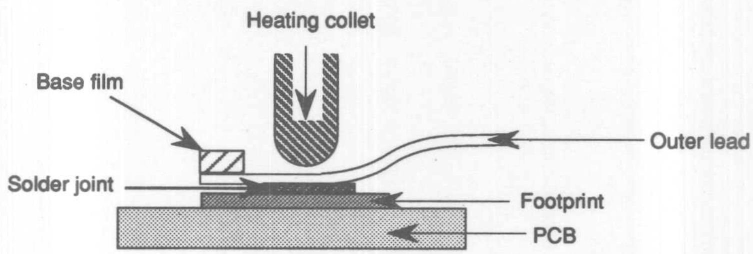
Figure 12 Bonding Temperature Profile

Soldering Conditions: Solder TCPs on the PCB under the following conditions. If soldering temperature is low, solder may not melt. However, if soldering temperature is too high, solder may not adequately spread over the leads owing to their oxidized surfaces, and/or the leads plating may become attached to the heating collet. In the latter case, copper foil of leads may become exposed. Please determine adequate soldering conditions for mass production carefully.

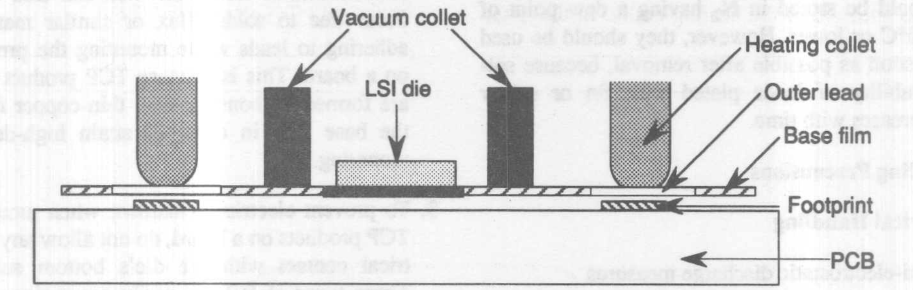
- Soldering temperature (at solder joint): 230 to 260°C
- Soldering time: 10 seconds max.

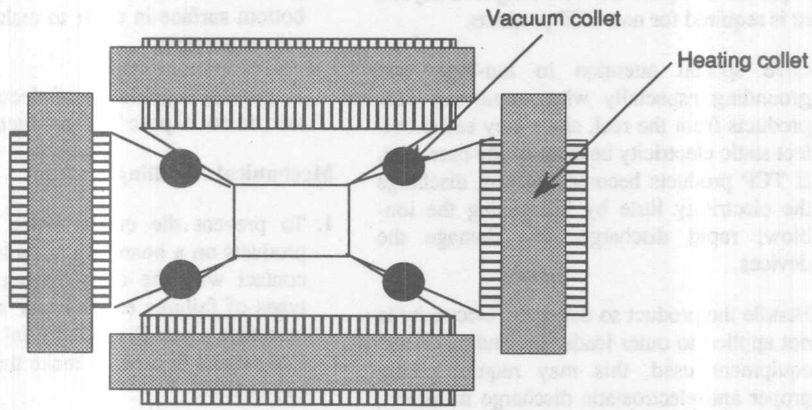


Note 1: Temperature at solder joint is normally 30 to 50°C lower than the heating collet temperature. Soldering temperature has a great impact on the quality of the products. Operating conditions should therefore be specified after examining the temperature relationship between the tip of the heating collet and solder joint.



Note 2: In case of soldering quad type TCPs, please fix the TCPs using vacuum collets or equivalent to prevent base film warpage and circuit position misalignment.





Storage Restrictions

1. Packed TCP products should be used within six months.

2. TCP products removed from the antistatic sheet should be stored in N_2 having a dew point of –30°C or lower. However, they should be used as soon as possible after removal, because solderability of leads plated with Sn or solder decreases with time.

Handling Precautions

Electrical Handling

1. Anti-electrostatic discharge measures

   TCP products require the following care beyond what is required for non-TCP products.

   - Give special attention to ion-blow and grounding especially when removing TCP products from the reel, since they easily collect static electricity because of the base film. If TCP products become charged, discharge the electricity little by little using the ion-blow; rapid discharge may damage the devices.

   - Handle the product so that static electricity is not applied to outer leads. Depending on the equipment used, this may require taking proper anti-electrostatic discharge measures, such as not allowing the tapeguide to contact the outer leads.

2. Outer lead coating

   Outer leads should be coated with resin or other appropriate materials to prevent short-circuits and disconnections due to corrosion. Conductive foreign particles can easily cause short-circuits since lead spacing for TCP products is much narrower than that for non-TCP products. Disconnections from corrosion can also easily occur due to solder flux or similar materials adhering to leads while mounting the products on a board. This is because TCP product leads are formed by bonding very thin copper foil to the base film in order to attain high-density mounting.

3. To prevent electric breakdown when mounting TCP products on a board, do not allow any electrical contact with the die's bottom surface. These types of failures easily occur since TCP products have a bare Si monocrystal on the die's bottom surface in order to make the product as thin as possible.

   To prevent degradation of electrical characteristics, do not expose TCP products to sunlight.

Mechanical Handling

1. To prevent die cracks when mounting TCP products on a board, do not allow any physical contact with the die's bottom surface. These types of failures easily occur since TCP products have a bare Si monocrystal on the die's bottom surface in order to make the product as thin as possible.

2. Handle TCP products carefully to avoid bending the leads from base film transformation.

3. Do not bend TCP products since this may cause cracks in the solder resist.

4. Punching

Punching the continuous base film to extract single TCP products requires the following care.

- Align each product correctly according to tape perforations (sprocket holes).

- Use a metal punching die with pressing installation to prevent resin cracks and reduce cutting stresses in the outer leads. (Refer to figure 13.)

- Determine the punching position so that the cutting edge does not touch the molding area based on the relationship between maximum molding area (specified in the design drawing) and the punching die accuracy.

Punch TCP products in the section where outer leads are straight (not slanted) to prevent short-circuits caused by conductive particles. (Refer to figure 14.)

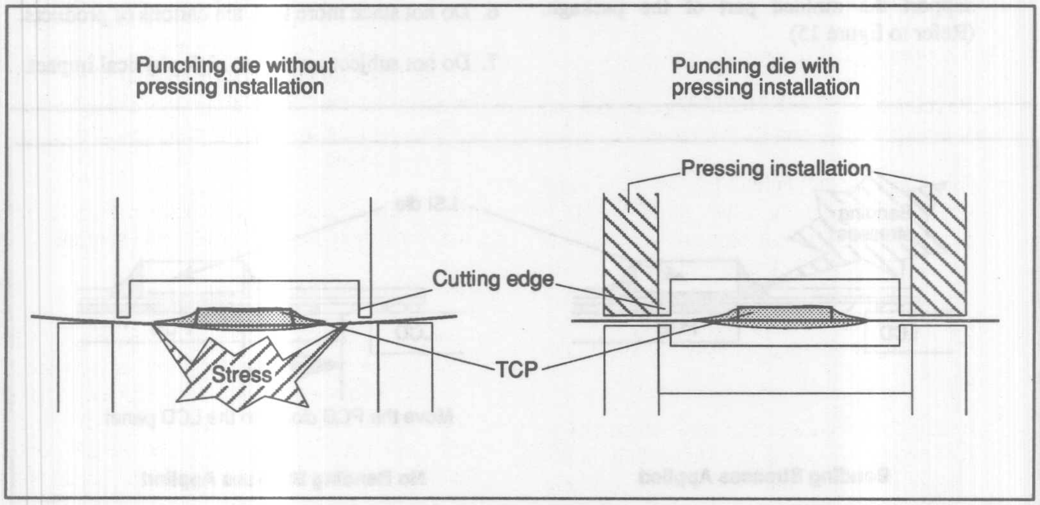


Figure 13 Punching Die

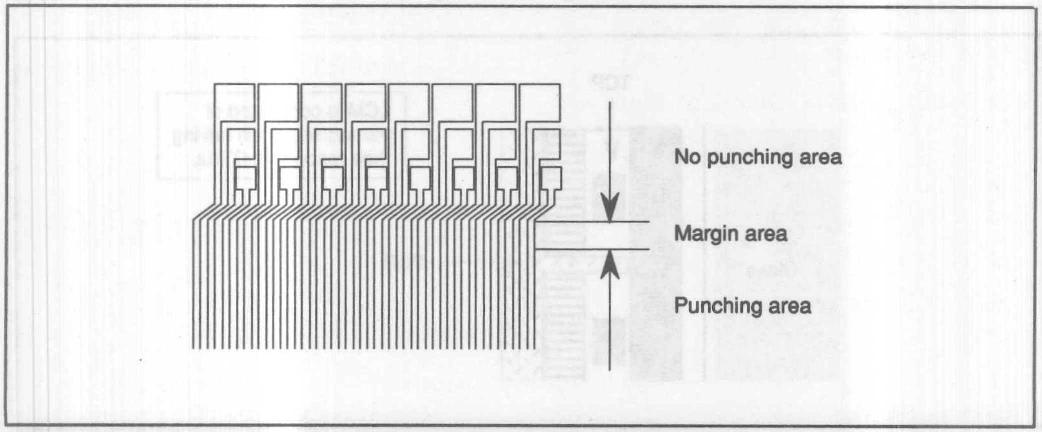


Figure 14 Punching Position

5. Mounting structure

Copper foil can easily break even from a small physical stress because of its thinness needed to accommodate fine patterns. Large stresses should therefore not be applied to the copper foil when mounting TCP products on a board.

- Bending stresses

When the edges of a die and a PCB are aligned, resin cracks may occur due to bending stresses. To avoid this problem, locate the board closer to the LCD panel so that it can support the molded part of the package. (Refer to figure 15)

- Thermal stresses

LCM consists of glass, TCPs and a glass-epoxy substrate having their respective coefficients of thermal expansion (CTE). This difference in expansion effects may cause "thermal stresses" that especially concentrate in TCPs. The joining structure of LCMs is roughly shown in figure 16. Before beginning mass production, investigate and determine a joining structure that reduces thermal stresses so as to prevent contact and other defects from occurring.

6. Do not stack more than ten cartons of products.

7. Do not subject cartons to high physical impact.

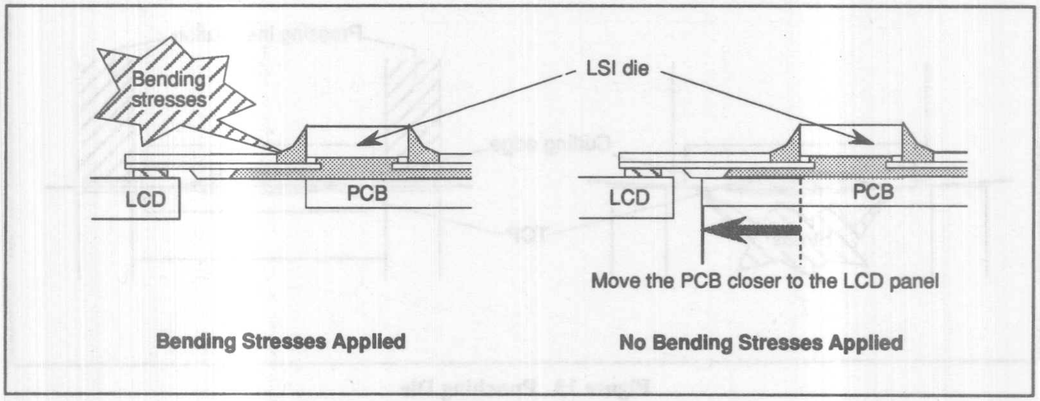


Figure 15 Positioning of Mounting TCPs on a PCB

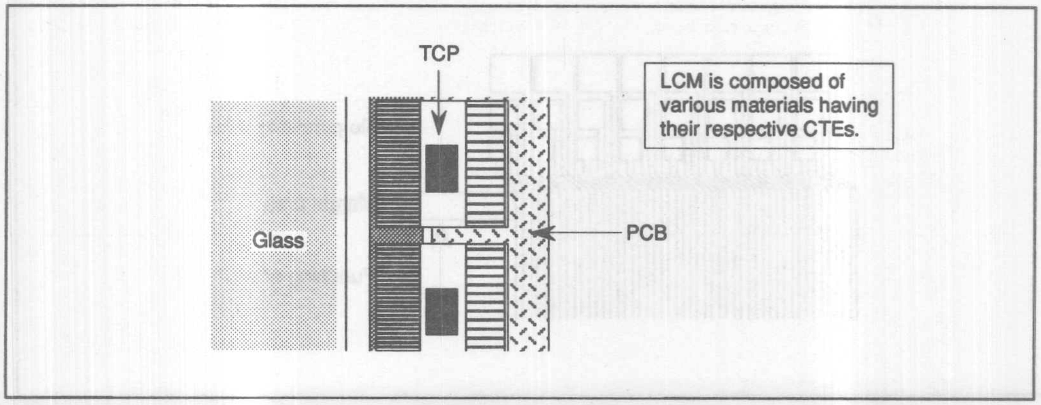


Figure 16 Joining Structure of LCM

Correction of ITO (Indium Tin Oxide) Electrode Pitch: TCP products expand by absorbing moisture or heat during storage and assembly. Pitch correction for the ITO electrode should be performed based on the TCP dimensions after it is mounted on a conductive film. However, if ITO pitch correction is performed based on TCP dimensions before mounting, it must be based on data measured after removing TCP products from the package and storing at a temperature of 20 to 25°C and a humidity of 50 to 70% RH for 48 hours.

Correct the ITO electrode pitch depending on the bonding equipment and conditions used.

Miscellaneous

1. Do not heat the lead tape and separator; they have poor heat-resistivity and will expand.
2. Do not subject TCPs to high temperature for a long period of time while cleaning or other operations; copper foil may peel off due to the rapid deterioration of adhesion between the copper foil and base film.
3. Carrier tapes have some waviness that may cause problems in tape transport. Use a tapeguide or equivalent to secure the tape.

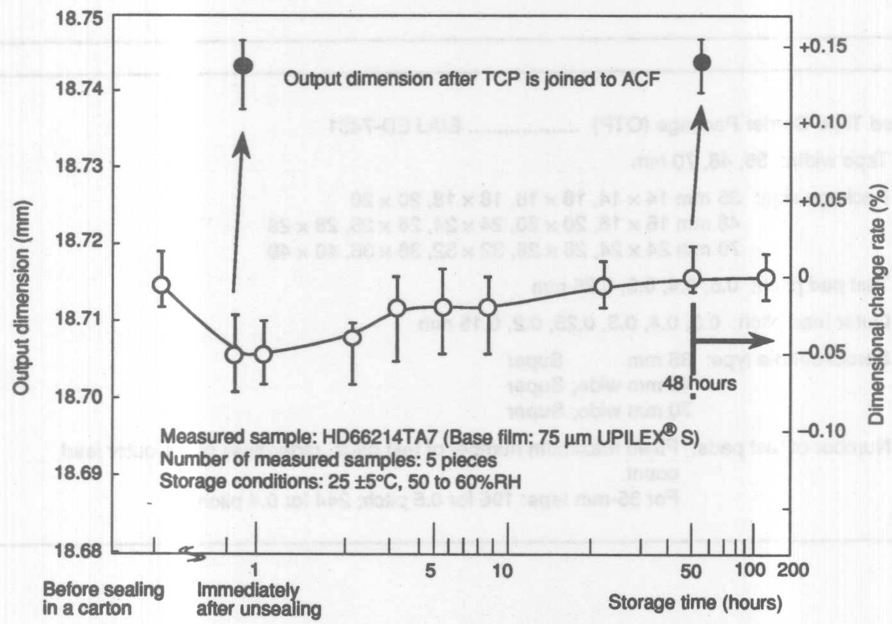


Figure 17 Dimensional Change of Output

TCP Standardization

The "Tape Carrier Package W/G" in the Semiconductor External Standards Committee of the EIAJ (Electronics Industries Association of Japan) has standardized TCPs having leads on four sides (EIAJ ED-7431('93.4)). The standardization W/G, which is composed of various semiconductor manufacturers including Hitachi, tape manufacturers, and socket manufacturers, is taking a comprehensive approach.

EIAJ has adopted metric control standard against JEDEC*'s inch control standards (UO-017) and has determined standards based on the following two items:

- Fixed test pad layout, variable package size
- Fixed package size, variable terminal pitch

Accordingly, users can share the socket by deciding the width of tape and the test pad pitch. As JEDEC has already agreed to the metric-control TCP (UO-018), Hitachi is now making efforts to produce metric-control TCPs.

The basic concept of TCP having leads on four sides by EIAJ is shown below. Standardization of TCP having leads on two sides is also under discussion.

Note: * JEDEC:
Joint Electronic Device Engineering Council.

Quad Tape Carrier Package (QTP) .... EIAJ ED-7431

1. Tape width: 35, 48, 70 mm
2. Package size: 35 mm 14 × 14, 16 × 16, 18 × 18, 20 × 20
   48 mm 16 × 16, 20 × 20, 24 × 24, 26 × 26, 28 × 28
   70 mm 24 × 24, 28 × 28, 32 × 32, 36 × 36, 40 × 40
3. Test pad pitch: 0.5, 0.4, 0.3, 0.25 mm
4. Outer lead pitch: 0.5, 0.4, 0.3, 0.25, 0.2, 0.15 mm
5. Sprocket-hole type: 35 mm Super
   48 mm wide, Super
   70 mm wide, Super
6. Number of test pads: Fixed maximum number of test pads, regardless of the outer lead count.
   For 35-mm tape: 196 for 0.5 pitch; 244 for 0.4 pitch.

Reference Materials

TCP Mounting Equipment Manufacturer

Manufacturer: Hitachi Chemical Co., Ltd.

Area	Address	Tel No.	Fax No.
USA	Hitachi Chemical Co., America, Ltd. 4 International Drive, Rye Brook, NY 10573, U.S.A.	(914) 934-2424	(914) 934-8991
Europe	Hitachi Chemical Europe Gm bH. Immermmstr. 43, D-4000 Düsseldorf 1, F. R. Germany	(211) 35-0366 to 9	(211) 16-1634
S.E. Asia	Hitachi Chemical Asia-Pacific Pte, Ltd. 51 Bras Basah Road, #08-04 Plaza By The Park, Singapore 0718	337-2408	337-7132
Taiwan	Hitachi Chemical Taipei Office Room No. 1406, Chia Hsim Bldg., No. 96, Sec. 2, Chung Shang Road N, Taipei, Taiwan	(2) 581-3632, (2) 561-3810	(2) 521-7509
Beijing	Hitachi Chemical Beijing Office Room No. 1207, Beijing Fortune Building, 5 Dong, San Huan Bei-Lu, Chao Yang District, Beijing, China	(1) 501-4331 to 2	(1) 501-4333
Hong Kong	Hitachi Chemical Co. (Hong Kong) Ltd. Room 912, Houston Centre, 63 Mady Road, Tsimshatsui East, Kowloon, Hong Kong	(3) 66-9304 to 7	(3) 723-3549

TCP

Manufacturer: Matsushita Electric Industrial Co., Ltd.

Area	Address	Tel No.	Fax No.
USA (Illinois)	Panasonic Factory Automation Company	(708) 452-2500	
Deutschland	Panasonic Factory Automation Deutchland	(040) 8549-2628	
Asia (Japan)	Matsushita Manufacturing Equipment D.	(0552) 75-6222	

Manufacturer: Shinkawa Co., Ltd.

Area	Address	Tel No.	Fax No.
U.S.A.	MARUBENI INTERNATIONAL ELECTRONICS CORP. U.S.A. 3285 Scott Blvd, Santa Clara, CA. 95054	408-727-8447	408-727-8370
Singapore, Malaysia, Thailand	MARUBENI INTERNATIONAL ELECTRONICS CORP. SINGAPORE 18 Tannery Lane #06-01/02, Lian Teng Building, SGB 1334	741-2300	741-4870
Korea, Hong Kong, China, Taiwan, Philippine, Brazil	MARUBENI HYTECH CORP. Japan 20-22, Koishikawa 4-chome, Bunkyo-ku, Tokyo 112, Japan	(03)-3817-4952	(03)-3817-4959
Europe	MARUBENI INTERNATIONAL ELECTRONICS EUROPE GMBH Niederrhein STR, 42 4000 Düsseldorf 30 Federal Republic of Germany	0211-4376-00	0211-4332-85

Manufacturer: Kyushu Matsushita Electric Co., Ltd.

Area	Address	Tel No.	Fax No.
CHICAGO	1240 Landmeier Rd. Elk Grove Village, IL 60007	(708) 822-7262	(708) 952-8079
ATLANTA	1080 Holcomb Bridge Rd. Building 100, Suite 300 Roswell, Georgia 30076	(404) 906-1515	(404) 998-9830
San Jose	177 Bovet Road, Suite 600 San Mateo, CA 99402	(415) 608-0317	(415) 341-1395
LONDON	238/246 King Street, London W6 ORF United Kingdom	(081) 748-2447	(081) 846-9580
SINGAPORE	1 Scotts Road, #21-10/13 Shaw Centre Singapore 0922	7387681	7325238
SEOUL	2ND Floor, Donghwa Bldg. 454-5, Dokok-1 Dong, Kangnam-Ku, Seoul, Korea	(02) 571-2911	(02) 571-2910
TAIWAN	6TH, FL., 360, FU HSING 1ST ROAD, KWEISHAN, TAOYUAN HSIEN, TAIWAN	(03) 328-7070	(03) 328-7080 (03) 328-7090
MALAYSIA	KUALALUMPUR BRANCH 8TH FLOOR, WISMA LEE RUBBER, JAPAN MELAKA, 50100 KUALALUMPUR	(03) 291-0066	(03) 291-8002
BANGKOK	20TH FL., Thaniya Plaza Bldg, 52 Silom Road, Bangrak, BANGKOK, 10500 THAILAND	(02) 231-2345	(02) 231-2342

Manufacturer: Japan Abionis Co., Ltd.

Area	Address	Tel No.	Fax No.
Worldwide	Overseas Department Contact: Mr. K. Asami, or Mr. K. Ito	81-3-3501-7358	81-3-3504-2829

TCP Tape Manufacturers

Manufacturer: Hitachi Cable Ltd.

Area	Address	Tel No.	Fax No.
U.S.A.	HITACHI CABLE AMERICA INC.	1-914-993-0991	001-1-914-993-0997
Europe	HITACHI CABLE INTERNATIONAL, LTD. (LONDON)	001-44-71-439-7223	001-44-71-494-1956
Sigapore	HITACHI CABLE INTERNATIONAL, LTD (SINGAPORE)	001-65-2681146	001-65-2680461
Hong Kong	HITACHI CABLE INTERNATIONAL, LTD (HONG KONG)	001-852-721-2077	001-852-369-3472

Manufacturer: Mitsui Mining and Smelting Co., Ltd.

Area	Address	Tel No.	Fax No.
U.S.A.	MITSUI MINING AND SMELTING CO. (USA) INC.	212-679-9300 to 2	212-679-9303
Europe	MITSUI MINING AND SMELTING CO., LTD. London Office	71-405-7717 to 8	71-405-0227
Asia	MITSUI MINING AND SMELTING CO., LTD. MICROCIRCUIT DIVISION	03-3246-8079	03-3246-8063

Manufacturer: Shindo Company Ltd.

Area	Address	Tel No.	Fax No.
U.S.A.	SHINDO COMPANY LTD., U.S. BRANCH OFFICE 2635 NORTH FIRST ST., STE. 124 SAN JOSE, CA 95134 U.S.A.	408-435-0808	408-435-0809

Aeolotropy Conductive Film Manufacturers

Manufacturer: Hitachi Chemical Co., Ltd.

Area	Address	Tel No.	Fax No.
USA	Hitachi Chemical Co., America, Ltd. 4 International Drive, Rye Brook, NY 10573, U.S.A.	(914) 934-2424	(914) 934-8991
Europe	Hitachi Chemical Europe GmbH. Immermannstr. 43, D-4000 Düsseldorf 1, F. R. Germany	(211) 35-0366 to 9	(211) 16-1634
S.E. Asia	Hitachi Chemical Asia-Pacific Pte, Ltd. 51 Bras Basah Road, #08-04 Plaza By The Park, Singapore 0718	337-2408	337-7132
Taiwan	Hitachi Chemical Taipei Office Room No. 1406, Chia Hsin Bldg., No. 96, Sec. 2, Chung Shang Road N, Taipei, Taiwan	(2) 581-3632, (2) 561-3810	(2) 521-7509
Beijing	Hitachi Chemical Beijing Office Room No. 1207, Beijing Fortune Building, 5 Dong, San Huan Bei-Lu, Chao Yang District, Beijing, China	(1) 501-4331 to 2	(1) 501-4333
Hong Kong	Hitachi Chemical Co. (Hong Kong) Ltd. Room 912, Houston Centre, 63 Mady Road, Tsimshatsui East, Kowloon, Hong Kong	(3) 66-9304 to 7	(3) 723-3549

Manufacturer: Sony Chemicals

Area	Address	Tel No.	Fax No.
U.S.A.	SONY CHEMICALS CORPORATION OF AMERICA	1-(708) 616-0070	1-(708) 616-0073
Europe	SONY CHEMICALS EUROPE B.V.	31-20-658-1850	31-20-659-8481
Southeast Asia	SONY CHEMICALS SINGAPORE PTE LTD.	65-382-1500	65-382-1750

References

1. KAPTON® V Catalog — Du Pont-Toray Co., Ltd.
2. UPILEX® S Catalog — Ube Industries, Ltd.
3. Electro-deposited Foil Comparison List — Mitsui Mining Smelting Co., Ltd. Electronic Devices Group
4. Hitachi Anisotropic Discharge Film — Hitachi Chemical Co., Ltd. 1992.7.21

Hitach Standard TCP Product Structure

Hitachi can provide the standard TCP products listed in table 7 immediately. Figures 18 to 50 show the structure of each TCP product.

Table 7 Hitachi Standard TCP Product Specifications

No.	Product	Function	No. of Outputs	Output Lead Pitch (µm)	Output Lead Length (mm)	Input Lead Pitch (µm)	Input Lead Length (mm)	Input Lead Arrange*1	User Pattern Area Width X (mm)	User Pattern Area Width Y (mm)	Solder Resist Width (mm)	Product Length*2	Tape Material*3	Plating
1	HD66107T00	LCD driver	160	280	2.5	800	2.0	A	50.20	20.25	46.80	12	K	Sn
2	HD66107T01	LCD driver	80	280	2.5	800	2.0	A	32.00	20.25	28.00	12	K	Sn
3	HD66107T11	LCD driver	160	180	3.3	800	2.5	A	32.42	20.00	31.60	8	K	Sn
4	HD66107T12	LCD driver	160	250	3.3	800	2.5	A	43.50	20.00	42.40	10	K	Sn
5	HD66107T24	LCD driver	160	180	3.3	800	2.5	A	32.52	20.00	31.60	8	U	Sn
6	HD66107T25	LCD driver	80	280	2.5	800	2.0	A	32.00	20.25	28.00	8	K	Sn
7	HD66108T00	LCD driver	165	400	2.0	400	2.0	C	—	—	—	8	K	Sn
8	HD66300T00	TFT analog driver	120	300	2.9	800	3.0	A	46.00	21.50	46.20	10	K	Sn
9	HD66310T00	TFT 8 level gray scale	160	180	3.0	650	2.5	A	33.40	21.00	31.95	8	K	Sn
10	HD66330TA0	TFT 64 level gray scale	192	160	3.5	650	1.5	A	35.30	11.70	33.60	4	U	Sn
11	HD66214TA1	Column LCD driver	80	150	3.0	800	2.2	A	15.75	10.50	13.60	3	U	Sn
12	HD66214TA2	Column LCD driver	80	180	3.0	800	2.2	A	18.30	10.50	18.40	3	U	Sn
13	HD66214TA3	Column LCD driver	80	200	2.5	800	2.2	A	20.00	9.80	19.80	3	U	Sn
14	HD66214TA6	Column LCD driver	80	200	2.3	450	2.0	B	22.70	8.00	22.50	3	U	Sn
15	HD66214TA9L	Column LCD driver	80	220	2.3	450	1.8	B	22.70	8.00	22.50	2	U	Sn
16	HD66205TA1	Common LCD driver	80	150	3.0	800	2.0	A	15.75	14.70	13.40	4	U	Sn
17	HD66205TA2	Common LCD driver	80	180	2.9	800	2.0	A	18.30	14.70	16.40	4	U	Sn
18	HD66205TA3	Common LCD driver	80	200	3.0	800	2.0	A	20.00	14.70	17.80	4	U	Sn
19	HD66205TA6	Common LCD driver	80	220	2.8	700	1.8	B	22.70	12.50	18.20	4	U	Sn
20	HD66205TA7	Common LCD driver	80	250	2.8	700	1.8	B	24.25	12.50	18.20	4	U	Sn
21	HD66205TA9L	Common LCD driver	80	220	2.8	700	1.8	B	22.70	12.50	18.20	3	U	Sn
22	HD66224TA1	Column LCD driver	80	210	3.2	800	1.2	A	20.30	8.20	18.00	2	U	Sn
23	HD66224TA2	Column LCD driver	80	200	3.3	780	1.3	A	18.40	9.00	17.80	3	U	Sn
24	HD66224TB0	Column LCD driver	80	200	2.5	650	1.5	A	18.20	7.80	17.40	2	U	Sn
25	HD66215TA0	Common LCD driver	100	230	2.0	1200	1.7	A	25.60	11.90	24.40	3	U	Sn
26	HD66215TA1	Common LCD driver	101	220	3.0	1000	1.8	A	25.00	10.80	24.40	3	U	Sn
27	HD66215TA2	Common LCD driver	100	180	4.0	850	1.5	A	20.40	11.40	19.80	3	U	Sn
28	HD66110TA4	Column LCD driver	160	80	2.8	500	1.5	A	15.60	9.66	15.00	4	U	Sn
29	HD66110RTA8	Column LCD driver	160	140	3.2	600	2.0	A	25.00	10.85	15.00	4	U	Sn
30	HD66110RTB0	Column LCD driver	160	92	3.8	500	2.0	A	15.60	11.90	15.10	4	U	Sn
31	HD66110RTB1	Column LCD driver	160	92	2.4	500	1.2	A	15.60	9.00	15.10	4	U	Sn
32	HD66115TA0	Common LCD driver	160	180	3.0	800	2.0	A	32.40	11.00	31	3	U	Sn
33	HD66115TA1	Common LCD driver	160	250	4.2	800	2.0	A	44.00	13.70	42.9	4	U	Sn

Notes: 1. Input lead arrange: A = Straight, B = Divided, C = Directions
2. Number of perforations
3. Tape material: K = Kapton, U = Upilex
"Kapton" is a trademark of Dupont, Ltd.
"Upilex" is a trademark of Ube Industries, Ltd.

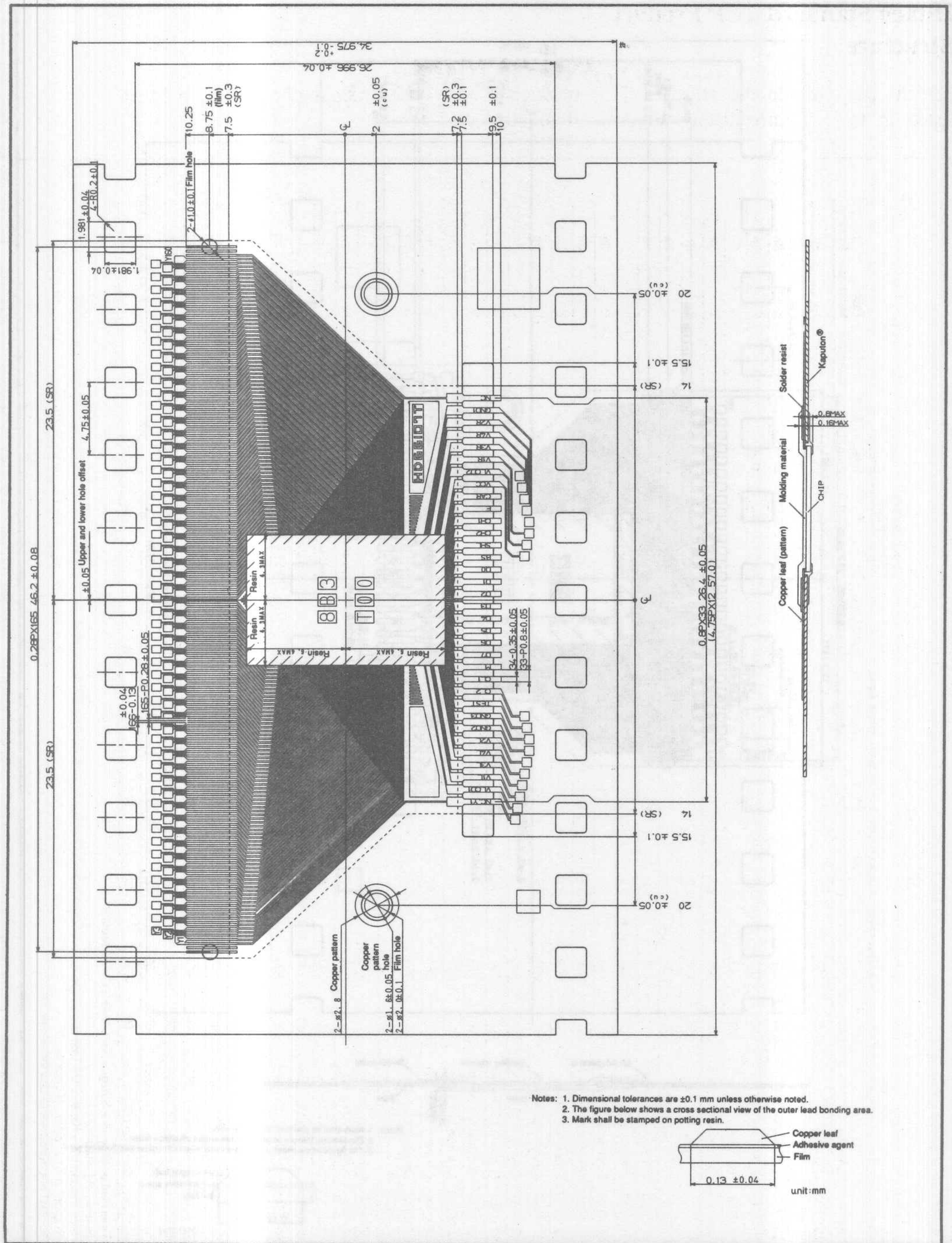


Figure 18 Hitachi Standard TCP 1 — HD61107T00 —

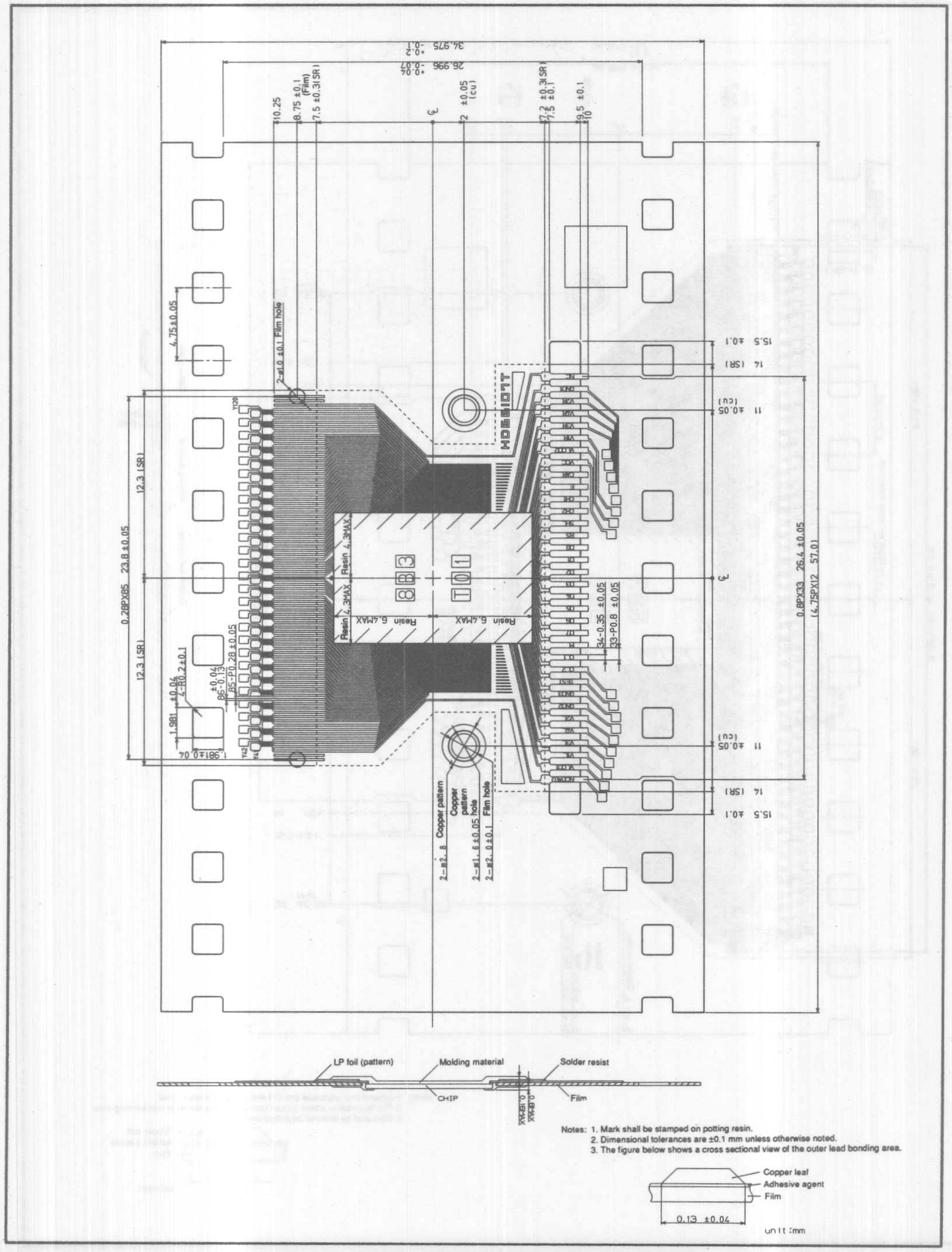


Figure 19 Hitachi Standard TCP 2 — HD66107T01 —

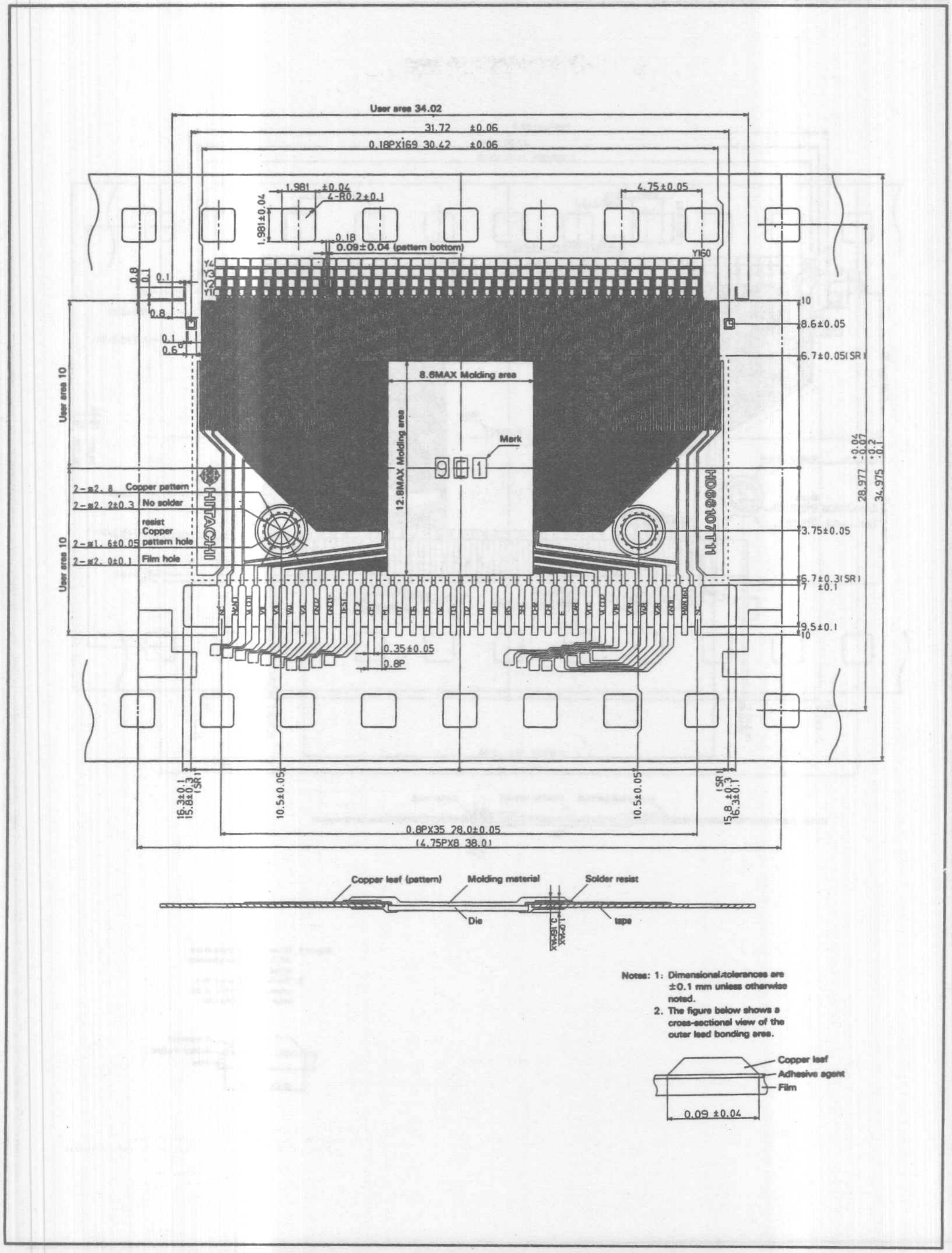
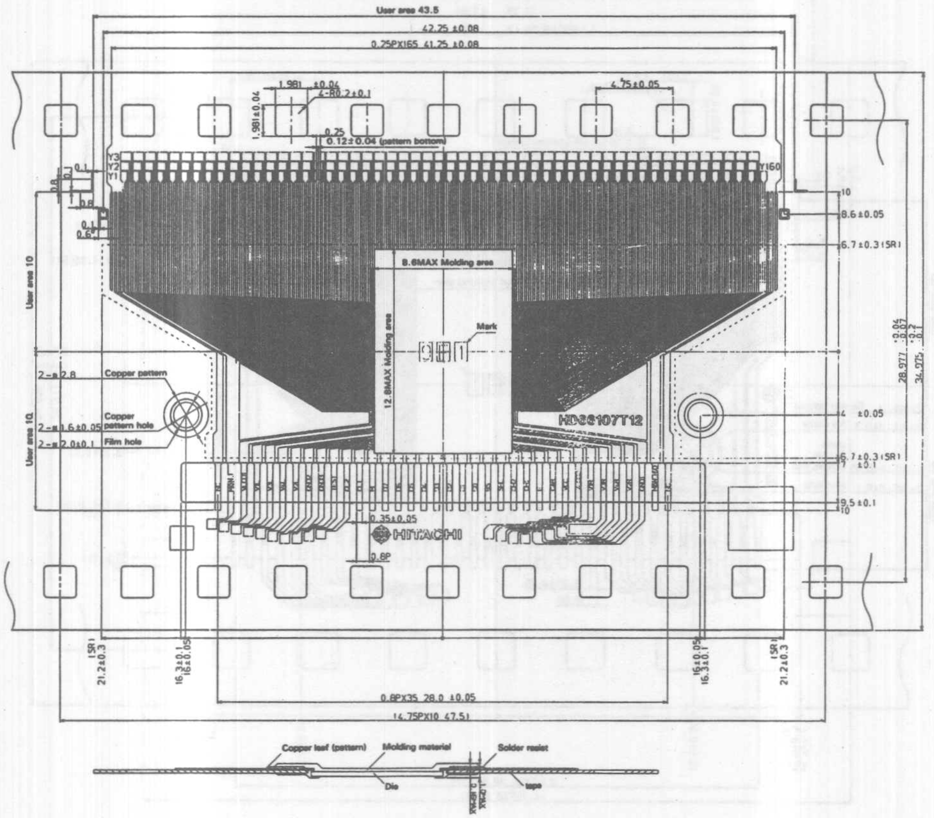


Figure 20 Hitachi Standard TCP 3 — HD66107T11 —



Notes: 1. Dimensional tolerances are ±0.1 mm unless otherwise noted.
2. The figure below shows a cross-sectional view of the outer lead bonding area.

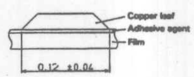


Figure 21 Hitachi Standard TCP 4 — HD66107T12 —

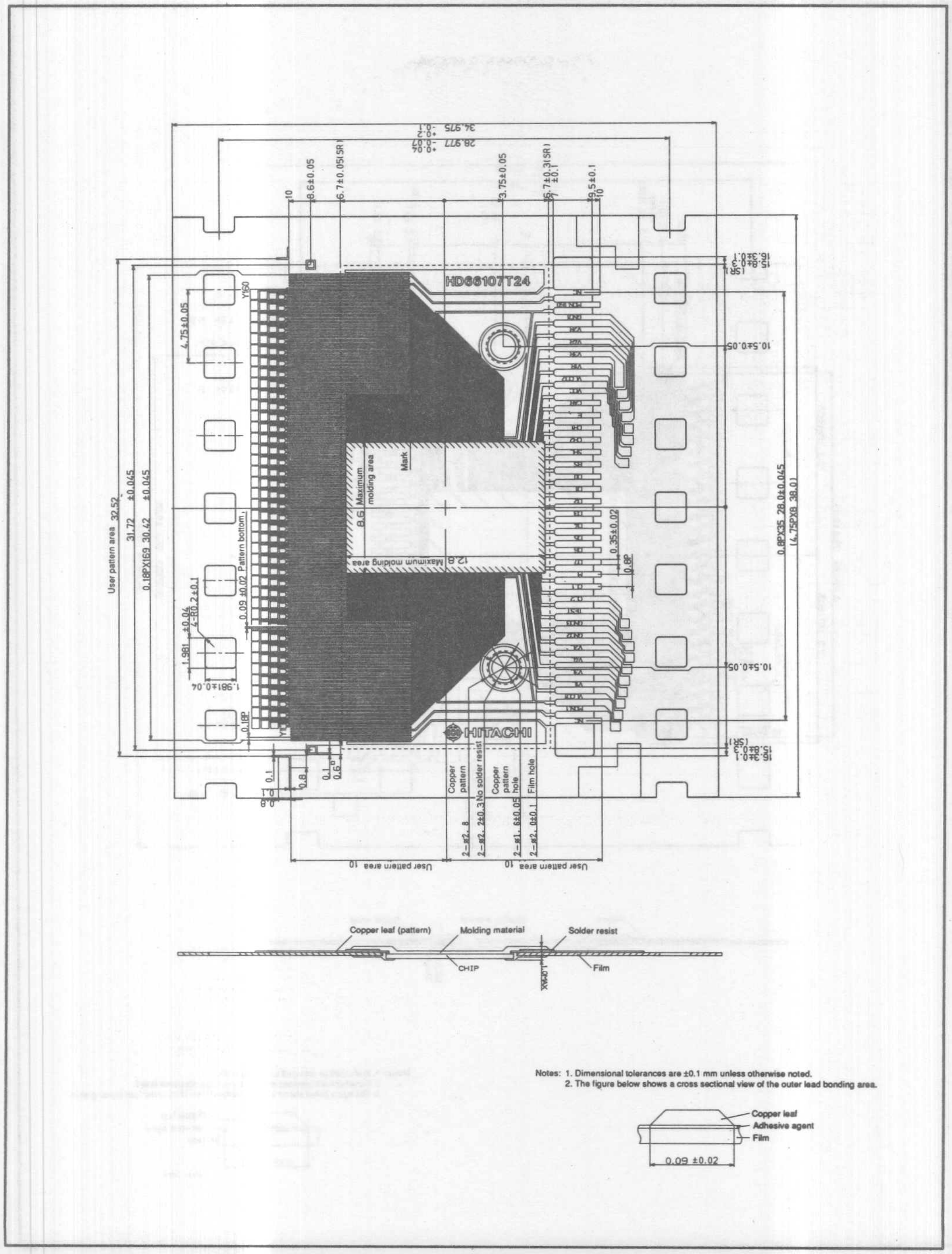
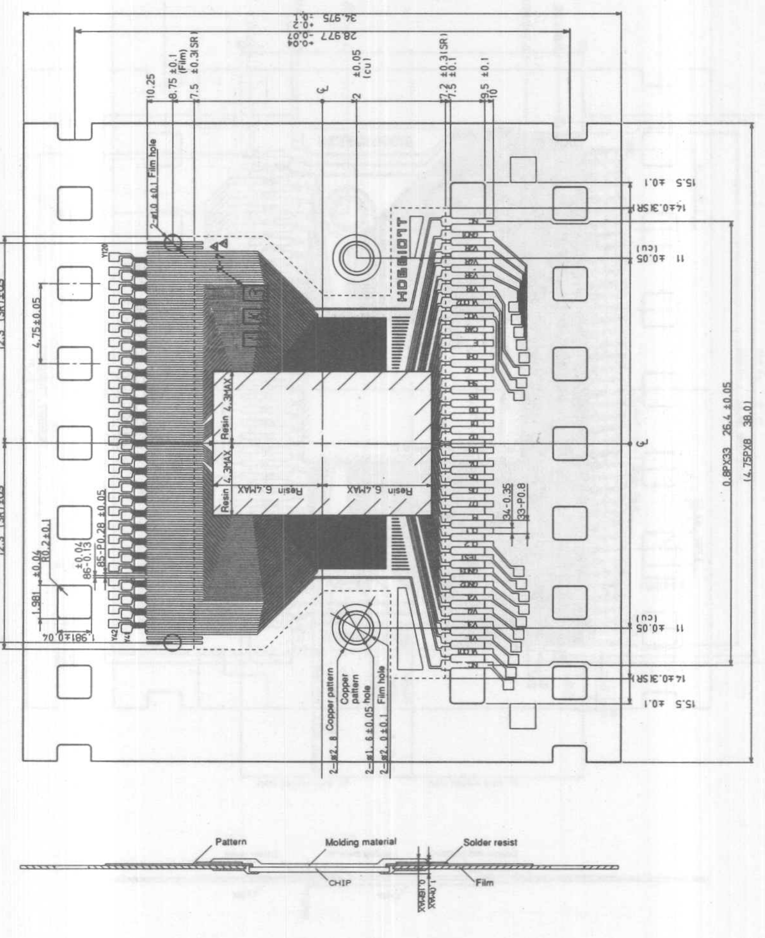
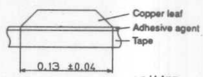


Figure 22 Hitachi Standard TCP 5 — HD66107T24 —

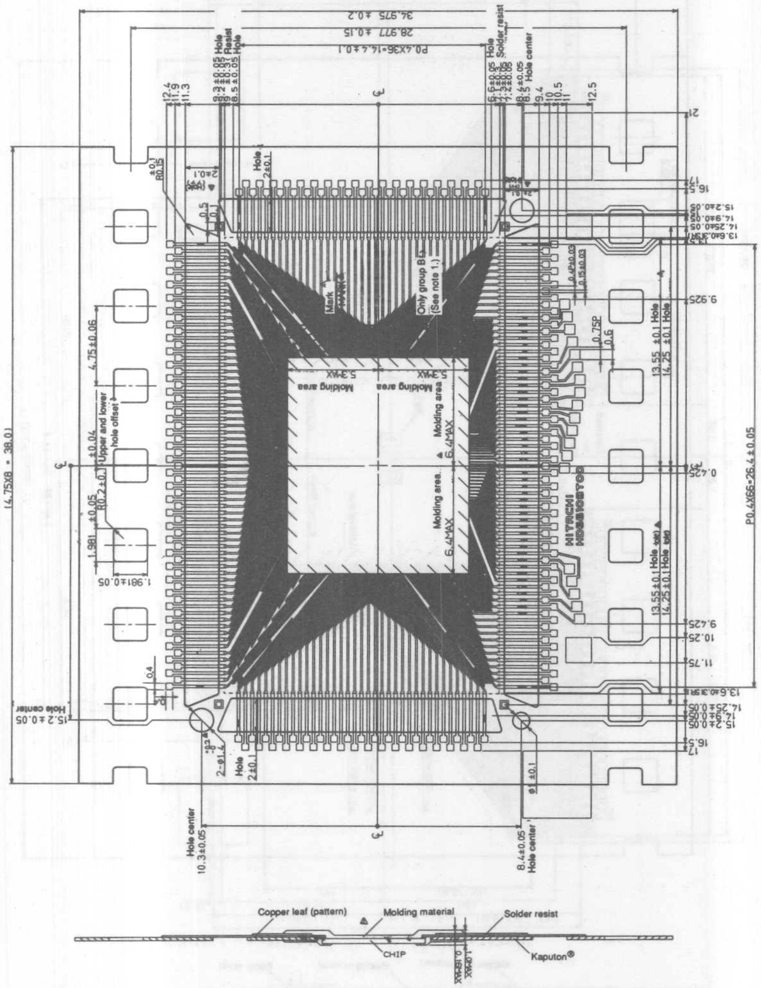


Notes: 1. Mark shall be stamped on potting resin.
2. Dimensional tolerances are ±0.1 mm unless otherwise noted.
3. The figure below shows a cross sectional view of the outer lead bonding area.



unit :mm

Figure 23 Hitachi Standard TCP 6 — HD66107T25 —



Note 1: Mark specifications

Group	Code
A	Only the year, month, and week code
B	The year, month, week code, and "P"

UNIT : mm

- Intersection dimensions are to be read from the figure unless otherwise noted.
- Dimensional tolerances are ±0.1 mm unless otherwise noted.
- Tolerance for deviation between pattern and hole centers is ±0.05 mm.
- A mark is stamped on the shaded area, which is to the right of the molded area within the solder resist.

Figure 24 Hitachi Standard TCP 7 — HD66108T00 —

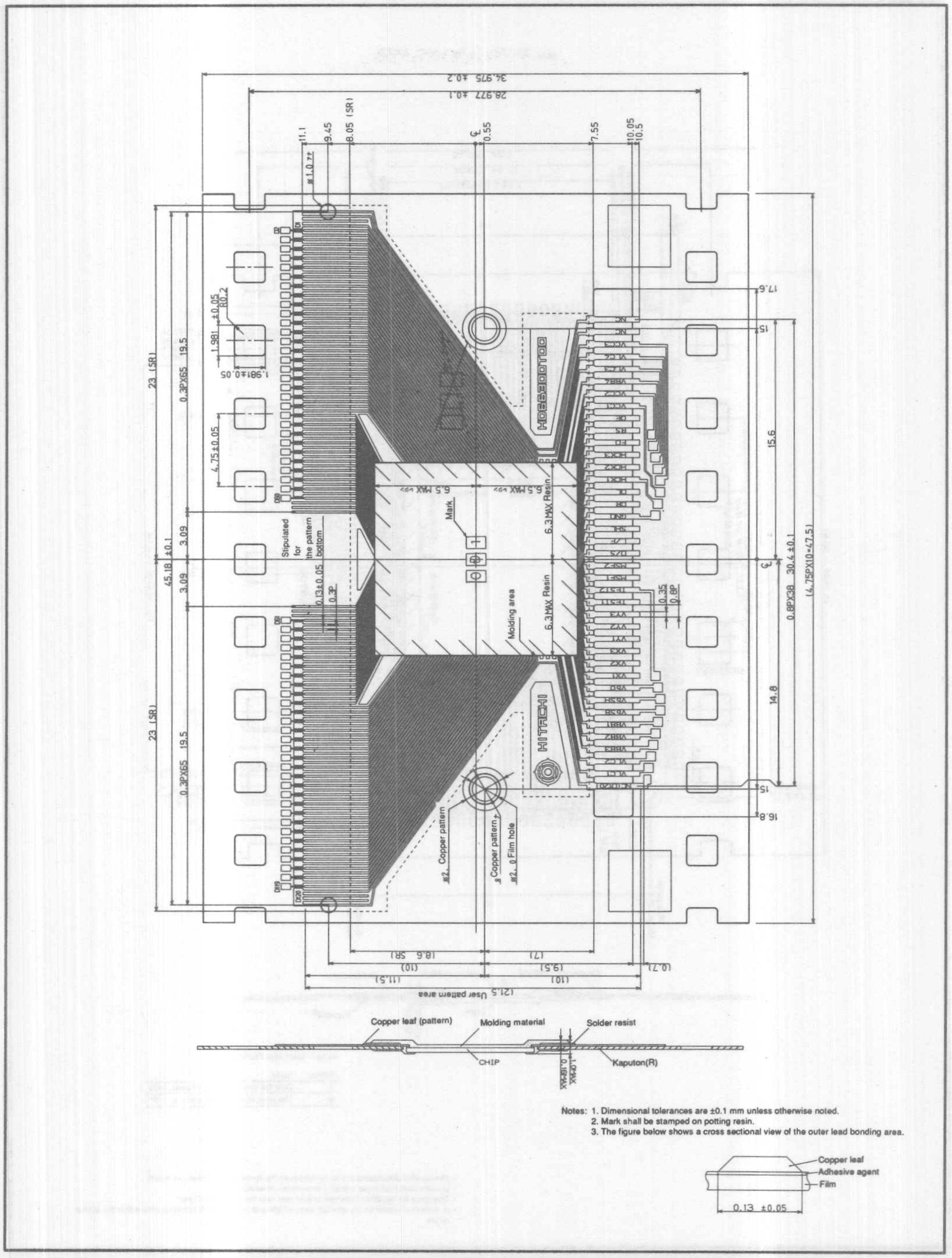


Figure 25 Hitachi Standard TCP 8 — HD66300T00 —

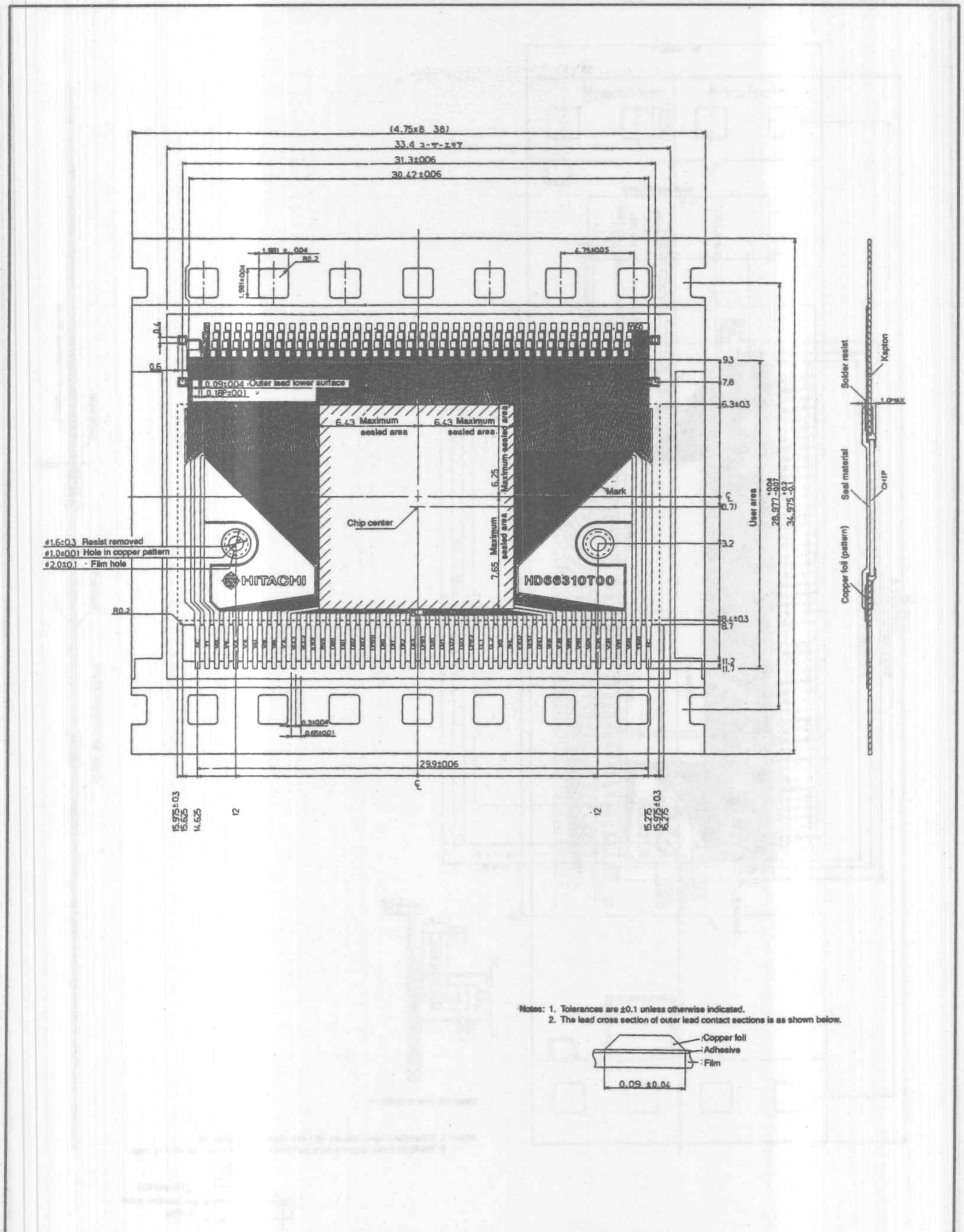


Figure 26 Hitachi Standard TCP 9 — HD66310T00 —

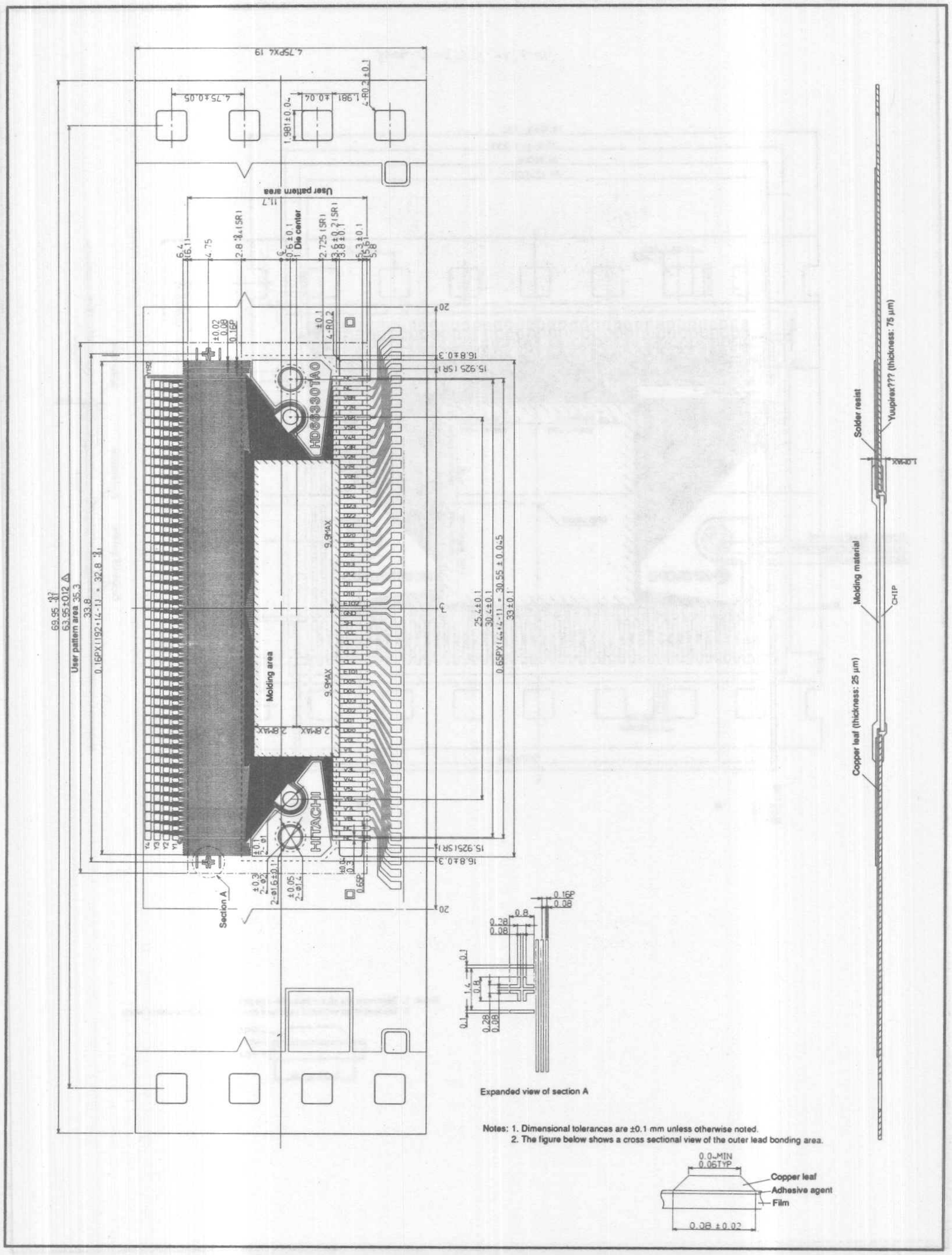


Figure 27 Hitachi Standard TCP 10 — HD66330TA0 —

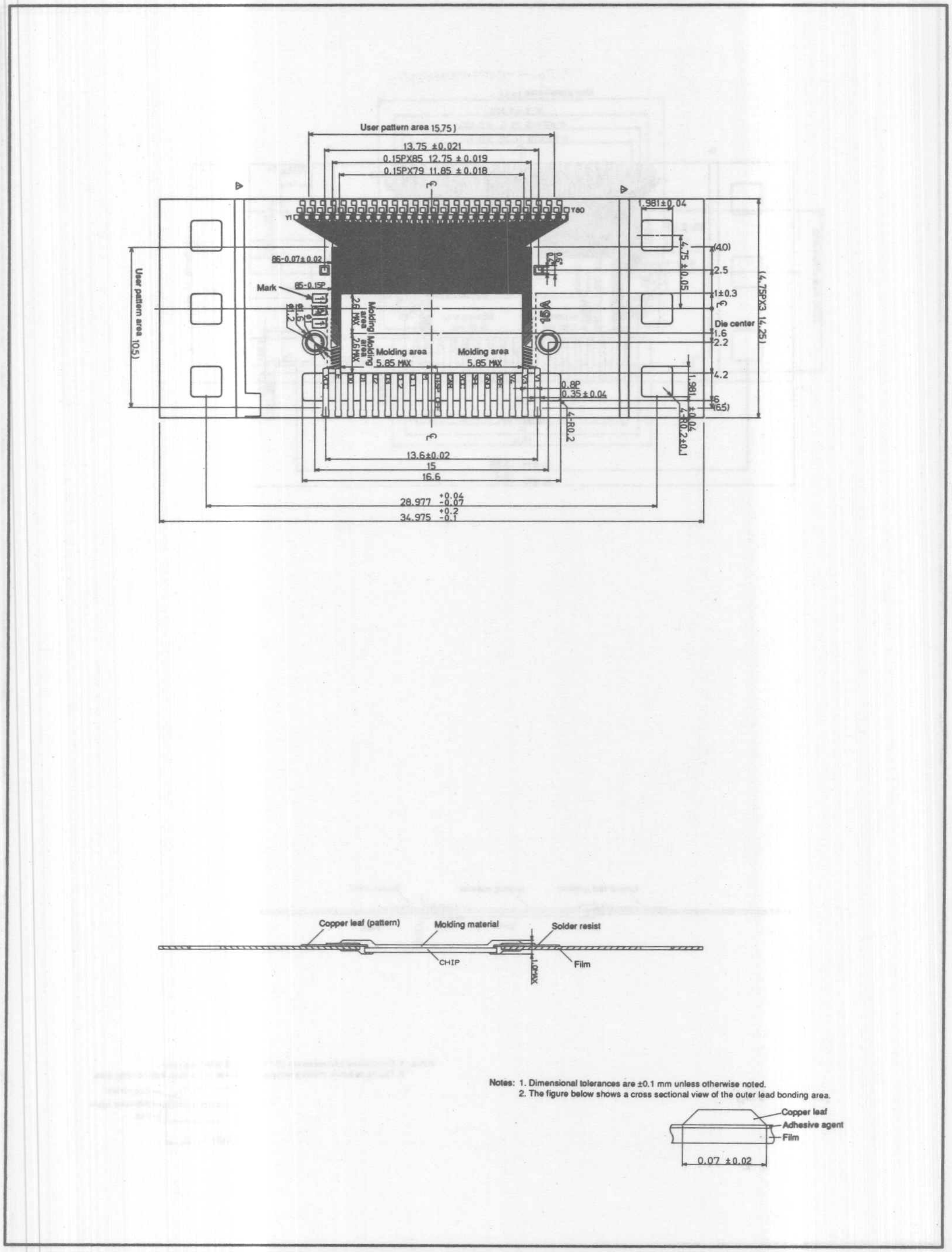
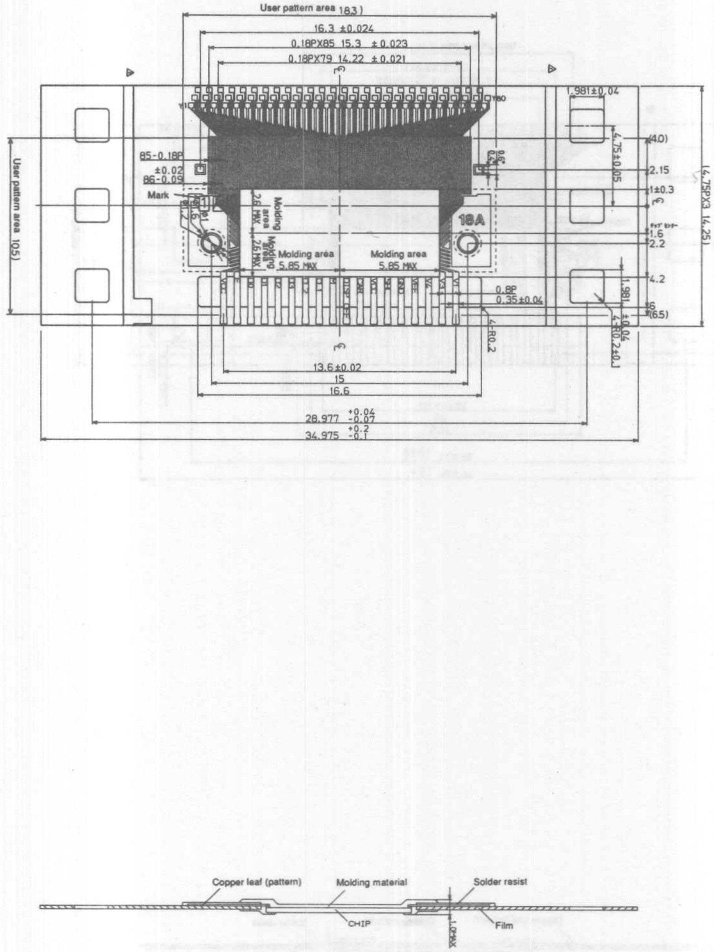


Figure 28 Hitachi Standard TCP 11 — HD66214TA1 —



Notes: 1. Dimensional tolerances are ±0.1 mm unless otherwise noted.
2. The figure below shows a cross sectional view of the outer lead bonding area.

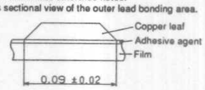
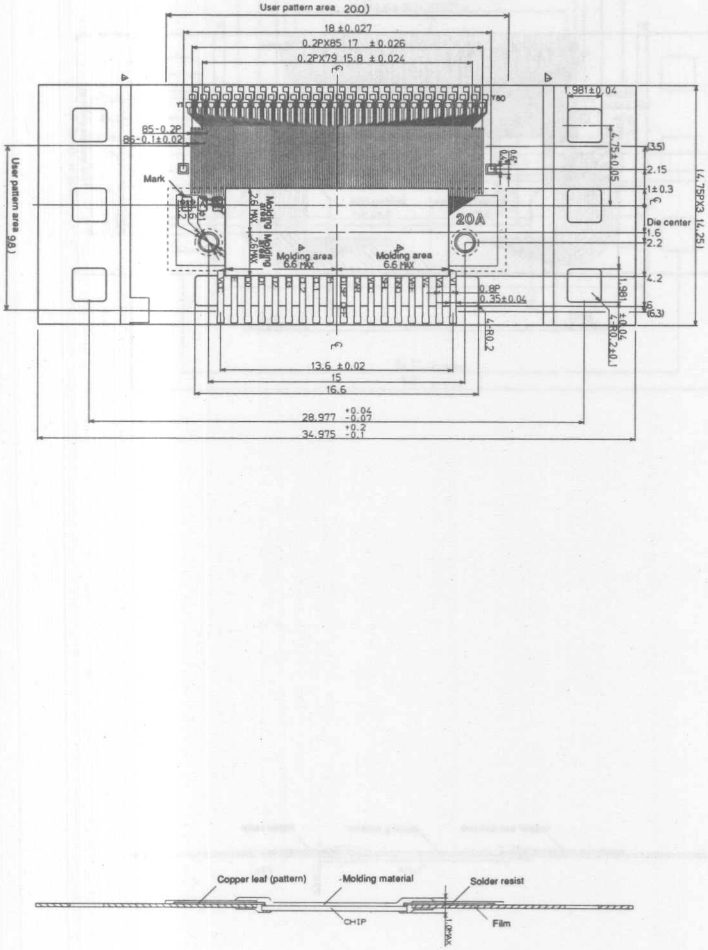


Figure 29 Hitachi Standard TCP 12 — HD66214TA2 —



Notes: 1. Dimensional tolerances are ±0.1 mm unless otherwise noted.
2. The figure below shows a cross sectional view of the outer lead bonding area.

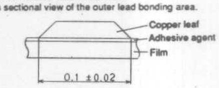


Figure 30 Hitachi Standard TCP 13 — HD66214TA3 —

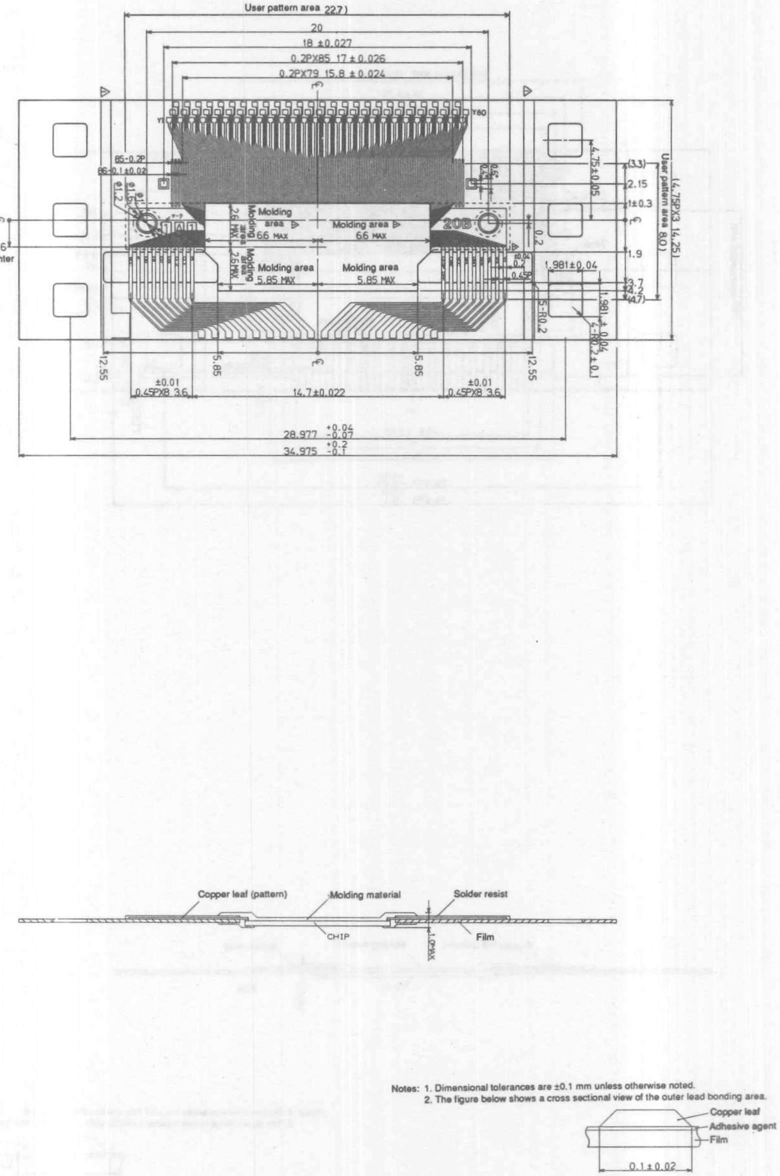


Figure 31 Hitachi Standard TCP 14 — HD66214TA6 —

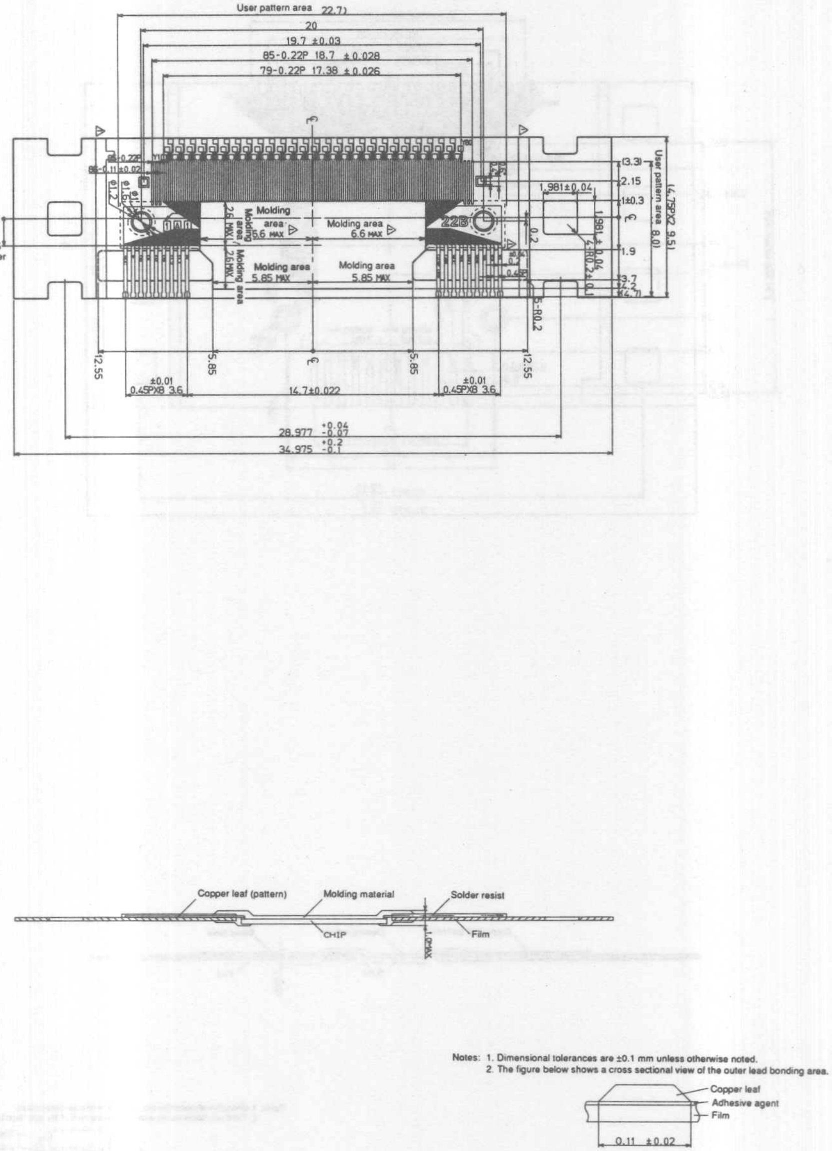
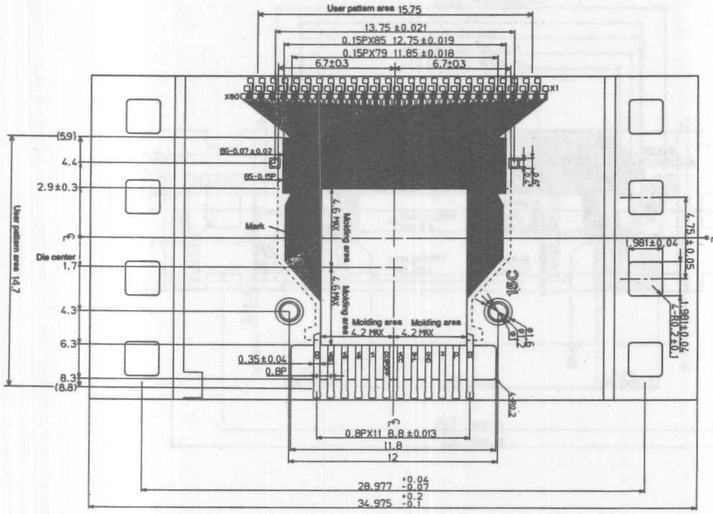
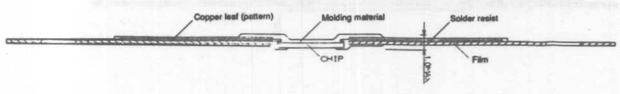


Figure 32 Hitachi Standard TCP 15 — HD66214TA9L —





Notes: 1. Dimensional tolerances are ±0.1 mm unless otherwise noted.
2. The figure below shows a cross sectional view of the outer lead bonding area.

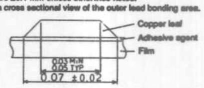
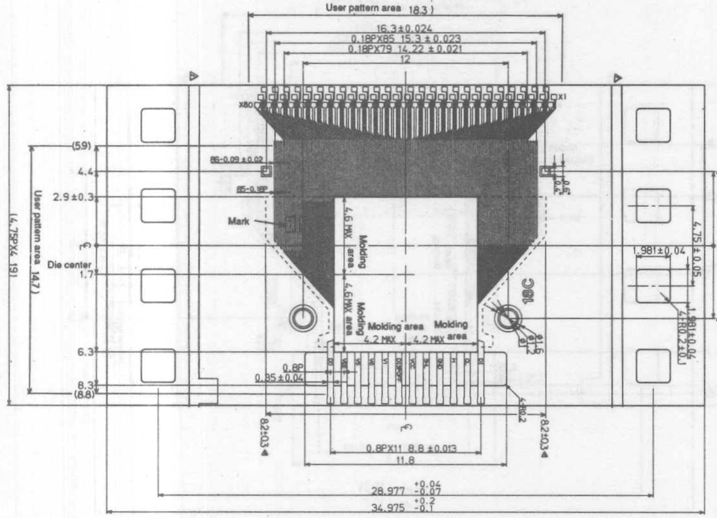
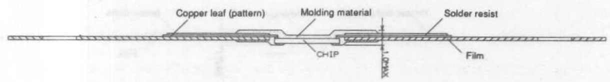


Figure 33 Hitachi Standard TCP 16 — HD66205TA1 —





Notes: 1. Dimensional tolerances are ±0.1 mm unless otherwise noted.
2. The figure below shows a cross sectional view of the outer lead bonding area.

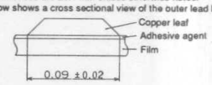
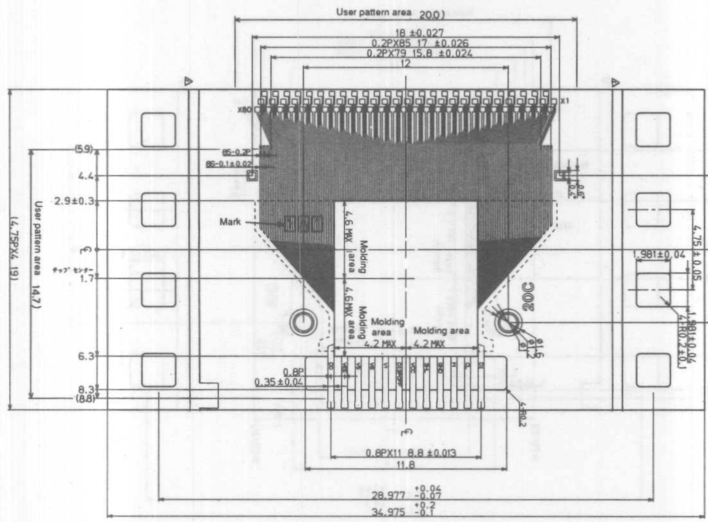
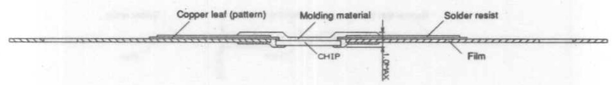


Figure 34 Hitachi Standard TCP 17 — HD66205TA2 —





Notes: 1. Dimensional tolerances are ±0.1 mm unless otherwise noted.
2. The figure below shows a cross sectional view of the outer lead bonding area.

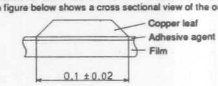
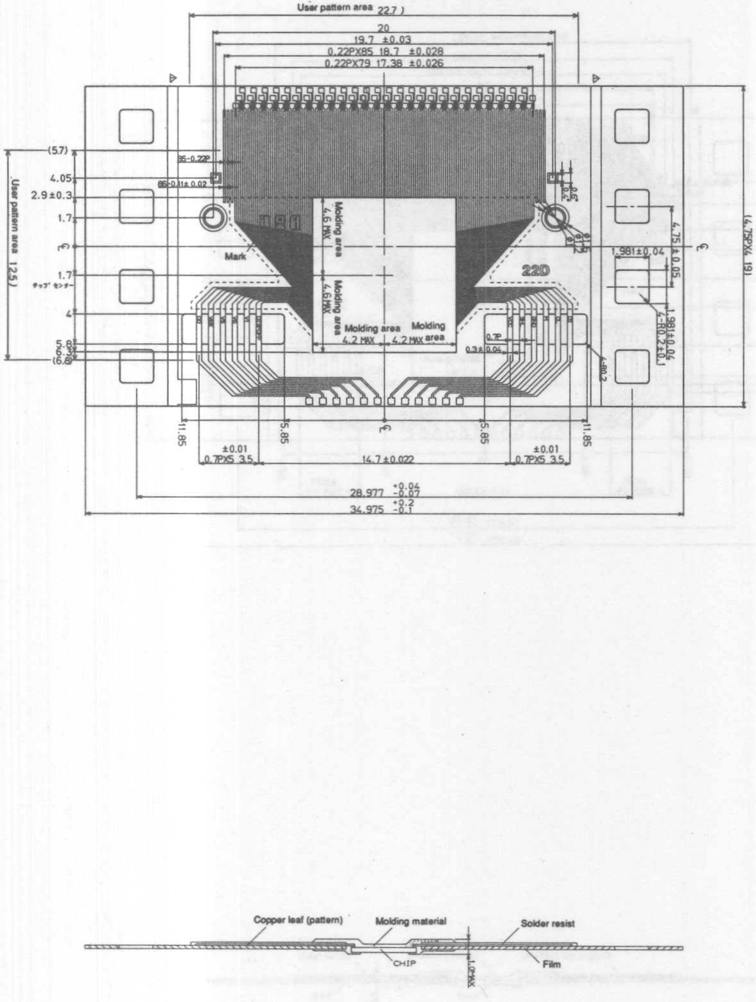


Figure 35 Hitachi Standard TCP 18 — HD66205TA3 —



Notes: 1. Dimensional tolerances are ±0.1 mm unless otherwise noted.
2. The figure below shows a cross sectional view of the outer lead bonding area.

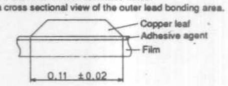


Figure 36 Hitachi Standard TCP 19 — HD66205TA6 —

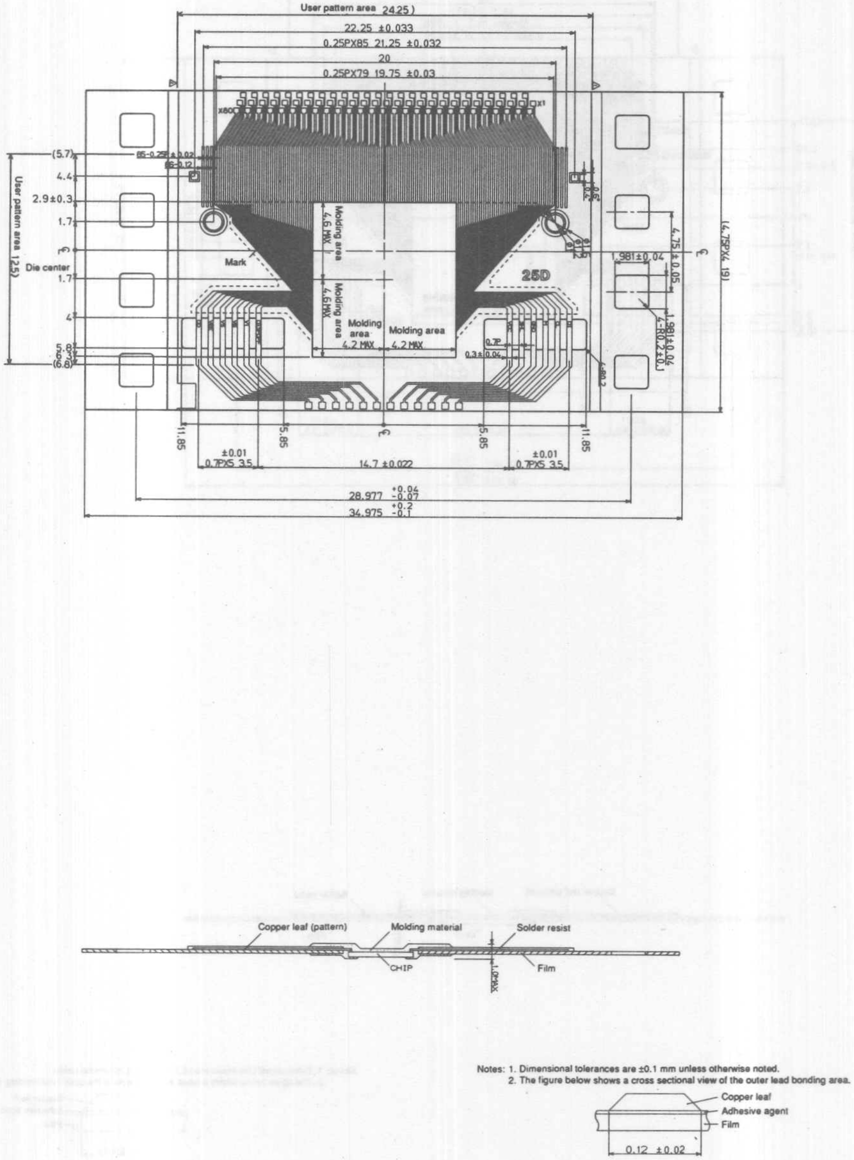


Figure 37 Hitachi Standard TCP 20 — HD66205TA7 —

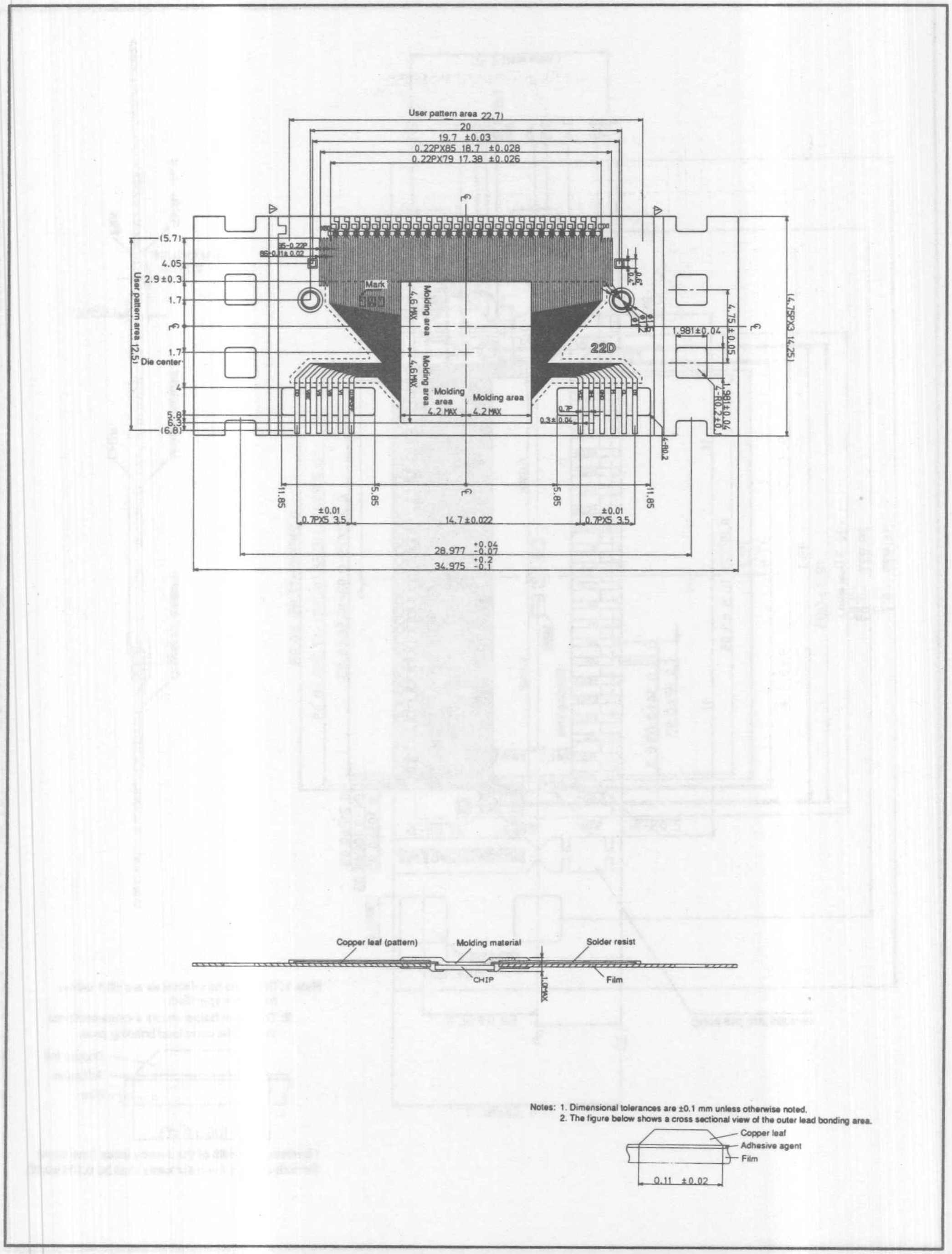
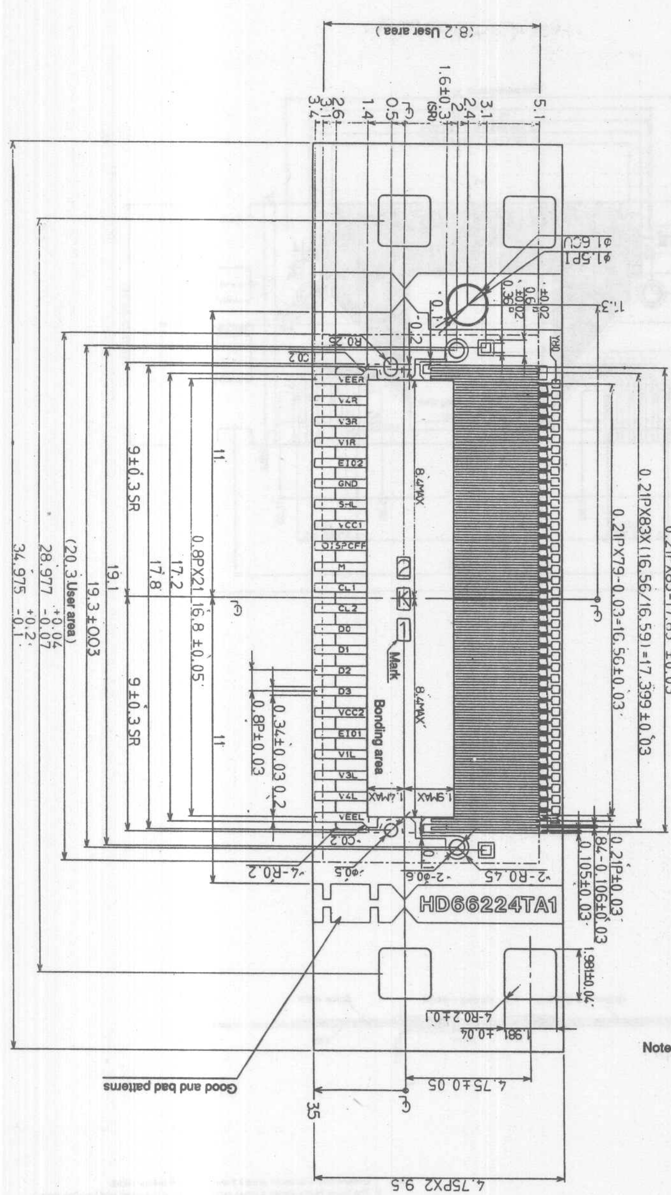
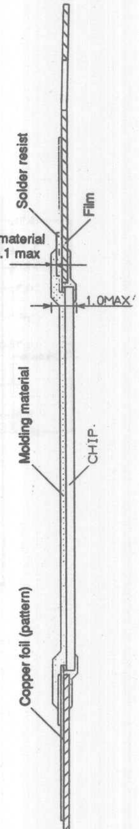
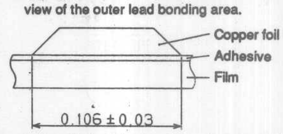


Figure 38 Hitachi Standard TCP 21 — HD66205TA9L —

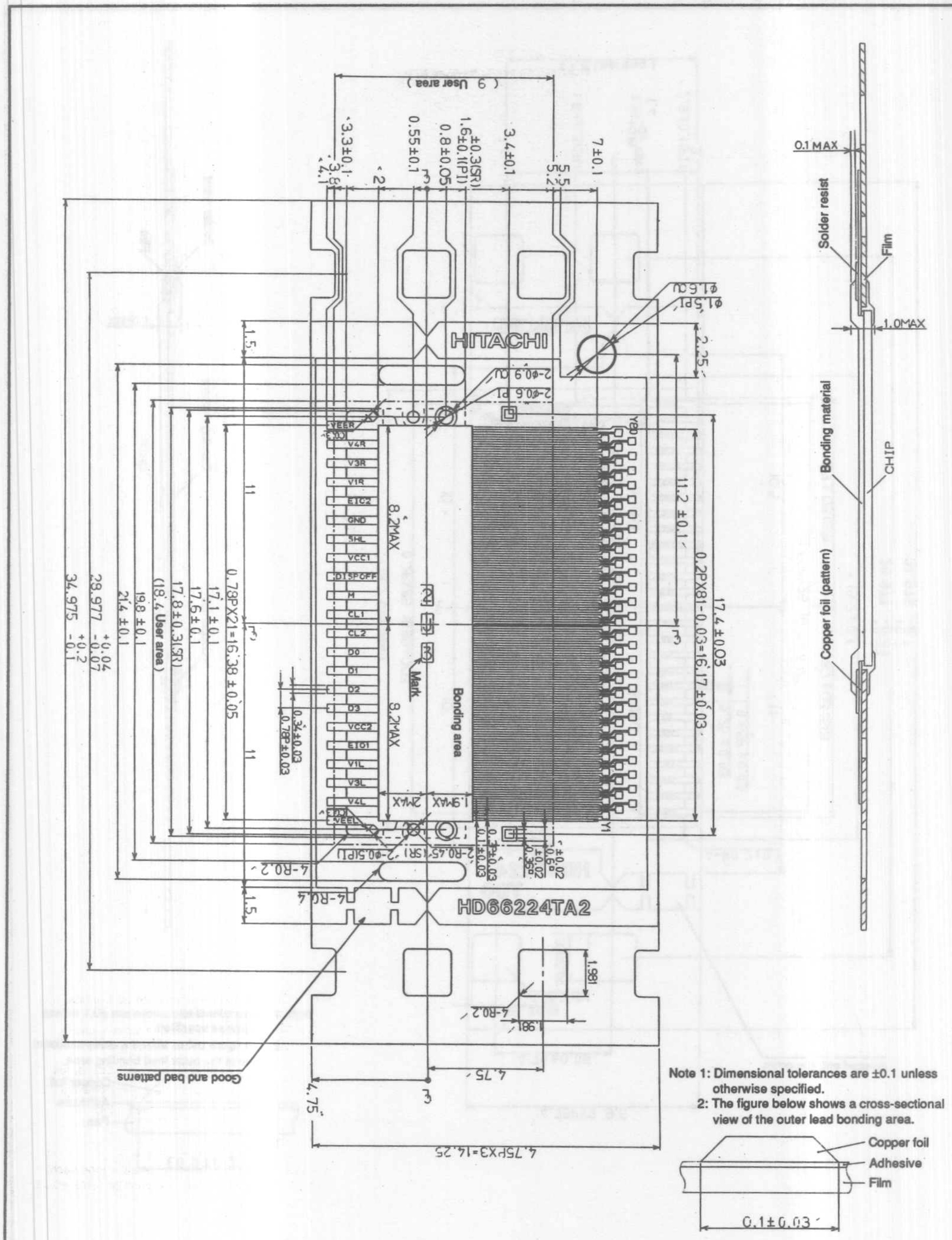
Note 1: Dimensional tolerances are ±0.1 unless otherwise specified.

2: The figure below shows a cross-sectional view of the outer lead bonding area.



However, the width of the dummy leads (one each) for both sides of the outer leads shall be 0.105 ±0.03.

Figure 39 Hitachi Standard TCP 22 — HD66224TA1 —



Note 1: Dimensional tolerances are ±0.1 unless otherwise specified.
2: The figure below shows a cross-sectional view of the outer lead bonding area.

Figure 40 Hitachi Standard TCP 23 — HD66224TA2 —

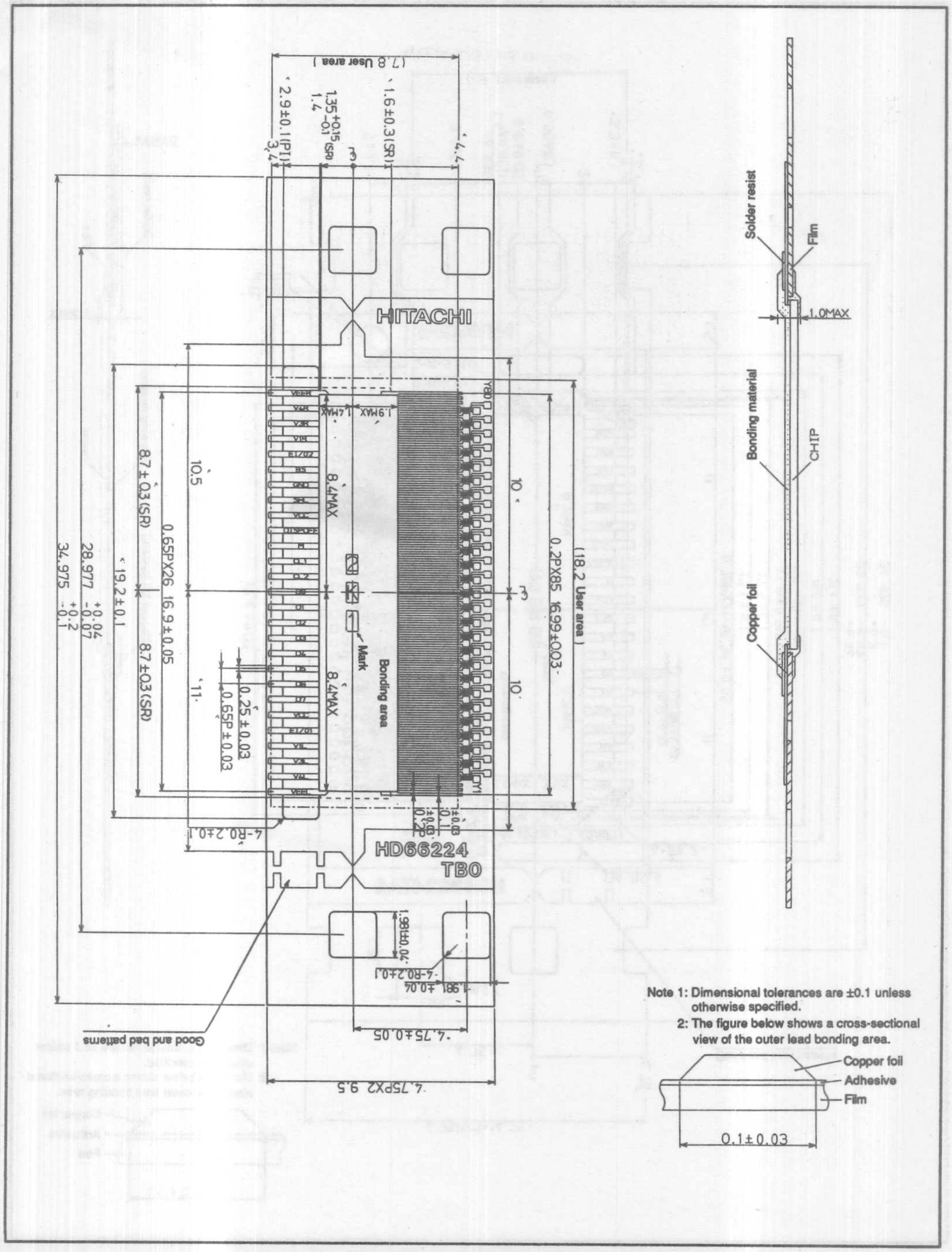


Figure 41 Hitachi Standard TCP 24 — HD66224TB0 —

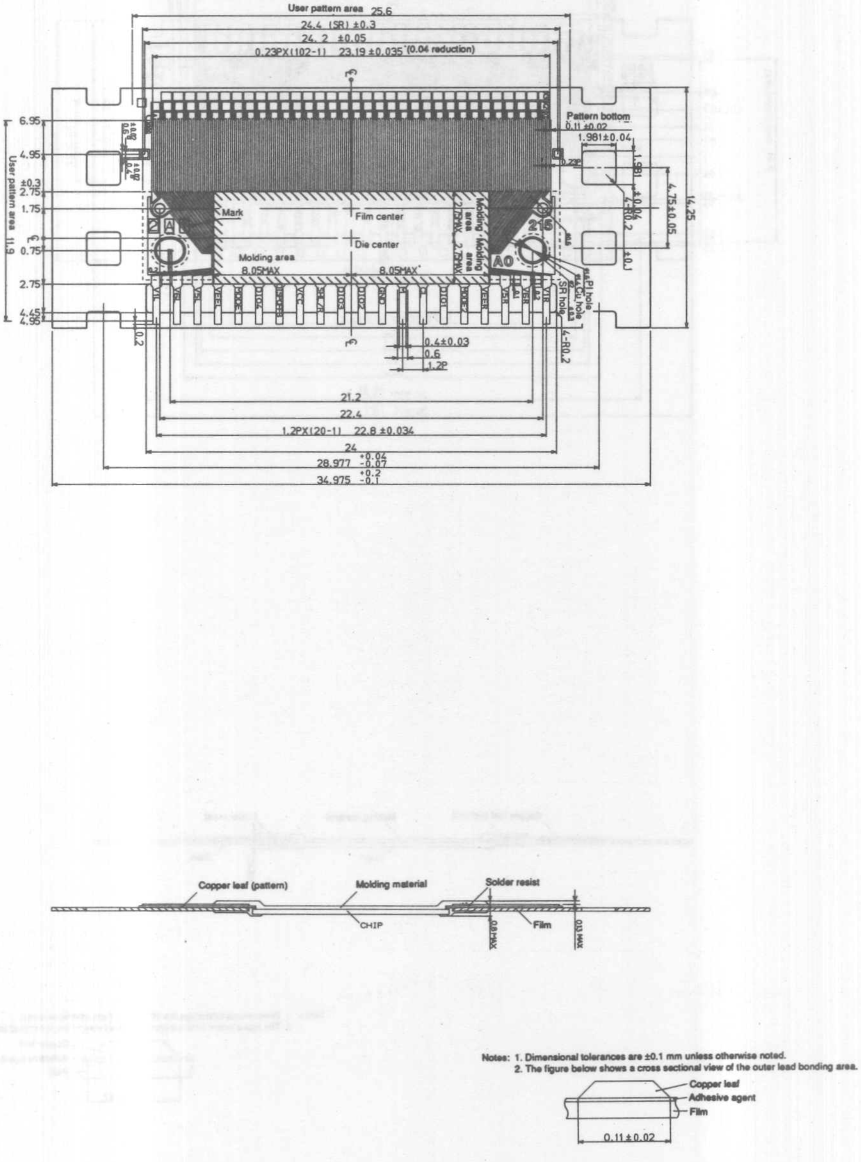


Figure 42 Hitachi Standard TCP 25 — HD66215TA0 —

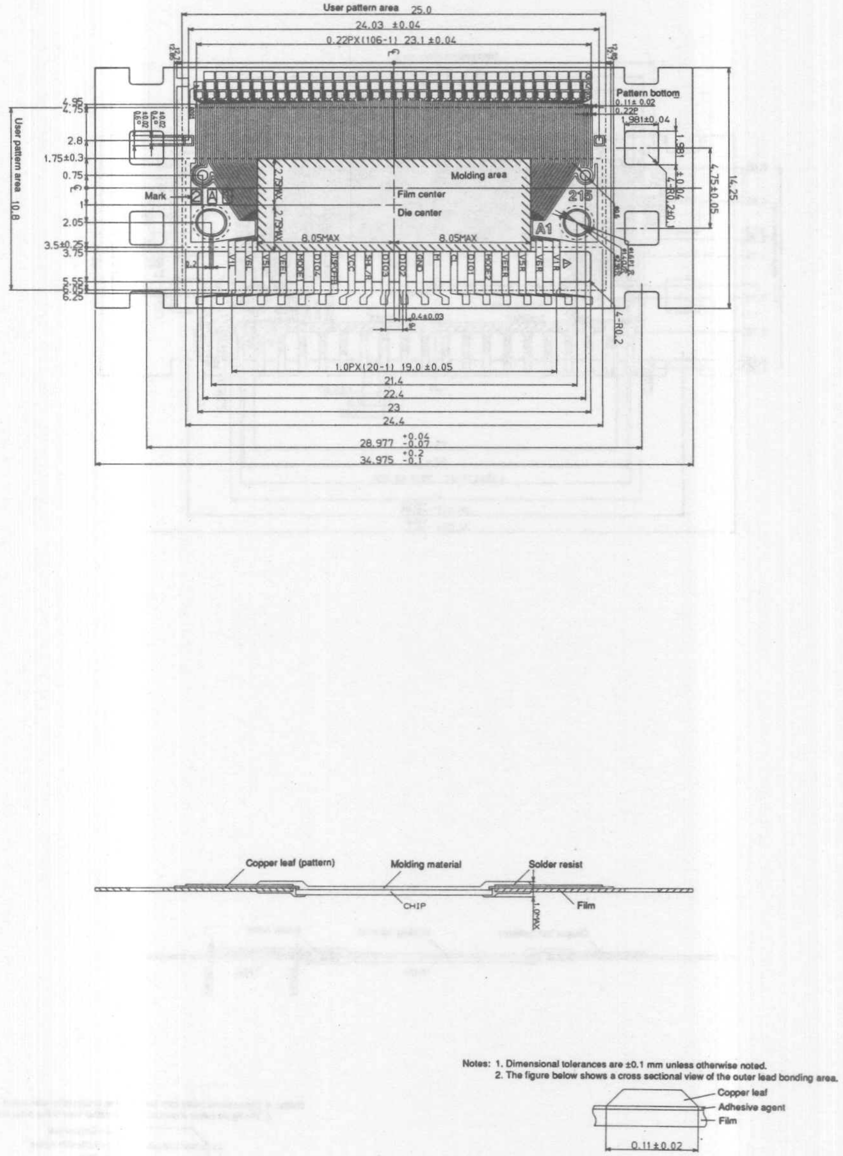
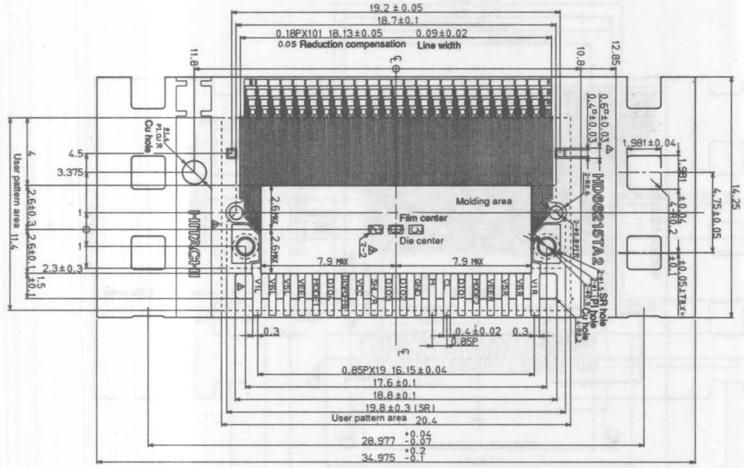
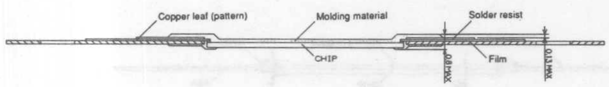


Figure 43 Hitachi Standard TCP 26 — HD66215TA1 —





Notes: 1. Dimensional tolerances are ±0.1 mm unless otherwise noted.
2. The figure below shows a cross sectional view of the outer lead bonding area.

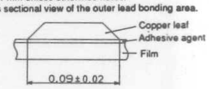


Figure 44 Hitachi Standard TCP 27 — HD66215TA2 —

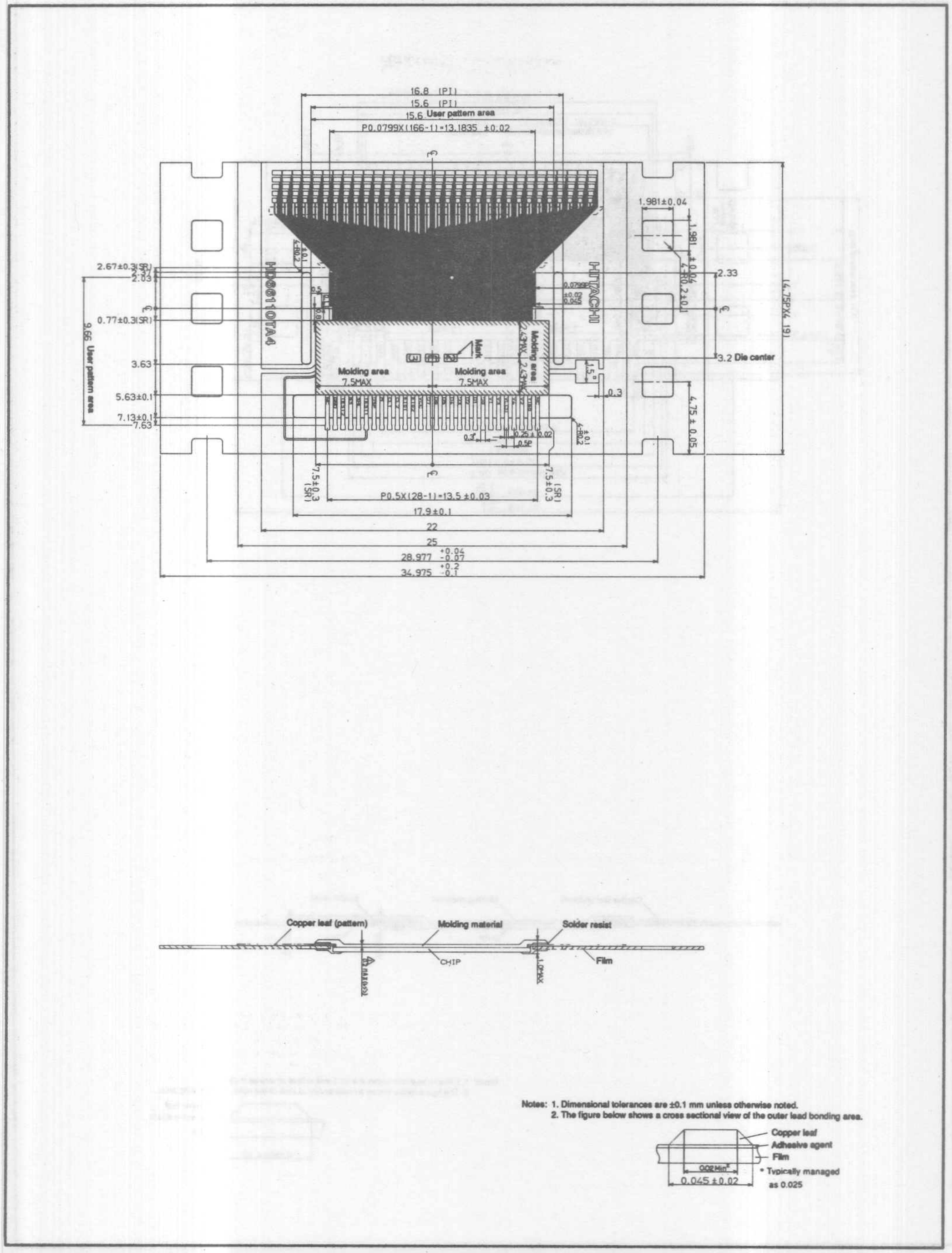
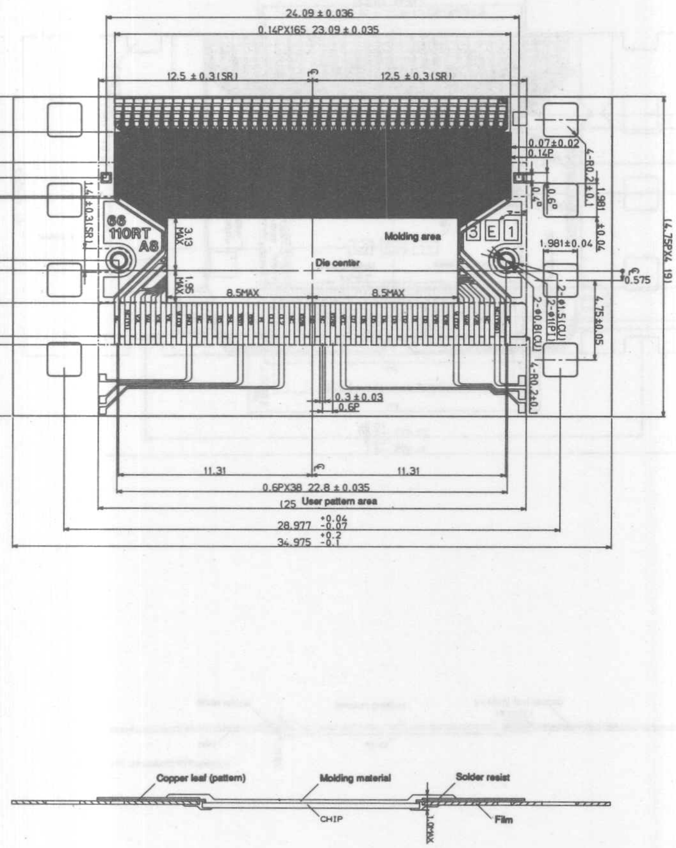
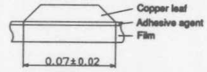


Figure 45 Hitachi Standard TCP 28 — HD66110TA4 —

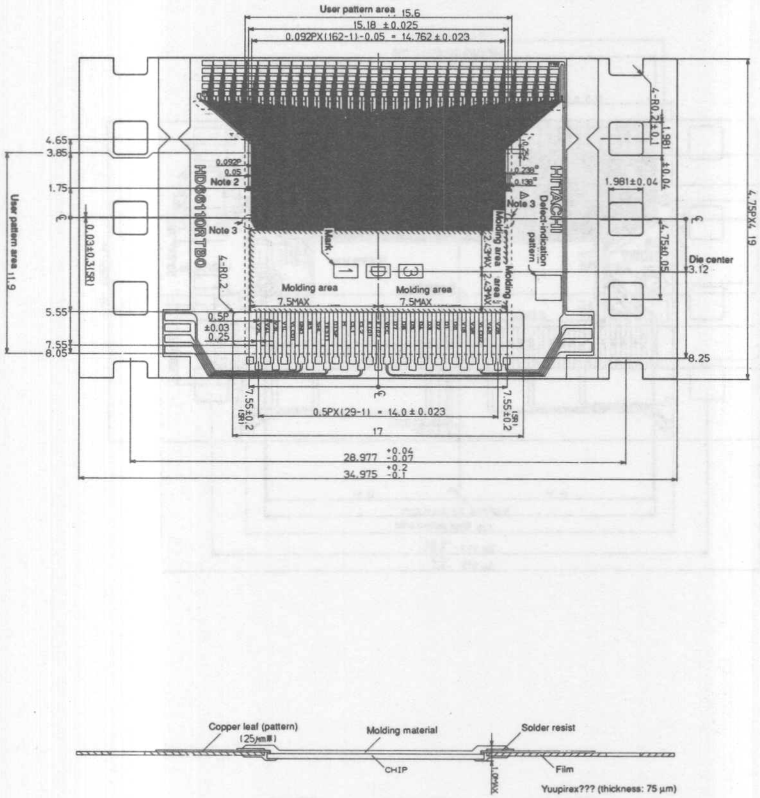


Notes: 1. Dimensional tolerances are ±0.1 mm unless otherwise noted.
2. The figure below shows a cross sectional view of the outer lead bonding area.



3. 4.4 ±0.01 is taken as the SR management target value.

Figure 46 Hitachi Standard TCP 29 — HD66110RTA8 —



Notes: 1. Dimensional tolerances are ±0.1 mm unless otherwise noted.
2. The figure below shows a cross sectional view of the outer lead bonding area.
3. Solder resist exposure of the output side outer lead outermost line (dummy lead) is allowed.

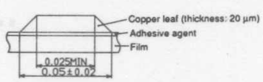


Figure 47 Hitachi Standard TCP 30 — HD66110RTB0 —

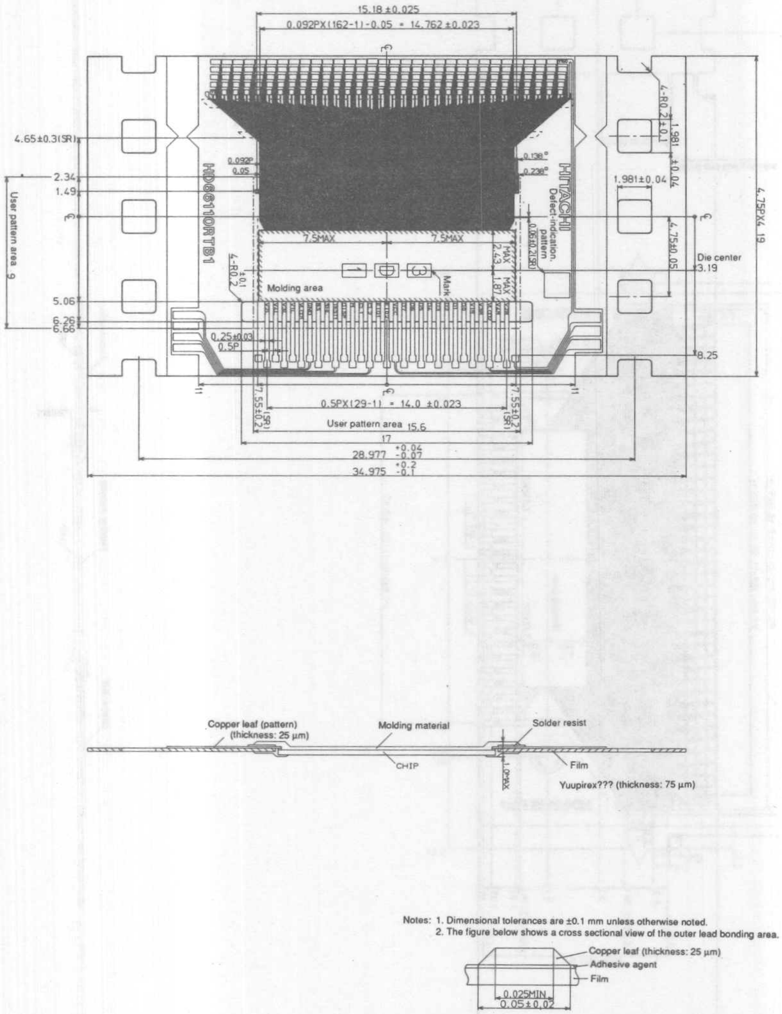
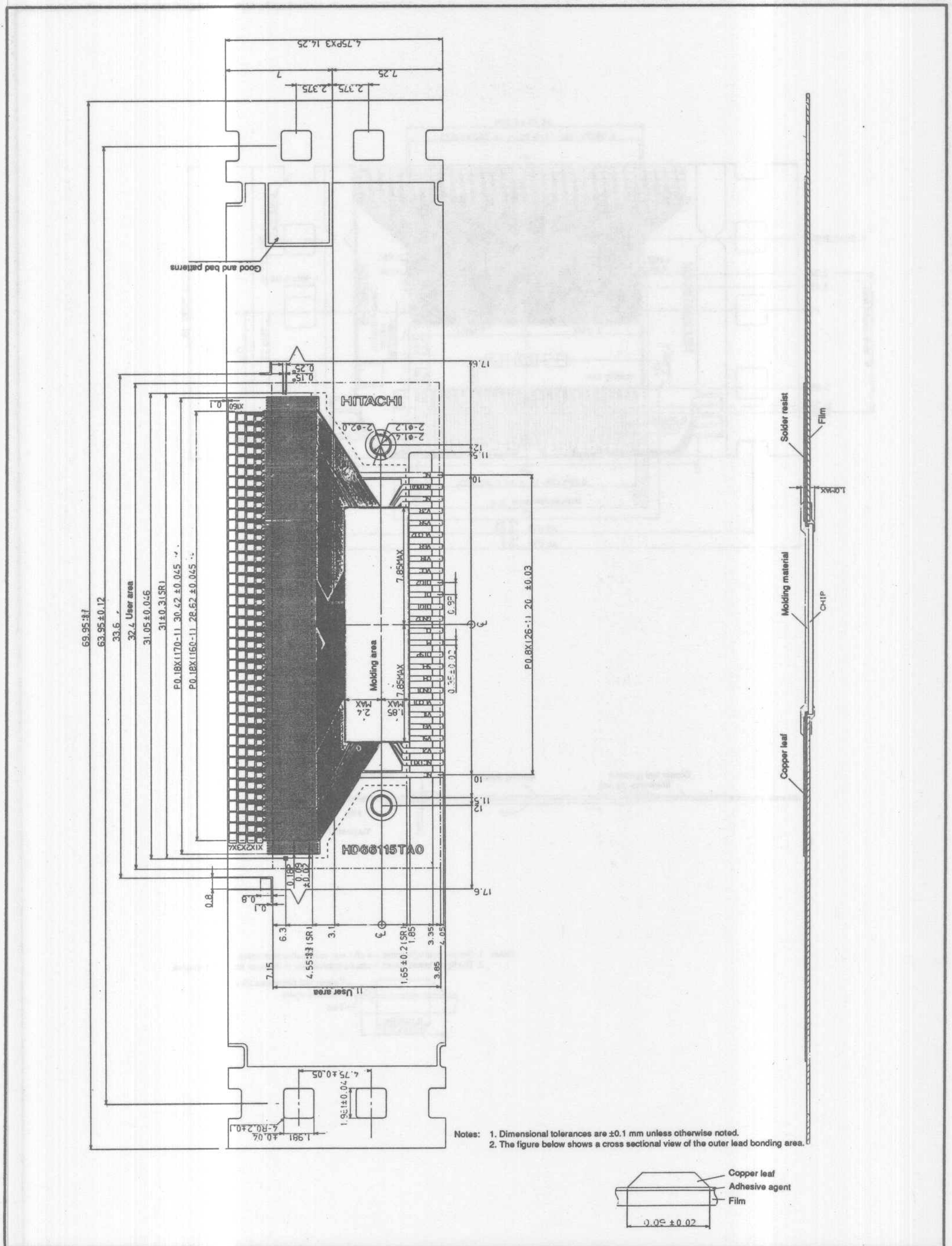


Figure 48 Hitachi Standard TCP 31 — HD66110RTB1 —



Notes: 1. Dimensional tolerances are ±0.1 mm unless otherwise noted.
2. The figure below shows a cross sectional view of the outer lead bonding area.

Figure 49 Hitachi Standard TCP 32 — HD66115TA0 —

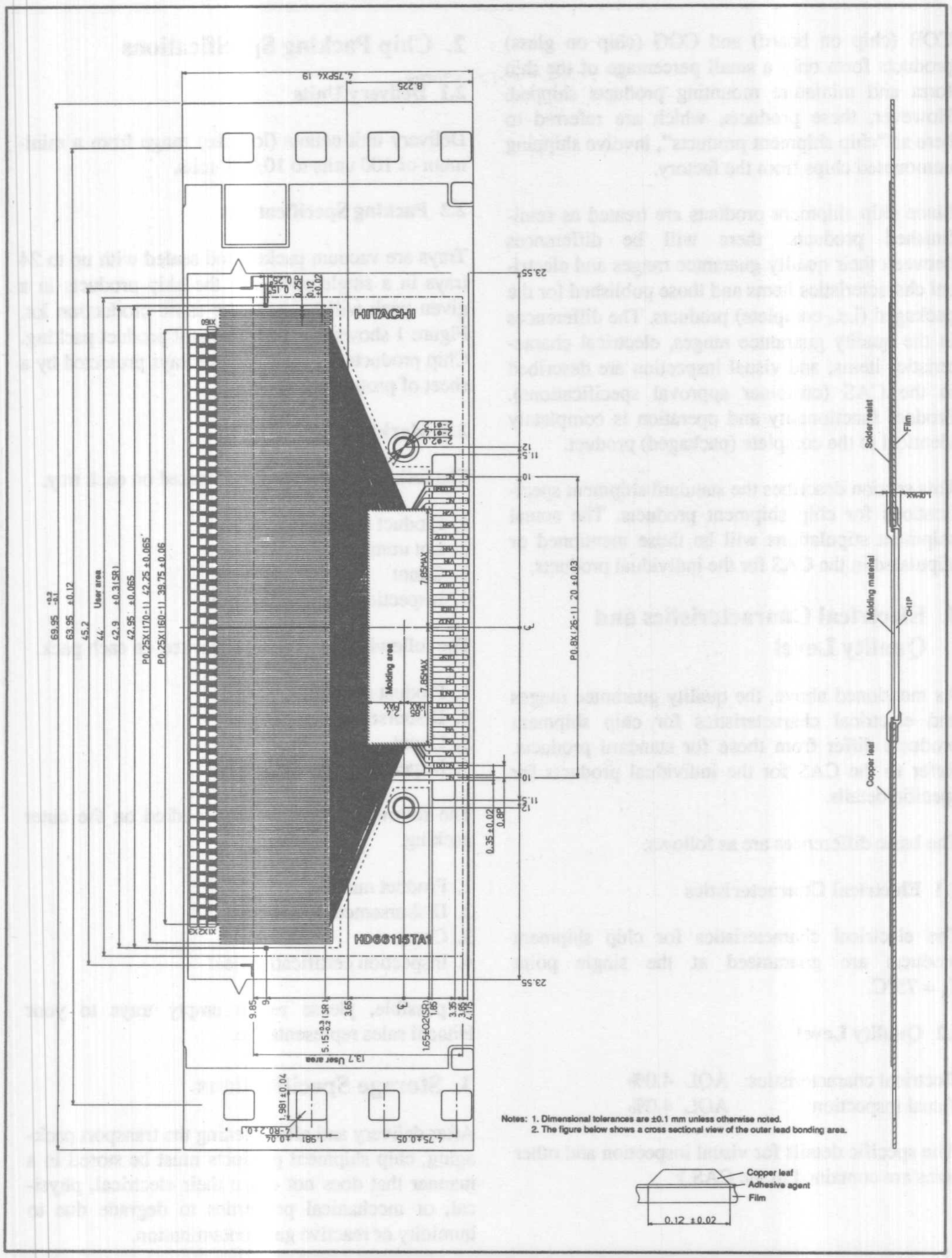


Figure 50 Hitachi Standard TCP 33 — HD66115TA1 —

Chip Shipment Products

COB (chip on board) and COG (chip on glass) products form only a small percentage of the thin form and miniature mounting products shipped. However, these products, which are referred to here as "chip shipment products", involve shipping unmounted chips from the factory.

Since chip shipment products are treated as semi-finished products, there will be differences between their quality guarantee ranges and electrical characteristics items and those published for the packaged (i.e., complete) products. The differences in the quality guarantee ranges, electrical characteristics items, and visual inspection are described in the CAS (customer approval specifications). Product functionality and operation is completely identical to the complete (packaged) product.

This section describes the standard shipment specifications for chip shipment products. The actual shipment stipulations will be those mentioned or stipulated in the CAS for the individual products.

1. Electrical Characteristics and Quality Level

As mentioned above, the quality guarantee ranges and electrical characteristics for chip shipment products differ from those for standard products. Refer to the CAS for the individual products for specific details.

The basic differences are as follows.

1.1 Electrical Characteristics

The electrical characteristics for chip shipment products are guaranteed at the single point $T_a = 75°C$.

1.2 Quality Level

Electrical characteristics: AQL 4.0%
Visual inspection: AQL 4.0%

(The specific details for visual inspection and other items are contained in the CAS.)

2. Chip Packing Specifications

2.1 Delivery Units

Delivery unit counts (lot size) range from a minimum of 100 units to 10,000 units.

2.2 Packing Specifications

Trays are vacuum packed and sealed with up to 24 trays in a single pack. All the chip products in a given pack will be from the same production lot. Figure 1 shows the chip shipment product packing. Chip products are stored in the trays protected by a sheet of protective paper.

2.3 Markings

The following items will be marked on each tray.

1. Product number
2. Lot number
3. Count
4. Inspection certification seal

The following items will be marked on each pack.

1. Product number
2. Disbursement lot number
3. Count
4. Inspection certification seal

The following items will be marked on the outer packing.

1. Product number
2. Disbursement lot number
3. Count
4. Inspection certification seal

If possible, please return empty trays to your Hitachi sales representative.

3. Storage Specifications

After delivery and after opening the transport packaging, chip shipment products must be stored in a manner that does not cause their electrical, physical, or mechanical properties to degrade due to humidity or reactive gas contamination.

We recommend the following storage conditions for these products.

3.1 When Stored in the Packed State

Storage conditions: In dry Nitrogen, at –30°C (30 degrees below zero, Celsius)

Storage period: Six months

The date of the inspection certification seal shall be used as the start of the storage period.

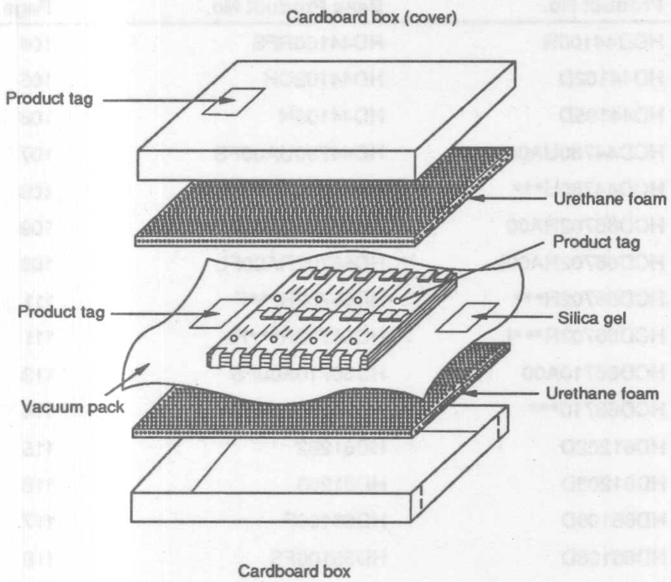
3.2 When Stored after Die Bonding or Wire Bonding

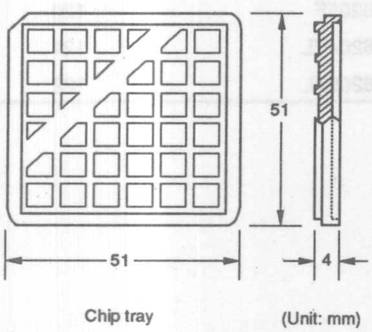
Storage condition 1: Temperature: under 30°C, Humidity: under 70%, Airborne particles: less than 5000 per cubic foot

Storage period 1: Seven days

Storage conditions 2: In dry Nitrogen, at –30°C

Storage period 2: 20 days





36 pcs./ tray	HD44780SA00D, HCD66702, HD44102D, HD44105D, HD61202D, HD61203D, HD61104AD, HD61105AD, HD66106D
49 pcs./ tray	
64 pcs./ tray	HD44100D, HD66100D, HCD66204, HCD66205

Figure 1 Chip Packing

4. Chip Shape Specifications

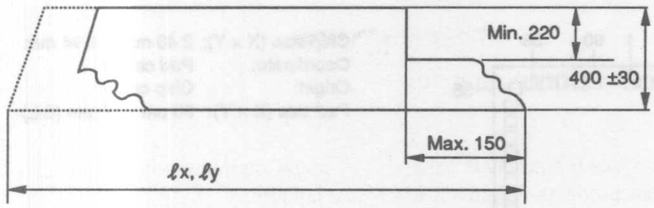
See figure 2.

5. Products Available as Chip Shipment Products

Hitachi, Ltd. currently provides the products listed in table 1 as chip shipment products. Figures 3 to 19 show their respective chip sizes and bonding pad layouts.

Table 1 Chip Shipment Product Table

Figure No.	Product No.	Base Product No.	Page
3	HCD44100R	HD44100RFS	104
4	HD44102D	HD44102CH	105
5	HD44105D	HD44105H	106
6	HCD44780UA00	HD44780UA00FS	107
7	HCD44780U***	HD44780U***FS	108
8	HCD66702RA00	HD66702RA00F	109
8	HCD66702RA00L	HD66702RA00FL	109
9	HCD66702R***	HD66702R***F	111
9	HCD66702R***L	HD66702R***FL	111
10	HCD66710A00	HD66710A00FS	113
11	HCD66710***	HD66710***FS	114
12	HD61202D	HD61202	115
13	HD61203D	HD61203	116
14	HD66100D	HD66100F	117
15	HD66106D	HD66106FS	118
16	HCD66204	HD66204F	119
17	HCD66205	HD66205F	120
18	HCD66204L	HD66204FL	121
19	HCD66205L	HD66205FL	122

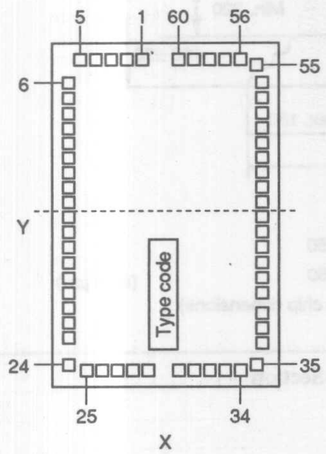


Surface shape maximum values X direction: ℓx + 250
Y direction: ℓy + 250
(ℓx and ℓy are the chip dimensions) (unit: µm)

Figure 2 Chip Cross-Section

Chip Shipment Products

- HCD44100R



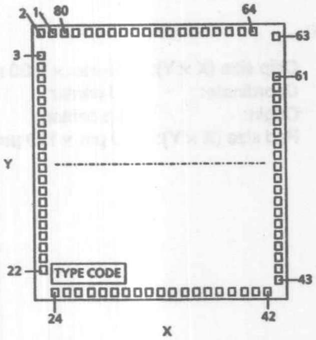
Chip size (X × Y): 2.40 mm × 3.94 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 90 µm × 90 µm (SiL)

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y
1	Y30	–280	1815	21	Y14	–1045	–1100	41	DR1	1075	–630
2	Y31	–460	1815	22	Y13	–1045	–1300	42	DL2	1075	–450
3	Y32	–640	1815	23	Y12	–1045	–1500	43	DR2	1075	–270
4	Y33	–820	1815	24	Y9	–1045	–1740	44			
5	Y34	–1000	1815	25	Y10	–850	–1815	45	M	1075	–90
6	Y29	–1045	1600	26	Y11	–670	–1815	46	SHL1	1075	90
7	Y28	–1045	1420	27	Y8	–490	–1815	47	SHL2	1075	270
8	Y27	–1045	1240	28	Y7	–310	–1815	48	FCS	1075	450
9	Y26	–1045	1060	29	V_{CC}	–130	–1815	49	V1	1075	630
10	Y25	–1045	880	30	Y6	130	–1815	50	V2	1075	810
11	Y24	–1045	700	31	Y5	310	–1815	51	V3	1075	990
12	Y23	–1045	520	32	Y4	490	–1815	52	V4	1075	1170
13	Y22	–1045	340	33	Y3	670	–1815	53	V5	1075	1350
14	Y21	–1045	160	34	Y2	870	–1815	54	V6	1075	1550
15	Y20	–1045	–20	35	Y1	1030	–1780	55	Y40	1045	1800
16	Y19	–1045	–200	36	V_{EE}	1075	–1600	56	Y39	850	1815
17	Y18	–1045	–380	37	CL1	1075	–1410	57	Y38	670	1815
18	Y17	–1045	–560	38	CL2	1075	–1235	58	Y37	490	1815
19	Y16	–1045	–740	39	GND	1075	–990	59	Y36	310	1815
20	Y15	–1045	–920	40	DL1	1075	–810	60	Y35	130	1815

Figure 3 HCD44100R

• HD44102D



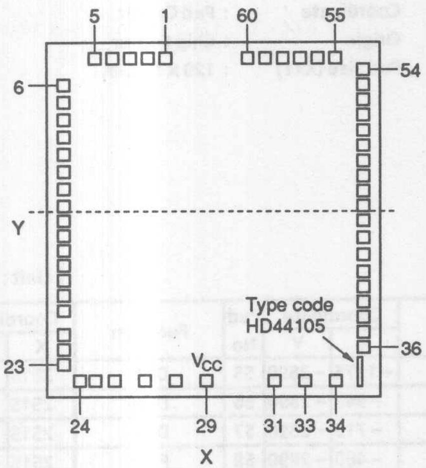
Chip Size (XxY) : 5.40×6.16mm
Coordinate : Pad Center
Origin : Chip Center
Pad Size (XxY) : 120×120μm

[Unit : μm]

Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y
1	Y39	−2130	2890	28	Y13	−1175	−2890	55	DB5	2515	500
2	Y38	−2465	2890	29	Y12	−945	−2890	56	DB6	2515	770
3	Y37	−2515	2465	30	Y11	−715	−2890	57	DB7	2515	1050
4	Y36	−2515	2215	31	Y10	−480	−2890	58	FRM	2515	1320
5	Y35	−2515	1965	32	Y9	−255	−2890	59	CL	2515	1560
6	Y34	−2515	1715	33	Y8	−25	−2890	60	P1 (ϕ1)	2515	1800
7	Y33	−2515	1465	34	Y7	205	−2890	61	P2 (ϕ2)	2515	2040
8	Y32	−2515	1215	35	Y6	435	−2890	62			
9	Y31	−2515	965	36	Y5	665	−2890	63	M	2515	2815
10	Y30	−2515	715	37	Y4	915	−2890	64	GND	2070	2890
11	Y29	−2515	465	38	Y3	1160	−2890	65	VEE	1835	2890
12	Y28	−2515	215	39	Y2	1410	−2890	66	V1	1600	2890
13	Y27	−2515	−35	40	Y1	1640	−2890	67	V2	1365	2890
14	Y26	−2515	−285	41	VCC	1930	−2890	68	V3	1135	2890
15	Y25	−2515	−535	42	BS	2245	−2890	69	V4	890	2890
16	Y24	−2515	−785	43	RST	2515	−2605	70	Y50	640	2890
17	Y23	−2515	−1035	44	CS1	2515	−2365	71	Y49	410	2890
18	Y22	−2515	−1285	45	CS2	2515	−2125	72	Y48	180	2890
19	Y21	−2515	−1535	46	CS3	2515	−1885	73	Y47	−50	2890
20	Y20	−2515	−1785	47	E	2515	−1645	74	Y46	−340	2890
21	Y19	−2515	−2035	48	RW	2515	−1405	75	Y45	−605	2890
22	Y18	−2515	−2285	49	D1	2515	−1165	76	Y44	−850	2890
23				50	DB0	2515	−880	77	Y43	−1100	2890
24	Y17	−2155	−2890	51	DB1	2515	−600	78	Y42	−1350	2890
25	Y16	−1865	−2890	52	DB2	2515	−330	79	Y41	−1600	2890
26	Y15	−1635	−2890	53	DB3	2515	−50	80	Y40	−1845	2890
27	Y14	−1405	−2890	54	DB4	2515	220				

Figure 4 HD44102D

- HD44105D



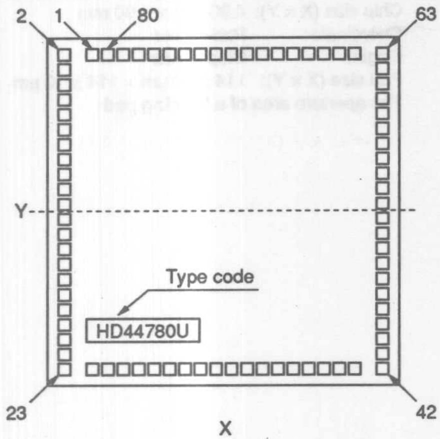
Chip size (X × Y): 4.56 mm × 6.00 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 120 µm × 120 µm

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y
1	X12	–575	2822	20	C	–2105	–1628	42	X31	2105	–833
2	X11	–875	2822	21	R	–2105	–2053	43	X30	2105	–528
3	X10	–1175	2822	22	CR	–2105	–2363	44	X29	2105	–223
4	X9	–1475	2822	23	$\overline{STB}$	–2105	–2593	45	X28	2105	82
5	X8	–1775	2822	24	SHL	–2005	–2822	46	X27	2105	387
6	X7	–2105	2372	25	M/S	–1770	–2822	47	X26	2105	697
7	X6	–2105	2047	26	ø2	–1460	–2822	48	X25	2105	1002
8	X5	–2105	1732	27	ø1	–1010	–2822	49	X24	2105	1307
9	X4	–2105	1417	28	FRM	–605	–2822	50	X23	2105	1587
10	X3	–2105	1102	29	V_{CC}	–265	–2822	51	X22	2105	1867
11	X2	–2105	787	31	M	770	–2822	52	X21	2105	2147
12	X1	–2105	472	33	CL	1290	–2822	53	X20	2105	2427
13	DL	–2105	117	34	DR	1730	–2822	54	X19	2105	2707
14	GND	–2105	–208	36	V_{EE}	2105	–2308	55	X18	1855	2822
15	FS1	–2105	–438	37	V1	2105	–2078	56	X17	1555	2822
16	FS2	–2105	–668	38	V2	2105	–1848	57	X16	1255	2822
17	DS1	–2105	–898	39	V5	2105	–1610	58	X15	955	2822
18	DS2	–2105	–1128	40	V6	2105	–1388	59	X14	655	2822
19	DS3	–2105	–1358	41	X32	2105	–1138	60	X13	355	2822

Figure 5 HD44105D

- HCD44780UA00



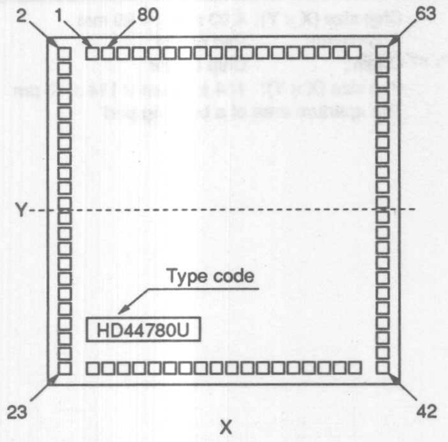
Chip size (X × Y): 4.90 mm × 4.90 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 114 ± 10 µm × 114 ± 10 µm
The aperture area of a bonding pad

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	SEG22	–2100	2313
2	SEG21	–2280	2313
3	SEG20	–2313	2089
4	SEG19	–2313	1833
5	SEG18	–2313	1617
6	SEG17	–2313	1401
7	SEG16	–2313	1186
8	SEG15	–2313	970
9	SEG14	–2313	755
10	SEG13	–2313	539
11	SEG12	–2313	323
12	SEG11	–2313	108
13	SEG10	–2313	–108
14	SEG9	–2313	–323
15	SEG8	–2313	–539
16	SEG7	–2313	–755
17	SEG6	–2313	–970
18	SEG5	–2313	–1186
19	SEG4	–2313	–1401
20	SEG3	–2313	–1617
21	SEG2	–2313	–1833
22	SEG1	–2313	–2073
23	GND	–2280	–2290
24	OSC1	–2080	–2290
25	OSC2	–1749	–2290
26	V1	–1550	–2290
27	V2	–1268	–2290
28	V3	–941	–2290
29	V4	–623	–2290
30	V5	–304	–2290
31	CL1	–48	–2290
32	CL2	142	–2290
33	V_{CC}	309	–2290
34	M	475	–2290
35	D	665	–2290
36	RS	832	–2290
37	R/$\overline{W}$	1022	–2290
38	E	1204	–2290
39	DB0	1454	–2290
40	DB1	1684	–2290
41	DB2	2070	–2290
42	DB3	2260	–2290
43	DB4	2290	–2099
44	DB5	2290	–1883
45	DB6	2290	–1667
46	DB7	2290	–1452
47	COM1	2313	–1186
48	COM2	2313	–970
49	COM3	2313	–755
50	COM4	2313	–539
51	COM5	2313	–323
52	COM6	2313	–108
53	COM7	2313	108
54	COM8	2313	323
55	COM9	2313	539
56	COM10	2313	755
57	COM11	2313	970
58	COM12	2313	1186
59	COM13	2313	1401
60	COM14	2313	1617
61	COM15	2313	1833
62	COM16	2313	2095
63	SEG40	2296	2313
64	SEG39	2100	2313
65	SEG38	1617	2313
66	SEG37	1401	2313
67	SEG36	1186	2313
68	SEG35	970	2313
69	SEG34	755	2313
70	SEG33	539	2313
71	SEG32	323	2313
72	SEG31	108	2313
73	SEG30	–108	2313
74	SEG29	–323	2313
75	SEG28	–539	2313
76	SEG27	–755	2313
77	SEG26	–970	2313
78	SEG25	–1186	2313
79	SEG24	–1401	2313
80	SEG23	–1617	2313

Figure 6 HCD44780UA00

- HCD44780U***



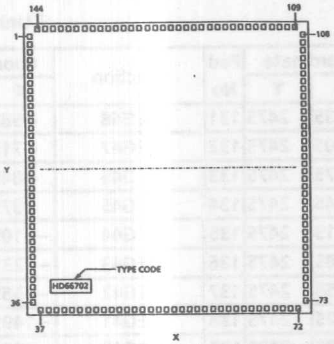
Chip size (X × Y): 4.90 mm × 4.90 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 114 ± 10 µm × 114 ± 10 µm
The aperture area of a bonding pad

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y
1	SEG22	–2100	2313	28	V3	–941	–2290	55	COM9	2313	539
2	SEG21	–2280	2313	29	V4	–623	–2290	56	COM10	2313	755
3	SEG20	–2313	2089	30	V5	–304	–2290	57	COM11	2313	970
4	SEG19	–2313	1833	31	CL1	–48	–2290	58	COM12	2313	1186
5	SEG18	–2313	1617	32	CL2	142	–2290	59	COM13	2313	1401
6	SEG17	–2313	1401	33	V_{CC}	309	–2290	60	COM14	2313	1617
7	SEG16	–2313	1186	34	M	475	–2290	61	COM15	2313	1833
8	SEG15	–2313	970	35	D	665	–2290	62	COM16	2313	2095
9	SEG14	–2313	755	36	RS	832	–2290	63	SEG40	2296	2313
10	SEG13	–2313	539	37	R/$\overline{W}$	1022	–2290	64	SEG39	2100	2313
11	SEG12	–2313	323	38	E	1204	–2290	65	SEG38	1617	2313
12	SEG11	–2313	108	39	DB0	1454	–2290	66	SEG37	1401	2313
13	SEG10	–2313	–108	40	DB1	1684	–2290	67	SEG36	1186	2313
14	SEG9	–2313	–323	41	DB2	2070	–2290	68	SEG35	970	2313
15	SEG8	–2313	–539	42	DB3	2260	–2290	69	SEG34	755	2313
16	SEG7	–2313	–755	43	DB4	2290	–2099	70	SEG33	539	2313
17	SEG6	–2313	–970	44	DB5	2290	–1883	71	SEG32	323	2313
18	SEG5	–2313	–1186	45	DB6	2290	–1667	72	SEG31	108	2313
19	SEG4	–2313	–1401	46	DB7	2290	–1452	73	SEG30	–108	2313
20	SEG3	–2313	–1617	47	COM1	2313	–1186	74	SEG29	–323	2313
21	SEG2	–2313	–1833	48	COM2	2313	–970	75	SEG28	–539	2313
22	SEG1	–2313	–2073	49	COM3	2313	–755	76	SEG27	–755	2313
23	GND	–2280	–2290	50	COM4	2313	–539	77	SEG26	–970	2313
24	OSC1	–2080	–2290	51	COM5	2313	–323	78	SEG25	–1186	2313
25	OSC2	–1749	–2290	52	COM6	2313	–108	79	SEG24	–1401	2313
26	V1	–1550	–2290	53	COM7	2313	108	80	SEG23	–1617	2313
27	V2	–1268	–2290	54	COM8	2313	323				

Figure 7 HCD44780U***

- HCD66702RA00, HCD66702RA00L



Chip Size (XxY) : 5.20 × 5.20mm
Coordinate : Pad Center
Origin : Chip Center
Pad Size (XxY) : 90 × 90μm

[Unit : μm]

Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y
1	SEG34	−2475	2350	35	GND	−2475	−2180	69	COM7	1990	−2475
2	SEG33	−2475	2205	36	OSC2	−2475	−2325	70	COM8	2125	−2475
3	SEG32	−2475	2065	37	OSC1	−2445	−2475	71	COM9	2265	−2475
4	SEG31	−2475	1925	38	VCC	−2305	−2475	72	COM10	2410	−2475
5	SEG30	−2475	1790	39	VCC	−2165	−2475	73	COM11	2475	−2290
6	SEG29	−2475	1655	40	V1	−2025	−2475	74	COM12	2475	−2145
7	SEG28	−2475	1525	41	V2	−1875	−2475	75	COM13	2475	−2005
8	SEG27	−2475	1395	42	V3	−1745	−2475	76	COM14	2475	−1865
9	SEG26	−2475	1265	43	V4	−1595	−2475	77	COM15	2475	−1730
10	SEG25	−2475	1135	44	V5	−1465	−2475	78	COM16	2475	−1595
11	SEG24	−2475	1005	45	CL1	−1335	−2475	79	SEG100	2475	−1465
12	SEG23	−2475	875	46	CL2	−1185	−2475	80	SEG99	2475	−1335
13	SEG22	−2475	745	47	M	−1055	−2475	81	SEG98	2475	−1205
14	SEG21	−2475	615	48	D	−905	−2475	82	SEG97	2475	−1075
15	SEG20	−2475	485	49	EXT	−775	−2475	83	SEG96	2475	−945
16	SEG19	−2475	355	50	TEST	−625	−2475	84	SEG95	2475	−815
17	SEG18	−2475	225	51	GND	−495	−2475	85	SEG94	2475	−685
18	SEG17	−2475	95	52	RS	−345	−2475	86	SEG93	2475	−555
19	SEG16	−2475	−35	53	R/W	−195	−2475	87	SEG92	2475	−425
20	SEG15	−2475	−165	54	E	−45	−2475	88	SEG91	2475	−295
21	SEG14	−2475	−295	55	DB0	85	−2475	89	SEG90	2475	−165
22	SEG13	−2475	−425	56	DB1	235	−2475	90	SEG89	2475	−35
23	SEG12	−2475	−555	57	DB2	365	−2475	91	SEG88	2475	95
24	SEG11	−2475	−685	58	DB3	515	−2475	92	SEG87	2475	225
25	SEG10	−2475	−815	59	DB4	645	−2475	93	SEG86	2475	355
26	SEG9	−2475	−945	60	DB5	795	−2475	94	SEG85	2475	485
27	SEG8	−2475	−1075	61	DB6	925	−2475	95	SEG84	2475	615
28	SEG7	−2475	−1205	62	DB7	1075	−2475	96	SEG83	2475	745
29	SEG6	−2475	−1335	63	COM1	1205	−2475	97	SEG82	2475	875
30	SEG5	−2475	−1465	64	COM2	1335	−2475	98	SEG81	2475	1005
31	SEG4	−2475	−1600	65	COM3	1465	−2475	99	SEG80	2475	1135
32	SEG3	−2475	−1735	66	COM4	1595	−2475	100	SEG79	2475	1265
33	SEG2	−2475	−1870	67	COM5	1725	−2475	101	SEG78	2475	1395
34	SEG1	−2475	−2010	68	COM6	1855	−2475	102	SEG77	2475	1525

Figure 8 HCD66702RA00, HCD66702RA00L (1)

Chip Shipment Products

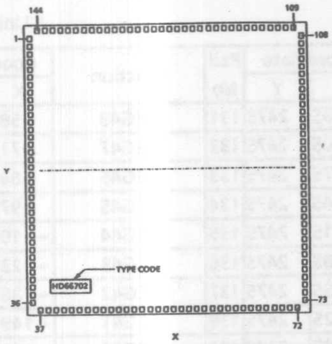
- HCD66702RA00, HCD66702RA00L

[Unit : μm]

Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y
103	SEG76	2475	1655	117	SEG62	1235	2475	131	SEG48	−585	2475
104	SEG75	2475	1790	118	SEG61	1105	2475	132	SEG47	−715	2475
105	SEG74	2475	1925	119	SEG60	975	2475	133	SEG46	−845	2475
106	SEG73	2475	2065	120	SEG59	845	2475	134	SEG45	−975	2475
107	SEG72	2475	2205	121	SEG58	715	2475	135	SEG44	−1105	2475
108	SEG71	2475	2350	122	SEG57	585	2475	136	SEG43	−1235	2475
109	SEG70	2320	2475	123	SEG56	455	2475	137	SEG42	−1365	2475
110	SEG69	2175	2475	124	SEG55	325	2475	138	SEG41	−1495	2475
111	SEG68	2035	2475	125	SEG54	195	2475	139	SEG40	−1625	2475
112	SEG67	1895	2475	126	SEG53	65	2475	140	SEG39	−1760	2475
113	SEG66	1760	2475	127	SEG52	−65	2475	141	SEG38	−1895	2475
114	SEG65	1625	2475	128	SEG51	−195	2475	142	SEG37	−2035	2475
115	SEG64	1495	2475	129	SEG50	−325	2475	143	SEG36	−2175	2475
116	SEG63	1365	2475	130	SEG49	−455	2475	144	SEG35	−2320	2475

Figure 8 HCD66702RA00, HCD66702RA00L (2)

- HCD66702R***, HCD66702R***L



Chip Size (XxY) : 5.20 × 5.20mm
Coordinate : Pad Center
Origin : Chip Center
Pad Size (XxY) : 90 × 90μm

[Unit : μm]

Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y
1	SEG34	−2475	2350	35	GND	−2475	−2180	69	COM7	1990	−2475
2	SEG33	−2475	2205	36	OSC2	−2475	−2325	70	COM8	2125	−2475
3	SEG32	−2475	2065	37	OSC1	−2445	−2475	71	COM9	2265	−2475
4	SEG31	−2475	1925	38	VCC	−2305	−2475	72	COM10	2410	−2475
5	SEG30	−2475	1790	39	VCC	−2165	−2475	73	COM11	2475	−2290
6	SEG29	−2475	1655	40	V1	−2025	−2475	74	COM12	2475	−2145
7	SEG28	−2475	1525	41	V2	−1875	−2475	75	COM13	2475	−2005
8	SEG27	−2475	1395	42	V3	−1745	−2475	76	COM14	2475	−1865
9	SEG26	−2475	1265	43	V4	−1595	−2475	77	COM15	2475	−1730
10	SEG25	−2475	1135	44	V5	−1465	−2475	78	COM16	2475	−1595
11	SEG24	−2475	1005	45	CL1	−1335	−2475	79	SEG100	2475	−1465
12	SEG23	−2475	875	46	CL2	−1185	−2475	80	SEG99	2475	−1335
13	SEG22	−2475	745	47	M	−1055	−2475	81	SEG98	2475	−1205
14	SEG21	−2475	615	48	D	−905	−2475	82	SEG97	2475	−1075
15	SEG20	−2475	485	49	EXT	−775	−2475	83	SEG96	2475	−945
16	SEG19	−2475	355	50	TEST	−625	−2475	84	SEG95	2475	−815
17	SEG18	−2475	225	51	GND	−495	−2475	85	SEG94	2475	−685
18	SEG17	−2475	95	52	RS	−345	−2475	86	SEG93	2475	−555
19	SEG16	−2475	−35	53	R/W	−195	−2475	87	SEG92	2475	−425
20	SEG15	−2475	−165	54	E	−45	−2475	88	SEG91	2475	−295
21	SEG14	−2475	−295	55	DB0	85	−2475	89	SEG90	2475	−165
22	SEG13	−2475	−425	56	DB1	235	−2475	90	SEG89	2475	−35
23	SEG12	−2475	−555	57	DB2	365	−2475	91	SEG88	2475	95
24	SEG11	−2475	−685	58	DB3	515	−2475	92	SEG87	2475	225
25	SEG10	−2475	−815	59	DB4	645	−2475	93	SEG86	2475	355
26	SEG9	−2475	−945	60	DB5	795	−2475	94	SEG85	2475	485
27	SEG8	−2475	−1075	61	DB6	925	−2475	95	SEG84	2475	615
28	SEG7	−2475	−1205	62	DB7	1075	−2475	96	SEG83	2475	745
29	SEG6	−2475	−1335	63	COM1	1205	−2475	97	SEG82	2475	875
30	SEG5	−2475	−1465	64	COM2	1335	−2475	98	SEG81	2475	1005
31	SEG4	−2475	−1600	65	COM3	1465	−2475	99	SEG80	2475	1135
32	SEG3	−2475	−1735	66	COM4	1595	−2475	100	SEG79	2475	1265
33	SEG2	−2475	−1870	67	COM5	1725	−2475	101	SEG78	2475	1395
34	SEG1	−2475	−2010	68	COM6	1855	−2475	102	SEG77	2475	1525

Figure 9 HCD66702R***, HCD66702R***L (1)

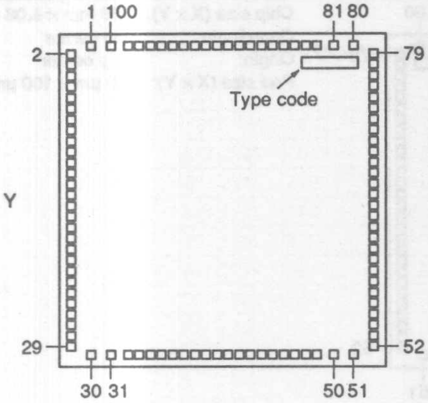
- HCD66702R***, HCD66702R***L

[Unit : μm]

Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y
103	SEG76	2475	1655	117	SEG62	1235	2475	131	SEG48	−585	2475
104	SEG75	2475	1790	118	SEG61	1105	2475	132	SEG47	−715	2475
105	SEG74	2475	1925	119	SEG60	975	2475	133	SEG46	−845	2475
106	SEG73	2475	2065	120	SEG59	845	2475	134	SEG45	−975	2475
107	SEG72	2475	2205	121	SEG58	715	2475	135	SEG44	−1105	2475
108	SEG71	2475	2350	122	SEG57	585	2475	136	SEG43	−1235	2475
109	SEG70	2320	2475	123	SEG56	455	2475	137	SEG42	−1365	2475
110	SEG69	2175	2475	124	SEG55	325	2475	138	SEG41	−1495	2475
111	SEG68	2035	2475	125	SEG54	195	2475	139	SEG40	−1625	2475
112	SEG67	1895	2475	126	SEG53	65	2475	140	SEG39	−1760	2475
113	SEG66	1760	2475	127	SEG52	−65	2475	141	SEG38	−1895	2475
114	SEG65	1625	2475	128	SEG51	−195	2475	142	SEG37	−2035	2475
115	SEG64	1495	2475	129	SEG50	−325	2475	143	SEG36	−2175	2475
116	SEG63	1365	2475	130	SEG49	−455	2475	144	SEG35	−2320	2475

Figure 9 HCD66702R***, HCD66702R***L (2)

• HCD66710A00



Chip size (X × Y): 5.36 mm × 6.06 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 100 µm × 100 µm

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	SEG27	–2495	2910
2	SEG28	–2695	2730
3	SEG29	–2695	2499
4	SEG30	–2695	2300
5	SEG31	–2695	2100
6	SEG32	–2695	1901
7	SEG33	–2695	1698
8	SEG34	–2695	1498
9	SEG35	–2695	1295
10	SEG36	–2695	1099
11	SEG37	–2695	900
12	SEG38	–2695	700
13	SEG39	–2695	501
14	SEG40	–2695	301
15	COM9	–2695	98
16	COM10	–2695	–113
17	COM11	–2695	–302
18	COM12	–2695	–501
19	COM13	–2695	–701
20	COM14	–2695	–900
21	COM15	–2695	–1100
22	COM16	–2695	–1303
23	COM25	–2695	–1502
24	COM26	–2695	–1702
25	COM27	–2695	–1901
26	COM28	–2695	–2101
27	COM29	–2695	–2300
28	COM30	–2695	–2500
29	COM31	–2695	–2731
30	COM32	–2495	–2910
31	COM24	–2051	–2910
32	COM23	–1701	–2910
33	COM22	–1498	–2910
34	COM21	–1302	–2910

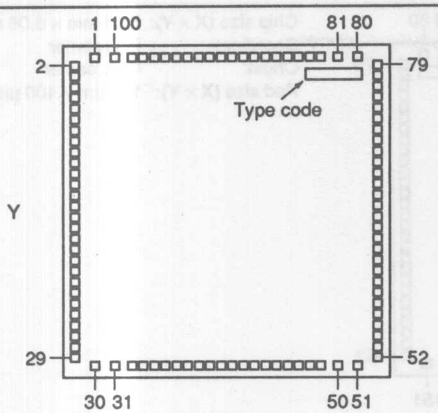
Pad No.	Pad Name	Coordinate X	Coordinate Y
35	COM20	–1102	–2910
36	COM19	–899	–2910
37	COM18	–700	–2910
38	COM17	–500	–2910
39	COM8	–301	–2910
40	COM7	–101	–2910
41	COM6	99	–2910
42	COM5	302	–2910
43	COM4	502	–2910
44	COM3	698	–2910
45	COM2	887	–2910
46	COM1	1077	–2910
47	COM33	1266	–2910
48	V1	1488	–2910
49	V2	1710	–2910
50	V3	2063	–2910
51	V4	2458	–2910
52	V5	2660	–2731
53	V5OUT3	2660	–2500
54	V5OUT2	2660	–2300
55	GND	2640	–2090
56	C1	2650	–1887
57	C2	2675	–1702
58	VCI	2675	–1502
59	OSC1	2675	–1303
60	OSC2	2675	–1103
61	RS	2675	–900
62	R/W	2675	–701
63	E	2675	–501
64	DB0	2675	–302
65	DB1	2675	–99
66	DB2	2675	98
67	DB3	2675	301

Pad No.	Pad Name	Coordinate X	Coordinate Y
68	DB4	2675	501
69	DB5	2675	700
70	DB6	2675	900
71	DB7	2675	1099
72	EXT	2675	1299
73	TEST	2675	1502
74	V_{CC}	2695	1698
75	SEG1	2695	1901
76	SEG2	2695	2104
77	SEG3	2695	2300
78	SEG4	2695	2503
79	SEG5	2695	2730
80	SEG6	2495	2910
81	SEG7	2049	2910
82	SEG8	1699	2910
83	SEG9	1499	2910
84	SEG10	1300	2910
85	SEG11	1100	2910
86	SEG12	901	2910
87	SEG13	701	2910
88	SEG14	502	2910
89	SEG15	299	2910
90	SEG16	99	2910
91	SEG17	–101	2910
92	SEG18	–301	2910
93	SEG19	–500	2910
94	SEG20	–700	2910
95	SEG21	–899	2910
96	SEG22	–1099	2910
97	SEG23	–1302	2910
98	SEG24	–1501	2910
99	SEG25	–1701	2910
100	SEG26	–2051	2910

Figure 10 HCD66710A00

Chip Shipment Products

- HCD66710***



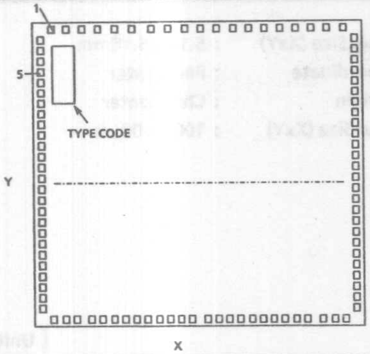
Chip size (X × Y): 5.36 mm × 6.06 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 100 µm × 100 µm

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y
1	SEG27	–2495	2910	35	COM20	–1102	–2910	68	DB4	2675	501
2	SEG28	–2695	2730	36	COM19	–899	–2910	69	DB5	2675	700
3	SEG29	–2695	2499	37	COM18	–700	–2910	70	DB6	2675	900
4	SEG30	–2695	2300	38	COM17	–500	–2910	71	DB7	2675	1099
5	SEG31	–2695	2100	39	COM8	–301	–2910	72	EXT	2675	1299
6	SEG32	–2695	1901	40	COM7	–101	–2910	73	TEST	2675	1502
7	SEG33	–2695	1698	41	COM6	99	–2910	74	V_{CC}	2695	1698
8	SEG34	–2695	1498	42	COM5	302	–2910	75	SEG1	2695	1901
9	SEG35	–2695	1295	43	COM4	502	–2910	76	SEG2	2695	2104
10	SEG36	–2695	1099	44	COM3	698	–2910	77	SEG3	2695	2300
11	SEG37	–2695	900	45	COM2	887	–2910	78	SEG4	2695	2503
12	SEG38	–2695	700	46	COM1	1077	–2910	79	SEG5	2695	2730
13	SEG39	–2695	501	47	COM33	1266	–2910	80	SEG6	2495	2910
14	SEG40	–2695	301	48	V1	1488	–2910	81	SEG7	2049	2910
15	COM9	–2695	98	49	V2	1710	–2910	82	SEG8	1699	2910
16	COM10	–2695	–113	50	V3	2063	–2910	83	SEG9	1499	2910
17	COM11	–2695	–302	51	V4	2458	–2910	84	SEG10	1300	2910
18	COM12	–2695	–501	52	V5	2660	–2731	85	SEG11	1100	2910
19	COM13	–2695	–701	53	V5OUT3	2660	–2500	86	SEG12	901	2910
20	COM14	–2695	–900	54	V5OUT2	2660	–2300	87	SEG13	701	2910
21	COM15	–2695	–1100	55	GND	2640	–2090	88	SEG14	502	2910
22	COM16	–2695	–1303	56	C1	2650	–1887	89	SEG15	299	2910
23	COM25	–2695	–1502	57	C2	2675	–1702	90	SEG16	99	2910
24	COM26	–2695	–1702	58	VCI	2675	–1502	91	SEG17	–101	2910
25	COM27	–2695	–1901	59	OSC1	2675	–1303	92	SEG18	–301	2910
26	COM28	–2695	–2101	60	OSC2	2675	–1103	93	SEG19	–500	2910
27	COM29	–2695	–2300	61	RS	2675	–900	94	SEG20	–700	2910
28	COM30	–2695	–2500	62	R/W	2675	–701	95	SEG21	–899	2910
29	COM31	–2695	–2731	63	E	2675	–501	96	SEG22	–1099	2910
30	COM32	–2495	–2910	64	DB0	2675	–302	97	SEG23	–1302	2910
31	COM24	–2051	–2910	65	DB1	2675	–99	98	SEG24	–1501	2910
32	COM23	–1701	–2910	66	DB2	2675	98	99	SEG25	–1701	2910
33	COM22	–1498	–2910	67	DB3	2675	301	100	SEG26	–2051	2910
34	COM21	–1302	–2910								

Figure 11 HCD66710***

• HD61202D



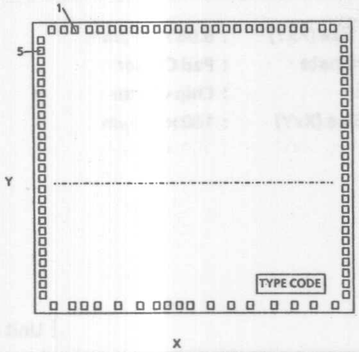
Chip Size (XxY) : 6.08 × 5.92mm
Coordinate : Pad Center
Origin : Chip Center
Pad Size (XxY) : 100 × 100μm

[Unit : μm]

Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y
1	ADC	−2674	2806	35	Y38	−1174	−2806	69	Y4	2882	610
2	M	−2882	2612	36	Y37	−962	−2806	70	Y3	2882	826
3	VCC	−2882	2400	37	Y36	−750	−2806	71	Y2	2882	1042
4	V4R	−2882	2213	38	Y35	−538	−2806	72	Y1	2882	1258
5	V3R	−2882	2030	39	Y34	−326	−2806	73	VEE1	2882	1490
6	V2R	−2882	1838	40	Y33	−114	−2806	74	V1L	2882	1670
7	V1R	−2882	1655	41	Y32	98	−2806	75	V2L	2882	1847
8	VEE2	−2882	1478	42	Y31	314	−2806	76	V3L	2882	2030
9	Y64	−2882	1258	43	Y30	530	−2806	77	V4L	2882	2213
10	Y63	−2882	1042	44	Y29	746	−2806	78	GND	2882	2400
11	Y62	−2882	826	45	Y28	962	−2806	79	DB0	2882	2618
12	Y61	−2882	610	46	Y27	1178	−2806	80	DB1	2514	2806
13	Y60	−2882	394	47	Y26	1394	−2806	81	DB2	2262	2806
14	Y59	−2882	178	48	Y25	1610	−2806	82	DB3	1922	2806
15	Y58	−2882	−38	49	Y24	1826	−2806	83	DB4	1670	2806
16	Y57	−2882	−254	50	Y23	2042	−2806	84	DB5	1330	2806
17	Y56	−2882	−470	51	Y22	2378	−2806	85	DB6	1078	2806
18	Y55	−2882	−686	52	Y21	2590	−2806	86	DB7	738	2806
19	Y54	−2882	−902	53	Y20	2802	−2806	87			
20	Y53	−2882	−1118	54	Y19	2882	−2630	88			
21	Y52	−2882	−1334	55	Y18	2882	−2414	89			
22	Y51	−2882	−1550	56	Y17	2882	−2198	90	CS3	426	2806
23	Y50	−2882	−1766	57	Y16	2882	−1982	91	CS2	126	2806
24	Y49	−2882	−1982	58	Y15	2882	−1766	92	CS1	−134	2806
25	Y48	−2882	−2198	59	Y14	2882	−1550	93	RST	−434	2806
26	Y47	−2882	−2414	60	Y13	2882	−1334	94	RW	−694	2806
27	Y46	−2882	−2630	61	Y12	2882	−1118	95	DI	−994	2806
28	Y45	−2802	−2806	62	Y11	2882	−902	96	CL	−1254	2806
29	Y44	−2586	−2806	63	Y10	2882	−686	97	C2	−1554	2806
30	Y43	−2370	−2806	64	Y9	2882	−470	98	C1	−1814	2806
31	Y42	−2034	−2806	65	Y8	2882	−254	99	E	−2114	2806
32	Y41	−1818	−2806	66	Y7	2882	−38	100	FRM	−2374	2806
33	Y40	−1602	−2806	67	Y6	2882	178				
34	Y39	−1386	−2806	68	Y5	2882	394				

Figure 12 HD61202D

- HD61203D



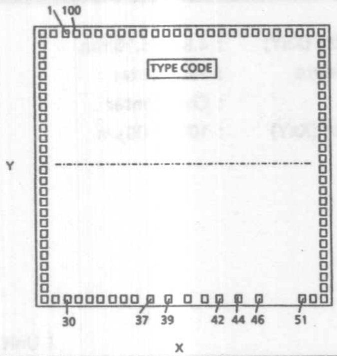
Chip Size (XxY) : 5.18×5.18mm
Coordinate : Pad Center
Origin : Chip Center
Pad Size (XxY) : 100×100μm

[Unit : μm]

Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y
1	X22	−1928	2440	35	R	−904	−2440	69	X54	2440	737
2	X21	−2103	2440	36				70	X53	2440	912
3	X20	−2278	2440	37	CR	−572	−2440	71	X52	2440	1087
4	X19	−2440	2224	38				72	X51	2440	1262
5	X18	−2440	2049	39	SHL	−372	−2440	73	X50	2440	1437
6	X17	−2440	1874	40	GND	−172	−2440	74	X49	2440	1612
7	X16	−2440	1699	41				75	X48	2440	1787
8	X15	−2440	1524	42	MS	16	−2440	76	X47	2440	1962
9	X14	−2440	1349	43	CK2	344	−2440	77	X46	2440	2137
10	X13	−2440	1174	44	CK1	644	−2440	78	X45	2440	2312
11	X12	−2440	999	45				79	X44	2265	2440
12	X11	−2440	824	46	FRM	908	−2440	80	X43	2090	2440
13	X10	−2440	649	47	M	1232	−2440	81	X42	1809	2440
14	X9	−2440	474	48				82	X41	1634	2440
15	X8	−2440	299	49	FCS	1568	−2440	83	X40	1459	2440
16	X7	−2440	124	50	DR	1868	−2440	84	X39	1284	2440
17	X6	−2440	−59	51				85	X38	1102	2440
18	X5	−2440	−234	52	CL2	2268	−2440	86	X37	922	2440
19	X4	−2440	−409	53				87	X36	742	2440
20	X3	−2440	−587	54	V1R	2440	−1980	88	X35	562	2440
21	X2	−2440	−762	55	V2R	2440	−1804	89	X34	387	2440
22	X1	−2440	−937	56	V5R	2440	−1549	90	X33	212	2440
23	VEE1	−2440	−1112	57	V6R	2440	−1374	91	X32	−55	2440
24	V6L	−2440	−1287	58	VEE2	2440	−1199	92	X31	−230	2440
25	V5L	−2440	−1462	59	X64	2440	−1024	93	X30	−405	2440
26	V2L	−2440	−1701	60	X63	2440	−849	94	X29	−580	2440
27	V1L	−2440	−1876	61	X62	2440	−674	95	X28	−767	2440
28	VCC	−2440	−2052	62	X61	2440	−499	96	X27	−942	2440
29	DL	−2248	−2440	63	X60	2440	−324	97	X26	−1117	2440
30	FS	−1944	−2440	64	X59	2440	−149	98	X25	−1292	2440
31	DS1	−1736	−2440	65	X58	2440	26	99	X24	−1483	2440
32	DS2	−1520	−2440	66	X57	2440	212	100	X23	−1658	2440
33	C	−1192	−2440	67	X56	2440	387				
34				68	X55	2440	562				

Figure 13 HD61203D

• HD66100D



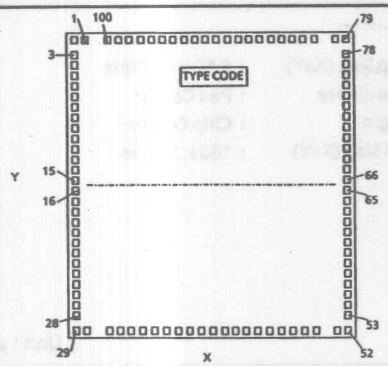
Chip Size (XxY)	: 4.50×4.50mm
Coordinate	: Pad Center
Origin	: Chip Center
Pad Size (XxY)	: 100×100μm

[Unit : μm]

Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y
1	Y30	−1725	2100	35	V4	−880	−2100	69	Y62	2100	560
2	Y29	−1925	2100	36	GND	−720	−2100	70	Y61	2100	720
3	Y28	−2100	2060	37	CL1	−470	−2100	71	Y60	2100	880
4	Y27	−2100	1865	38				72	Y59	2100	1040
5	Y26	−2100	1690	39	SHL	−270	−2100	73	Y58	2100	1200
6	Y25	−2100	1520	40	CL2	−70	−2100	74	Y57	2100	1360
7	Y24	−2100	1360	41	DI	130	−2100	75	Y56	2100	1520
8	Y23	−2100	1200	42	DO	350	−2100	76	Y55	2100	1690
9	Y22	−2100	1040	43				77	Y54	2100	1865
10	Y21	−2100	880	44	M	620	−2100	78	Y53	2100	2060
11	Y20	−2100	720	45				79	Y52	1925	2100
12	Y19	−2100	560	46	VCC	980	−2100	80	Y51	1725	2100
13	Y18	−2100	400	47				81	Y50	1520	2100
14	Y17	−2100	240	48				82	Y49	1360	2100
15	Y16	−2100	80	49				83	Y48	1200	2100
16	Y15	−2100	−80	50				84	Y47	1040	2100
17	Y14	−2100	−240	51	Y80	1725	−2100	85	Y46	880	2100
18	Y13	−2100	−400	52	Y79	1925	−2100	86	Y45	720	2100
19	Y12	−2100	−560	53	Y78	2100	−2060	87	Y44	560	2100
20	Y11	−2100	−720	54	Y77	2100	−1865	88	Y43	400	2100
21	Y10	−2100	−880	55	Y76	2100	−1690	89	Y42	240	2100
22	Y9	−2100	−1040	56	Y75	2100	−1520	90	Y41	80	2100
23	Y8	−2100	−1200	57	Y74	2100	−1360	91	Y40	−80	2100
24	Y7	−2100	−1360	58	Y73	2100	−1200	92	Y39	−240	2100
25	Y6	−2100	−1520	59	Y72	2100	−1040	93	Y38	−400	2100
26	Y5	−2100	−1690	60	Y71	2100	−880	94	Y37	−560	2100
27	Y4	−2100	−1865	61	Y70	2100	−720	95	Y36	−720	2100
28	Y3	−2100	−2060	62	Y69	2100	−560	96	Y35	−880	2100
29	Y2	−1925	−2100	63	Y68	2100	−400	97	Y34	−1040	2100
30	Y1	−1725	−2100	64	Y67	2100	−240	98	Y33	−1200	2100
31	VEE	−1520	−2100	65	Y66	2100	−80	99	Y32	−1360	2100
32	V1	−1360	−2100	66	Y65	2100	80	100	Y31	−1520	2100
33	V2	−1200	−2100	67	Y64	2100	240				
34	V3	−1040	−2100	68	Y63	2100	400				

Figure 14 HD66100D

- HD66106D



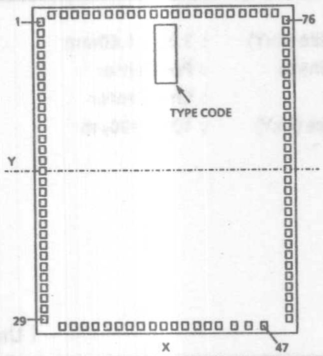
Chip Size (XxY) : 4.84 × 5.16mm
Coordinate : Pad Center
Origin : Chip Center
Pad Size (XxY) : 100 × 100μm

[Unit : μm]

Pad	Function	Coordinate		Pad	Function	Coordinate		Pad	Function	Coordinate	
No		X	Y	No		X	Y	No		X	Y
1	Y30	−2025	2430	35	V4	−963	−2430	69	Y62	2270	613
2	Y29	−2210	2430	36	VLCD2	−780	−2430	70	Y61	2270	788
3	Y28	−2270	2188	37	GND	−604	−2430	71	Y60	2270	963
4	Y27	−2270	2013	38	CL1	−428	−2430	72	Y59	2270	1138
5	Y26	−2270	1838	39	SHL	−235	−2430	73	Y58	2270	1313
6	Y25	−2270	1663	40	CL2	−44	−2430	74	Y57	2270	1488
7	Y24	−2270	1488	41	CH1	148	−2430	75	Y56	2270	1663
8	Y23	−2270	1313	42	M	341	−2430	76	Y55	2270	1838
9	Y22	−2270	1138	43	D3	532	−2430	77	Y54	2270	2013
10	Y21	−2270	963	44	D2	725	−2430	78	Y53	2270	2188
11	Y20	−2270	788	45	D1	916	−2430	79	Y52	2210	2430
12	Y19	−2270	613	46	D0	1109	−2430	80	Y51	2025	2430
13	Y18	−2270	438	47	E	1300	−2430	81	Y50	1663	2430
14	Y17	−2270	263	48	CAR	1484	−2430	82	Y49	1488	2430
15	Y16	−2270	88	49	VCC	1668	−2430	83	Y48	1313	2430
16	Y15	−2270	−88					84	Y47	1138	2430
17	Y14	−2270	−263	51	Y80	2025	−2430	85	Y46	963	2430
18	Y13	−2270	−438	52	Y79	2210	−2430	86	Y45	788	2430
19	Y12	−2270	−613	53	Y78	2270	−2188	87	Y44	613	2430
20	Y11	−2270	−788	54	Y77	2270	−2013	88	Y43	438	2430
21	Y10	−2270	−963	55	Y76	2270	−1838	89	Y42	263	2430
22	Y9	−2270	−1138	56	Y75	2270	−1663	90	Y41	88	2430
23	Y8	−2270	−1313	57	Y74	2270	−1488	91	Y40	−88	2430
24	Y7	−2270	−1488	58	Y73	2270	−1313	92	Y39	−263	2430
25	Y6	−2270	−1663	59	Y72	2270	−1138	93	Y38	−438	2430
26	Y5	−2270	−1838	60	Y71	2270	−963	94	Y37	−613	2430
27	Y4	−2270	−2013	61	Y70	2270	−788	95	Y36	−788	2430
28	Y3	−2270	−2188	62	Y69	2270	−613	96	Y35	−963	2430
29	Y2	−2210	−2430	63	Y68	2270	−438	97	Y34	−1138	2430
30	Y1	−2025	−2430	64	Y67	2270	−263	98	Y33	−1313	2430
31	VLCD1	−1663	−2430	65	Y66	2270	−88	99	Y32	−1488	2430
32	V1	−1488	−2430	66	Y65	2270	88	100	Y31	−1663	2430
33	V2	−1313	−2430	67	Y64	2270	263				
34	V3	−1138	−2430	68	Y63	2270	438				

Figure 15 HD66106D

- HCD66204



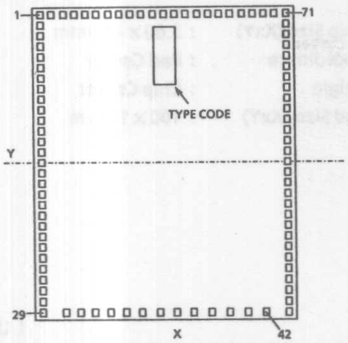
Chip Size (XxY) : 3.80 × 4.60mm
Coordinate : Pad Center
Origin : Chip Center
Pad Size (XxY) : 100 × 100μm

[Unit : μm]

Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y
1	Y51	−1748	2150	34	V4	−952	−2150	67	Y20	1750	735
2	Y52	−1750	1940	35	VEE	−812	−2150	68	Y21	1750	880
3	Y53	−1750	1770	36	M	−652	−2150	69	Y22	1750	1025
4	Y54	−1750	1615	37	CL1	−438	−2150	70	Y23	1750	1170
5	Y55	−1750	1470	38	GND	−250	−2150	71	Y24	1750	1315
6	Y56	−1750	1325	39	DISPOFF	−82	−2150	72	Y25	1750	1460
7	Y57	−1750	1180	40	VCC	98	−2150	73	Y26	1750	1605
8	Y58	−1750	1035	41	SHL	278	−2150	74	Y27	1750	1750
9	Y59	−1750	890	42	D3	426	−2150	75	Y28	1750	1900
10	Y60	−1750	745	43	D2	640	−2150	76	Y29	1750	2120
11	Y61	−1750	600	44	D1	788	−2150	77	Y30	1610	2150
12	Y62	−1750	455	45	D0	1002	−2150	78	Y31	1432	2150
13	Y63	−1750	310	46	CL2	1150	−2150	79	Y32	1273	2150
14	Y64	−1750	165	47	CAR	1458	−2150	80	Y33	1114	2150
15	Y65	−1750	20	48	Y1	1750	−2150	81	Y34	955	2150
16	Y66	−1750	−125	49	Y2	1750	−1930	82	Y35	796	2150
17	Y67	−1750	−270	50	Y3	1750	−1760	83	Y36	637	2150
18	Y68	−1750	−415	51	Y4	1750	−1605	84	Y37	478	2150
19	Y69	−1750	−560	52	Y5	1750	−1460	85	Y38	319	2150
20	Y70	−1750	−705	53	Y6	1750	−1315	86	Y39	160	2150
21	Y71	−1750	−850	54	Y7	1750	−1170	87	Y40	1	2150
22	Y72	−1750	−995	55	Y8	1750	−1025	88	Y41	−158	2150
23	Y73	−1750	−1140	56	Y9	1750	−860	89	Y42	−317	2150
24	Y74	−1750	−1285	57	Y10	1750	−715	90	Y43	−476	2150
25	Y75	−1750	−1430	58	Y11	1750	−570	91	Y44	−635	2150
26	Y76	−1750	−1575	59	Y12	1750	−425	92	Y45	−794	2150
27	Y77	−1750	−1720	60	Y13	1750	−280	93	Y46	−953	2150
28	Y78	−1750	−1865	61	Y14	1750	−135	94	Y47	−1112	2150
29	Y79	−1750	−2110	62	Y15	1750	10	95	Y48	−1271	2150
30	Y80	−1610	−2150	63	Y16	1750	155	96	Y49	−1430	2150
31	E	−1434	−2150	64	Y17	1750	300	97	Y50	−1589	2150
32	V1	−1232	−2150	65	Y18	1750	445				
33	V3	−1092	−2150	66	Y19	1750	590				

Figure 16 HCD66204

- HCD66205



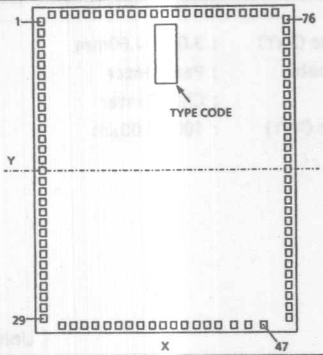
Chip Size (XxY) : 3.80 × 4.60mm
Coordinate : Pad Center
Origin : Chip Center
Pad Size (XxY) : 100 × 100μm

[Unit : μm]

Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y
1	X51	– 1748	2150	32	VEE	– 1042	– 2150	63	X21	1750	880
2	X52	– 1750	1940	33	V5	– 842	– 2150	64	X22	1750	1025
3	X53	– 1750	1770	34	V6	– 644	– 2150	65	X23	1750	1170
4	X54	– 1750	1615	35	V1	– 444	– 2150	66	X24	1750	1315
5	X55	– 1750	1470	35	DISPOFF	– 222	– 2150	67	X25	1750	1460
6	X56	– 1750	1325	37	VCC	– 16	– 2150	68	X26	1750	1605
7	X57	– 1750	1180	38	SHL	206	– 2150	69	X27	1750	1750
8	X58	– 1750	1035	39	GND	474	– 2150	70	X28	1750	1900
9	X59	– 1750	890	40	M	746	– 2150	71	X29	1750	2120
10	X60	– 1750	745	41	CL	1010	– 2150	72	X30	1610	2150
11	X61	– 1750	600	42	D1	1274	– 2150	73	X31	1432	2150
12	X62	– 1750	455	43	X1	1750	– 2150	74	X32	1273	2150
13	X63	– 1750	310	44	X2	1750	– 1930	75	X33	1114	2150
14	X64	– 1750	165	45	X3	1750	– 1760	76	X34	955	2150
15	X65	– 1750	20	46	X4	1750	– 1605	77	X35	796	2150
16	X66	– 1750	– 125	47	X5	1750	– 1460	78	X36	637	2150
17	X67	– 1750	– 270	48	X6	1750	– 1315	79	X37	478	2150
18	X68	– 1750	– 415	49	X7	1750	– 1170	80	X38	319	2150
19	X69	– 1750	– 560	50	X8	1750	– 1025	81	X39	160	2150
20	X70	– 1750	– 705	51	X9	1750	– 860	82	X40	1	2150
21	X71	– 1750	– 850	52	X10	1750	– 715	83	X41	– 158	2150
22	X72	– 1750	– 995	53	X11	1750	– 570	84	X42	– 317	2150
23	X73	– 1750	– 1140	54	X12	1750	– 425	85	X43	– 476	2150
24	X74	– 1750	– 1285	55	X13	1750	– 280	86	X44	– 635	2150
25	X75	– 1750	– 1430	56	X14	1750	– 135	87	X45	– 794	2150
26	X76	– 1750	– 1575	57	X15	1750	10	88	X46	– 953	2150
27	X77	– 1750	– 1720	58	X16	1750	155	89	X47	– 1112	2150
28	X78	– 1750	– 1865	59	X17	1750	300	90	X48	– 1271	2150
29	X79	– 1750	– 2110	60	X18	1750	445	91	X49	– 1430	2150
30	X80	– 1610	– 2150	61	X19	1750	590	92	X50	– 1589	2150
31	D0	– 1294	– 2150	62	X20	1750	735				

Figure 17 HCD66205

- HCD66204L



Chip Size (XxY) : 3.80×4.60mm
Coordinate : Pad Center
Origin : Chip Center
Pad Size (XxY) : 100×100μm

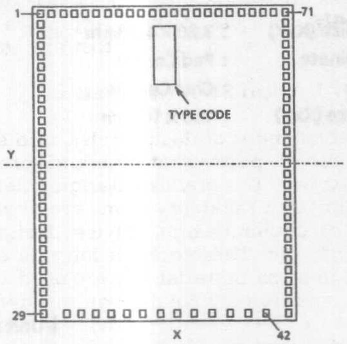
[Unit : μm]

Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y
1	Y51	−1748	2150	34	V4	−952	−2150	67	Y20	1750	735
2	Y52	−1750	1940	35	VEE	−812	−2150	68	Y21	1750	880
3	Y53	−1750	1770	36	M	−652	−2150	69	Y22	1750	1025
4	Y54	−1750	1615	37	CL1	−438	−2150	70	Y23	1750	1170
5	Y55	−1750	1470	38	GND	−250	−2150	71	Y24	1750	1315
6	Y56	−1750	1325	39	DISPOFF	−82	−2150	72	Y25	1750	1460
7	Y57	−1750	1180	40	VCC	98	−2150	73	Y26	1750	1605
8	Y58	−1750	1035	41	SHL	278	−2150	74	Y27	1750	1750
9	Y59	−1750	890	42	D3	426	−2150	75	Y28	1750	1900
10	Y60	−1750	745	43	D2	640	−2150	76	Y29	1750	2120
11	Y61	−1750	600	44	D1	788	−2150	77	Y30	1610	2150
12	Y62	−1750	455	45	D0	1002	−2150	78	Y31	1432	2150
13	Y63	−1750	310	46	CL2	1150	−2150	79	Y32	1273	2150
14	Y64	−1750	165	47	CAR	1458	−2150	80	Y33	1114	2150
15	Y65	−1750	20	48	Y1	1750	−2150	81	Y34	955	2150
16	Y66	−1750	−125	49	Y2	1750	−1930	82	Y35	796	2150
17	Y67	−1750	−270	50	Y3	1750	−1760	83	Y36	637	2150
18	Y68	−1750	−415	51	Y4	1750	−1605	84	Y37	478	2150
19	Y69	−1750	−560	52	Y5	1750	−1460	85	Y38	319	2150
20	Y70	−1750	−705	53	Y6	1750	−1315	86	Y39	160	2150
21	Y71	−1750	−850	54	Y7	1750	−1170	87	Y40	1	2150
22	Y72	−1750	−995	55	Y8	1750	−1025	88	Y41	−158	2150
23	Y73	−1750	−1140	56	Y9	1750	−860	89	Y42	−317	2150
24	Y74	−1750	−1285	57	Y10	1750	−715	90	Y43	−476	2150
25	Y75	−1750	−1430	58	Y11	1750	−570	91	Y44	−635	2150
26	Y76	−1750	−1575	59	Y12	1750	−425	92	Y45	−794	2150
27	Y77	−1750	−1720	60	Y13	1750	−280	93	Y46	−953	2150
28	Y78	−1750	−1865	61	Y14	1750	−135	94	Y47	−1112	2150
29	Y79	−1750	−2110	62	Y15	1750	10	95	Y48	−1271	2150
30	Y80	−1610	−2150	63	Y16	1750	155	96	Y49	−1430	2150
31	E	−1434	−2150	64	Y17	1750	300	97	Y50	−1589	2150
32	V1	−1232	−2150	65	Y18	1750	445				
33	V3	−1092	−2150	66	Y19	1750	590				

Figure 18 HCD66204L

Chip Shipment Products

- HCD66205L



Chip Size (XxY) : 3.80 × 4.60mm
Coordinate : Pad Center
Origin : Chip Center
Pad Size (XxY) : 100 × 100μm

[Unit : μm]

Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y	Pad No	Function	Coordinate X	Coordinate Y
1	X51	−1748	2150	32	VEE	−1042	−2150	63	X21	1750	880
2	X52	−1750	1940	33	V5	−842	−2150	64	X22	1750	1025
3	X53	−1750	1770	34	V6	−644	−2150	65	X23	1750	1170
4	X54	−1750	1615	35	V1	−444	−2150	66	X24	1750	1315
5	X55	−1750	1470	35	DISPOFF	−222	−2150	67	X25	1750	1460
6	X56	−1750	1325	37	VCC	−16	−2150	68	X26	1750	1605
7	X57	−1750	1180	38	SHL	206	−2150	69	X27	1750	1750
8	X58	−1750	1035	39	GND	474	−2150	70	X28	1750	1900
9	X59	−1750	890	40	M	746	−2150	71	X29	1750	2120
10	X60	−1750	745	41	CL	1010	−2150	72	X30	1610	2150
11	X61	−1750	600	42	D1	1274	−2150	73	X31	1432	2150
12	X62	−1750	455	43	X1	1750	−2150	74	X32	1273	2150
13	X63	−1750	310	44	X2	1750	−1930	75	X33	1114	2150
14	X64	−1750	165	45	X3	1750	−1760	76	X34	955	2150
15	X65	−1750	20	46	X4	1750	−1605	77	X35	796	2150
16	X66	−1750	−125	47	X5	1750	−1460	78	X36	637	2150
17	X67	−1750	−270	48	X6	1750	−1315	79	X37	478	2150
18	X68	−1750	−415	49	X7	1750	−1170	80	X38	319	2150
19	X69	−1750	−560	50	X8	1750	−1025	81	X39	160	2150
20	X70	−1750	−705	51	X9	1750	−860	82	X40	1	2150
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23	X73	−1750	−1140	54	X12	1750	−425	85	X43	−476	2150
24	X74	−1750	−1285	55	X13	1750	−280	86	X44	−635	2150
25	X75	−1750	−1430	56	X14	1750	−135	87	X45	−794	2150
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28	X78	−1750	−1865	59	X17	1750	300	90	X48	−1271	2150
29	X79	−1750	−2110	60	X18	1750	445	91	X49	−1430	2150
30	X80	−1610	−2150	61	X19	1750	590	92	X50	−1589	2150
31	D0	−1294	−2150	62	X20	1750	735				

Figure 19 HCD66205L

Reliability and Quality Assurance

1. Views on Quality and Reliability

Hitachi's basic quality aims are to meet individual user's purchase purpose and quality required, and to be at a satisfactory quality level considering general marketability. Quality required by users is specifically clear if the contract specification is provided. If not, quality required is not always definite. In both cases, Hitachi tries to assure reliability so that semiconductor devices delivered can perform their function in actual operating circumstances. To realize this quality in the manufacturing process, the key points should be to establish a quality control system in the process and to enhance the quality ethic.

In addition, quality required by users of semiconductor devices is going toward higher levels as performance of electronic system in the market is increasing and expanding in size and application fields. To cover the situation, Hitachi is performing the following:

1. Building in reliability in design at the stage of new product development.
2. Buliding in quality at the sources of the manufacturing process.
3. Executing stricter inspection and reliability confirmation of final products.
4. Making quality levels higher with field data feedback.
5. Cooperating with research laboratories for higher quality and reliability.

With the views and methods mentioned above, utmost efforts are made to meet users' requirements.

2. Reliability Design of Semiconductor Devices

2.1 Reliability Targets

The reliability target is the important factor in manufacture and sales as well as performance and price. It is not practical to rate reliability targets with failure rates under certain common test conditions. The reliability target is determined corresponding to the character of equipment taking design, manufacture, inner process quality control, screening and test method, etc. into consideration, and considering the operating circumstances of equipment the semiconductor device is used in, reliability target of the system, derating applied in design, operating condition, maintenance, etc.

2.2 Reliability Design

To achieve the reliability required based on reliability targets, timely study and execution of design standardization, device design (including process . design, structure design), design review, reliability test are essential.

2.2.1 Design Standardization

Establishment of design rules, and standardization of parts, material and process are necessary. To establish design rules, critical quality and reliability items are always studied at circuit design, device design, layout design, etc. Therefore, as long as standardized process, material, etc. are used, reliability risk is extremely small even in newly developed devices, except in cases where special functions are needed.

2.2.2 Device Design

It is important in device design to consider the total balance of process design, structure design, circuit and layout design. Especially when new processes and new materials are employed, careful technical study is executed prior to device development.

2.2.3 Reliability Evaluation by Test Site

Test site is sometimes called test pattern. It is a useful method for design and process reliability evaluation of ICs and LSIs which have complicated functions.

Purposes of test site are:

- Making fundamental failure mode clear
- Analysis of relation between failure mode and manufacturing process condition
- Search for failure mechanism analysis
- Establishment of QC point in manufacturing

Evaluation by test site is effective because:

- Common fundamental failure mode and failure machanism in devices can be evaluated.
- Factors dominating failure mode can be picked up, and comparison can be made with processes that have been experienced in field.
- Relation between failure causes and manufacturing factors can be analyzed.
- Easy to run tests.
- Etc.

2.3 Design Review

Design review is an organized method to confirm that a design satisfies the required performance (including users') and that design work follows the specified methods, and whether or not improved technical items accumulated in test data of individual major

fields and field data are effectively built in. In addition, from the standpoint of enhancement of the competitive power of products, the major purpose of the design review is to ensure quality and reliability of the products. In Hitachi, design reviews are performed from the planning stage for new products and even for design changed products. Items discussed and determined at design review are as follows:

1. Description of the products based on specified design documents.
2. From the standpoint of the specialties of individual participants, design documents are studied, and if unclear matter is found, calculation, experiments, investigation, etc. will be carried out.
3. Determine contents of reliability and methods, etc. based on design documents and drawings.
4. Check process ability of manufacturing line to achieve design goal.
5. Discussion about preparation for production.
6. Planning and execution of subprograms for design changes proposed by individual specialists, and for tests, experiments and calculation to confirm the design changes.
7. Reference of past failure experiences with similar devices, confirmation of methods to prevent them, and planning and execution of test programs for confirmation of them. These studies and decisions are made using check lists made individually depending on the objects.

3. Quality Assurance System of Semiconductor Devices

3.1 Activity of Quality Assurance

General views of overall quality assurance in Hitachi are:

1. Problems in an individual process should be solved in the process. Therefore, at final product stage, the potential failure factors have been already removed.
2. Feedback of information should be used to ensure satisfactory level of process capability.
3. To assure required reliability as a result of the items mentioned above is the purpose of quality assurance.

The following discusses device design, quality approval at mass production, inner process quality control, product inspection and reliability tests.

3.2 Quality Approval

To ensure required quality and reliability, quality approval is carried out at the trial production stage of device design and the mass production stage based on reliability design as described in section 2.

Hitachi's views on quality approval are:

1. A third party must perform approval objectively from the standpoint of customers.
2. Fully consider past failure experiences and information from the field.
3. Approval is needed for design change or work change.
4. Intensive approval is executed on parts material and process.
5. Study process capability and variation factor, and set up control points at mass production stage.

Considering the views mentioned above, figure 1 shows how quality approval is performed.

3.3 Quality and Reliability Control at Mass Production

For quality assurance of products in mass production, quality control execution is divided organically by function between manufacturing department and quality assurance department, and other related departments. The total function flow is shown in figure 2. The main points are described below.

3.3.1 Quality Control of Parts and Material

As the performance and the reliability of semiconductor devices improve, the importance of quality control of material and parts (crystal, lead frame, fine wire for wire bonding, package) to build products, and materials needed in manufacturing process (mask pattern and chemicals) increases. Besides quality approval on parts and materials stated in section 3.2, the incoming inspection is also key in quality control of parts and materials. The incoming inspection is performed based on an incoming inspection specification, following purchase specification and drawings, and sampling inspection is executed based mainly on MIL-STD-105D.

The other activities of quality assurance are as follows:

1. Outside vendor technical information meeting
2. Approval on outside vendors, and guidance of outside vendors
3. Physical chemical analysis and test

The typical check points of parts and materials are shown in table 1.

3.3.2 Inner Process Quality Control

Inner process quality control performs a very important function in quality assurance of a semiconductor devices. The following is a description of control of semifinal products, final products, manufacturing facilities, measuring equipments, circumstances and submaterials. The quality control in the manufacturing process is shown in figure 3 corresponding to the manufacturing process.

1. Quality Control of Semifinal Products and Final Production Products
   Potential failure factors of semiconductor devices should be removed in manufacturing process. To achieve this, check points are setup in each process, and products that have potential failure factors are not transferred to the next process. For high reliability semiconductor devices, especially manufacturing line is carefully selected, and the quality control in the manufacturing process is tightly executed: Strict check on each process and each lot, 100% inspection to remove failure factor caused by manufacturing variation, and necessary screening, such as high temperature aging and temperature cycling. Contents of inner process quality control are:
   - Condition control on individual equipment and workers, and sampling check of semifinal products.
   - Proposal and carrying-out of work improvement
   - Education of workers
   - Maintenance and improvement of yield
   - Detection of quality problems, and execution of countermeasures
   - Transmission of information about quality

2. Quality Control of Manufacturing Facilities and Measuring Equipment
   Equipment for manufacturing semicon-

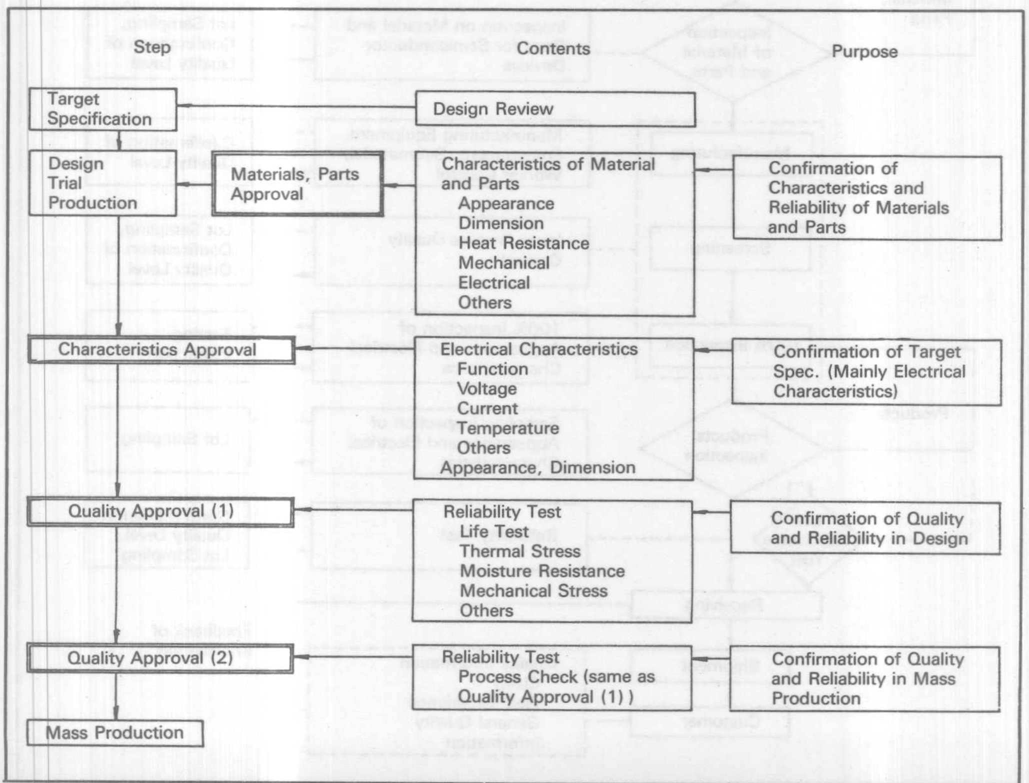


Figure 1. Quality Approval Flowchart

ductor devices have been developing extraordinarily, with required high performance devices and production improvements. They are important factors to determine quality and reliability. In Hitachi, automation of manufacturing equipment is promoted to improve manufacturing variation, and controls maintain proper operation and function of high performance equipment. Maintenance inspection for quality control is performed daily based on related specifications, and also periodical inspections. At the inspection, inspection points listed in the specification are checked one by one to avoid any omissions. During adjustment and maintenance of measuring equipment, maintenance number and specifications are checked one by one to maintain and improve quality.

3. Quality Control of Manufacturing Circumstances and Submaterials

Quality and reliability of semiconductor devices is greatly affected by manufacturing process. Therefore, manufacturing circumstances (temperature, humidity, dust) and the control of submaterials (gas, pure water) used in manufacturing process are intensively controlled. Dust control is described in more detail below.

Dust control is essential to realize higher integration and higher reliability of devices. In Hitachi, maintenance and

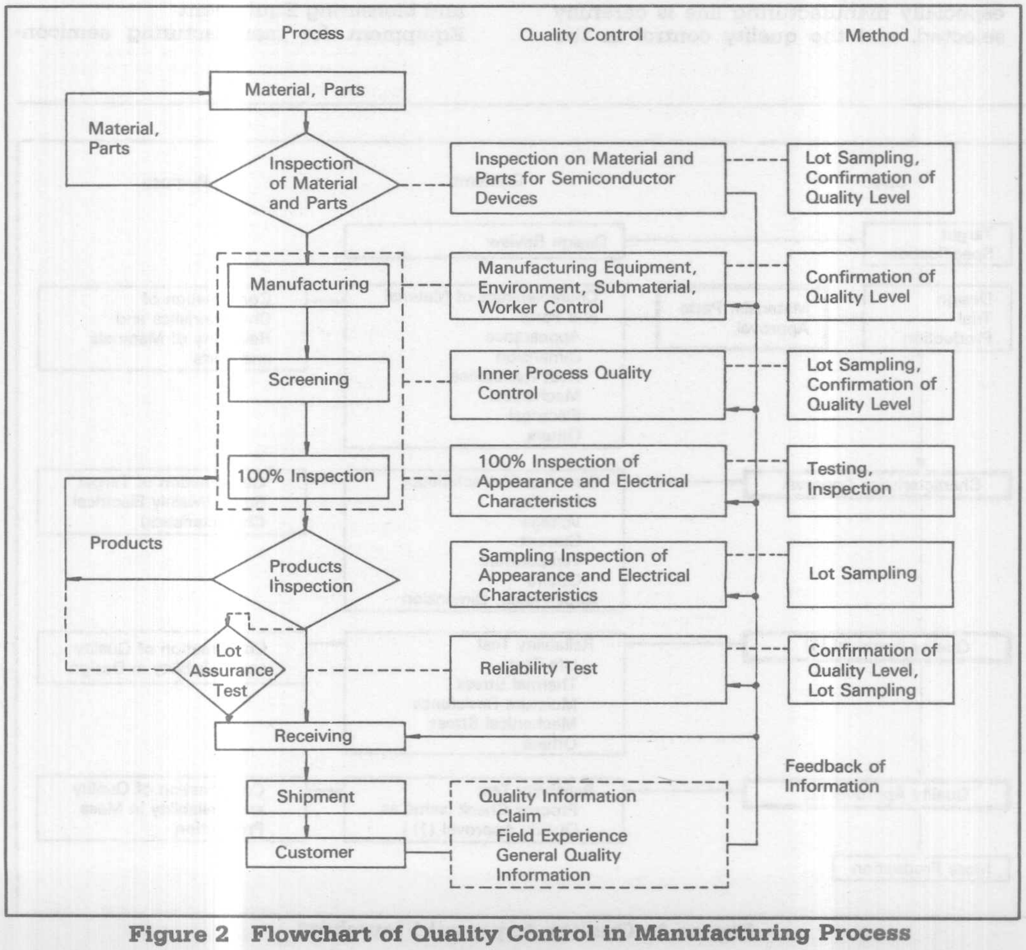


Figure 2 Flowchart of Quality Control in Manufacturing Process

improvement of cleanness and manufacturing site cleanness are executed paying close attention to buildings, facilities, air-conditioning systems, packaging materials, clothes, work, etc., and periodical inspection for floating dust in room, falling dust, and floor dust.

3.3.3 Final Product Inspection and Reliability Assurance

1. Final Product Inspection
Lot inspection is done by quality assurance department for products that were judged to be 100% good in tests, which is the final process in the manufacturing department. Though 100% good products is expected, sampling inspection is executed to prevent inclusion of failed products by mistake, etc. The inspection is executed not only to confirm that the products meet users' requirements, but to consider potential trouble factors. Lot inspection is executed based on MIL-STD-105D.

1. Reliability Assurance Tests
To assure reliability of semiconductor devices, periodical reliability tests and reliability tests on individual manufacturing lots required by user are performed.

Table 1 Quality Control Check Points of Material and Parts (Example)

Material, Parts	Important Control Items	Points to Check
Wafer	Appearance	Damage and contamination on surface
	Dimension	Flatness
	Sheet resistance	Resistance
	Defect density	Defect numbers
	Crystal axis	
Mask	Appearance	Defect numbers, scratch
	Dimension	Dimension level
	Registration	
	Gradation	Uniformity of gradation
Fine wire for wire bonding	Appearance	Contamination, scratch, bend, twist
	Dimension	
	Purity	Purity level
	Elongation ratio	Mechanical strength
Frame	Appearance	Contamination, scratch
	Dimension	Dimension level
	Processing accuracy	
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
Ceramic package	Appearance	Contamination, scratch
	Dimension	Dimension level
	Leak resistance	Airtightness
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
	Electrical characteristics	
	Mechanical strength	Mechanical strength
Plastic	Composition	Characteristics of plastic material
	Electrical characteristics	
	Thermal characteristics	
	Molding performance	Molding performance
	Mounting characteristics	Mounting characteristics

Process		Control point	Purpose of control
Purchase of material			
Wafer	Wafer	Characteristics, Appearance	Scratch, removal of crystal defect wafer
Surface oxidation	Oxidation		Assurance of resistance
Inspection of surface oxidation		Appearance, Thickness of oxide film	Pinhole, Scratch
Photo resist	Photo resist		
Inspection of photo resist		Dimension, Appearance	Dimension level
PQC level check			Check of photo resist
Diffusion	Diffusion	Diffusion depth, Sheet resistance	Diffusion status
Inspection of diffusion		Gate width	Control of basic parameters (V_{TH}, etc.) cleanness of surface
PQC level check		Characteristics of oxide film, Breakdown voltage	Prior check of V_{TH} Breakdown voltage check
Evaporation	Evaporation	Thickness of vapor film, Scratch, Contamination	Assurance of standard thickness
Inspection of evaporation			
PQC level check			
Wafer inspection	Wafer	Thickness, V_{TH} characteristics	Prevention of cracks, Quality assurance of scribe
Inspection of chip electrical characteristics	Chip	Electrical characteristics	
Chip scribe		Appearance of chip	
Inspection of chip appearance			
PQC lot judgement			
Frame			
Assembling	Assembling	Appearance after chip bonding	Quality check of chip Bonding
		Appearance after wire bonding	Quality check of wire Bonding
PQC level check		Pull strength, Compression width, Shear strength	Prevention of open and short
Inspection after assembling		Appearance after assembling	
PQC lot judgement			
Package			
Sealing	Sealing	Appearance after sealing Outline, Dimension	Guarantee of appearance and dimension
PQC level check	Marking	Marking strength	
Final electrical inspection			
Failure analysis		Analysis of failures, Failure mode, Mechanism	Feedback of analysis information
Appearance inspection			
Sampling inspection of products			
Receiving			
Shipment			

Figure 3 Example of Inner Process Quality Control

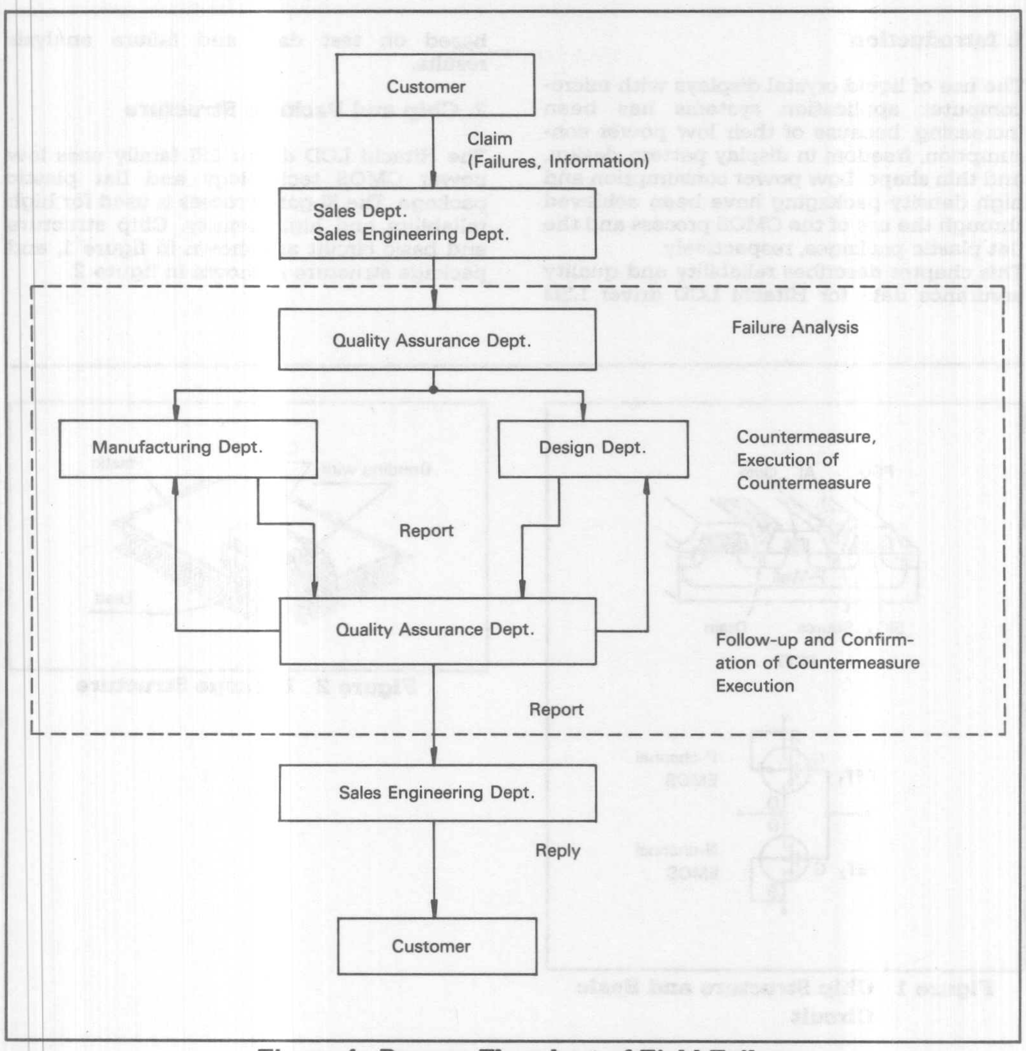


Figure 4 Process Flowchart of Field Failure

Reliability Test Data of LCD Drivers

1. Introduction

The use of liquid crystal displays with microcomputer application systems has been increasing, because of their low power consumption, freedom in display pattern design, and thin shape. Low power consumption and high density packaging have been achieved through the use of the CMOS process and the flat plastic packages, respectively.

This chapter describes reliability and quality assurance data for Hitachi LCD driver LSIs based on test data and failure analysis results.

2. Chip and Package Structure

The Hitachi LCD driver LSI family uses low power CMOS technology and flat plastic package. The Si-gate process is used for high reliability and high density. Chip structure and basic circuit are shown in figure 1, and package structure is shown in figure 2.

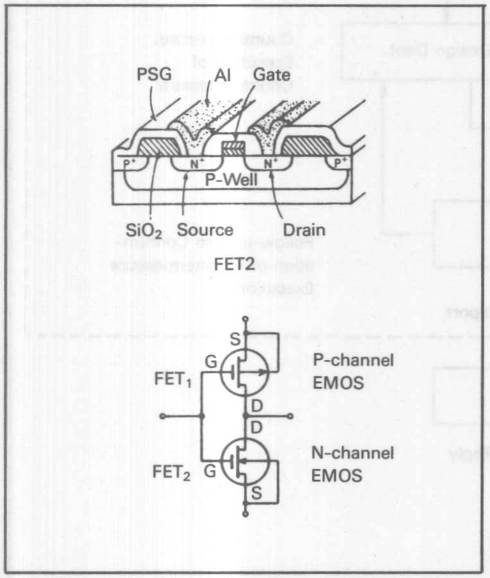


Figure 1 Chip Structure and Basic Circuit

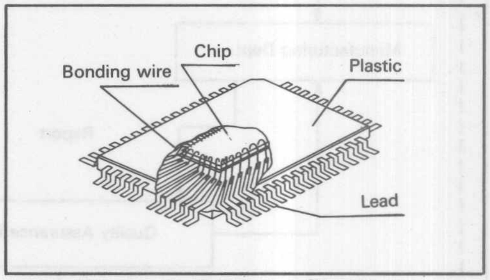


Figure 2 Package Structure

3. Reliability Test Results

The test results of LCD driver LSI family are shown in Tables 1, 2, and 3.

Table 1 Test Result 1, High Temperature Operation (Ta=125°C, V_{CC}=5.5V)

Device	Sample Size	Component Hour	Failure
HD44100H	40	40,000	0
HD44102H	40	40,000	0
HD44103H	40	40,000	0
HD44780	90	90,000	0
HD66100F	45	45,000	0
HD61100A	80	80,000	0
HD61102	50	50,000	0
HD61103A	50	50,000	0
HD61200	40	40,000	0
HD61202	50	50,000	0
HD61203	40	40,000	0
HD61830	40	40,000	0
HD61830B	40	40,000	0
HD63645	32	32,000	0
HD64645	32	32,000	0
HD61602	38	38,000	0
HD61603	32	32,000	0
HD61604	32	32,000	0
HD61605	32	32,000	0
HD66840	45	45,000	0

Table 2 Test Result 2

Test Item	Test Condition	Sample Size	Component Hour	Failure
High temp, storage	Ta=150°C, 1000 h	180	180,000	0
Low temp, storage	Ta=-55°C, 1000 h	140	140,000	0
Steady state humidity	65°C, 95% RH, 1000 h	860	860,000	1*
Steady state humidity, biased	85°C, 90% RH, 1000 h	165	170,000	2*
Pressure cooker	121°C, 2 atm.100 h	200	20,000	0

Note: *Aluminum corrosion

Table 3 Test Results 3

Test Items	Test Condition	Sample Size	Failure
Thermal shock	0 to 100°C 10 cycles	108	0
Temperature cycling	-55°C to 150°C 10 cycles	678	0
Soldering heat	260°C, 10 seconds	283	0
Resistance to VPS	215°C, 30 seconds	88	0
Solderability	230°C, 5 seconds	140	0

4. Quality Data from Field Use

Field failure rate is estimated in advance through production process evaluation and reliability tests. Past field data on similar devices provides the basis for this estimation. Quality information from the users is indispensable to the improvement of product quality. Therefore, field data on products delivered to the users is followed up carefully. On the basis of information furnished by the user, failure analysis is conducted and the results are quickly fed back to the design and production divisions.
Failure analysis results on MOS LSIs returned to Hitachi is shown in figure 3.

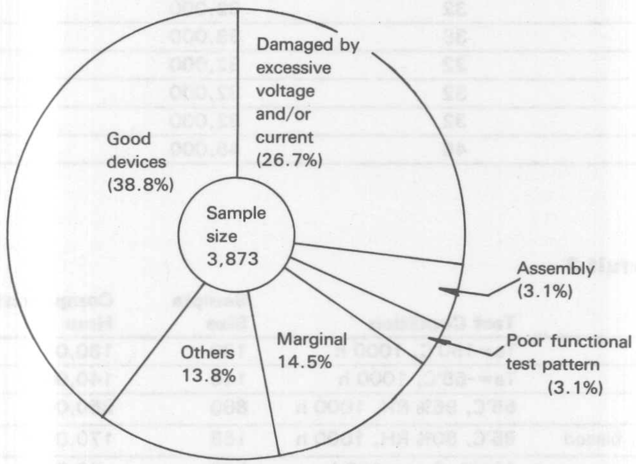


Figure 3 Failure Analysis Result

5. Precautions

5.1 Storage

It is preferable to store semiconductor devices in the following ways to prevent deterioration in their electrical characteristics, solderability, and appearance, or breakage.

1. Store in an ambient temperature of 5 to 30° C, and in a relative humidity of 40 to 60%.
2. Store in a clean air environment, free from dust and reactive gas.
3. Store in a container that does not induce static electricity.
4. Store without any physical load.
5. If semiconductor devices are stored for a long time, store them in unfabricated form. If their lead wires wires are formed beforehand, bent parts may corrode during storage.
6. If the chips are unsealed, store them in a cool, dry, dark, and dustless place. Assemble them within 5 days after unpacking. Storage in nitrogen gas is desirable. They can be stored for 20 days or less in dry nitrogen gas with a dew point at -30°C or lower. Unpackaged devices must not be stored for over 3 months.
7. Take care not to allow condensation during storage due to rapid temperature changes.

5.2 Transportation

As with storage methods, general precautions for other electronic component parts are applicable to the transportation of semiconductors, semiconductor-incorporating units and other similar systems. In addition, the following considerations must be taken, too:

1. Use containers or jigs whch will not induce static electricity as the result of vibration during transportation. It is desirable to use an electrically conductive container or aluminium foil.
2. Prevent device breakage from clothes-induced static electricity.
3. When transporting the printed circuit boards on which semiconductor devices are mounted, suitable preventive measures against static electricity induction must be taken; for example, voltage built-up is prevented by shorting terminal circuit. When a conveyor belt is used, prevent the conveyor belt from being electrically charged by applying some surface treatment.
4. When transporting semiconductor devices or printed circuit boards, minimize mechanical vibration and shock.

5.3 Handling for Measurement

Avoid static electricity, noise, and surge voltage when measuring semiconductor devices are measured. It is possible to prevent breakage by shorting their terminal circuits to equalize electrical potential during transportation. However, when the devices are to be measured or mounted, their terminals are left open providing the possibility that they may be accidentally touched by a worker, measuring instrument, work bench, soldering iron, conveyor belt, etc. The device will fail if it touches something that leaks current or has a static charge. Take care not to allow curve tracers, synchroscopes, pulse generators, D.C. stabilizing power supply units, etc. to leak current through their terminals or housings.

Especially, while testing the devices, take care not to apply surge voltage from the tester, to attach a clamping circuit to the tester, or not to apply any abnormal voltage through a bad contact from a current source. During measurement, avoid miswiring and short-circuiting. When inspecting a printed circuit board, make sure that there is no soldering bridge or foreign matter before turning on the power switch.

Since these precautions depend upon the types of semiconductor devices, contact Hitachi for further details.

Flat Plastic Package (QFP) Mounting Methods

Surface Mounting Package Handling Precautions

1. Package temperature distribution

The most common method used for mounting a surface mounting device is infrared reflow. Since the package is made of a black epoxy resin, the portion of the package directly exposed to the infrared heat source will absorb heat faster and thus rise in temperature more quickly than other parts of the package unless precautions are taken. As shown in the example in figure 1, the surface directly facing the infrared heat source is 20° to 30°C higher than the leads being soldered and 40° to 50°C higher than the bottom of the package. If soldering is performed under these conditions, package cracks may occur.

To avoid this type of problem, it is recommended that an aluminum infrared heat shield be placed over the resin surface of the package. By using a 2-mm thick aluminum heat shield, the top and bottom surfaces of the resin can be held to 175°C when the peak temperature of the leads is 240°C.

2. Package moisture absorption

The epoxy resin used in plastic packages will absorb moisture if stored in a high-humidity environment. If this moisture absorption becomes excessive, there will be sudden vaporization during soldering, causing the interface of the resin and lead frame to spread apart. In extreme cases, package cracks will occur. Therefore, especially for thin packages, it is important that moisture-proof storage be used.
To remove any moisture absorbed during transportation, storage, or handling, it is recommended that the package be baked at 125°C for 16 to 24 hours before soldering.

3. Heating and cooling

One method of soldering electrical parts is the solder dip method, but compared to the reflow method, the rate of heat transmission is an order of magnitude higher. When this method is used with plastic items, there is thermal shock resulting in package cracks and a deterioration of moisture-resistant characteristics. Thus, it is recommended that the solder dip method not be used.
Even with the reflow method, an excessive rate of heating or cooling is undesirable. A rate in temperature change of less than 4°C/sec is recommended.

4. Package contaminants

It is recommended that a resin-based flux be used during soldering. Acid-based fluxes have a tendency of leaving an acid residue which adversely affects product reliability. Thus, acid-based fluxes should not be used.
With resin-based fluxes as well, if a residue is left behind, the leads and other package parts will begin to corrode. Thus, the flux must be thoroughly washed away. If cleansing solvents used to wash away the flux are left on the package for an extended period of time, package markings may fade, so care must be taken.

The precautions mentioned above are general points to be observed for reflow. However, specific reflow conditions will depend on such factors as the package shape, printed circuit board type, reflow method, and device type. For reference purposes, an example of reflow conditions for a QFP infrared reflow furnace is given in figure 2. The values given in the figure refer to the temperature of the package resin, but the leads must also be limited to a maximum of 260°C for 10 seconds or less.

Of the reflow methods, infrared reflow is the most common. In addition, there is also the paper phase reflow method. The recommended conditions for a paper phase reflow furnace are given in figure 3.
For details on surface mounting small thin packages, please consult the separate manual available on mounting. If there are any additional questions, please contact Hitachi, Ltd.

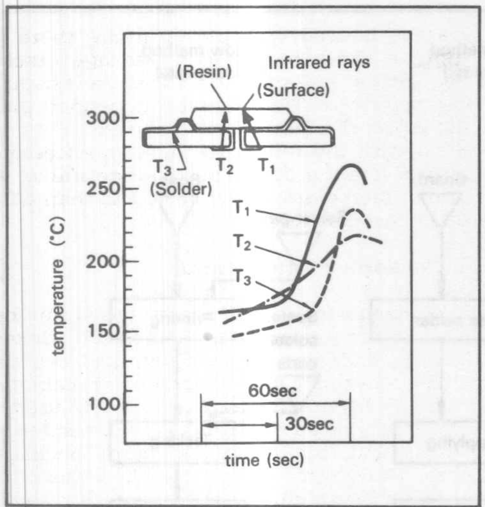


Figure 1 Temperature Profile During Infrared Heat Soldering (Example)

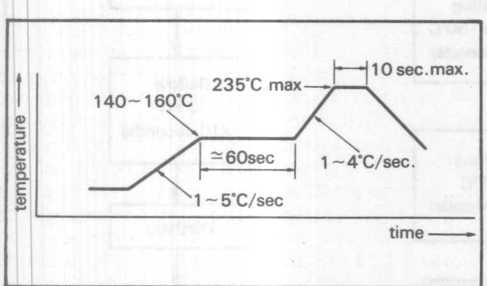


Figure 2 Recommended Reflow Conditions for QFP

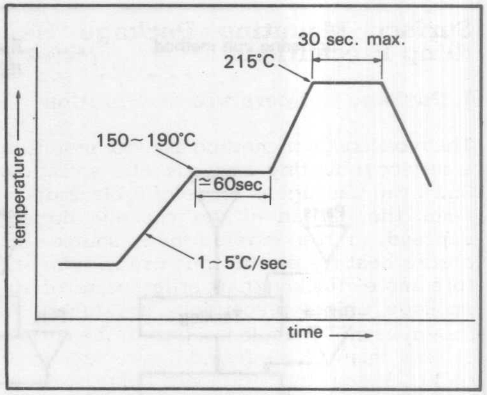


Figure 3 Example Vapor-phase Reflow Conditions

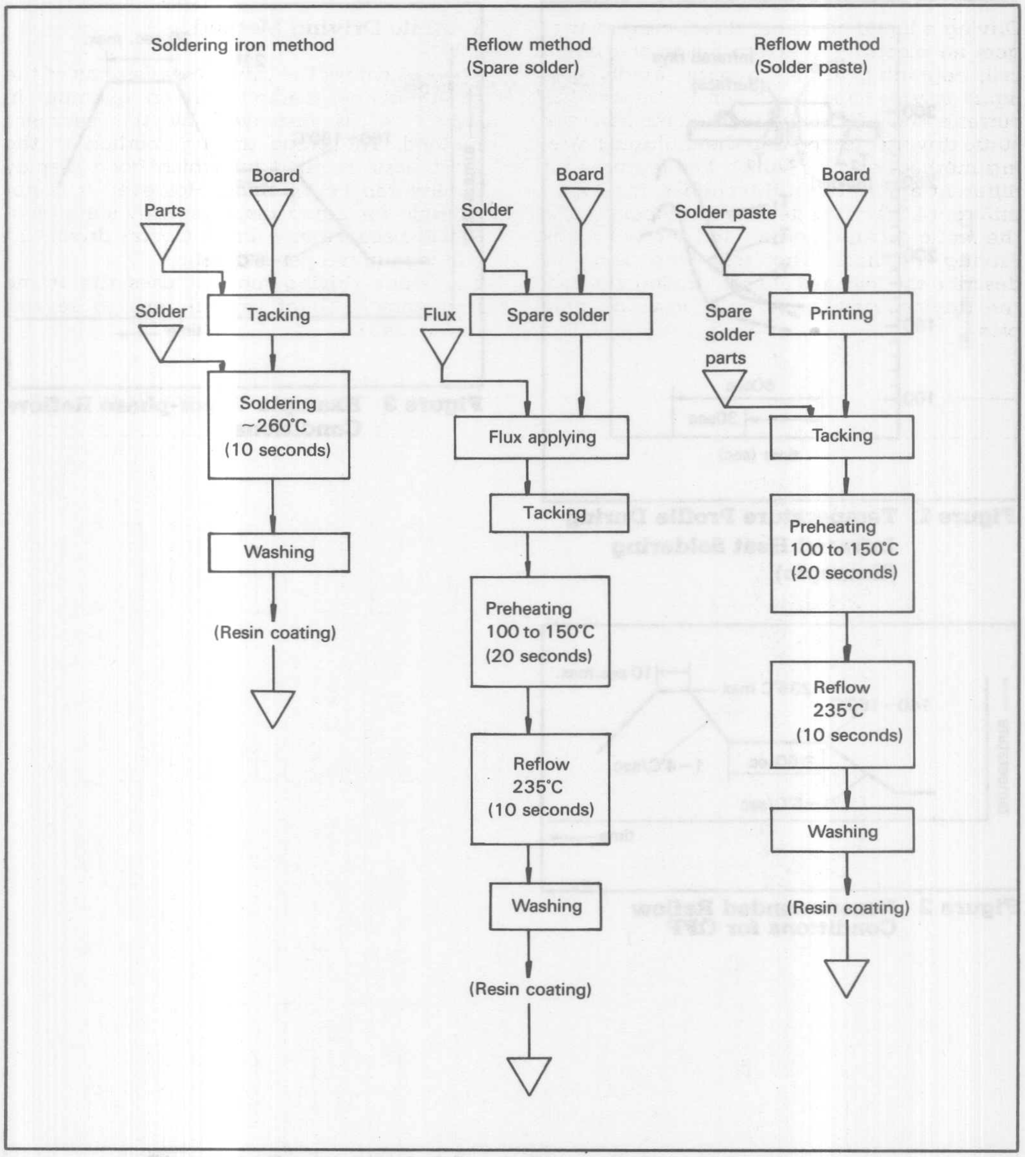


Figure 4 Recommended Paper Phase Reflow Conditions

Liquid Crystal Driving Methods

Driving a liquid crystal at direct current triggers an electrode reaction inside the liquid cell, degrading display quality rapidly. The liquid crystal must be driven by alternating current. The AC driving method includes the static driving method and the multiplex driving method, each of which has features for different applications. Hitachi has developed different LCD driver devices corresponding to the static driving method and the multiplex driving method. The following sections describe the features of each driving method, the driving waveforms, and how to apply bias.

1. Static Driving Method

Figure 1 shows the driving waveforms of the static driving method and an example in which "4" is displayed by the segment method. The static driving method is the most basic method by which good display quality can be obtained. However, it is not suitable for liquid displays with many segments because one liquid crystal driver circuit is required per segment.

The static driving method uses the frame frequency ($1/t_f$) of several tens to several hundreds Hz.

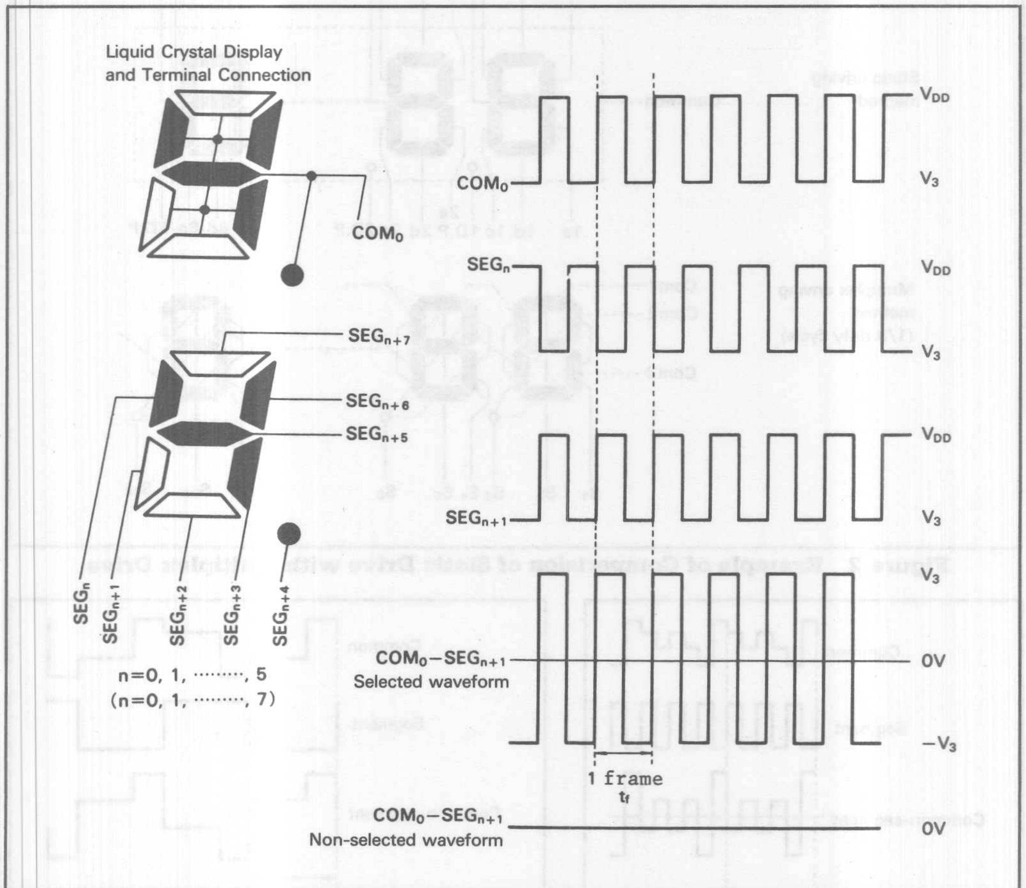


Figure 1 Example of Static Drive Waveforms (Example of HD61602/HD61603)

2. Multiplex Driving Method

The multiplex driving method is effective in reducing the number of driver circuits, the number of connections between the circuit and the display cell, and the cost when driving many display picture elements. Figure 2 shows a comparision of the static drive with the multiplex drive (1/3 duty cycle) in an 8-dight numeric display. The number of liquid crystal driver circuits required is 65 for the former and 27 for the latter. The multiplex drive reduces the number of driver circuits. However, greater multiplexing reduces the driving voltage tolerance. Thus, there are limits to the extent of multiplexing.

There are two types of multiplex drive waveforms: A type and B type. A type, shown in figure 3, is used for alternation in 1 frame. B type is used for alternation in between 2 frames (figure 4). B type has better display quality than A type in high multiplex drive.

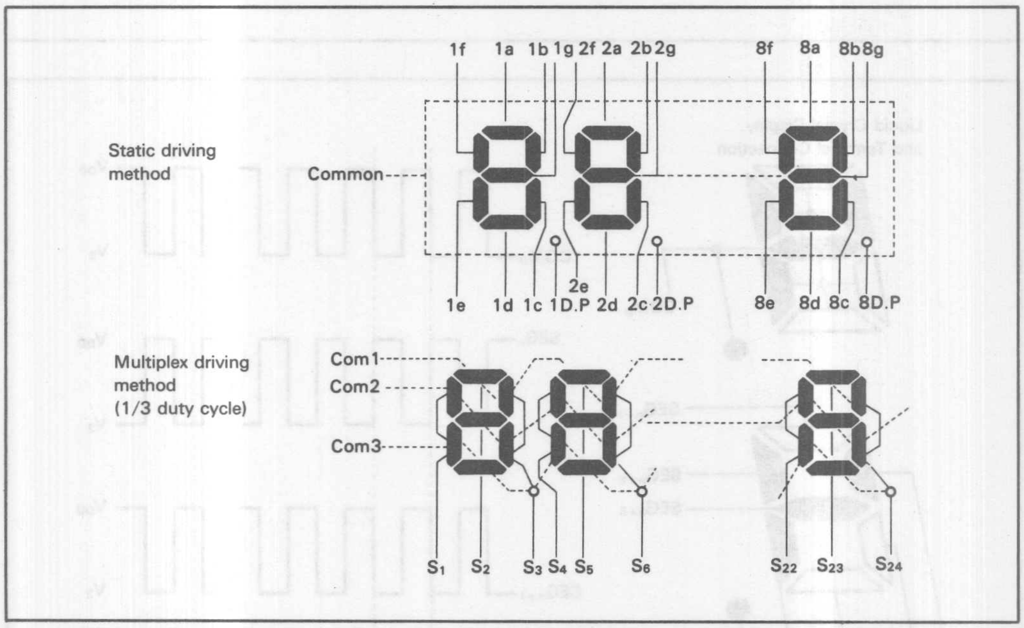


Figure 2 Example of Comparision of Static Drive with Multiplex Drive

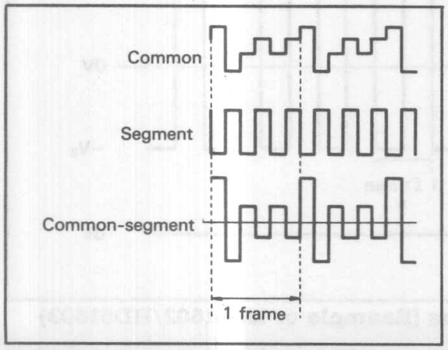


Figure 3 A Type Waveforms (1/3 duty cycle, 1/3 bias)

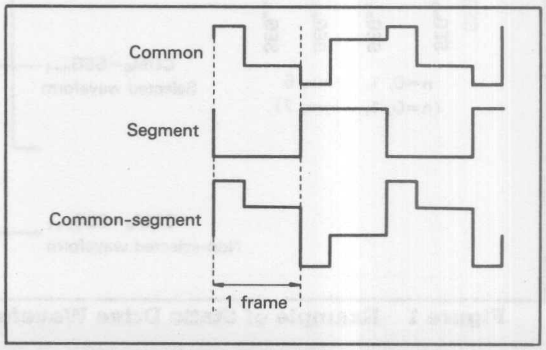


Figure 4 B Type Waveforms (1/3 duty cycle, 1/3 bias)

2.1. 1/2 Bias, 1/2 Duty Drive

In the 1/2 duty drive method, 1 driver circuit drives 2 segments. Figure 5 shows an example of the connection to display '4' on a liquid crystal display of 7-segment type, and the output waveforms.

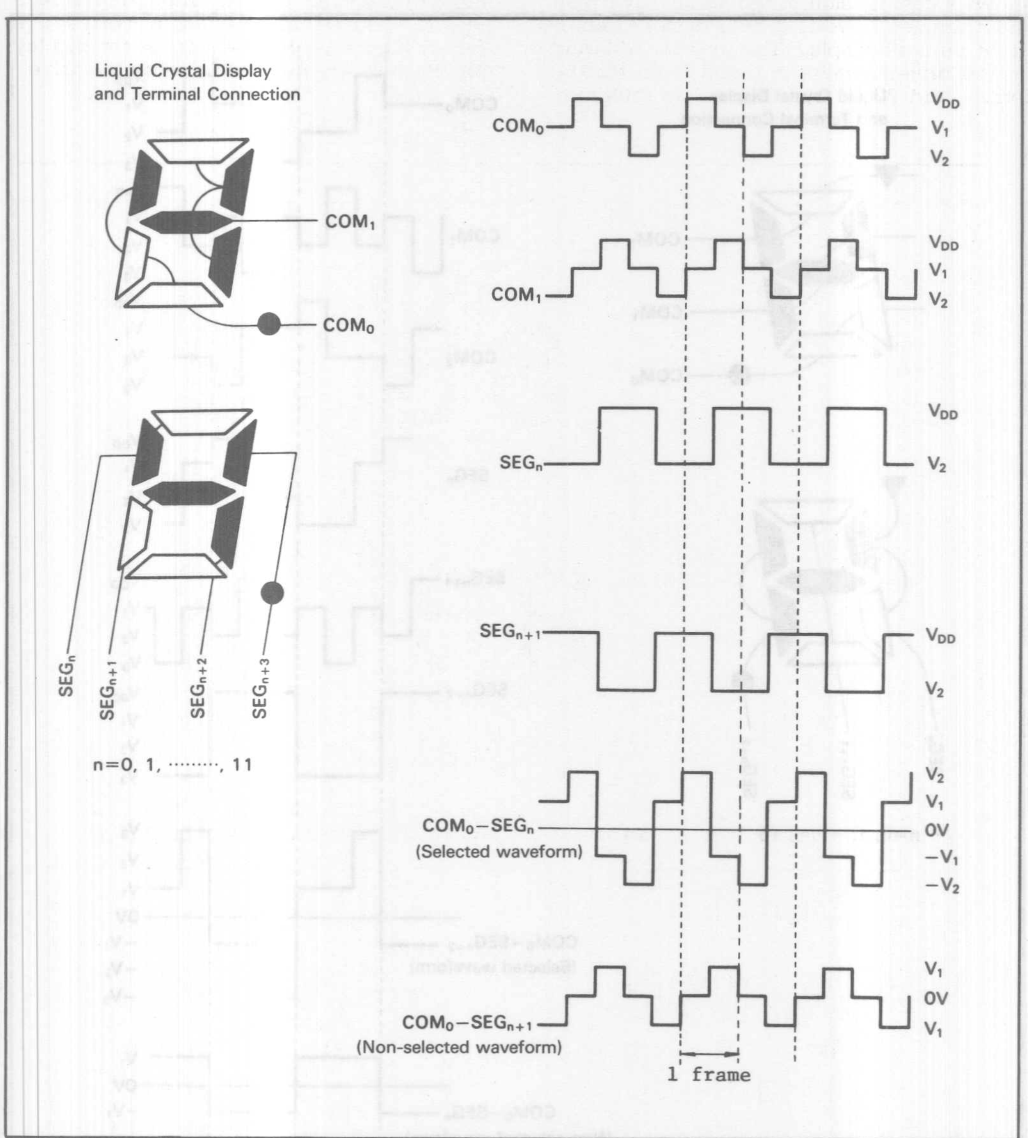


Figure 5 Example of Waveforms in 1/2 Duty Cycle Drive (B type) (Example of HD61602)

2.2 1/3 Bias, 1/3 Duty Cycle Drive

In the 1/3 duty cycle drive, 3 segments are driven by 1 segment output driver. Figure 6 shows an example of the connection to display '4' on a liquid crystal display of 7-segment type, and the output waveforms.

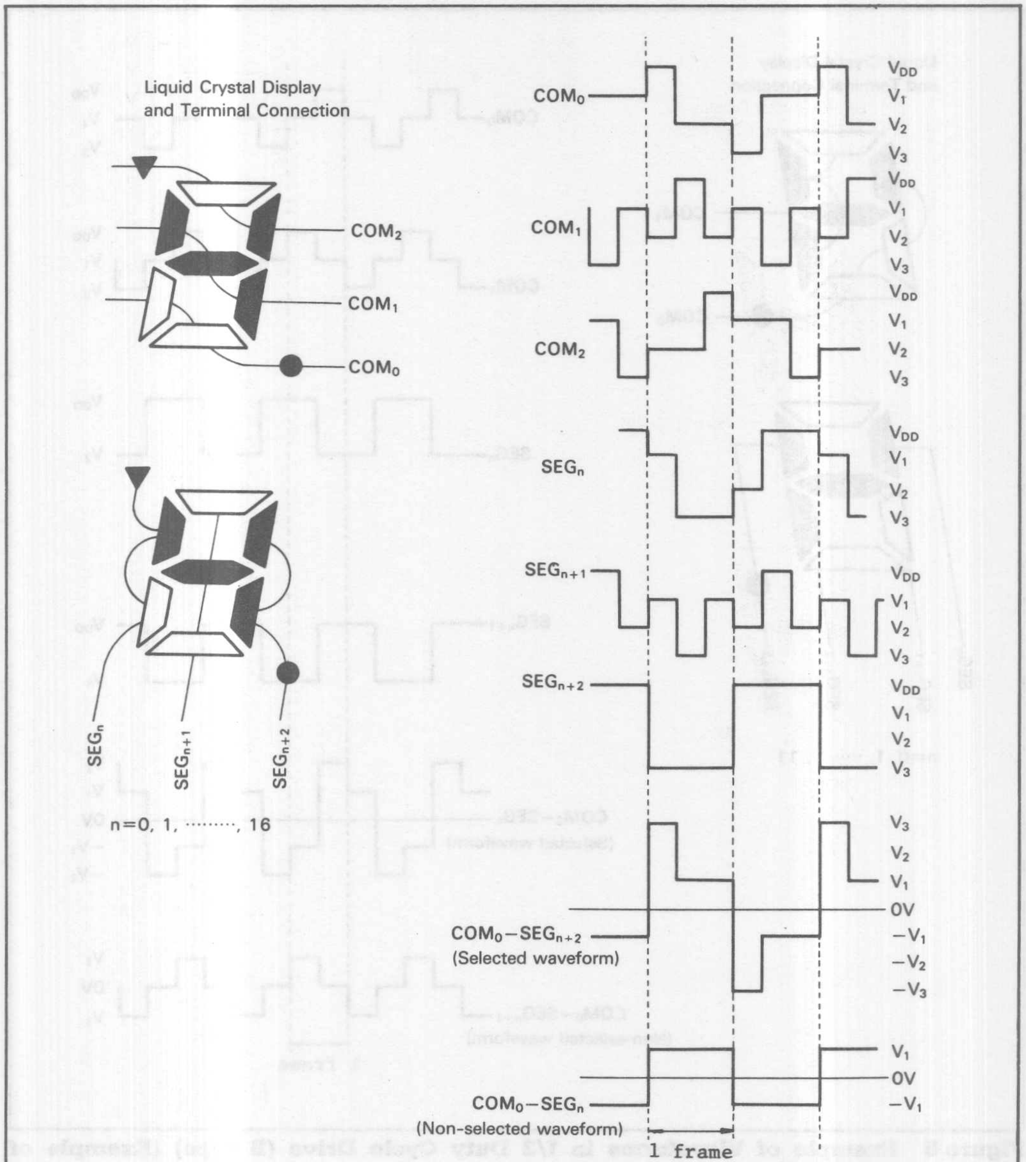


Figure 6 Example of Waveforms in 1/3 Duty Cycle Drive (B type) (Example of HD61602)

2.3 1/3 Bias, 1/4 Duty Cycle Drive

In the 1/4 duty cucle drive, 4 segments are driven by 1 segment output driver. Figure 7 shows an example of the connection to display '4' on a liquid crystal display of 7-segment type, and the output waveforms.

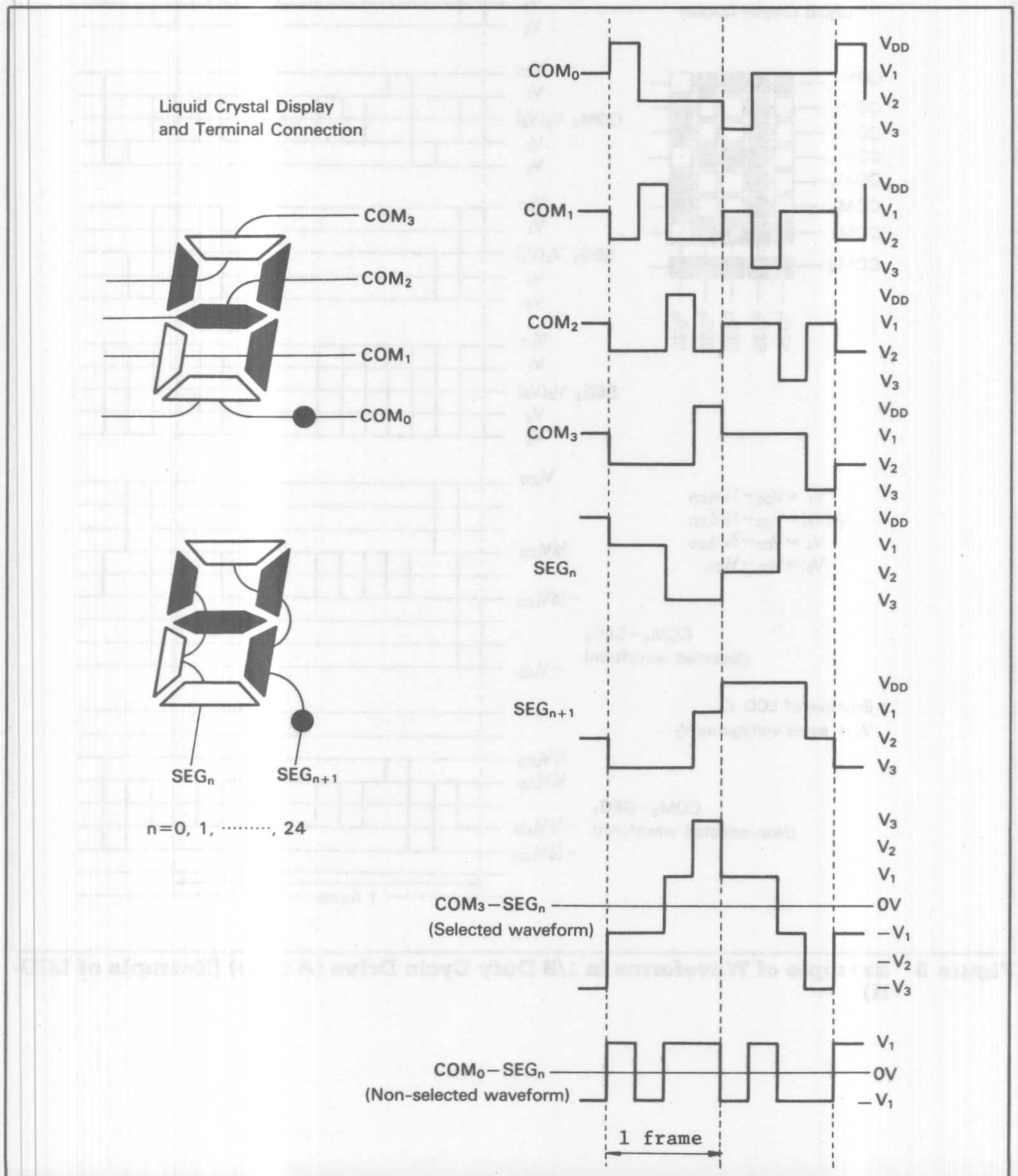


Figure 7 Example of Waveforms in 1/4 Duty Cycle Drive (B type) (Example of HD61602)

2.4 1/4 Bias, 1/8 Duty Cycle Drive

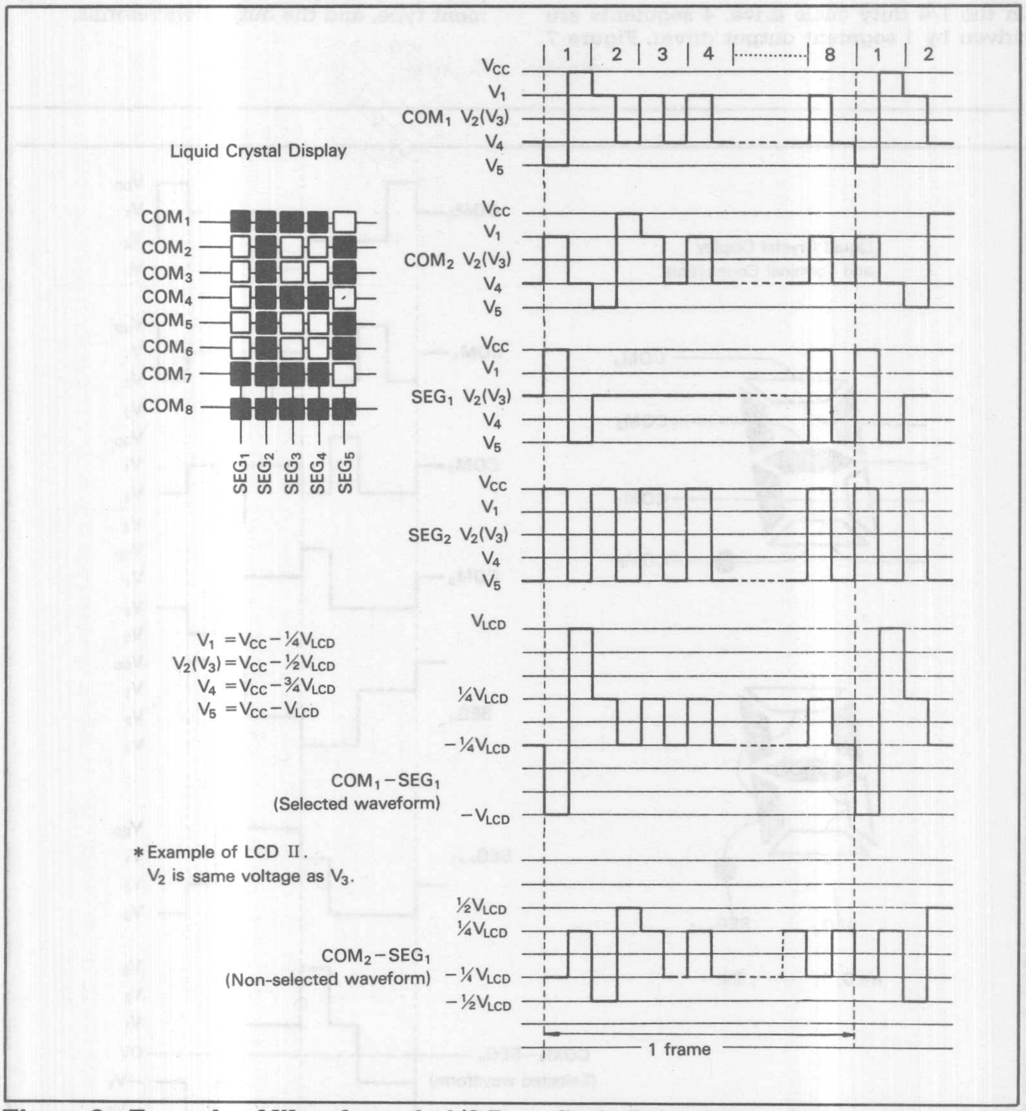


Figure 8 Example of Waveforms in 1/8 Duty Cycle Drive (A type) (Example of LCD-II)

2.5 1/5 Bias, 1/8 Duty Cycle Drive

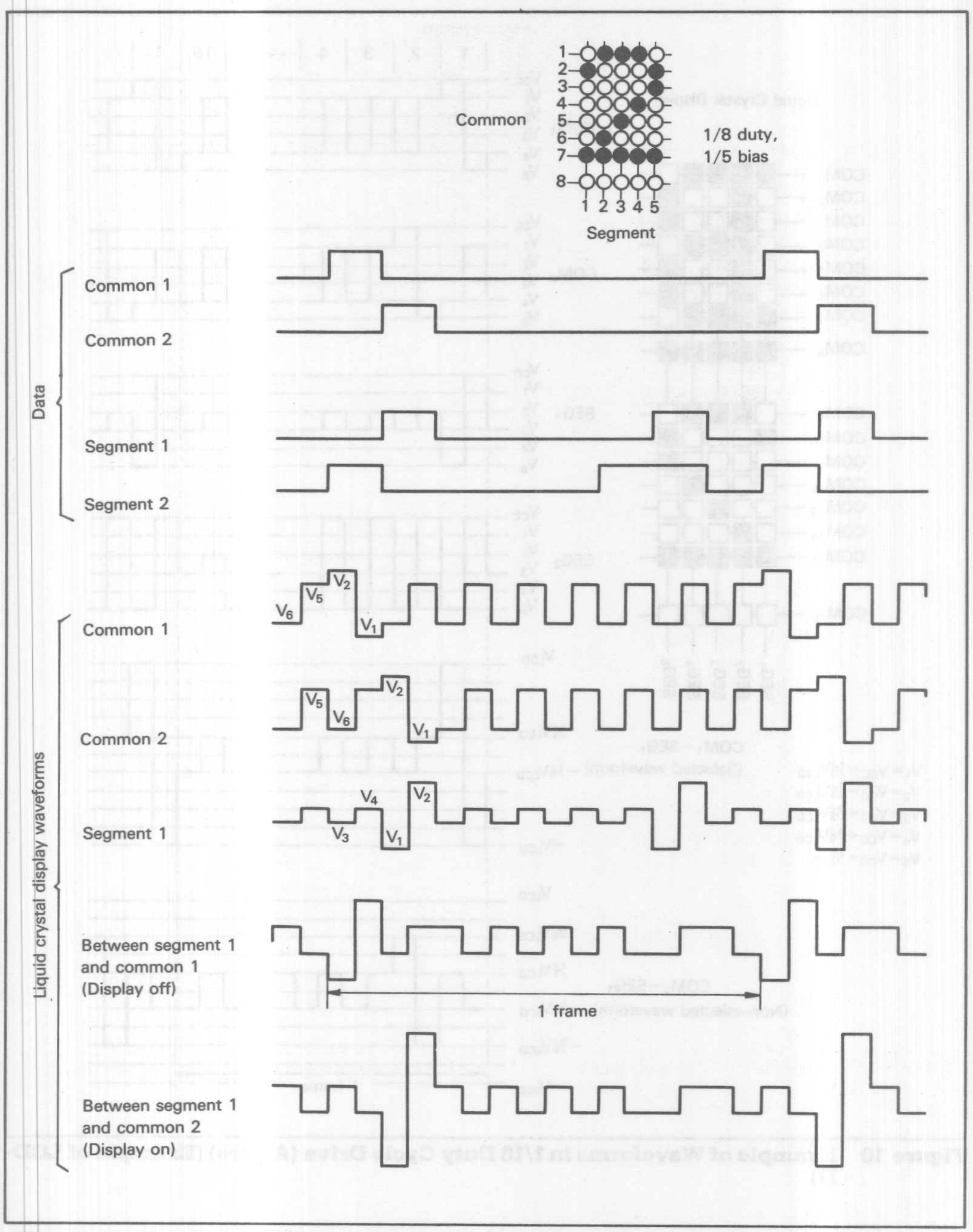


Figure 9 Example of Waveforms in 1/8 Duty Cycle Drive (A type) (Example of HD44100R)

2.6 1/5 Bias, 1/16 Duty Cycle Drive

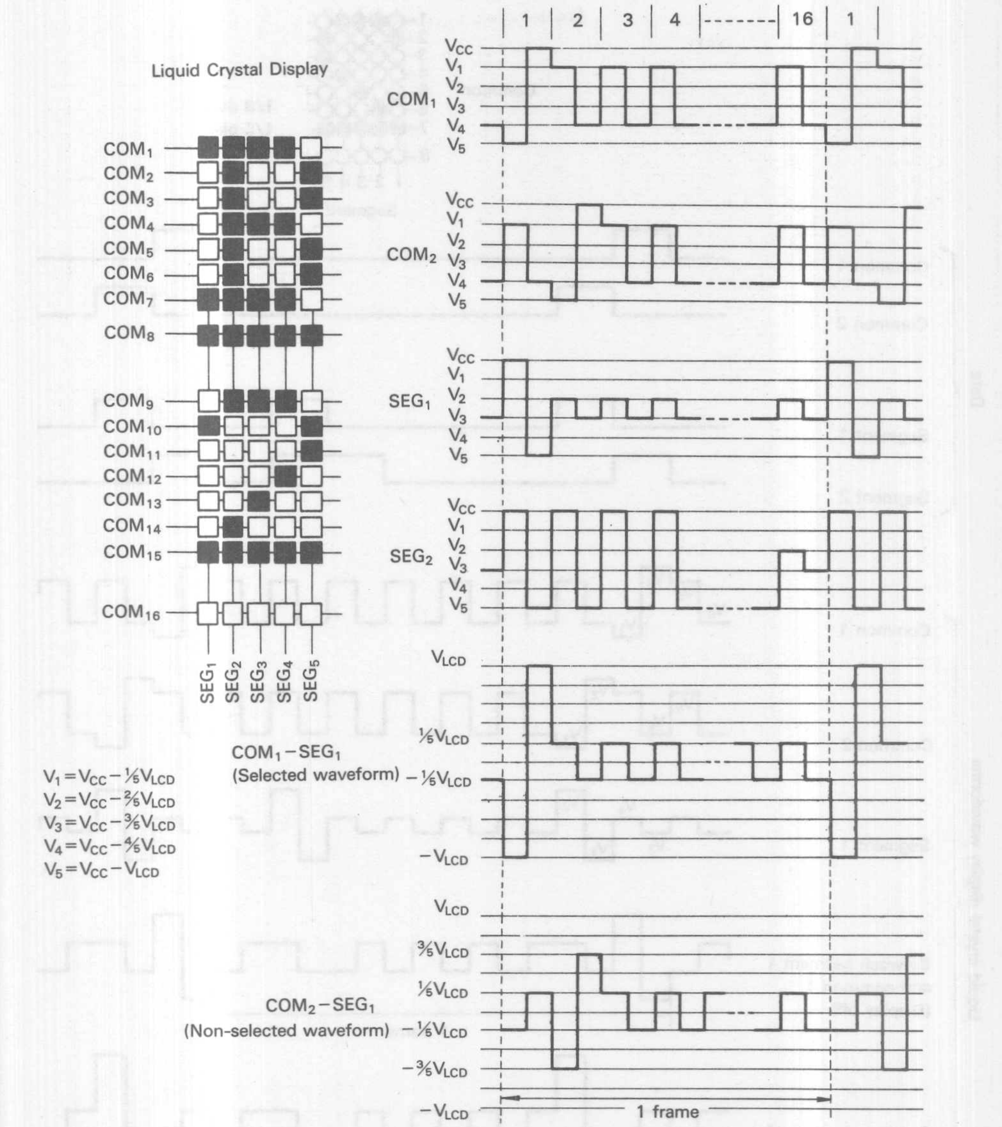


Figure 10 Example of Waveforms in 1/16 Duty Cycle Drive (A type) (Example of LCD-II)

2.7 1/5 Bias, 1/32 Duty Cycle Drive

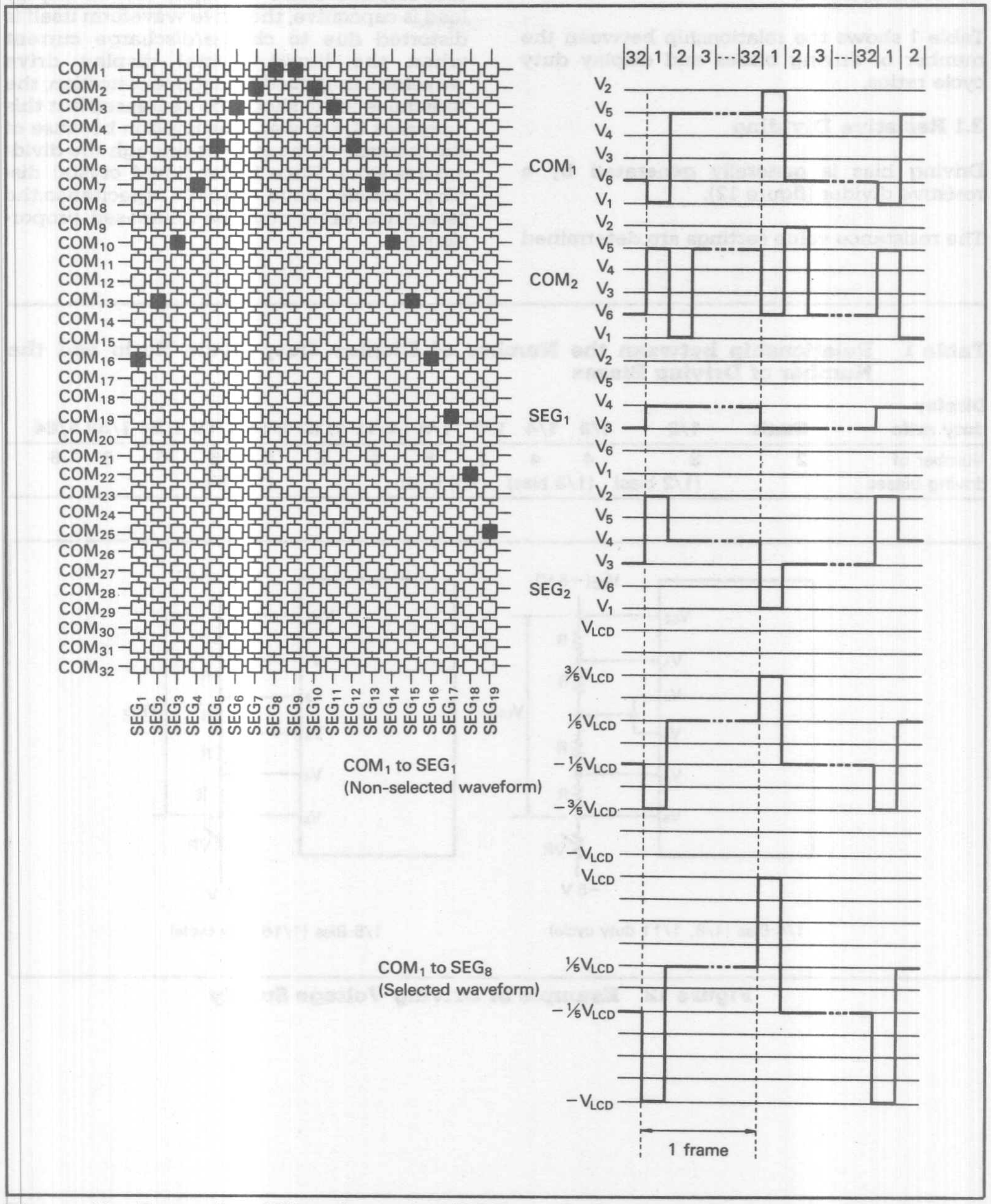


Figure 11 Example of Waveforms in 1/32 Duty Cycle Drive (Example of HD44102CH, HD44103CH)

3. Power Supply Circuit for Liquid Crystal Drive

Table 1 shows the relationship between the number of driving biases and display duty cycle ratios.

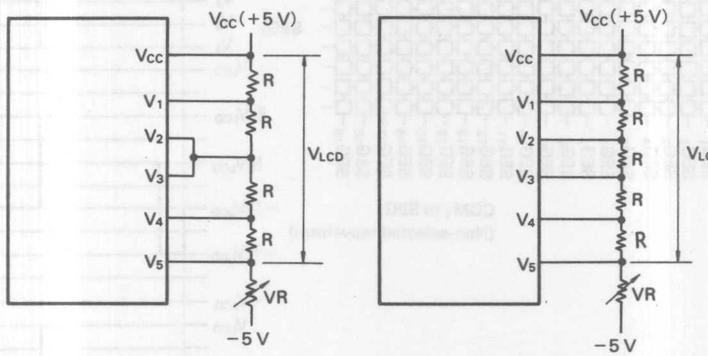
3.1 Resistive Dividing

Driving bias is generally generated by a resistive divider (figure 12).

The resistance value settings are determined by considering operating margin and power consumption. Since the liquid crystal display load is capacitive, the drive waveform itself is distorted due to charge/discharge current when the liquid crystal display drive waveform is applied. To reduce distortion, the resistance value should be decreased but this increases the power consumption because of the increase of the current through the dividing resistors. Since larger liquid crystal display panels have larger capacitance, the resistance value must be decreased proportionally.

Table 1 Relationship between the Number of Display Duty Cycle Ratio and the Number of Driving Biases

Display duty ratio	Static	1/2	1/3	1/4	1/7	1/8	1/11	1/12	1/14	1/16	1/24	1/32	1/64
Number of driving biases	2	3 (1/2 bias)	4 (1/3 bias)	4	5 (1/4 bias)	5	5	5	6 (1/5 bias)	6	6	6	6



1/4 Bias (1/8, 1/11 duty cycle)

1/5 Bias (1/16 duty cycle)

Figure 12 Example of Driving Voltage Supply

It is efficient to connect a capacitor to the resistors in parallel as shown in figure 13 in order to improve charge/discharge distortion. However, the effect is limited. Even if it is attempted to reduce the power consumption with a large resistor and improve waveform distortion with a large capacitor, a level shift occurs and the operating margin is not improved.

Since the liquid crystal display load is in a matrix configuration, the path of the charge/discharge current through the load is complicated. Moreover, it varies depending on display condition. Thus, a value of resistance cannot be simply determined from the load capacitance of liquid crystal display. It must be experimentally determined according to the demand for the power consumption of the equipment in which the liquid crystal display is incorporated.

Generally, R is 1 kΩ to 10 kΩ, and VR is 5kΩ to 50 kΩ. No capacitor is required. A capacitor of 0.1 uF is usually used if necessary.

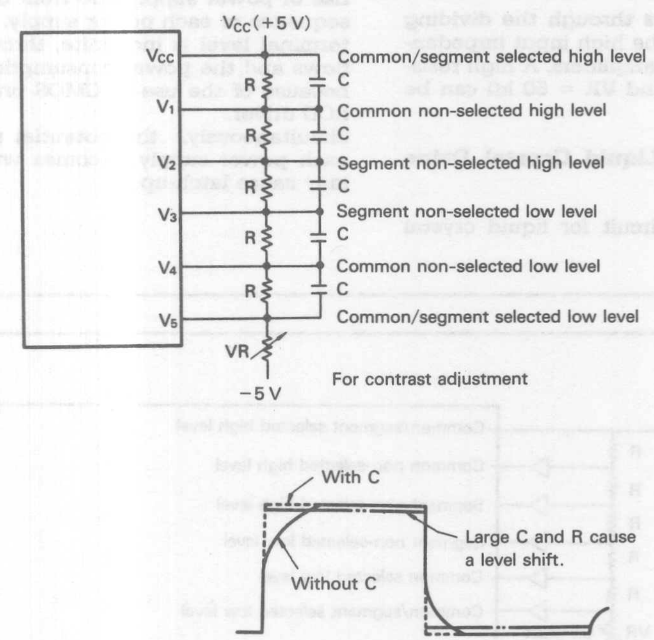


Figure 13 Example of Capacitor Connection for Improvement of Liquid Crystal Display Drive Waveform Distortion (1/5 bias) (Example of LCD-II)

3.2 Drive by Operational Amplifier

In graphic displays, the size of the liquid crystal becomes larger and the display duty ratio becomes smaller, so the stability of liquid crystal drive level is more important than in small display system.
Since the liquid crystal for graphic displays is large and has many picture elements, the load capacitance becomes large. The high impedance of the power supply for liquid crystal drive produces distortion in the drive waveforms, and degcades disiplay quality. For this reason, the liquid crystal drive level impedance should be reduced with operational amplifiers. Figure 14 shows an example of an operational amplifier configuration.

No load current flows through the dividing resistors because of the high input impedance of the operational amplifiers. A high resistance of R = 10 kΩ and VR = 50 kΩ can be used.

3.3 Generation of Liquid Crystal Drive Levels in LSI

The power supply circuit for liquid crystal drive level may be incorporated in the LSI, such as one for a portable calculator with liquid crystal display.
HD61602, HD61603 for small display systems has a built-in power suply circuit for liquid crystal drive levels.

3.4 Precaution on Power Supply Circuits

The LCD driver LSI has two types of power supplies: the one for logical circuits and the other for the liquid crystal display drive circuit. The power supply system is complicated because of several liquid crystal drive levels. For this reason, in the power supply design, take care not to deviate from the voltage range assured in the maximum rating at the rise of power supply and from the potential sequence of each power supply. If the input terminal level is indefinite, through current flows and the power consumption increases because of the use of CMOS process in the LCD driver.
Simultaneously, the potential sequence of each power supply becomes wrong, which may cause latch-up.

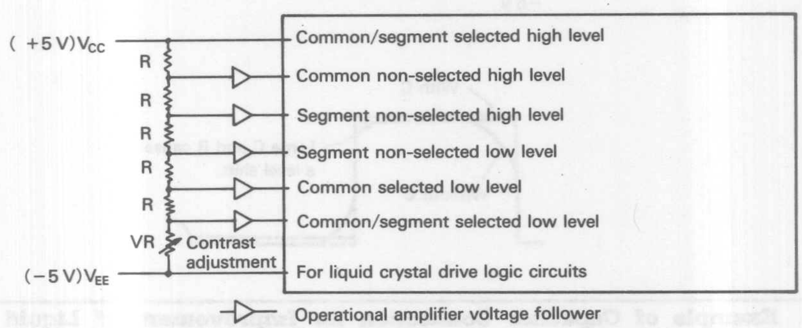


Figure 14 Drive by Operational Amplifier (1/5 bias)

Data Sheets

HITACHI

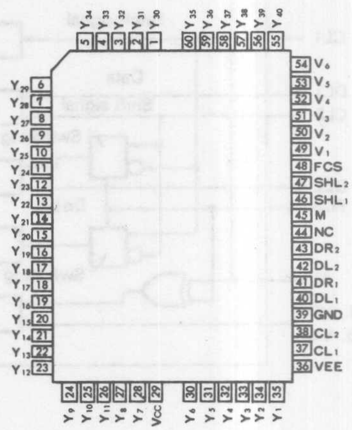
HD44100R
(LCD Driver with 40-Channel Outputs)

— Preliminary —

Description

The HD44100R has two sets of 20-bit bidirectional shift registers, 20 data latch flipflops and 20 liquid crystal display driver circuits. It receives serial display data from a display control LSI, converts it into parallel data and supplies liquid crystal display waveforms to the liquid crystal.
The HD44100R is a highly general liquid crystal display driver which can drive a static drive liquid crystal and a dynamic drive liquid crystal, and can be applied as a common driver or segment driver.

Pin Arrangement



(Top View)

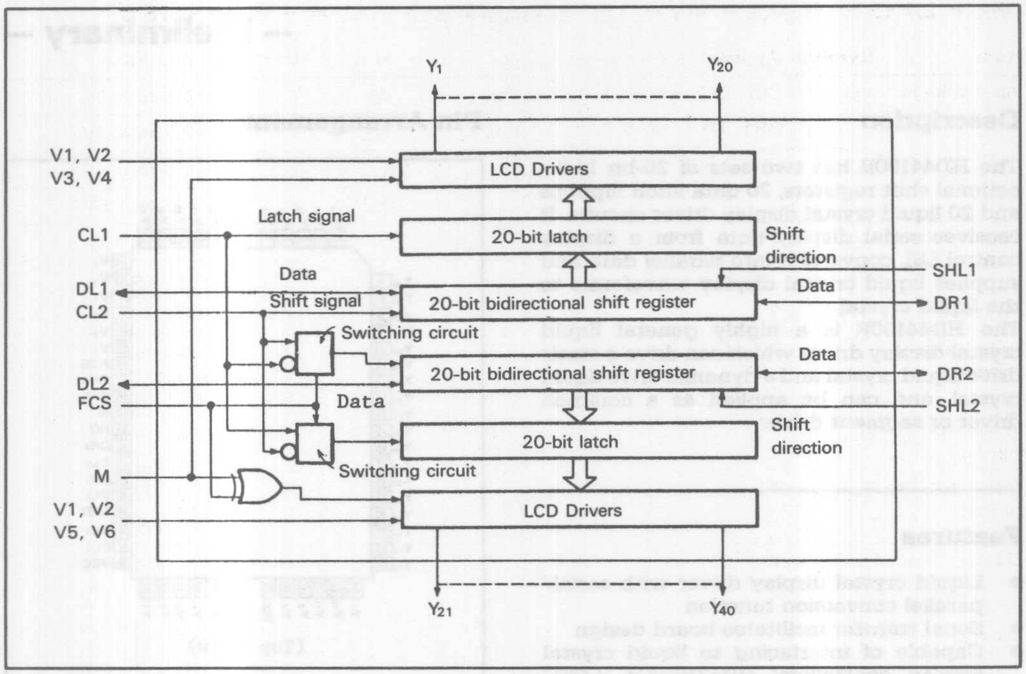
Features

- Liquid crystal display driver with serial/parallel conversion function
- Serial transfer facilitates board design
- Capable of interfacing to liquid crystal display controllers: HD43160AH, LCTC (HD61830/61830B), LCD-II (HD44780S, HD44780U), LCD-IIA (HD66780), LCD-II/E (HD66702), LCD-III (HD44790), HD66710
- 40 internal liquid crystal display drivers
- Internal serial/parallel conversion circuits:
  —20-bit shift register × 2
  —20-bit data latch × 2
- Display bias: Static to 1/5
- Power supply:
  —Internal logic: V_{CC}=2.7 to 5.5V
  —Liquid crystal display driver circuit:
  $V_{CC}-V_{EE}$=3 to 13V
- Separation of internal logic from liquid crystal display driver circuit increases applicable controllers and liquid crystal types
- CMOS process

Ordering Information

Type No.	V_{CC} (V)	$V_{CC}-V_{EE}$ (V)	Package
HD44100RFS	2.7 to 5.5	3 to 13	60-pin Plastic QFP (FP-60A)
HCD44100R	2.7 to 5.5	3 to 13	Chip

Block Diagram



Absolute Maximum Ratings

Item		Symbol	Value	Unit
Supply	Logic	V_{CC} *1	− 0.3 to + 7.0	V
voltage	LCD drivers	V_{EE} *2	V_{CC} − 15.0 to V_{CC} + 0.3	V
Input voltage		V_{T1} *1	− 0.3 to V_{CC} + 0.3	V
Input voltage		V_{T2} *3	V_{CC} + 0.3 to V_{EE} − 0.3	V
Operating temperature		T_{opr}	− 20 to + 75	°C
Storage temperature		T_{stg}	− 55 to + 125	°C

Notes: *1 All voltage values are referred to GND.
*2 Connect a protection resistor of 220 Ω ± 5 % to V_{EE} power supply in series.
*3 Applies to V_1 to V_6.

Electrical Characteristics

(V_{CC} = 2.7 to 5.5 V, $V_{CC} - V_{EE}$ = 3 to 13 V, GND = 0 V, T_a = − 20 to + 75°C)

Item	Symbol	Applicable Terminals	Min	Typ	Max	Unit	Test Condition
Input voltage	V_{IH}	CL1, CL2, DL1, DL2,	0.7 V_{CC}	—	V_{CC}	V	V_{CC}=4.5 to 5.5V
		DR1, DR2, M, SHL1,	0.8 V_{CC}	—	V_{CC}	V	V_{CC}=2.7 to 4.5V
	V_{IL}	SHL2, FCS	0	—	0.3 V_{CC}	V	V_{CC}=4.5 to 5.5V
			0	—	0.2 V_{CC}	V	V_{CC}=2.7 to 4.5V
Output voltage	V_{OH}	DL1, DL2, DR1, DR2	V_{CC} − 0.4	—	—	V	I_{OH} = − 0.4 mA
	V_{OL}		—	—	0.4	V	I_{OL} = + 0.4 mA
On resistance	R_{ON}	*1	—	—	20	kΩ	±I_d = 0.05 mA, $V_{CC}-V_{EE}$=4V
Input leakage current	I_{IL}	CL1, CL2, DL1, DL2, DR1, DR2, M, SHL1, SHL2, FCS, NC	− 5.0	—	5.0	μA	V_{in} = 0 to V_{CC}
Vi leakage current	I_{VL}	*2	− 10.0	—	10.0	μA	V_{in} = V_{CC} to V_{EE}
Power supply current	I_{CC}	*3	—	—	1.0	mA	f_{CL2} = 400 kHz
	I_{EE}		—	—	10	μA	f_{CL1} = 1 kHz

Notes: *1 Applies to the resistance between V_i and Y_j when a current ± I_d = 0.05 mA flows through all of the Y pins.

*2 Output Y1 to Y40 open.

*3 Input/output current is excluded; when input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

Timing Characteristics

(V_{CC} = 2.7 to 5.5 V, $V_{CC} - V_{EE}$ = 3 to 13 V, GND = 0 V, T_a = − 20 to + 75°C)

Item		Symbol	Applicable Terminals	Min	Typ	Max	Unit	Test Condition
Data shift frequency		f_{CL}	CL2	—		400	kHz	
Clock width	high level	t_{CWH}	CL1, CL2	800	—	—	ns	
	Low level	t_{CWL}	CL2	800	—	—	ns	
Data set-up time		t_{SU}	DL1, DL2, DR1, DR2, FLM	300	—	—	ns	
Clock set-up time		t_{SL}	CL1, CL2	500	—	—	ns	(CL2→CL1)
Clock set-up time		t_{LS}	CL1, CL2	500	—	—	ns	(CL1→CL2)
Data delay time		t_{pd}	DL1, DL2, DR1, DR2	—	—	500	ns	C_L = 15 pF
Clock rise/fall time		t_{ct}	CL1, CL2	—		200	ns	
Data hold time		t_{DH}	DL1, DL2, DR1, DR2, FLM	300	—	—	ns	

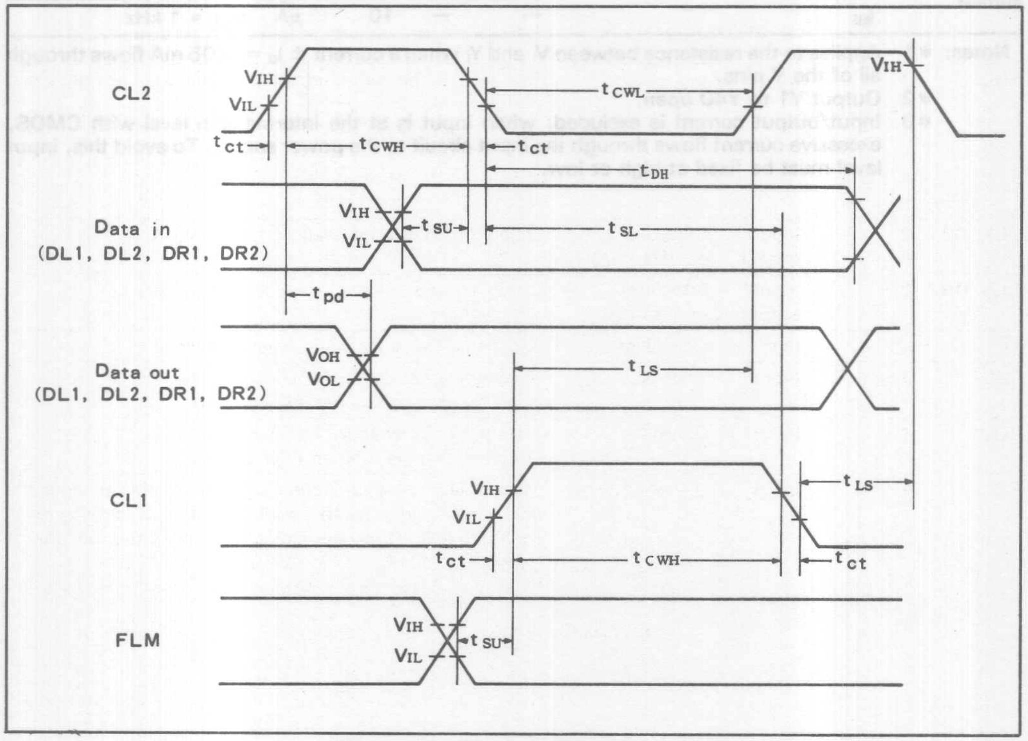


Figure 1 Timing Waveform

Terminal Function

Table 1 Functional Description of Terminals

Signal Name	Number of Lines	Input/ Output	Connected to	Function
V_{CC}	1		power supply	Power supply for logical circuit
GND	1		Power supply	0 V
V_{EE}	1		Power supply	Power supply for liquid crystal display drive
Y_1—Y_{20}	20	Output	Liquid crystal	Liquid crystal driver output (Channel 1)
Y_{21}—Y_{40}	20	Output	Liquid crystal	Liquid crystal driver output (Channel 2)
V_1, V_2	2	Input	Power supply	Power supply for liquid crystal display drive (Select level)
V_3, V_4	2	Input	Power supply	Power supply for liquid crystal display drive (Non-select level for channel 1)
V_5, V_6	2	Input	Power supply	Power supply for liquid crystal display drive (Non-select level for channel 2)
SHL1	1	Input	V_{CC} or GND	Selection of the shift direction of channel 1 shift register

SHL1	DL1	DR1
V_{CC}	Out	In
GND	In	Out

Signal Name	Number of Lines	Input/ Output	Connected to	Function
SHL2	1	Input	V_{CC} or GND	Selection of the shift direction of channel 2 shift register

SHL2	DL2	DR2
V_{CC}	Out	In
GND	In	Out

Signal Name	Number of Lines	Input/ Output	Connected to	Function
DL1, DR1	2	Input/ output	Controller or HD44100R	Data input/output of channel 1 shift register
DL2, DR2	2	Input/ output	Controller or HD44100R	Data input/output of channel 2 shift register
M	1	Input	Controller	Alternated signal for liquid crystal driver output
CL1	1	Input	Controller	Latch signal for channel 1 (↓) *1 Used for channel 2 when FCS is GND
CL2	1	Input	Controller	Shift signal for channel 1 (↓) *1 Used for channel 2 when FCS is GND
FCS	1	Input	V_{CC} or GND	Mode select signal of channel 2. FCS signal exchanges the latch signal and the shift signal of channel 2 and inverts M for channel 2. Thus, this signal exchanges the function of channel 2.

FCS Level	Channel 2 Latch signal	Channel 2 Shift signal	M Polarity	Function
V_{CC}	CL2 ↑	CL1 ↑	$\overline{M}$	For common drive
GND	CL1 ↓	CL2 ↓	M	For segment drive
	*1	*1	*2	

Signal Name	Number of Lines	Input/ Output	Connected to	Function
NC	1			Don't connect any wires to this terminal.

Notes: *1 ↑ and ↓ indicate the latches at rise and fall times, respectively.
*2 The output level relationship between channel 1 and channel 2 based on the FCS signal level is as follows:

FCS	Data	M	Output Level: Channel 1 (Y_1—Y_{20})	Output Level: Channel 2 (Y_{21}—Y_{40})
V_{CC} (1)	1 (Select)	1	V_1	V_2
		0	V_2	V_1
	0 (Non-select)	1	V_3	V_6
		0	V_4	V_5
GND (0)	1 (Select)	1	V_1	V_1
		0	V_2	V_2
	0 (Non-select)	1	V_3	V_5
		0	V_4	V_6

1 and 0 indicate high and low levels, respectively.

Applications

Segment Driver

When the HD44100R is used as a segment driver, FCS is set to GND to transfer display data with the timing shown in figure 2. In this case, both channel 1 and channel 2 shift data at the fall of CL2 and latch it at the fall of CLI. V_3 and V_5, V_4 and V_6 of the liquid crystal display driver power supply are short-circuited, respectively.

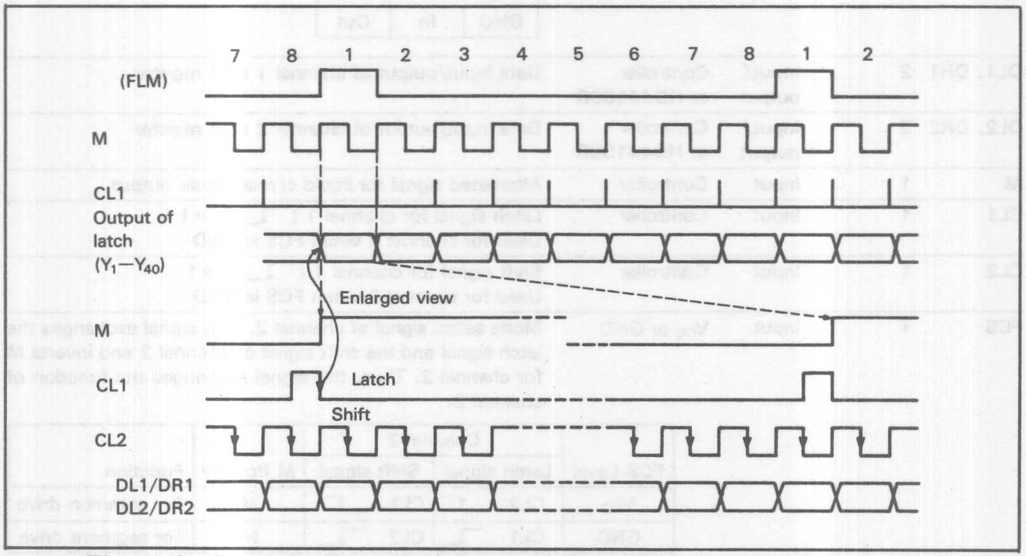


Figure 2 Segment Data Waveforms (A Type Waveforms, 1/8 Duty Cycle)

Common Driver

In this case, channel 1 is used as a segment driver and channel 2 as common driver. When channel 2 of HD44100R is used as common driver, FCS is set to V_{CC} to transfer display data with the timing shown in figure 3.

In this case, channel 2 shifts data at the rise of CL1 and latches it at the rise of CL2. Channel 1 shifts and latches as shown in figure 2.

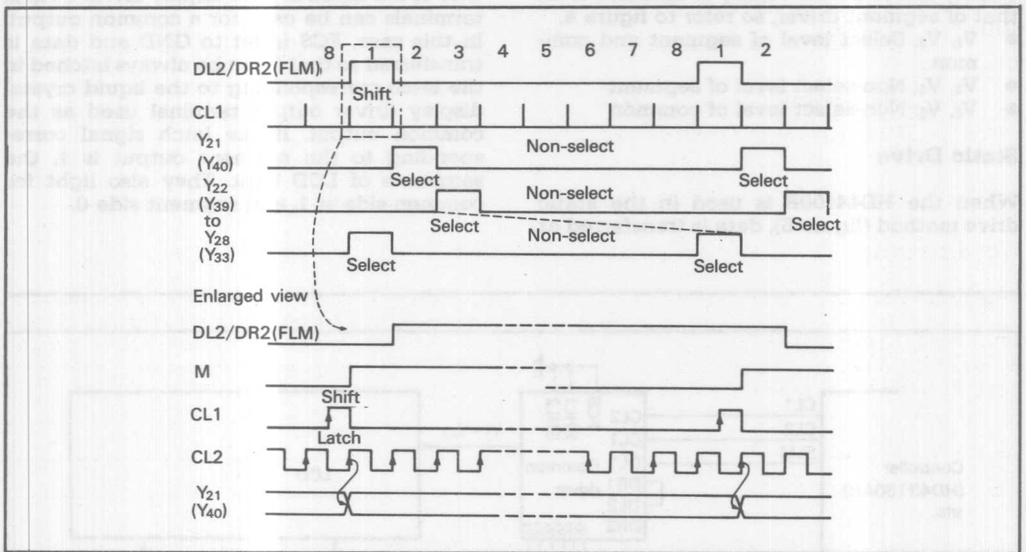


Figure 3 Common Data Waveforms (A Type Waveforms of Channel 2, 1/8 Duty Cycle)

Both Channel 1 and Channel 2 Used as Common Drivers (FCS = GND)

When both of channel 1 and channel 2 of HD44100R are used common drivers, FCS is set to GND and the signals (CL1, CL2, FLM) from the controller are connected as shown in figure 4.
In this case, connection of the liquid crystal display driver power supply is different from that of segment driver, so refer to figure 4.

- V_1, V_2: Select level of segment and common
- V_3, V_4: Non-select level of segment
- V_5, V_6: Non-select level of common

Static Drive

When the HD44100R is used in the static drive method (figure 5), data is transferred at the fall of CL2 and latched at the fall of CL1. The frequency of CL1 becomes the frame frequency of the liquid crystal display driver. The signal applied terminal M must have twice the frequency of CL1 and be synchronized at the fall of CL1. The power supply for liquid crystal display driver is used by short-circuiting V_1, V_4 and V_6, and V_2, V_3, and V_5 respectively.
One of the liquid crystal display driver output terminals can be used for a common output. In this case, FCS is set to GND and data is transferred so that 0 can be always latched in the latch corresponding to the liquid crystal display driver output terminal used as the common output. If the latch signal corresponding to the segment output is 1, the segments of LCD light. They also light for common side = 1, and segment side 0.

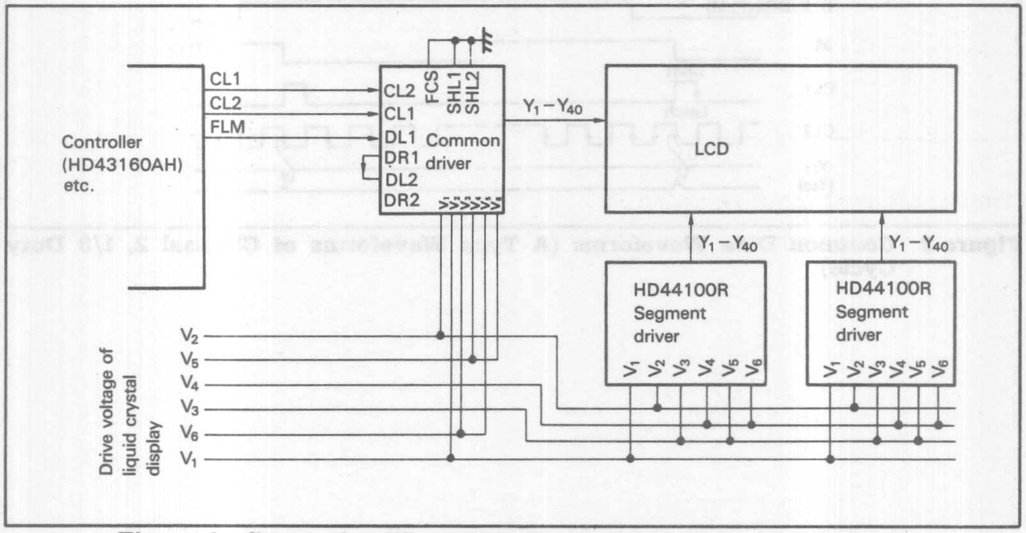


Figure 4 Connection When Both Channels Are Common Drivers

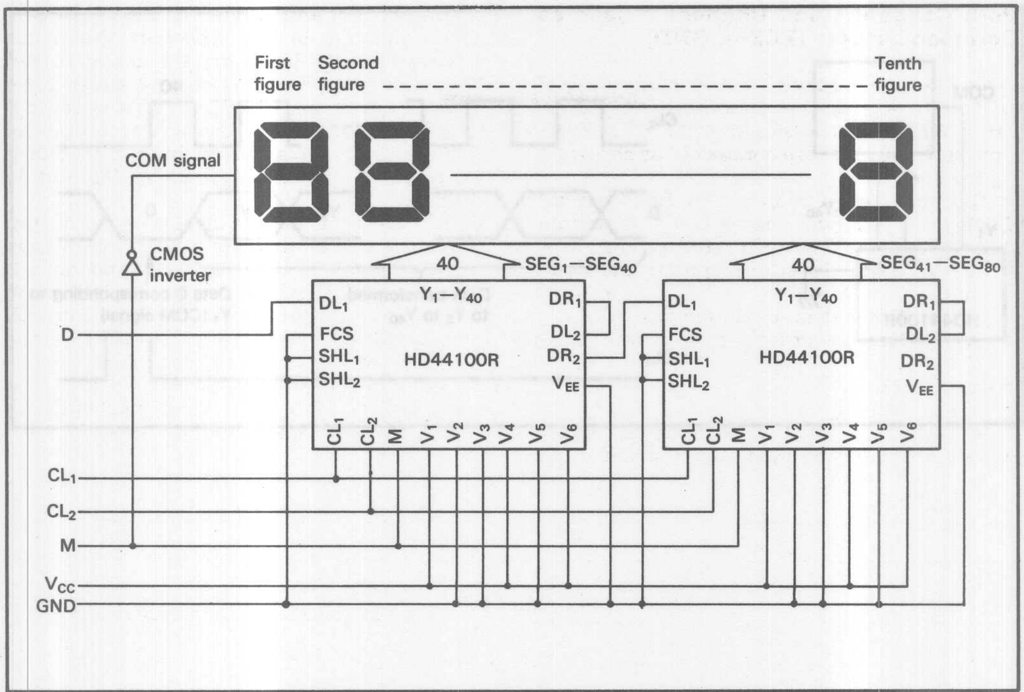
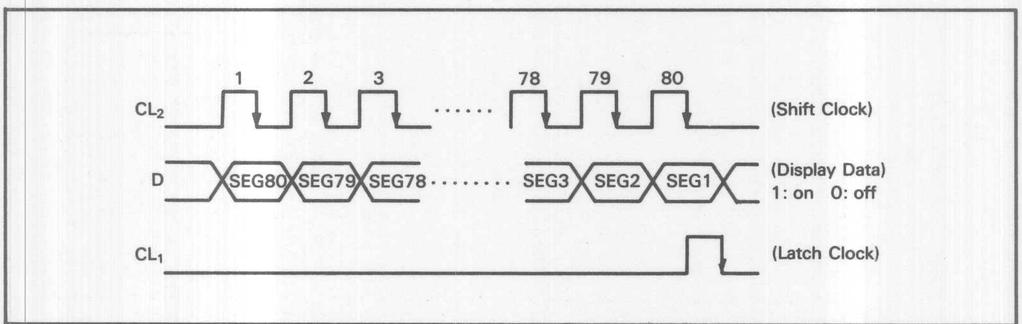


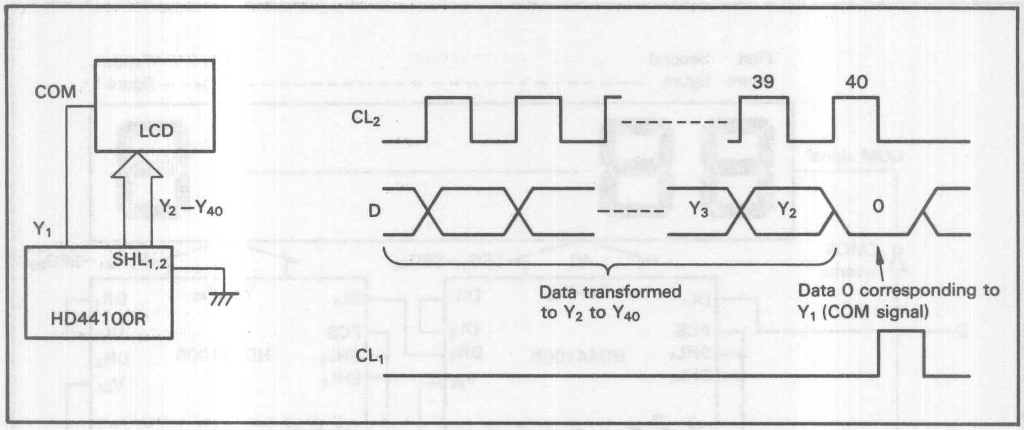
Figure 5 Static Drive Connection

Timing Chart of Input Waveforms



Notes:

1. Input square waves of 50% duty cycle (about 30—500 Hz) to M. The frequency depends on the specifications of LCD panels.
2. The drive waveforms corresponding to the new displayed data are output at the fall of CL1. Therefore, when the alternating signal M and CL1 do not fall synchronously, DC elements are produced on the LCD drive waveforms. These DC elements may shorten the life span of the LCD, if the displayed data frequently changes (e.g. display of hours, minutes, and seconds of a clock). To avoid this, have CL1 fall synchronously with the one edge of M.
3. In this example, the CMOS inverter is used as a COM signal driver in consideration of the large display area. (The load capacitance on COM is large because it is common to all the displayed segments.)
   Usually, one of the HD44100R outputs can be used as a COM signal. The displayed data corresponding to the terminal should be 0 in that case.


COM
LCD
Y_2-Y_{40}
Y_1
$SHL_{1,2}$
HD44100R
39
40
CL_2
D
Y_3
Y_2
0
Data transformed to Y_2 to Y_{40}
Data 0 corresponding to Y_1 (COM signal)
CL_1

HD66100F

(LCD Driver with 80-Channel Outputs)

The HD66100 description segment driver with 80 LCD drive circuits is the improved version of the no longer current HD44100H LCD driver with 40 circuits.
It is composed of a shift register, an 80-bit latch circuit, and 80 LCD drive circuits. Its interface is compatible with the HD44100H.
It reduces the number of LSI's and lowers the cost of an LCD module.

Features

- LCD driver with serial/parallel converting function
- Interface compatible with the HD44100H; connectable with HD43160AH, HD61830, HD61830B, LCD-II (HD44780), LCD-III (HD44790)
- Internal output circuits for LCD drive: 80
- Internal serial/parallel converting circuits:
  —80-bit bidirectional shift register
  —80-bit latch circuit
- Power supply
  —Internal logic circuit: +5 V ±10%
  —LCD drive circuit: 3.0 V to 6.0 V
- CMOS process

Comparison with HD44100H

Table 1 shows the main differences between HD66100 and HD44100H.

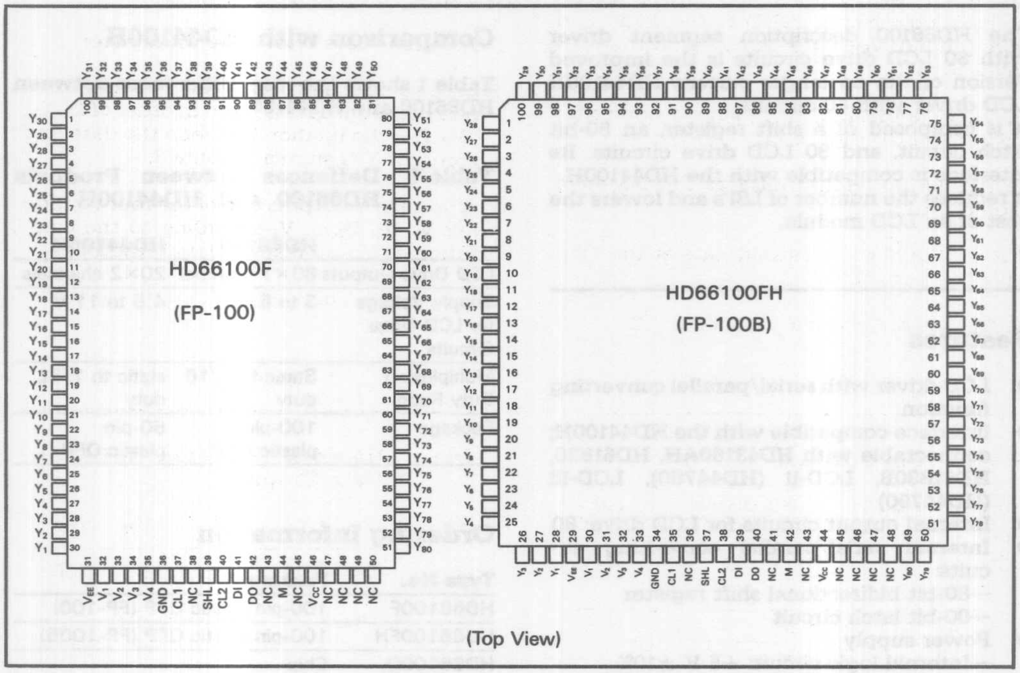
Table 1 Deffences between Products HD66100 and HD44100H

	HD66100	HD44100H
LCD Drive Outputs	80 × 1 Channel	20 × 2 channels
Supply Voltage for LCD Drive Circuits	3 to 6 V	4.5 to 11 V
Multiplexing Duty Ratio	Static to 1/16 duty	static to 1/32 duty
Package	100-pin plastic QFP	60-pin plastic QFP

Ordering Information

Type No.	Package
HD66100F	100-pin plastic QFP (FP-100)
HD66100FH	100-pin plastic QFP (FP-100B)
HD66100D	Chip

Pin Arrangement



Pin Description

V_{CC}, GND, V_{EE}: V_{CC} supplies power to the internal logic circuit. GND is the logic and drive ground. V_{EE} supplies power to the LCD drive circuit.

V_1, V_2, V_3, and V_4: V_1 to V_4 supply power for driving an LCD (figure 2).

CL1: HD66100 latches data at the negative edge of CL1.

CL2: HD66100 receives shift data at the negative edge of CL2.

M: Changes LCD drive outputs to AC.

DI: Inputs data to the shift register.

DO: Output data from the shift register.

SHL: Selects a shift direction of serial data. When the serial data is input in order of D_1, D_2, ..., D_{79}, D_{80}, the relation between the data and the output Y is shown in table 3.

Y_1-Y_{80}: Each Y outputs one of the four voltage levels-V_1, V_2, V_3, or V_4-according to the combination of M and display data (figure 2).

NC: Do not connect any wire to these terminals.

Table 2 Pin Function

Symbol	Pin No.	Pin Name	I/O
V_{CC}	46	V_{CC}	–
GND	36	Ground	–
V_{EE}	31	V_{EE}	–
V_1	32	V_1	–
V_2	33	V_2	–
V_3	34	V_3	–
V_4	35	V_4	–
CL1	37	Clock 1	I
CL2	40	Clock 2	I
M	44	M	I
DI	41	Date In	I
DO	42	Date Out	O
SHL	39	Shift Left	I
Y_1-Y_{80}	1-30,51-100	Y_1-Y_{80}	O
NC	38,43,45,47-50	No Connection	–

Table 3 Relation Between SHL and Data Output

SHL	Y_1	Y_2	Y_3......	Y_{79}	Y_{80}
High	D1	D2	D3......	D79	D80
Low	D80	D79	D78.....	D2	D1

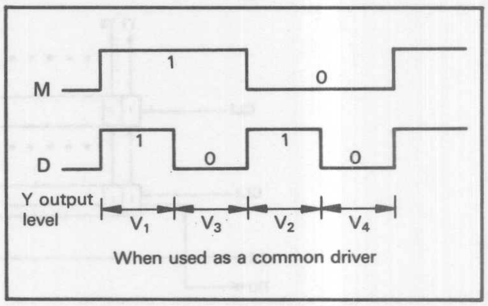


Figure 1 Selection of LCD Drive Output

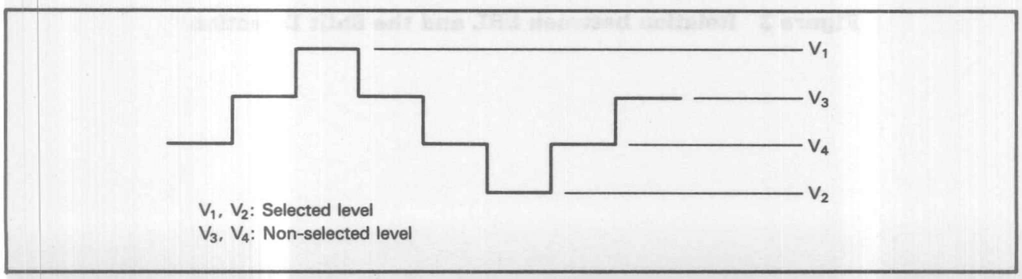


Figure 2 Power Supply for Driving an LCD

Block Functions

LCD Drive Circuits

Select one of four levels of voltage V_1, V_2, V_3, and V_4 for driving a LCD and transfer it to the output terminals according to the combination of M and the data in the latch circuit.

Latch Circuit

Latches the data input from the bidirectional shift register at the fall of CL1 and transfer its outputs to the LCD drive circuits.

Bidirectional Shift Reigster

Shifts the serial data at the fall of CL2 and transfers the output of each bit of the register to the latch circuit. When SHL = GND, the data input from DI shifts from bit 1 to bit 80 in order of entry. On the other hand, when SHL = V_{CC}, the data shifts from bit 80 to bit-1. In both cases, the data of the last bit of the register is latched to be output from DO at the rise of CL2.

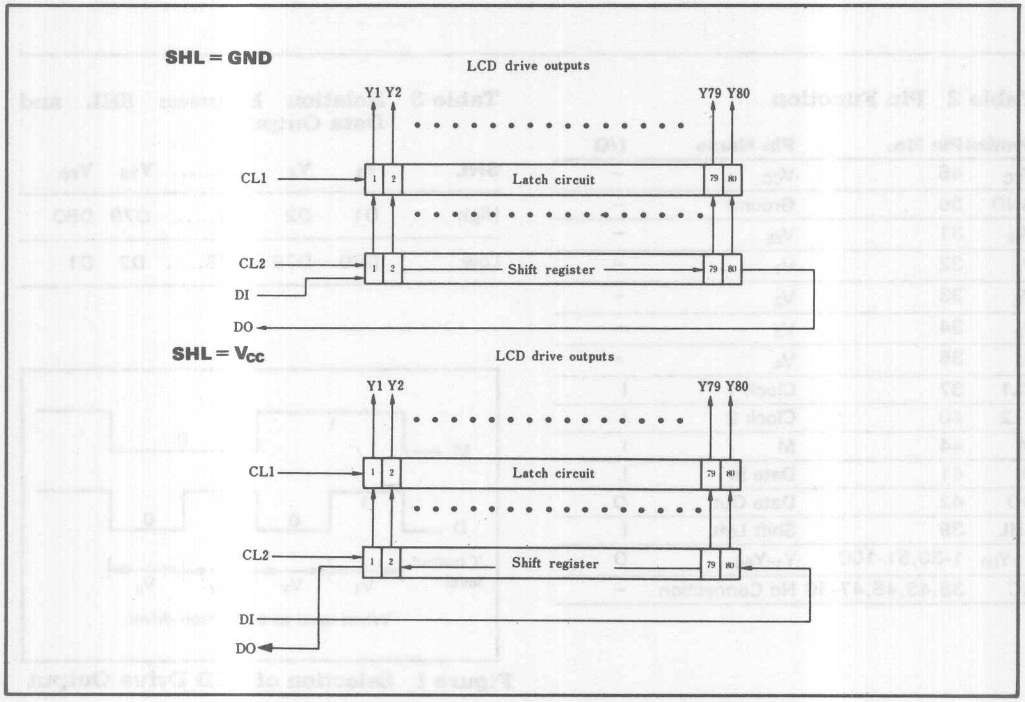


Figure 3 Relation between SHL and the Shift Direction

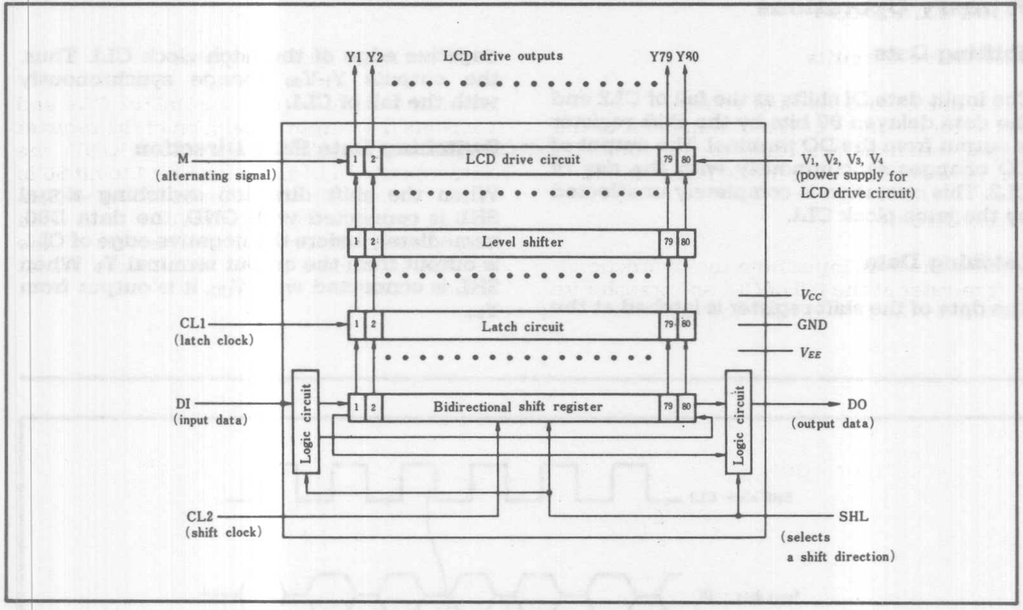


Figure 4 Block Diagram

Primary Operations

Shifting Data

The input data DI shifts at the fall of CL2 and the data delayed 80 bits by the shift register is output from the DO terminal. The output of DO changes synchronously with the rise of CL2. This operation is completely unaffected by the latch clock CL1.

Latching Data

The data of the shift register is latched at the negative edge of the latch clock CL1. Thus, the outputs Y_1-Y_{80} change synchronously with the fall of CL1.

Switching Data Shift Direction

When the shift direction switching signal SHL is connected with GND, the data D80, immediately before the negative edge of CL1, is output from the output terminal Y_1. When SHL is connected with V_{CC}, it is output from Y_{80}.

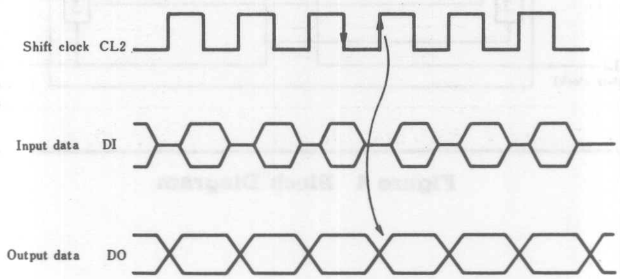


Figure 5 Timing of Receiving and Outputting Data

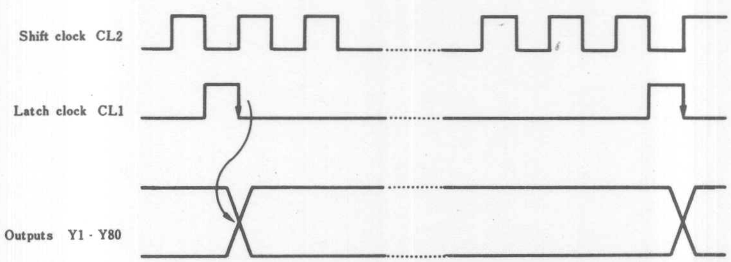


Figure 6 Timing of Latching Data

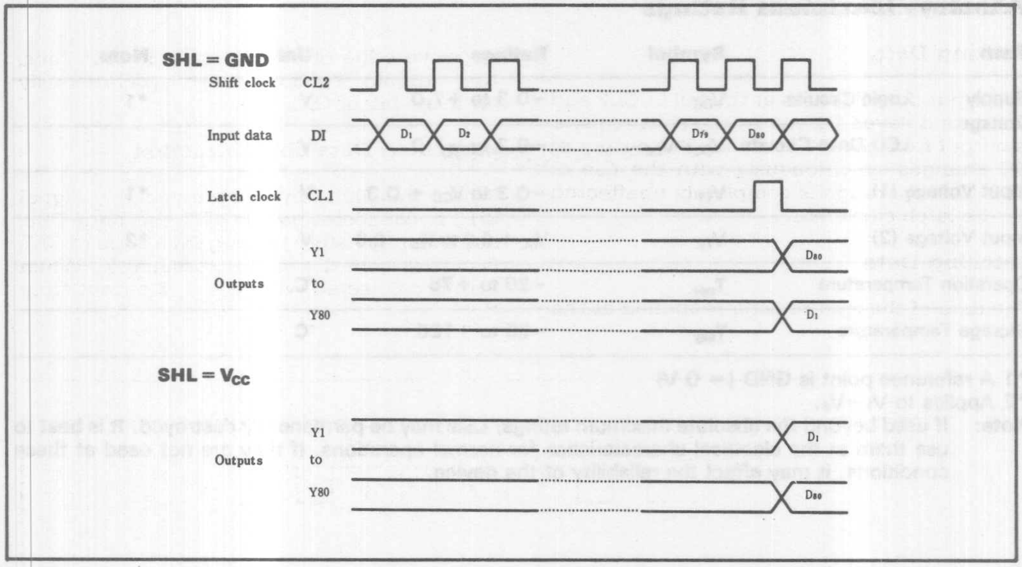


Figure 7 SHL and Waveforms of Data Shift

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Note
Supply Voltage	Logic Circuits	V_{CC}	−0.3 to +7.0	V	*1
	LCD Drive Circuits	V_{CC}—V_{EE}	−0.3 to +7.0	V	
Input Voltage (1)		V_{T1}	−0.3 to V_{CC} + 0.3	V	*1
Input Voltage (2)		V_{T2}	V_{CC} + 0.3 to V_{EE} − 0.3	V	*2
Operation Temperature		T_{opr}	−20 to +75	°C	
Storage Temperature		T_{stg}	−55 to +125	°C	

*1 A reference point is GND (= 0 V)
*2 Applies to $V_1 - V_4$.
Note: If used beyond the absolute maximum ratings, LSIs may be permanently destroyed. It is best to use them at the electrical characteristics for normal operations. If they are not used at these conditions, it may affect the reliability of the device.

Electrical Characteristics

DC Characteristics
(V_{CC} = 5 V ± 10%, $V_{CC}-V_{EE}$=3.0 to 6.0 V, GND = 0 V, T_a = −20 to +75°C)

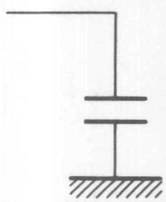
Item	Symbol	Terminals	Min.	Typ.	Max.	Unit	Test condition	Note
Input High Voltage	V_{IH}	CL1, CL2	0.8 × V_{CC}	–	V_{CC}	V		
Input Low Voltage	V_{IL}	M, DI, SHL	0	–	0.2 × V_{CC}	V		
Output High Voltage	V_{OH}	DO	V_{CC}−0.4	–	–	V	I_{OH} = −0.4 mA	
Output Low Voltage	V_{OL}		–	–	0.4	V	I_{OL} = +0.4 mA	
On Resistance Vi-Vj	R_{ON1}	Y_1-Y_{80}	–	–	11	kΩ	I_{ON} = 0.1 mA to one Y terminal	
	R_{ON2}	V_1-V_4	–	–	30	kΩ	I_{ON} = 0.05 mA to each Y terminal	
Input Leakage Current	I_{IL}	CL1, CL2, M, DI, SHL	−5.0	–	5.0	μA	V_{in} = 0 V to V_{CC}	
Vi Leakage Current	I_{VL}	V_1-V_4	−5.0	–	5.0	μA	Output Y_1-Y_{80} open V_{in} = V_{CC} to V_{EE}	
Current Dissipation	I_{GND}		–	–	2.0	mA	f_{CL2} = 1.0 MHz	*1
	I_{EE}		–	–	0.1	mA	f_{CL1} = 2.5 kHz	

*1 Input/output currents are excluded; when an input is at the intermediate level in CMOS, excessive current flows from the power supply through the input circuit.
To avoid this, V_{IH} and V_{IL} must be fixed at V_{CC} and GND level respectively.

AC Characteristics
(V_{CC} = 5 V ± 10%, $V_{CC}-V_{EE}$ = 3.0 to 6.0 V, GND = 0 V, T_a = −20 to +75°C)

Item	Symbol	Terminals	Min.	Typ.	Max.	Unit	Note
Data Shift Frequency	f_{CL}	CL2	–	–	1	MHz	
Clock High level Width	t_{CWH}	CL1,CL2	450	–	–	ns	
Clock Low level Width	t_{CWL}	CL2	450	–	–	ns	
Data Set-Up Time	f_{SU}	DI	100	–	–	ns	
Clock Set-Up Time (1)	t_{SL}	CL2	200	–	–	ns	*1
Clock Set-Up Time (2)	t_{LS}	CL1	200	–	–	ns	*2
Output Delay Time	t_{pd}	DO	–	–	250	ns	*3
Data Hold Time	t_{DH}	DI	100	–	–	ns	
Clock Rise/Fall Time	f_{CT}	CL1,CL2	–	–	50	ns	

*1 Set-up time from the fall of CL2 to that of CL1.
*2 Set-up time from the fall CL1 to that of CL2.
*3 Test terminal



C_L (Load capacitance on outputs) = 30pF
(Including jig capacitance)

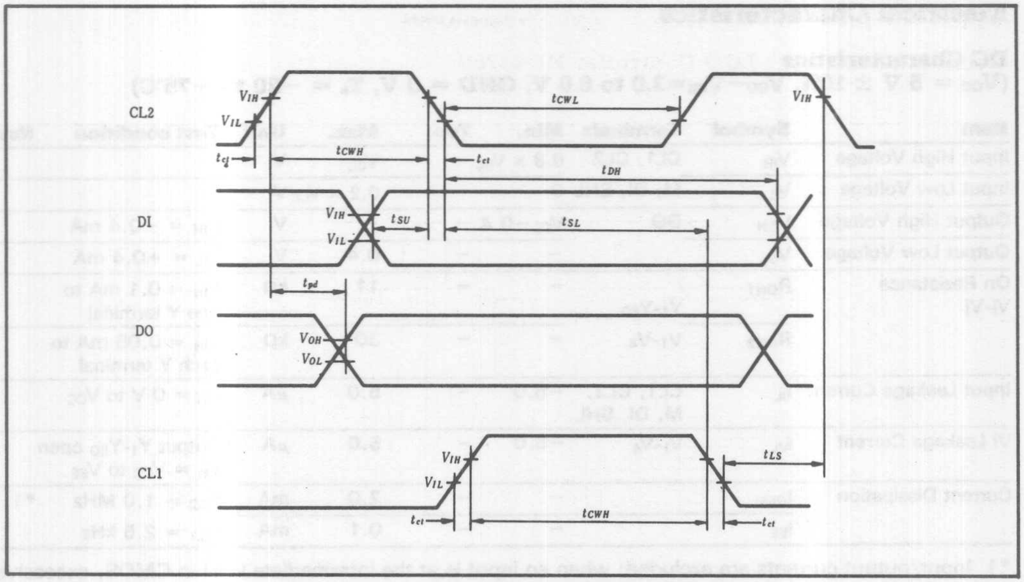


Figure 8 Timing Chart of HD66100F

Typical Applications

Connection with the LCD Controller HD44780

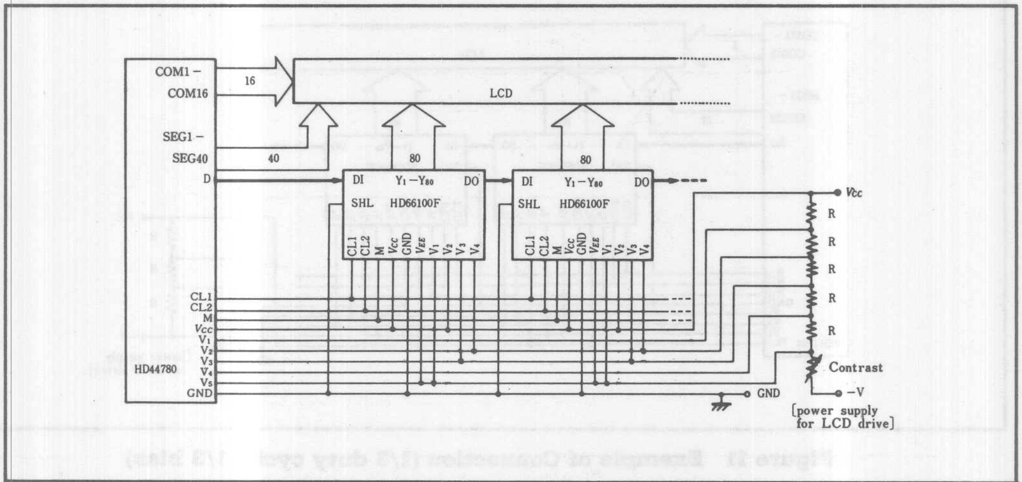


Figure 9 Example of Connection (1/16 duty cycle, 1/5 bias)

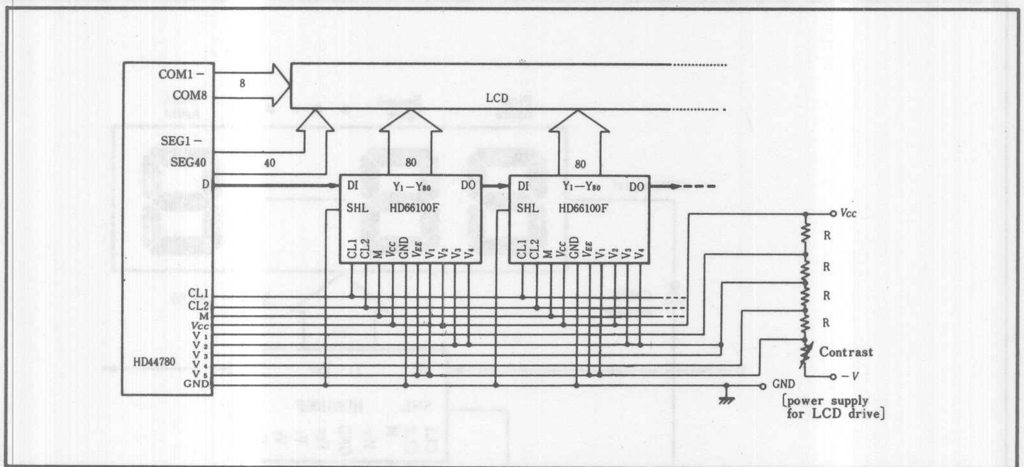


Figure 10 Example of Connection (1/8 duty cycle, 1/4 bias)

Connection with LCD III (HD44790)

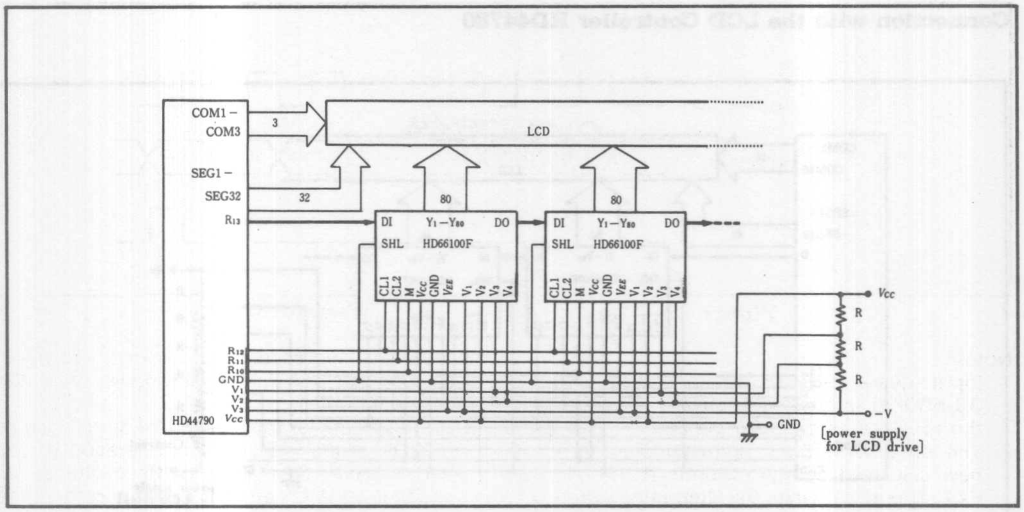


Figure 11 Example of Connection (1/3 duty cycle, 1/3 bias)

Static Drive

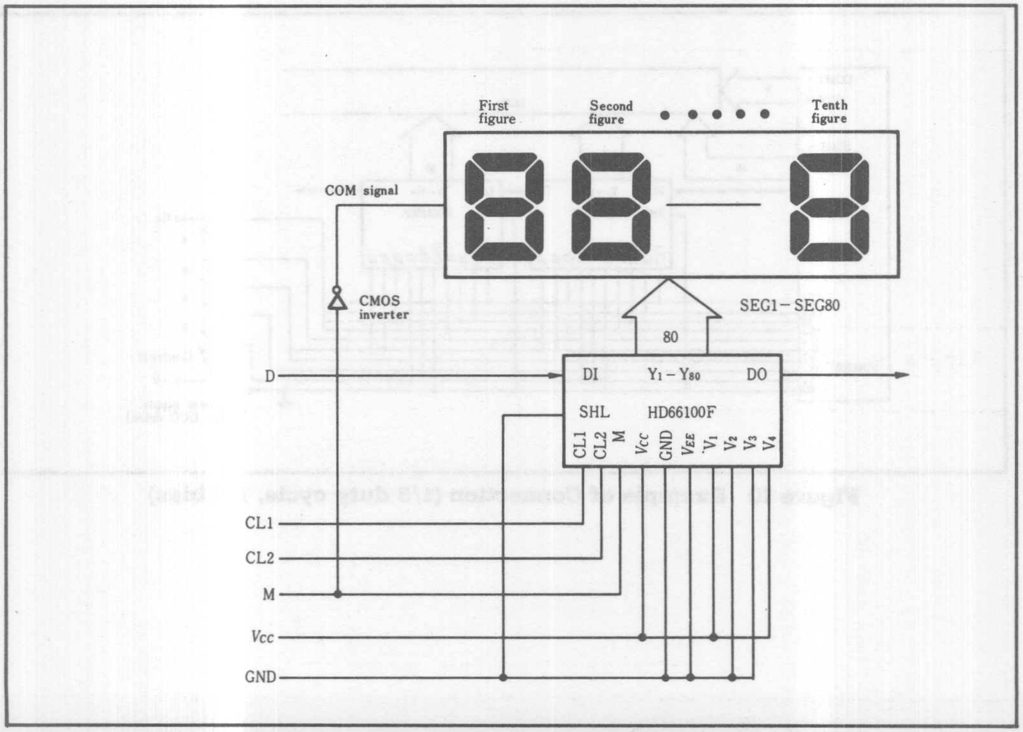


Figure 12 Example of Connection (80-segment display)

- **Timing Chart of Input Waveforms**

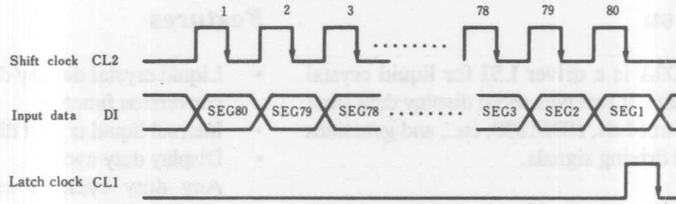


Figure 13 Timing Chart of Input Waveforms

Notes:

1. Input square waves of 50% duty cycle (about 30-500Hz) to M. The frequency depends on the specifications of LCD panels.
2. The drive waveforms corresponding to the new displayed data are output at the fall of CL1. Therefore, when the alternating signal M and CL1 do not fall synchronously, DC elements are produced on the LCD drive waveforms. These DC elements may shorten the life span of the LCD, if the displayed data frequently changes (e.g. display of hours, minutes, and seconds of a clock). To avoid this, make CL1 fall synchronously with the one edge of M.
3. In this example, the CMOS inverter is used as a COM signal driver in consideration of the large display area. (The load capacitance on COM is large because it is common to all the displayed segments.)
Usually, one of the HD66100F outputs can be used as a COM signal. The displayed data corresponding to the terminal should be 0 in that case.

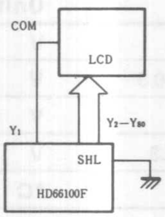


Figure 14 Example of Connection

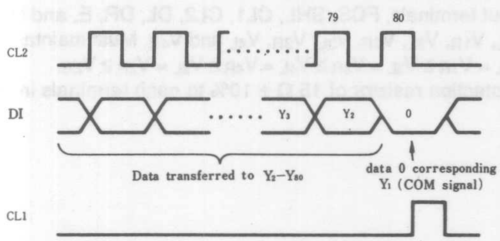


Figure 15 Timing Chart (when Y_1 is used as a COM signal)

HD61100A
(LCD Driver with 80-Channel Outputs)

Description

The HD61100A is a driver LSI for liquid crystal display systems. It receives serial display data from a display control LSI, HD61830, etc., and generates liquid crystal driving signals.

It has liquid crystal driving outputs which correspond to internal 80-bit flip/flops. Both static drive and dynamic drive are possible according to the combination of transfer clock frequency and latch clock frequency.

Ordering Information

Type No.	Package
HD61100A	100-pin plastic QFP(FP-100)

Features

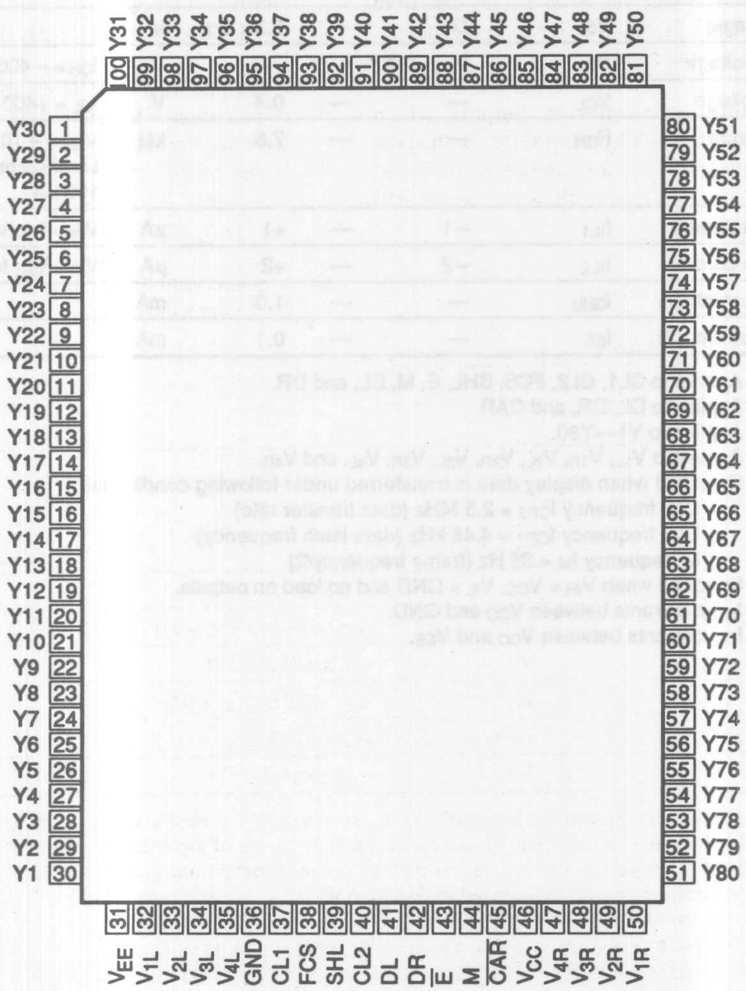
- Liquid crystal display driver with serial/parallel conversion function
- Internal liquid crystal display driver: 80 drivers
- Display duty cycle
  Any duty cycle is selectable according to combination of transfer clock and latch clock
- Data transfer rate: 2.5 MHz max.
- Power supply
  V_{CC}: +5 V ± 10% (Internal logic)
  V_{CC}–V_{EE}: 5.5 to 1.7 V (Liquid crystal display driver circuit)
- Liquid crystal driving level: 17.0 V max.
- CMOS process

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	– 0.3 to +7.0	V	2
Supply voltage (2)	V_{EE}	V_{CC} – 19.0 to V_{CC} + 0.3	V	
Terminal voltage (1)	V_{T1}	– 0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Operating temperature	Topr	– 20 to +75	°C	
Storage temperature	Tstg	– 55 to +125	°C	

Notes:
1. LSIs may be permanently destroyed if used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using it beyond these conditions may cause malfunction and poor reliability.
2. All voltage values are referred to GND = 0 V.
3. Applies to input terminals, FCS, SHL, CL1, CL2, DL, DR, E, and M.
4. Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L} and V_{4R}. Must maintain:
   $$V_{CC} \geq V_{1L} = V_{1R} \geq V_{3L} = V_{3R} \geq V_{4L} = V_{4R} \geq V_{2L} = V_{2R} \geq V_{EE}.$$
   Connect a protection resistor of 15 Ω ± 10% to each terminals in series.

Pin Arrangement



(Top view)

Electrical Characteristics

DC Characteristics
(V_{CC} = 5 V ± 10%, GND = 0 V, $V_{CC}-V_{EE}$ = 5.5 to 17 V, Ta = –20 to +75°C)

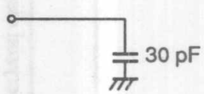
Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	$0.7 \times V_{CC}$	—	V_{CC}	V		1
Input low voltage	V_{IL}	O	—	$0.3 \times V_{CC}$	V		1
Output high voltage	V_{OH}	V_{CC} –0.4	—	—	V	I_{OH} = – 400 µA	2
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = +400 µA	2
Driver resistance	R_{ON}	—	—	7.5	kΩ	V_{EE} = – 10 V, Load current = 100 µA	3
Input leakage current	I_{IL1}	– 1	—	+1	µA	V_{IN} = 0 to V_{CC}	1
Input leakage current	I_{IL2}	– 2	—	+2	µA	V_{IN} = V_{EE} to V_{CC}	4
Dissipation current (1)	I_{GND}	—	—	1.0	mA		5
Dissipation current (2)	I_{EE}	—	—	0.1	mA		5

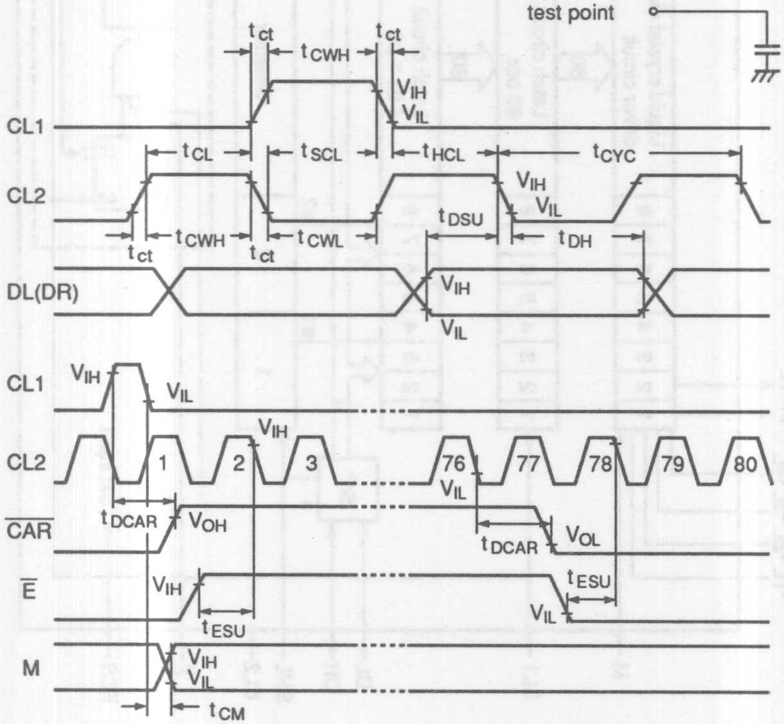
Notes:
1. Applies to CL1, CL2, FCS, SHL, E, M, DL, and DR.
2. Applies to DL, DR, and CAR.
3. Applies to Y1—Y80.
4. Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, and V_{4R}.
5. Specified when display data is transferred under following conditions:
   CL2 frequency f_{CP2} = 2.5 MHz (data transfer rate)
   CL1 frequency f_{CP1} = 4.48 kHz (data latch frequency)
   M frequency f_M = 35 Hz (frame frequency/2)
   Specified when V_{IH} = V_{CC}, V_{IL} = GND and no load on outputs.
   I_{GND}: currents between V_{CC} and GND.
   I_{EE}: currents between V_{CC} and V_{EE}.

AC Characteristics
(V_{CC} = 5 V ± 10%. GND = 0 V, $V_{CC}-V_{EE}$ = 5.5 to 17 V, Ta = –20 to +75°C)

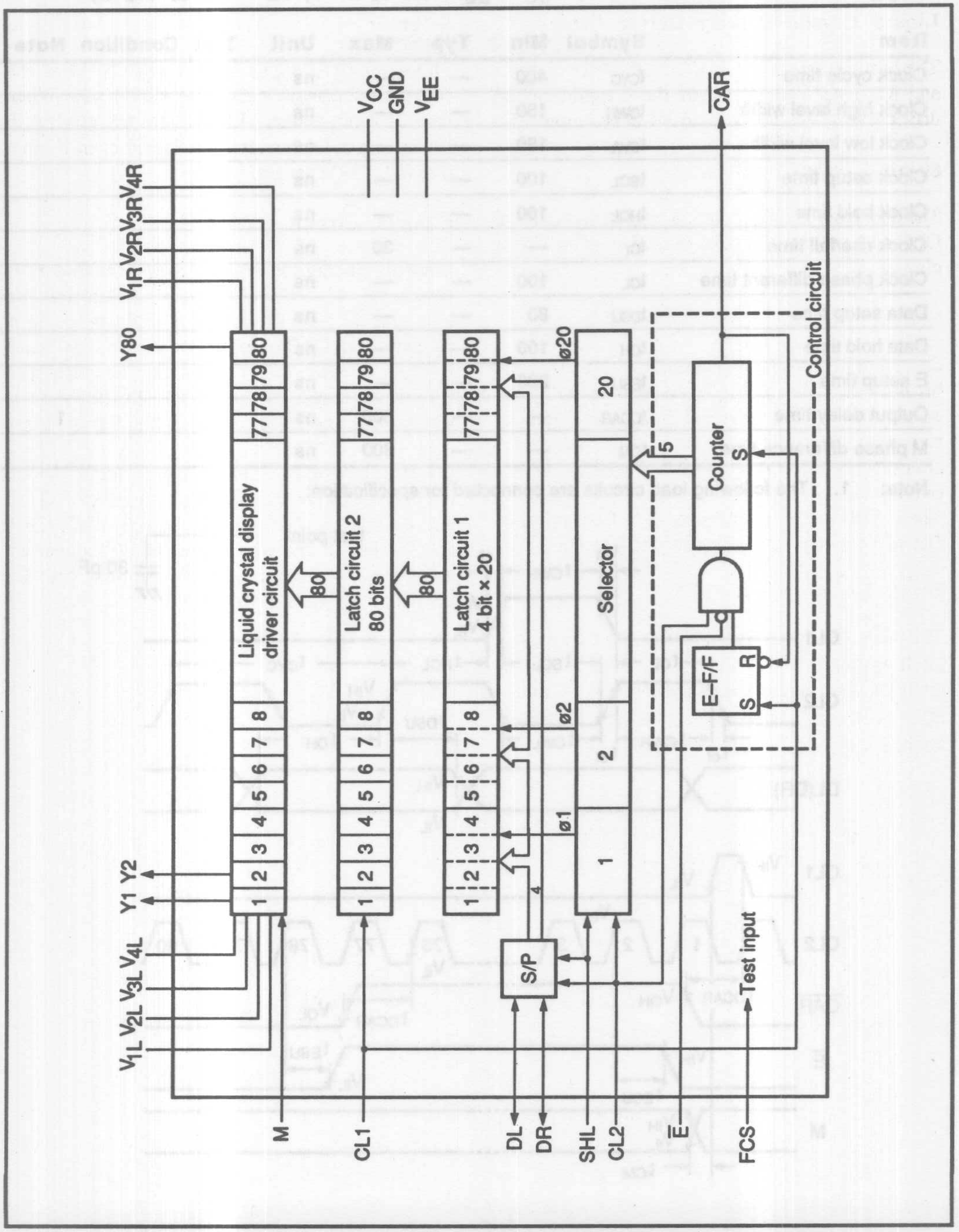
Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Clock cycle time	t_{CYC}	400	—	—	ns		
Clock high level width	t_{CWH}	150	—	—	ns		
Clock low level width	t_{CWL}	150	—	—	ns		
Clock setup time	t_{SCL}	100	—	—	ns		
Clock hold time	t_{HCL}	100	—	—	ns		
Clock rise/fall time	t_{ct}	—	—	30	ns		
Clock phase different time	t_{CL}	100	—	—	ns		
Data setup time	t_{DSU}	80	—	—	ns		
Data hold time	t_{DH}	100	—	—	ns		
E setup time	t_{ESU}	200	—	—	ns		
Output delay time	t_{DCAR}	—	—	300	ns		1
M phase difference time	t_{CM}	—	—	300	ns		

Note: 1. The following load circuits are connected for specification:





Block Diagram



Block Function

Liquid Crystal Display Driver Circuit

The combination of the data from the latch circuit 2 and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

80-bit Latch Circuit 2

The data from latch circuit 1 is latched at the fall of CL1 and output to liquid crystal display driver circuit.

S/P

Serial/Parallel conversion circuit which converts 1-bit data into 4-bit data. When SHL is "L" level, data from DL is converted into 4-bit data and transferred to the latch circuit 1. In this case, don't connect any lines to terminal DR which is in the output status.
When SHL is "H" level, input data from terminal DR without connecting any lines to terminal DL.

80-bit Latch Circuit 1

The 4-bit data is latched at $\phi 1$ to $\phi 20$ and output to latch circuit 2. When SHL is "L" level, the data from DL are latched one in order of $1 \rightarrow 2 \rightarrow 3 \ldots \rightarrow 80$ of each latch. When SHL is "H" level, they are latched in a reverse order ($80 \rightarrow 79 \rightarrow 78 \ldots \rightarrow 1$).

Selector

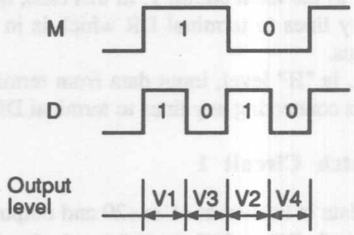
The selector decodes output signals from the counter and generates latch clock $\phi 1$ to $\phi 20$. When the LSI is not active, $\phi 1$ to $\phi 20$ are not generated, so the data at latch circuit 1 is stored even if input data (DL, DR) changes.

Control Circuit

Controls operation: When E—F/F (enable F/F) indicates "1", S/P conversion is started by inputting "L" level to $\overline{E}$. After 80-bit data has been all converted, $\overline{CAR}$ output turns into "L" level and E—F/F is reset to "0", and consequently the conversion stops. E—F/F is RS flip-flop circuit which gives priority to SET over RESET and is set at "H" level of CL1.
Counter consists of 7 bits, and the output signals of upper 5 bits are transferred to the selector. $\overline{CAR}$ signal turns into "H" level at the rise of CL1 and the number of bit which can be S/P-converted increases by connecting $\overline{CAR}$ terminal with $\overline{E}$ terminal of the next HD61100A.

Terminal Functions Description

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} – GND: Power supply for internal logic V_{CC} – V_{EE}: Power supply for LCD drive circuit
V_{1L}-V_{4L} V_{1R}-V_{4R}	8		Power supply	Power supply for liquid crystal drive. V_{1L} (V_{1R}), V_{2L} (V_{2R}): Selection level V_{3L} (V_{3R}), V_{4L} (V_{4R}): Non-selection level Power supplies connected with V_{1L} and V_{1R} (V_{2L} & V_{2R}, V_{3L} & V_{3R}, V_{4L} & V_{4R}) should have the same voltages.
Y1—Y80	80	O	LCD	Liquid crystal driver outputs. Selects one of the 4 levels, V1, V2, V3, and V4. Relation among output level, M and display data (D) is as follows:



Terminal Name	Number of Terminals	I/O	Connected to	Functions
M	1	I	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Latch clock of display data (fall edge trigger). Liquid crystal driver signals corresponding to the display data are output synchronized with the fall of CL1.
CL2	1	I	Controller	Shift clock of display data (D). Falling edge trigger.
DL, DR	2	I/O	Controller	Input of serial display data (D).

(D)	Liquid Crystal Driver Output	Liquid Crystal Display
1 (High)	Selection level	On
0 (Low)	Non-selection level	Off

I/O status of DL and DR terminals depends on SHL input level.

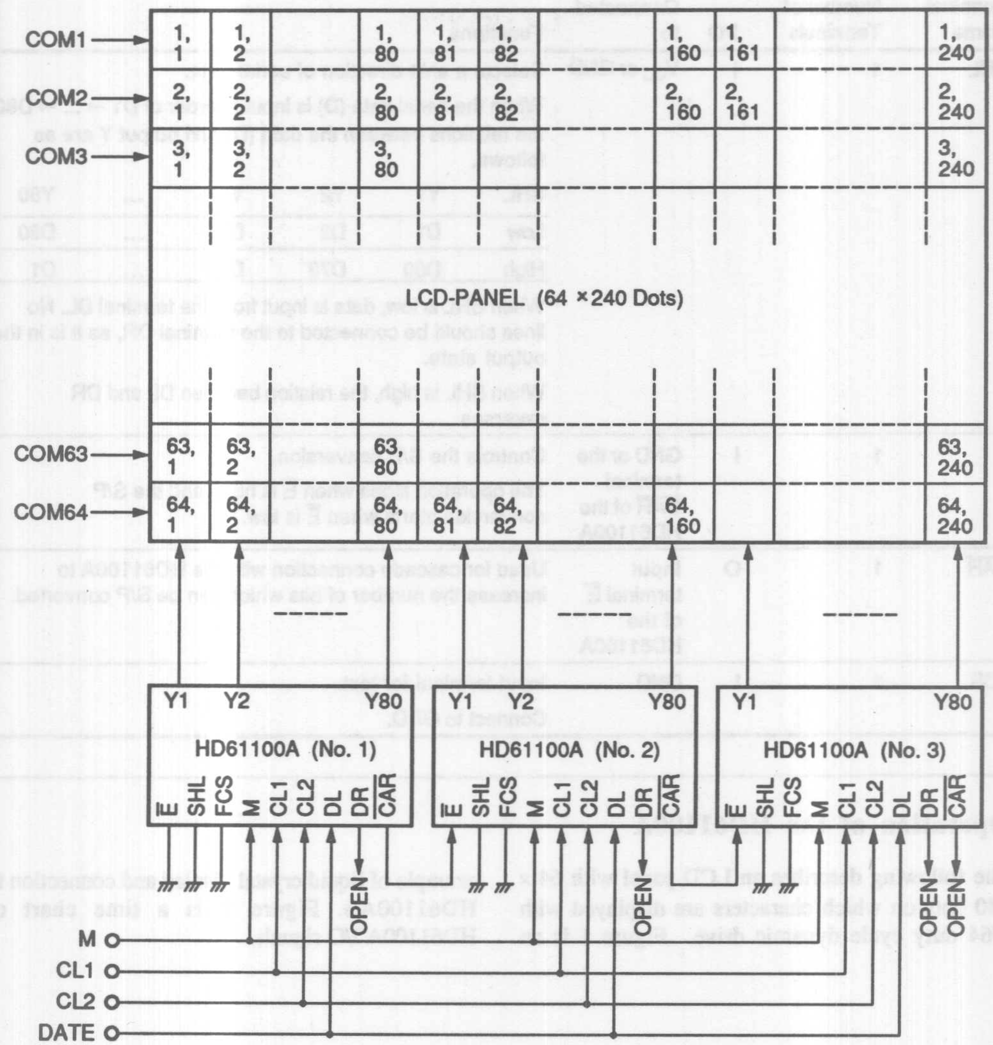
SHL	DL	DR
High	O	I
Low	I	O

Terminal Functions Description (cont)

Terminal Name	Number of Terminals	I/O	Connected to	Functions
SHL	1	I	V_{CC} or GND	Selects a shift direction of serial data. When the serial data (D) is input in order of D1 → ... → D80, the relations between the data (D) and output Y are as follows. <table><tr><th>SHL</th><th>Y1</th><th>Y2</th><th>Y3</th><th>...</th><th>Y80</th></tr><tr><td>Low</td><td>D1</td><td>D2</td><td>D3</td><td>...</td><td>D80</td></tr><tr><td>High</td><td>D80</td><td>D79</td><td>D78</td><td>...</td><td>D1</td></tr></table>When SHL is low, data is input from the terminal DL. No lines should be connected to the terminal DR, as it is in the output state. When SHL is high, the relation between DL and DR reverses.
$\overline{E}$	1	I	GND or the terminal $\overline{CAR}$ of the HD61100A	Controls the S/P conversion. The operation stops when $\overline{E}$ is high, and the S/P conversion starts when $\overline{E}$ is low.
$\overline{CAR}$	1	O	Input terminal $\overline{E}$ of the HD61100A	Used for cascade connection with the HD61100A to increase the number of bits which can be S/P converted.
FCS	1	I	GND	Input terminal for test. Connect to GND.

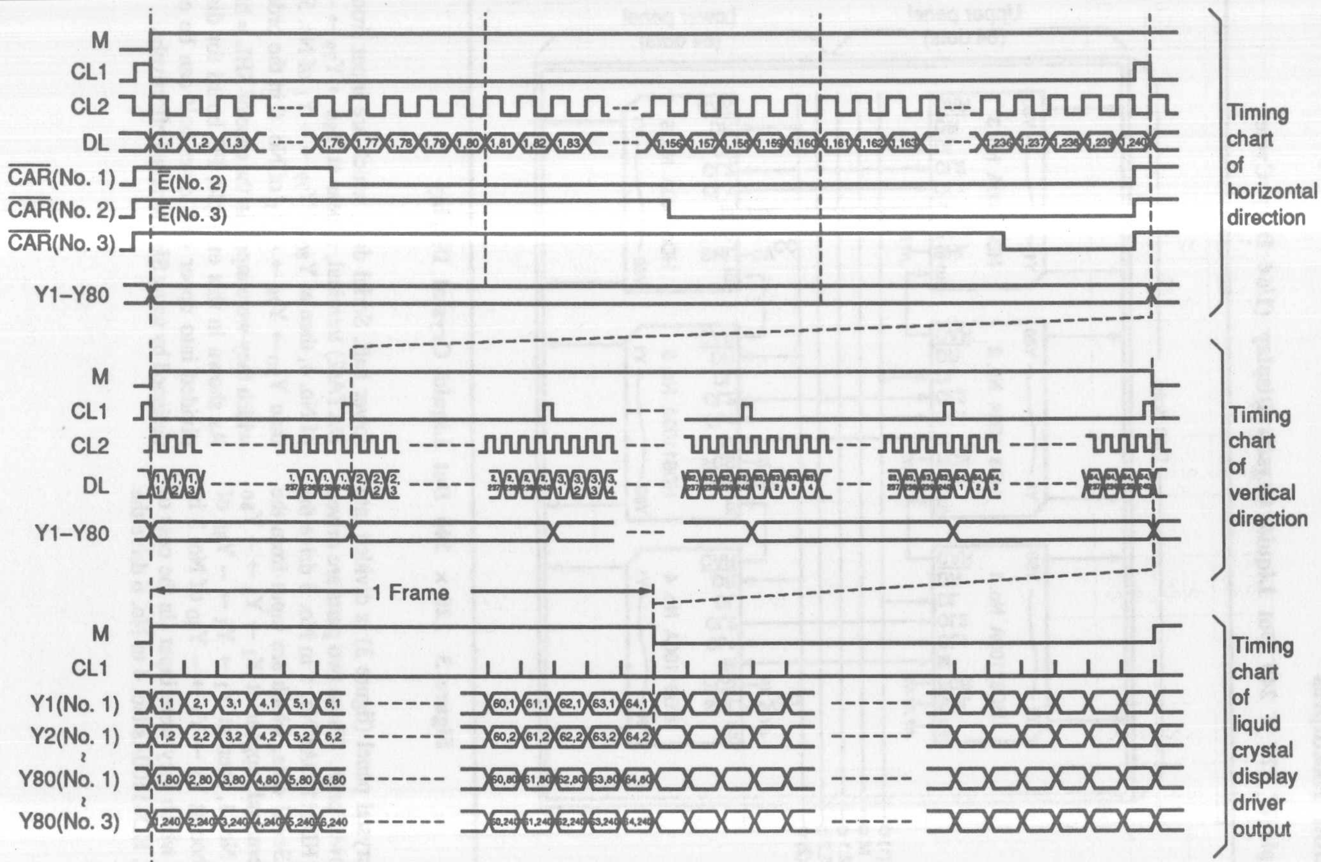
Operation of the HD61100A

The following describes an LCD panel with 64 × 240 dots on which characters are displayed with 1/64 duty cycle dynamic drive. Figure 1 is an example of liquid crystal display and connection to HD61100A's. Figure 2 is a time chart of HD61100A I/O signals.



Cascade three HD61100As. Input data to the terminal DL of No. 1, No 2, and No. 3. Connect $\overline{E}$ of No. 1 to GND. Don´t connect any lines to $\overline{CAR}$ of No. 3. Connect common signal terminals (COM1–COM64) to X1–X64 of common driver HD61103A. (m,n) in LCD panel is the address corresponding to each dot.

Figure 1 LCD driver with 64 × 240 dots



Timing chart for the example of connection in figure 1.
DL input (m, n) is the data that corresponds to each address (m, n) of LCD panel.

Figure 2 HD61100A Timing Chart

Application Examples

An Example of 128 × 240 Dot Liquid Crystal Display (1/64 Duty Cycle)

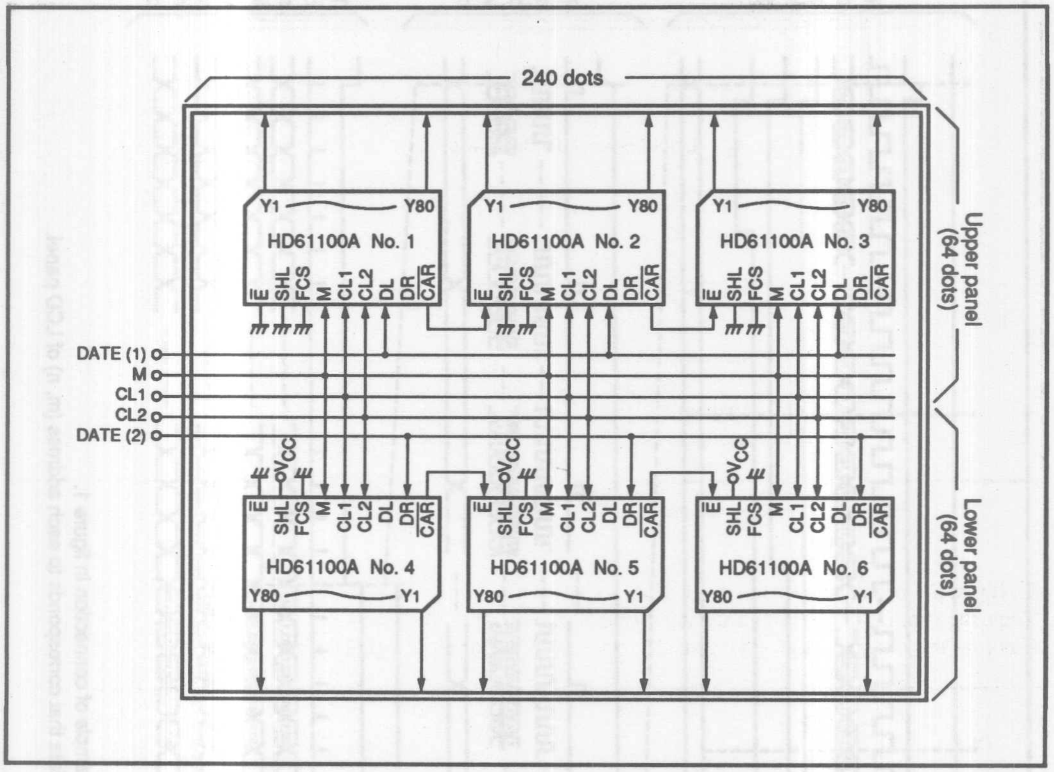


Figure 3 128 × 240 Dot Liquid Crystal Display

The liquid crystal panel (figure 3) is divided into upper and lower parts. These two parts are driven separately. HD61100As No. 1 to No. 3 drive the upper half. Serial data, which are input from the DATA(1) terminal, appear at $Y_1 \rightarrow Y_2 \rightarrow$ -- Y_{80} terminal of No. 1, then at $Y_1 \rightarrow Y_2 \rightarrow$ -- Y_{80} of No. 2 and then at $Y_1 \rightarrow Y_2 \rightarrow$ -- Y_{80} of No. 3 in the order in which they were input (in the case of SHL = low). HD61100As No. 4 to No. 6 drive the lower half. Serial data, which are input from the DATA(2) terminal, appear at $Y_{80} \rightarrow Y_{79} \rightarrow$ -- Y_1 of No. 4, then at $Y_{80} \rightarrow Y_{79} \rightarrow$ -- Y_1 of No. 5 and then $Y_{80} \rightarrow Y_{79} \rightarrow$ -- Y_1 of No. 6 in the order in which they were input (in the case of SHL = high). As shown in this example, PC board for display divided into upper and lower half can be easily designed by using SHL terminal effectively.

Example of 64 × 150 Dot Liquid Crystal Display (1/64 Duty Cycle, SHL = Low)

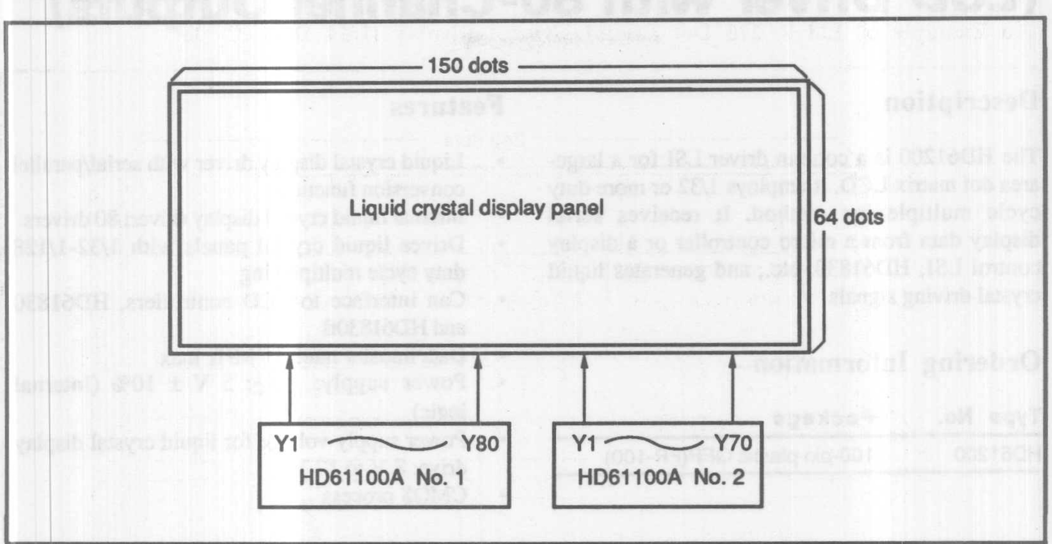


Figure 4 64 × 150 Dot Liquid Crystal Display

4-bit parallel process is used in this LSI to lessen the power dissipation.
Thus, the sum of the dots in horizontal direction should be multiple of 4.
If not, as this example (figure 4), consideration is needed for input signals (figure 5).

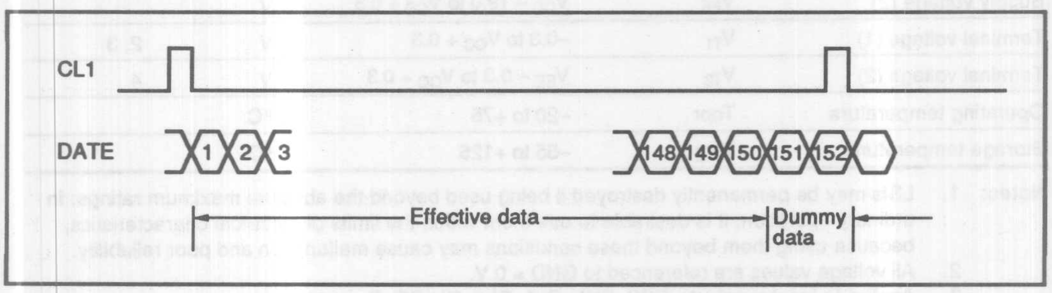


Figure 5 Input Dots, 150 Horizontal Dots

As the sum of dots in lateral direction is 150, 2 more dummy data bits are transferred (152 = 4 × 38). Dummy data, which is output from Y71 and Y72 of No. 2, can be either 0 or 1 because these terminals do not connect with the liquid crystal display panel.

HD61200

(LCD Driver with 80-Channel Outputs)

Description

The HD61200 is a column driver LSI for a large-area dot matrix LCD. It employs 1/32 or more duty cycle multiplexing method. It receives serial display data from a micro controller or a display control LSI, HD61830, etc., and generates liquid crystal driving signals.

Features

- Liquid crystal display driver with serial/parallel conversion function
- Internal liquid crystal display driver: 80 drivers
- Drives liquid crystal panels with 1/32-1/128 duty cycle multiplexing
- Can interface to LCD controllers, HD61830 and HD61830B
- Data transfer rate: 2.5 MHz max
- Power supply: V_{CC}: 5 V ± 10% (Internal logic)
- Power supply voltage for liquid crystal display drive: 8 V to 17 V
- CMOS process

Ordering Information

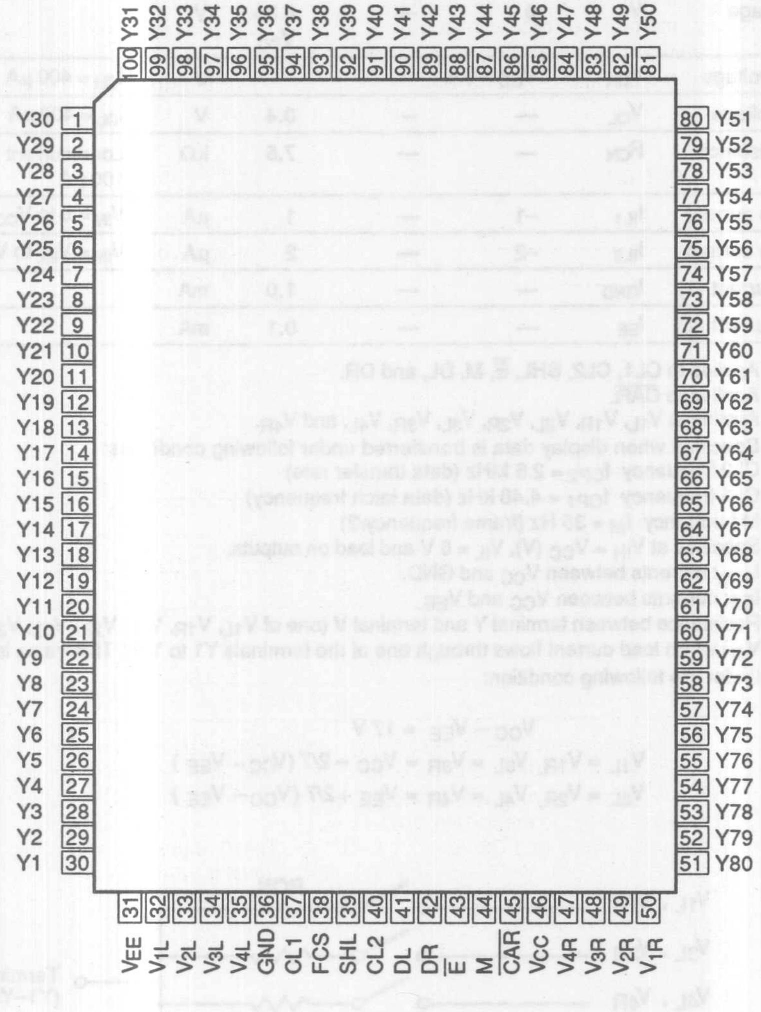
Type No.	Package
HD61200	100-pin plastic QFP(FP-100)

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V	2
Supply voltage (2)	V_{EE}	V_{CC} – 19.0 to V_{CC} + 0.3	V	
Terminal voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +125	°C	

Notes: 1. LSIs may be permanently destroyed if being used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using them beyond these conditions may cause malfunction and poor reliability.
2. All voltage values are referenced to GND = 0 V.
3. Applies to input terminals, FCS, SHL, CL1, CL2, DL, DR, E, and M.
4. Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, and V_{4R}. Must maintain $V_{CC} \geq V_{1L} = V_{1R} \geq V_{3L} = V_{3R} \geq V_{4L} = V_{4R} \geq V_{2L} = V_{2R} \geq V_{EE}$.
Connect a protection resistor of 15 Ω ± 10% to each terminal in series.

Pin Arrangement



(Top View)

Electrical Characteristics

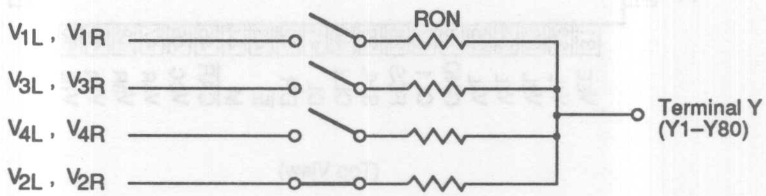
DC Characteristics

(V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – VEE = 8 V to 17 V, Ta = –20 to 75°C)

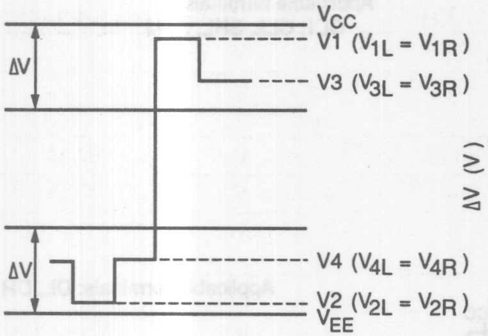
Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	$0.7 \times V_{CC}$	—	V_{CC}	V		1
Input low voltage	V_{IL}	0	—	$0.3 \times V_{CC}$	V		1
Output high voltage	V_{OH}	V_{CC} –0.4	—	—	V	I_{OH} = 400 µA	2
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 400 µA	2
Driver on resistance	R_{ON}	—	—	7.5	kΩ	Load current = 100 µA	5
Input leakage current	I_{IL1}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	1
Input leakage current	I_{IL2}	–2	—	2	µA	V_{IN} = V_{EE} to V_{CC}	3
Dissipation current (1)	I_{GND}	—	—	1.0	mA		4
Dissipation current (2)	I_{EE}	—	—	0.1	mA		4

Notes:
1. Applies to CL1, CL2, SHL, $\overline{E}$, M, DL, and DR.
2. Applies to $\overline{CAR}$.
3. Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, and V_{4R}.
4. Specified when display data is transferred under following conditions:
   CL2 frequency f_{CP2} = 2.5 MHz (data transfer rate)
   CL1 frequency f_{CP1} = 4.48 kHz (data latch frequency)
   M frequency f_M = 35 Hz (frame frequency/2)
   Specified at $V_{IH} = V_{CC}$ (V), V_{IL} = 0 V and load on outputs.
   I_{GND}: currents between V_{CC} and GND.
   I_{EE}: currents between V_{CC} and V_{EE}.
5. Resistance between terminal Y and terminal V (one of V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, and V_{4R} when load current flows through one of the terminals Y1 to Y80. This value is specified under the following condition:

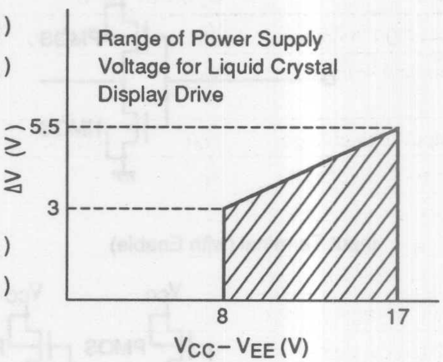
$$V_{CC} - V_{EE} = 17\text{ V}$$
$$V_{1L} = V_{1R},\ V_{3L} = V_{3R} = V_{CC} - 2/7\,(V_{CC} - V_{EE})$$
$$V_{2L} = V_{2R},\ V_{4L} = V_{4R} = V_{EE} + 2/7\,(V_{CC} - V_{EE})$$



The following here is a description of the range of power supply voltage for liquid crystal display drivers. Apply positive voltage to $V_{1L} = V_{1R}$ and $V_{3L} = V_{3R}$ and negative voltage to $V_{2L} = V_{2R}$ and $V_{4L} = V_{4R}$ within the ΔV range. This range allows stable impedance on driver output (RON). Notice the ΔV depends on power supply voltage $V_{CC}–V_{EE}$.



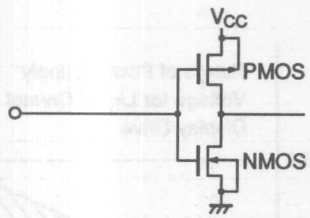
Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage $V_{CC}– V_{EE}$ and ΔV

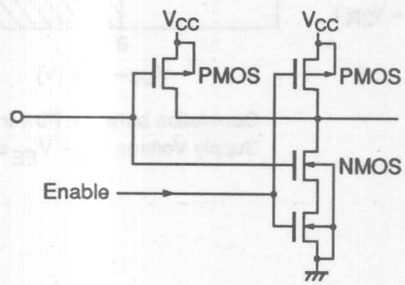
Terminal Configuration

Input Terminal

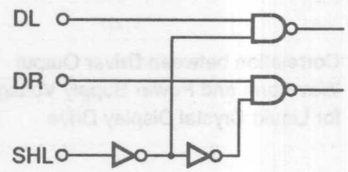


Applicable terminals :
CL1, CL2, SHL, $\overline{\text{E}}$, M

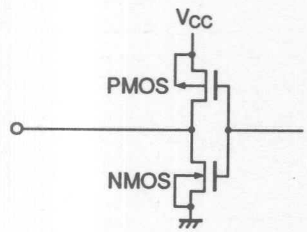
Input Terminal (with Enable)



Applicable terminals: DL, DR



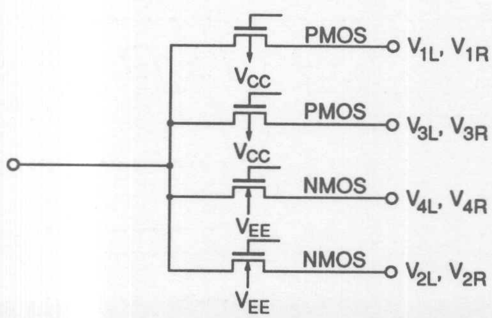
Output Terminal



Applicable terminal: $\overline{\text{CAR}}$

Output Terminal

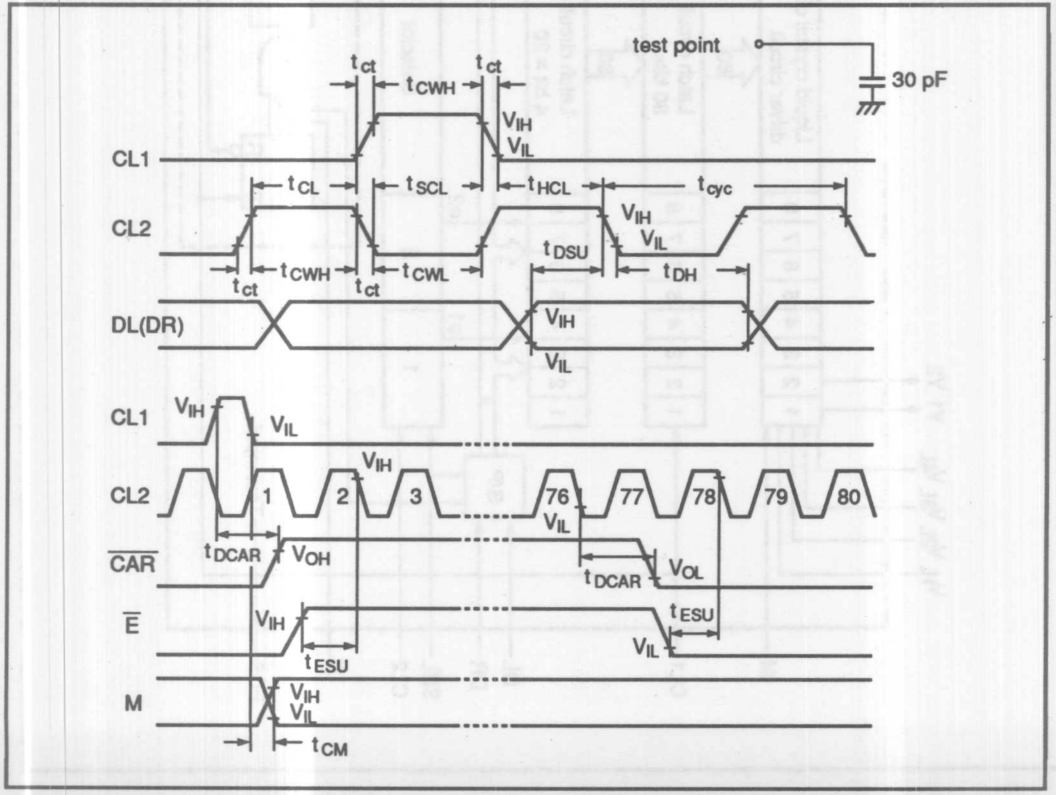
Applicable terminals:
Y1–Y80



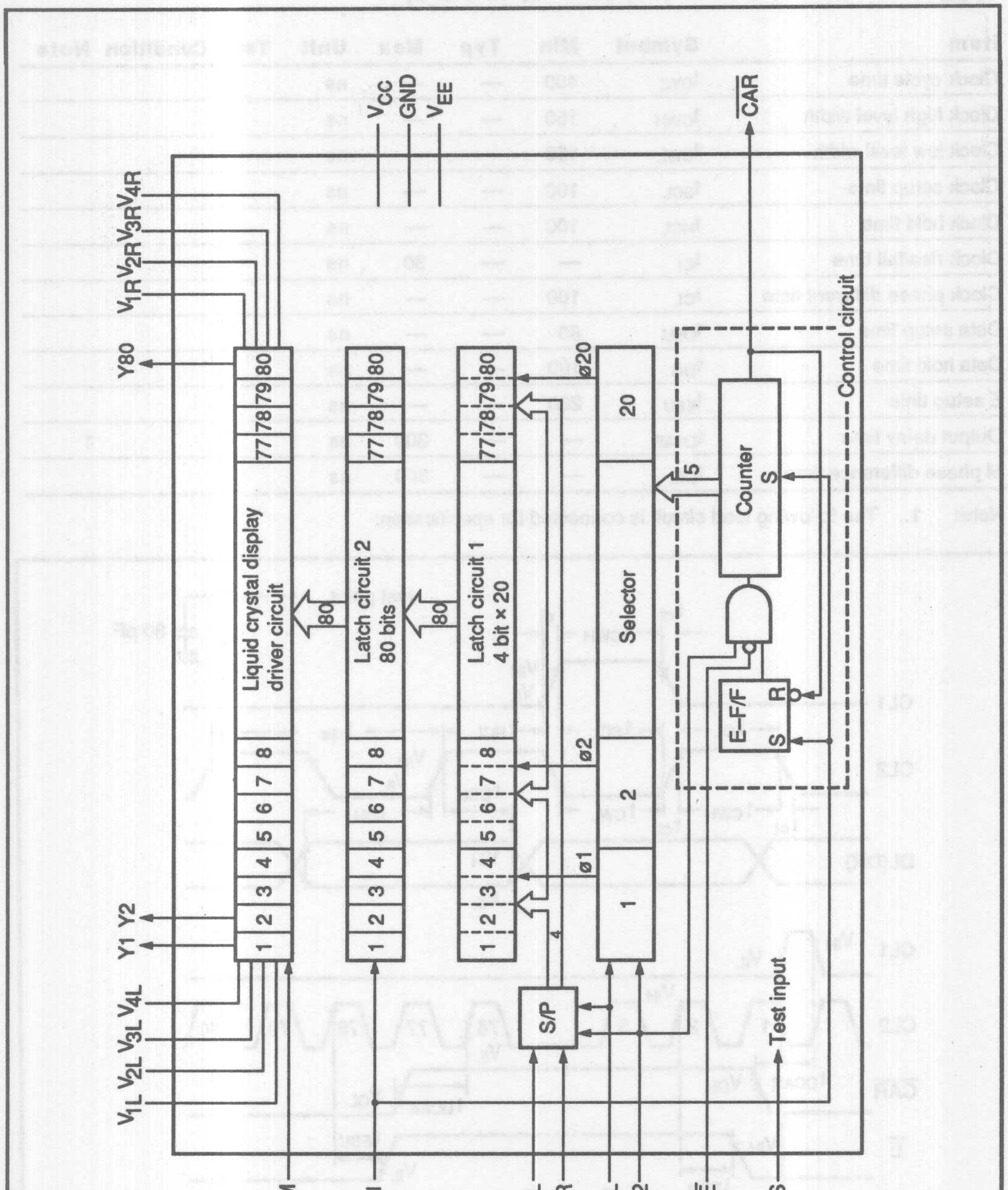
AC Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Clock cycle time	t_{CYC}	400	—	—	ns		
Clock high level width	t_{CWH}	150	—	—	ns		
Clock low level width	t_{CWL}	150	—	—	ns		
Clock setup time	t_{SCL}	100	—	—	ns		
Clock hold time	t_{HCL}	100	—	—	ns		
Clock rise/fall time	t_{Ct}	—	—	30	ns		
Clock phase different time	t_{CL}	100	—	—	ns		
Data setup time	t_{DSU}	80	—	—	ns		
Data hold time	t_{DH}	100	—	—	ns		
E setup time	t_{ESU}	200	—	—	ns		
Output delay time	t_{DCAR}	—	—	300	ns		1
M phase difference time	t_{CM}	—	—	300	ns		

Note: 1. The following load circuit is connected for specification:



Block Diagram



Block Function

Liquid Crystal Display Driver Circuit

The combination of the data from the latch circuit 2 and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3, and V4 to be output.

80-bit Latch Circuit 2

The data from latch circuit 1 is latched at the fall of CL1 and output to liquid crystal display driver circuit.

S/P

Serial/parallel conversion circuit which converts 1-bit data into 4-bit data. When SHL is low level, data from DL is converted into 4-bit data and transferred to the latch circuit 1. In this case, don't connect any lines to terminal DR.

When SHL is high level, input data from terminal DR without connecting any lines to terminal DL.

80-bit Latch Circuit 1

The 4-bit data is latched at ϕ1—ϕ20 and output to latch circuit 2. When SHL is low level, the data from DL are latched in order of 1→2→3 ... →80 of each latch. When SHL is high level, they are latched in a reverse order (80→79→78 ... →1).

Selector

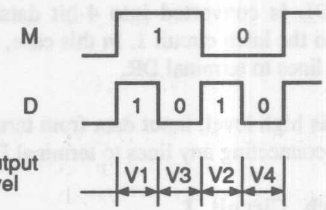
The selector decodes output signals from the counter and generates latch clock ϕ1 to ϕ20. When the LSI is not active, ϕ1–ϕ20 are not generated, so the data at latch circuit 1 is stored even if input data (DL, DR) changes.

Control Circuit

Controls operation: When E–F/F (enable F/F) indicates 1, S/P conversion is started by inputting low level to $\overline{\text{E}}$. After 80-bit data has been all converted, $\overline{\text{CAR}}$ output turns into low level and E–F/F is reset to 0, and consequently the conversion stops. E–F/F is RS flip-flop circuit which gives priority to SET over RESET and is set at high level of CL1.

The counter consists of 7 bits, and the output signals upper 5 bits are transferred to the selector. $\overline{\text{CAR}}$ signal turns into high level at the rise of CL1. The number of bits that can be S/P-converted can be increased by connecting $\overline{\text{CAR}}$ terminal with $\overline{\text{E}}$ terminal of the next HD61200.

Terminal Functions Description

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} – GND: Power supply for internal logic V_{CC} – V_{EE}: Power supply for LCD drive circuit
V_{1L}–V_{4L} V_{1R}–V_{4R}	8		Power supply	Power supply for liquid crystal drive. V_{1L} (V_{1R}), V_{2L} (V_{2R}): Selection level V_{3L} (V_{3R}), V_{4L} (V_{4R}): Non-selection level Power supplies connected with V_{1L} and V_{1R} (V_{2L} & V_{2R}, V_{3L} & V_{3R}, V_{4L} & V_{4R}) should have the same voltages.
Y1-Y80	80	O	LCD	Liquid crystal driver outputs. Selects one of the 4 levels, V1, V2 V3, and V4. Relation among output level, M, and display data (D) is as follows: 
M	1	I	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Synchronous signal (a counter is reset at high level). Latch clock of display data (falling edge triggered). Synchronized with the fall of CL1, liquid crystal driver signals corresponding to the display data are output.
CL2	1	I	Controller	Shift clock of display data (D). Falling edge triggered.
DL, DR	2	I	Controller	Input of serial display data (D). (D) / Liquid Crystal Driver Output / Liquid Crystal Display 1 (High level) / Selection level / On 0 (Low level) / Non-selection level / Off
SHL	1	I	V_{CC} or GND	Selects the shift direction of serial data. When the serial data (D) is input in order of D1→ ... →D80, the relations between the data (D) and output Y are as follows: SHL / Y1 / Y2 / Y3 / .... / Y80 Low / D1 / D2 / D3 / .... / D80 High / D80 / D79 / D78 / .... / D1

Terminal Functions Description (cont)

Terminal Name	Number of Terminals	I/O	Connected to	Functions
SHL (cont)	1	I	V_{CC} or GND	When SHL is low, data is input from the DL terminal. No lines should be connected to the DR terminal. When SHL is high, the relation between DL and DR reverses.
$\overline{E}$	1	I	GND or the terminal $\overline{CAR}$ of the HD61200	Controls the S/P conversion. The operation stops on high level, and the S/P conversion starts on low level.
$\overline{CAR}$	1	O	Input terminal $\overline{E}$ of the HD61200	Used for cascade connection with the HD61200 to increase the number of bits that can be S/P converted.
FCS	1	I	GND	Input terminal for test. Connect to GND.

Operation of the HD61200

The following describes an LCD panel with 64 × 240 dots on which characters are displayed with 1/64 duty cycle dynamic drive. Figure 1 is an example of liquid crystal display and connection to HD61200s. Figure 2 is a time chart of HD61200 I/O signals.

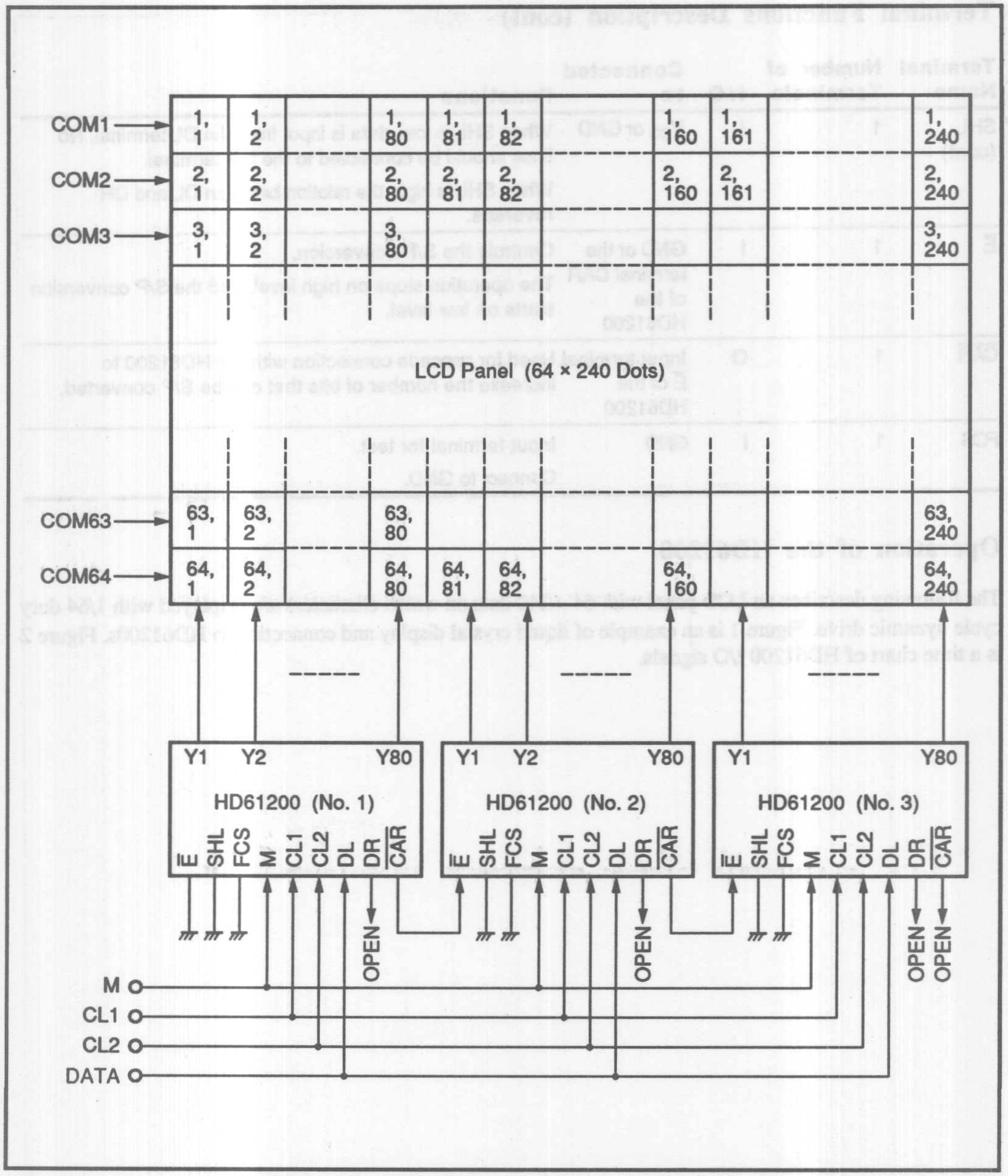
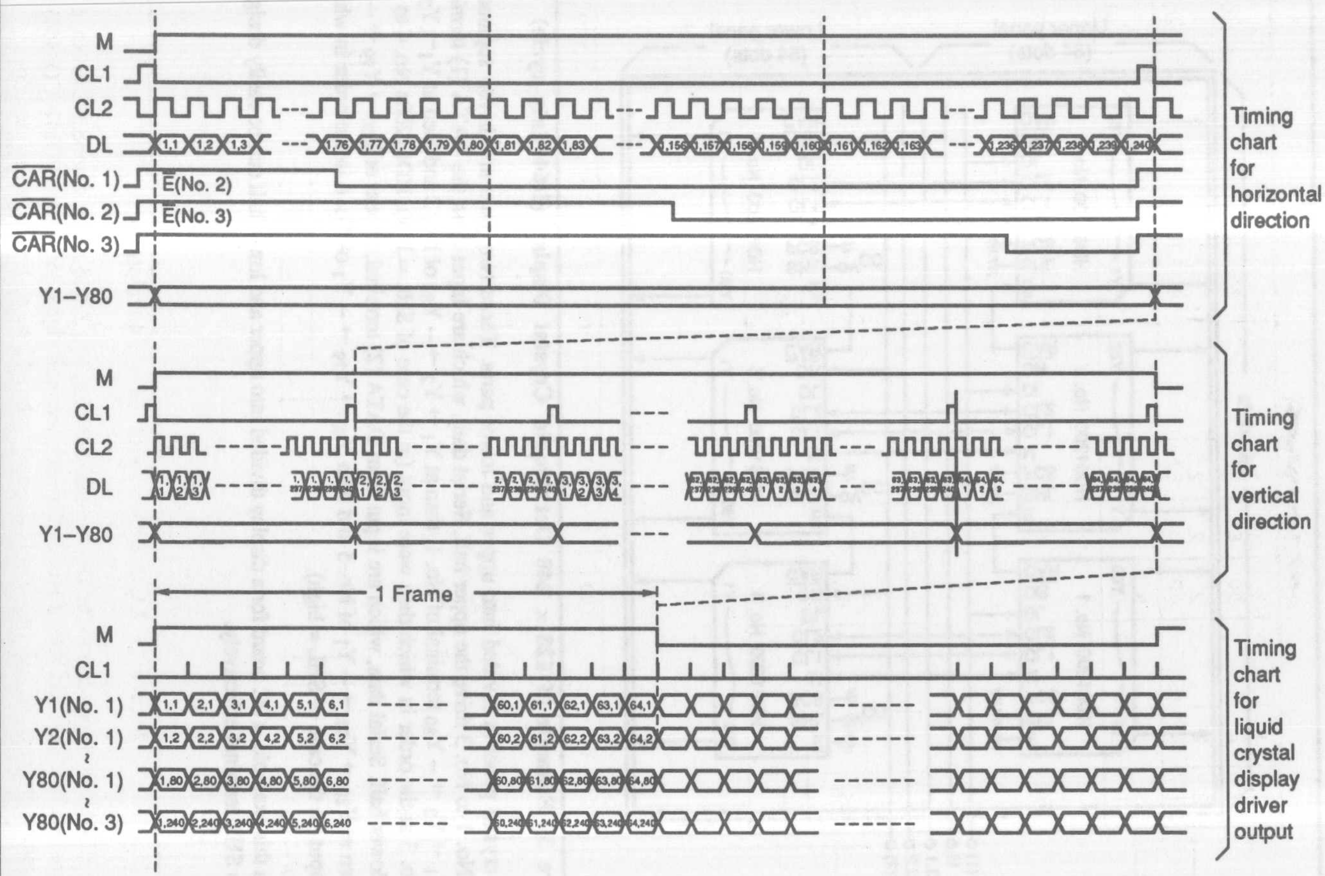


Figure 1 LCD Driver with 64 × 240 Dots

Cascade three HD61200s. Input data to the DL terminal of No. 1, No. 2, and No. 3. Connect $\overline{\text{E}}$ of No. 1 to GND. Don't connect any lines to $\overline{\text{CAR}}$ of No. 3. Connect common signal terminals (COM1–COM64) to X1–X64 of common driver HD61203. (m, n) of LCD panel is the address corresponding to each dot.



Timing chart for example of connection in figure 1.
DL input (m, n) is the data that corresponds to each address (m, n) of LCD panel.

Figure 2 HD61200 Timing Chart

Application Example

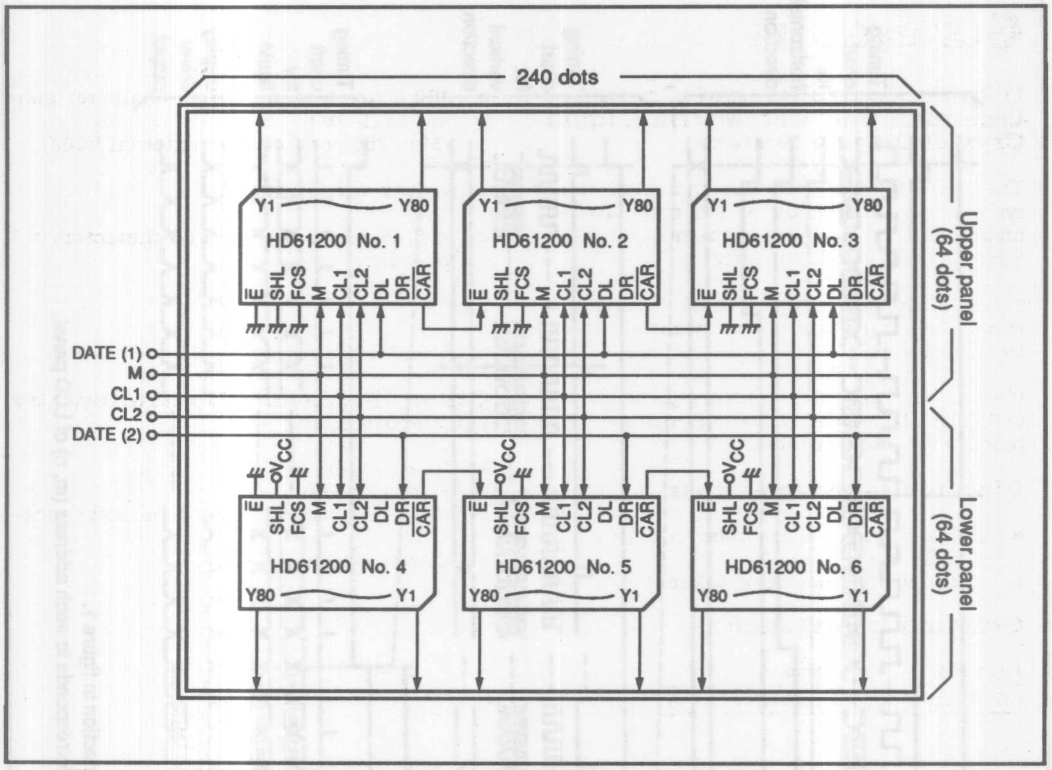


Figure 3 Example of 128 × 240 Dot Liquid Crystal Display (1/64 duty cycle)

The liquid crystal panel is divided into upper and lower parts. These two parts are driven separately. HD61200s No. 1 to No. 3 drive the upper half. Serial data, which are input from the DATA (1) terminal, appear at $Y_1 \rightarrow Y_2 \rightarrow$ -- Y_{80} terminal of No. 1, then at $Y_1 \rightarrow Y_2 \rightarrow$ -- Y_{80} of No. 2 and then at $Y_1 \rightarrow Y_2 \rightarrow$ -- Y_{80} of No. 3 in the order in which they were input (in the case of SHL = low). HD61200s No. 4 to No. 6 drive the lower half. Serial data, which are input from DATA (2) terminal, appear at $Y_{80} \rightarrow Y_{79} \rightarrow$ -- Y_1 of No. 4, then at $Y_{80} \rightarrow Y_{79} \rightarrow$ -- Y_1 of No. 5 and then $Y_{80} \rightarrow Y_{79} \rightarrow$ -- Y_1 of No. 6 in the order in which they were input (in the case of SHL = high).

As shown in this example, a PC board for a display divided into upper and lower half can be easily designed by using the SHL terminal effectively.

HD43160AH

(Controller with Built-in Character Generator)

Display Controller and Character Generator for Dot Matrix Liquid Crystal Display System

The HD43160AH receives character data written in ASCII code or JIS code from a microcomputer and stores them in its RAM which has 80 words capacity.

The HD43160AH converts these data into a serial character pattern, then transfers them to LCD drivers.

It also generates other control signals for the LCD. The HD44100H LCD driver can be combined with this controller.

Display Characters Types

- Alphanumeric characters: A-Z, a-z, @, #, %, &, etc.
- Japanese characters (katakana)
- 160 characters in internal character generator (ROM)
(Max 256 characters in external ROM)

Number Of Characters

- 4, 8, 16, 24, 32, 40, 64, or 80 characters in 1 or 2 lines

Font

- 5 × 7 + Cursor or 5 × 11 + Cursor

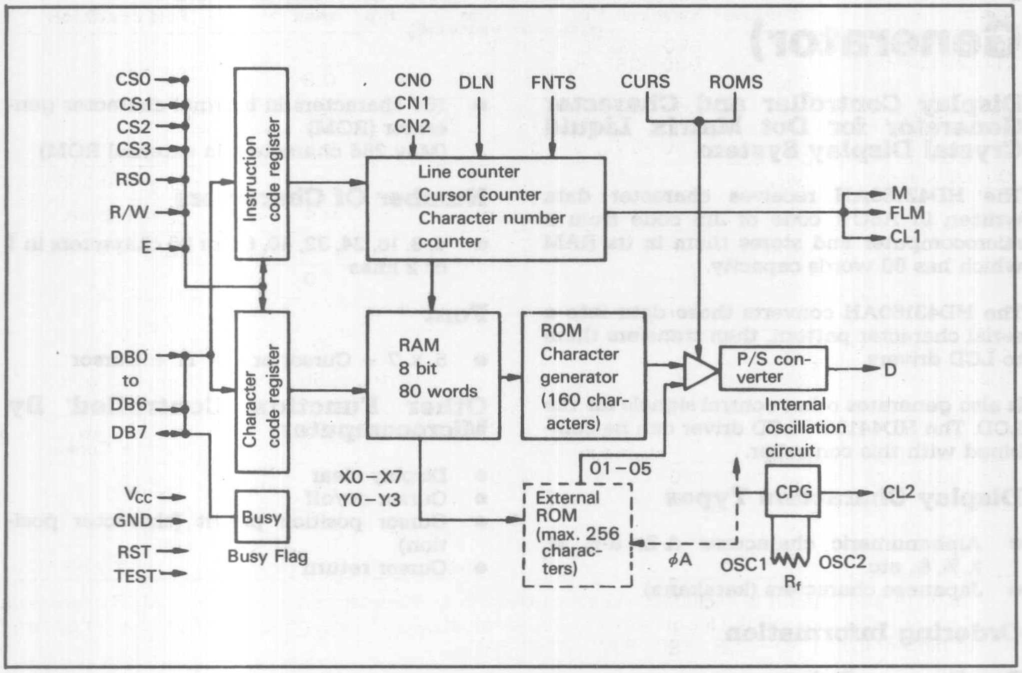
Other Function Controlled By Microcomputer

- Display clear
- Cursor on/off
- Cursor position preset (character position)
- Cursor return

Ordering Information

Type No.	Package
HD43160AH	54-pin plastic QFP (FP-54)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_T	−0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	−20 to +75	°C
Storage temperature	T_{stg}	−55 to +125	°C

Electrical Characteristics (V_{CC} = 5 V ± 5%, GND = 0 V, Ta = −20 to +75°C)

Item	Symbol	Terminal No.	min	typ	max	Unit	Test condition
Input voltage (TTL compatible)	V_{IH}	CS0—CS3, E, R/W, DB0—DB7, RS0	2.0	–	V_{CC}	V	
	V_{IL}		0	–	0.8	V	
Input voltage	V_{IHC}	OSC1, TEST, RST, FNTS, CURS, DLN, ROMS, CN0—CN2, O_1—O_5	0.7 V_{CC}	–	V_{CC}	V	
	V_{ILC}		0	–	0.3 V_{CC}	V	
Output voltage (TTL compatible)	V_{OH}	DB7	2.4	–	–	V	I_{OH} = −0.205 mA
	V_{OL}		–	–	0.4	V	I_{OL} = 1.6 mA
Output voltage	V_{OHC}	FLM, M, D, CL1, CL2,	V_{CC}−1.0	–	–	V	I_{load} = ±0.4 mA
	V_{OLC}	X0—X7, Y0—Y3	–	–	1.0	V	
Input leak current	I_{LI}	All inputs	−5	–	5	μA	
Output leak current	I_{LO}	DB7	−10	–	10	μA	
Oscillation frequency	f_{CP1}		130	192	250	kHz	R_f = 200 kΩ ±2%, 5 × 7 + Cursor
	f_{CP2}		200	288	375	kHz	R_f = 130 kΩ ±2%, 5 × 11 + Cursor
Input pull up current	I_{PL}	CS0—CS3, RS0, R/W, DB0—DB7	2	10	20	μA	V_{in} = 0V
Power dissipation	P_T	*	–	–	10	mW	Ta = 25°C, f_{CP} = 400 kHz (external clock)

* Input/output current is excluded. When an input is at the intermediate level in CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low, CS0—CS3, RS0, R/W, DB0—DB7.

Pin Arrangement

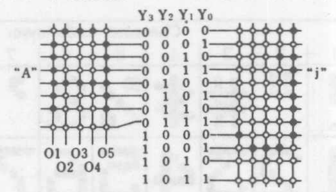
Pin No.	Power sup. OSC	Input	Output	Pin No.	Power sup. OSC	Input	Output	Pin No.	Power sup. OSC	Input	Output
1	GND (−)			19			D	37		DB3	
2			X4	20			FIM	38		DB4	
3			X3	21			ϕA	39		DB5	
4			X2	22	OSC1			40		DB6	
5			X1	23	OSC2			41		DB7	DB7
6			X0	24		RST		42		ROMS	
7			N.C.	25		TEST		43		O5	
8			N.C.	26		E		44		O4	
9			N.C.	27	V_{CC}(+)			45		O3	
10		CURS		28		R/W		46		O2	
11		FNTS		29		RS0		47		O1	
12		DLN		30		CS0		48			Y3
13		CN0		31		CS1		49			Y2
14		CN1		32		CS2		50			Y1
15		CN2		33		CS3		51			Y0
16			CL2	34		DB0		52			X7
17			CL1	35		DB1		53			X6
18			M	36		DB2		54			X5

Pin Function

Pin name	Number of terminals	Connected to	I/O	Function
V_{CC} GND	2	Power supply		+5 V ± 10% Power supply 0 V
CN0 CN1 CN2	3	GND or V_{CC}	I	Total displayed character number select

No.	4	8	16	24	32	40	64	80
CN0	GND	V_{CC}	GND	V_{CC}	GND	V_{CC}	GND	V_{CC}
CN1	GND	GND	V_{CC}	V_{CC}	GND	GND	V_{CC}	V_{CC}
CN2	GND	GND	GND	GND	V_{CC}	V_{CC}	V_{CC}	V_{CC}

Pin name	Number of terminals	Connected to	I/O	Function
CURS	1	GND or V_{CC}	I	Cursor select V_{CC}: 5 dots ●●●●● GND: 1 dot ●
DLN	1	GND or V_{CC}	I	Display line number select V_{CC}: 2 lines GND: 1 line
FNTS	1	GND or V_{CC}	I	Font select V_{CC}: 5 × 11 + Cursor GND: 5 × 7 + Cursor
RST	1	V_{CC}	I	Only for test. Normally V_{CC}.
TEST	1	GND	I	Only for test. Normally GND.
E	1	MPU	I	Strobe signal Write mode: The HD43160AH latches the data on DB0-DB7 at the falling edge of this signal Read mode: Busy/Ready signal is active on DB7 while this signal is high (Low: Ready, High: Busy)
R/W	1	MPU	I	Read/Write signal L: HD43160AH gets the data from MPU H: MPU gets the Busy/Ready signal from HD43160AH
CS0 CS1 CS2 CS3	4	MPU	I	Chip select When all of CS0—CS3 are 'H', HD43160AH is selected.
RS0	1	MPU	I	Register select HD43160AH has 2 registers. One is for character code and another is for instruction code. Each register latches the data on DB0—DB7 at the falling edge of E, when CS0—CS3 are high and R/W is low. High: Character code register is selected Low: Instruction code register is selected
DB0 to DB7	8	MPU	I I/O (DB7)	Data bus Inputs for character code and instruction code from MPU Output for Busy/Ready flag (DB7)
D	1	HD44100H	O	Serial dot data of characters for LCD drivers
CL2	1	HD44100H	O	Dot data shift signal for LCD drivers
CL1	1	HD44100H	O	Dot data latch signal for LCD drivers

Pin name	Number of terminals	Connected to	I/O	Function
M	1	HD44100H	O	Alternate signal for LCD drivers
FLM	1	HD44100H	O	Signal for common plates scanning
X0 to X7	8	ROM	O	Character code outputs for external character generator (for ext ROM) X7: MSB X0: LSB ex: character 'A' MSB … LSB 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 '1' = High '0' = Low
Y0 Y1 Y2 Y3	4	ROM	O	Character row code for external character generator 5 × 7 + Cursor 5 × 11 + Cursor 
ϕA	1	ROM	O	Clock signal for external character generator (dynamic ROM etc.) if necessary
O1 to O5	5	ROM	I	Dot data inputs from external character generator 1 (High): On 0 (Low): Off
ROMS	1	GND or V_{CC}	I	Select internal or external ROM High: External ROM Low: Internal ROM
OSC1 OSC2	2		(I) (O)	Oscillator 5 × 7 + Cursor: R_f = 200 kΩ (typ) 5 × 11 + Cursor: R_f = 130 kΩ (typ)
NC	3			Don't connect any signal to these terminals

Character Dot Patterns

5 × 7

The bottom lines of the English small characters "g, i, p, q, y," are on the cursor line (Figure 1).

5 × 11

Only the English small character "g, j, p, q, y," are displayed as below. The others are the same as for 5 × 7 (Figure 2).

Cursor 5 dots : ●●●●●
1 dot : ●

The cursor is displayed on the 8th or 12th line.

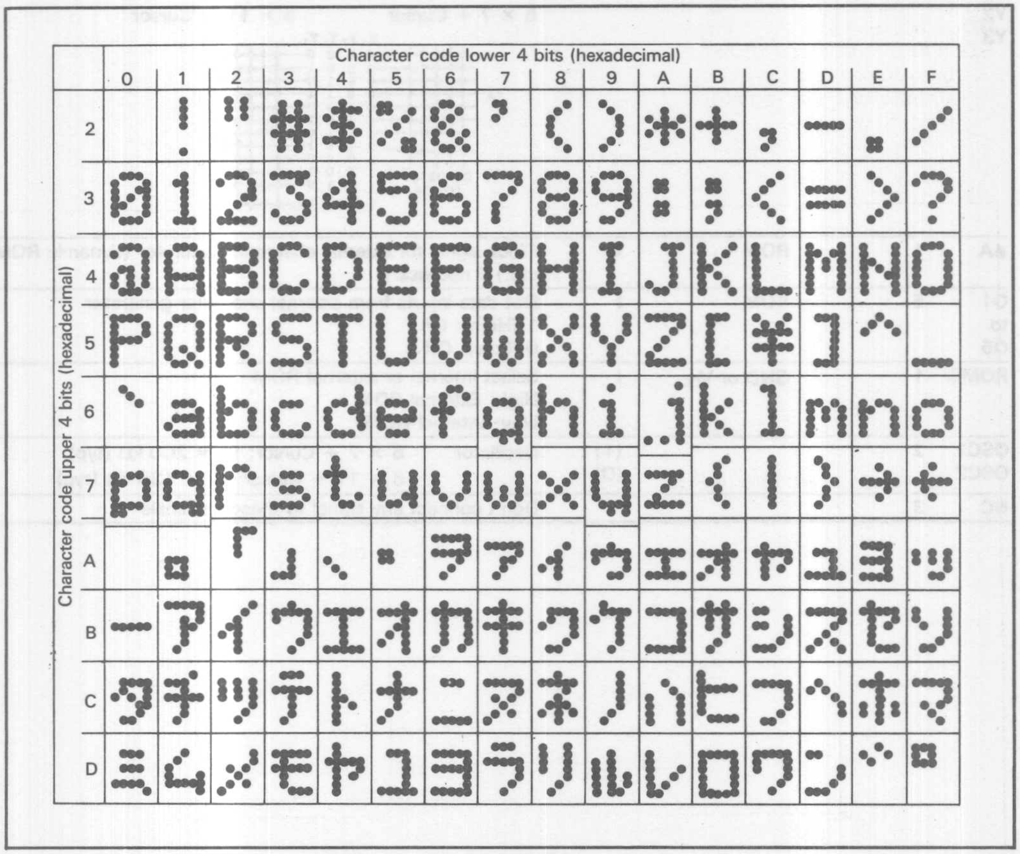


Figure 1 5 × 7 Characters

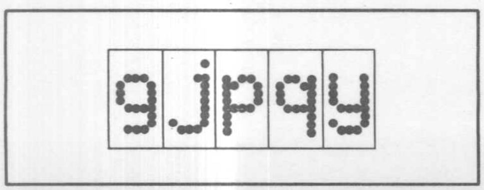


Figure 2 Special 5 × 11 Characters

Application

Setting Up

1. Total character number: CNO—CN2
2. Cursor pattern: CURS
3. Display line number: DLN
4. Font: FNTS

These terminals should be connected to V_{CC} or GND according to the LCD display system. RST and TEST should be connected to V_{CC} and GND respectively.

Interface to the Controller

1. Example 1 Interface to HD6800

In this example (Figure 3), the addresses of HD43160AH in the address area of the HD6800 microcomputer are:

Instruction code register	#'E***'	(R/W=0)
Character code register	#'F***'	(R/W=0)
Busy flag	#'E***' or #'F***'	(R/W=1)

*: don't care
#'': hexadecimal

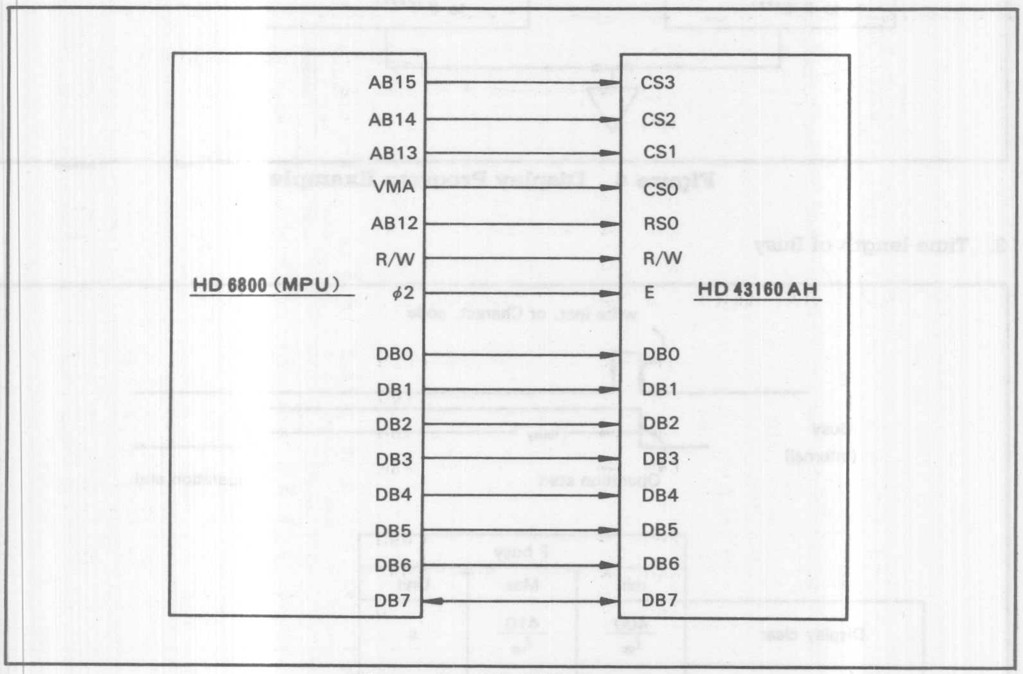


Figure 3 HD6800 Interface

2. Example of display program

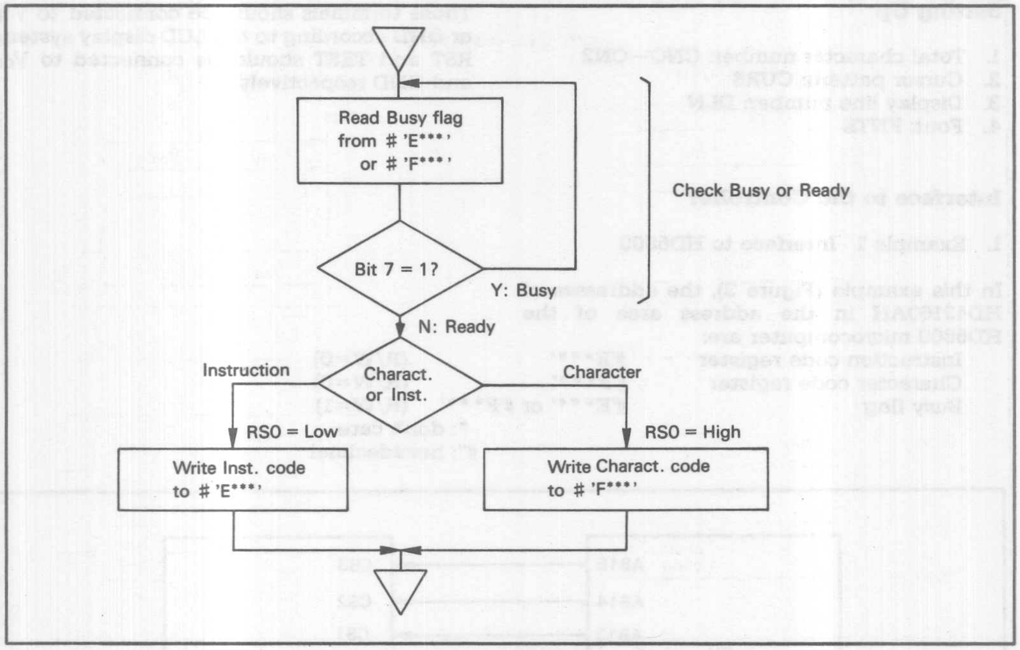
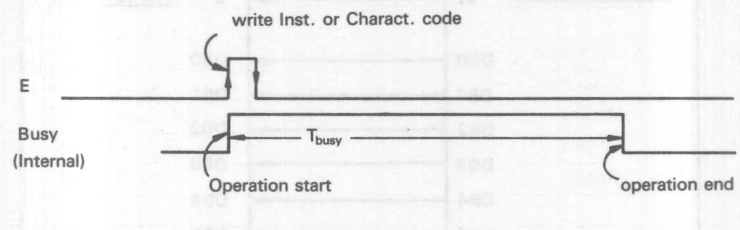


Figure 4 Display Program Example

3. Time length of Busy



	T busy		
	min	Max	Unit
Display clear	$\frac{400}{f_{cp}}$	$\frac{410}{f_{cp}}$	s
Other function	$\frac{10}{f_{cp}}$	$\frac{20}{f_{cp}}$	s

Figure 5 Busy timing

HD43160AH begins the operation from the rising edge of E (Figure 5). Instruction code register and character code register latch the data on DB0—DB7 at the falling edge of E.

4. Timing chart

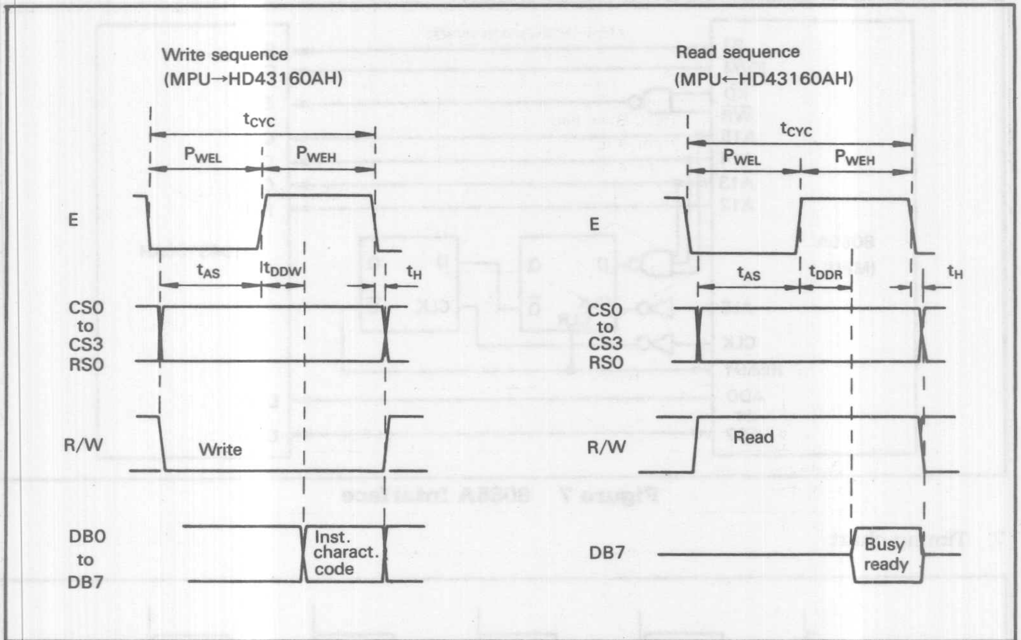


Figure 6 HD6800 Interface Timing

5. Timing characteristics

Item		Symbol	Min	Typ	Max	Unit
Cycle time of E		t_{cyc}	1.0	–	–	μs
Pulse width of E	High level	P_{WEH}	0.45	–	25	μs
	Low level	P_{WEL}	0.45	–	–	μs
Set up time of CS	Write	t_{AS}	140	–	–	ns
Data delay time	Write	t_{DDW}	–	–	225	ns
	Read	t_{DDR}	–	–	300	ns
Hold time		t_H	10	–	–	ns

6. Example 2 Interface to 8085A (Intel)

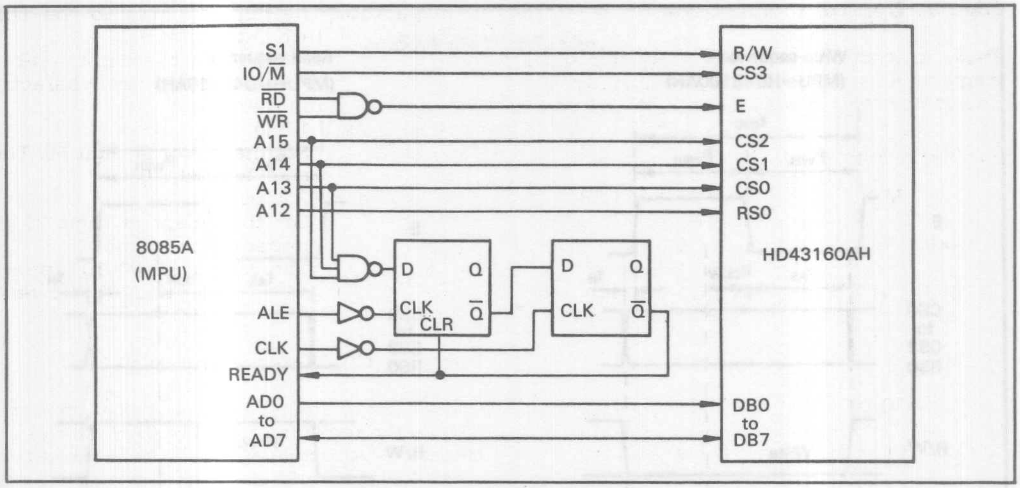


Figure 7 8085A Interface

7. Timing chart

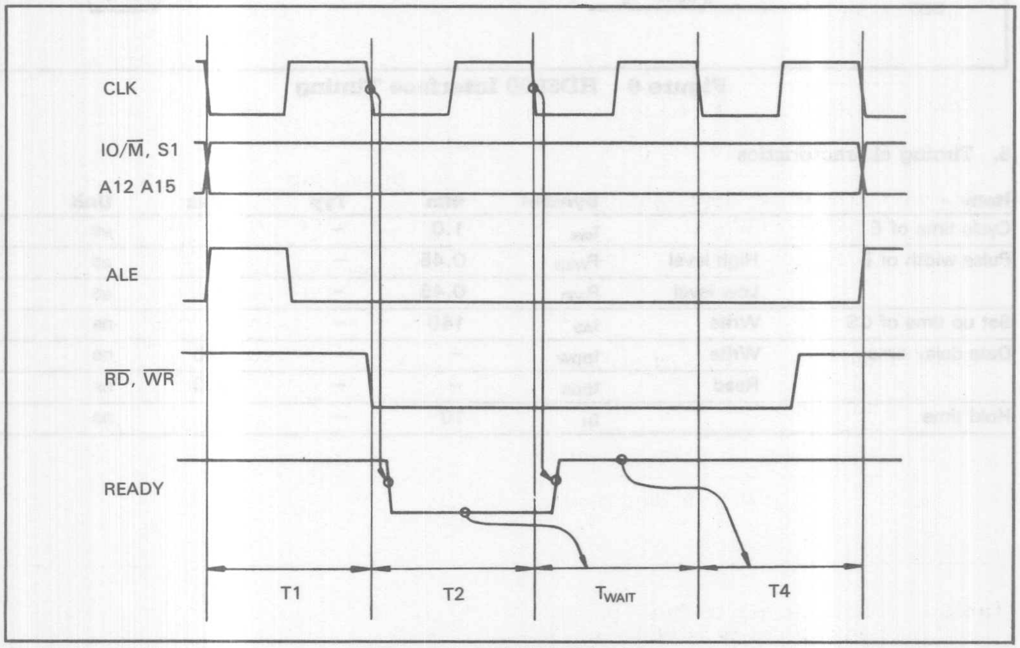


Figure 8 8085A Timing

Pulse widths of $\overline{RD}$ and $\overline{WR}$ signals of the 8085A are 400 ns min, while the pulse width of the E signal of the HD43160AH is 450 ns min (Figure 8).

Therefore, in this example, $\overline{RD}$ and $\overline{WR}$ signal pulse widths are widened by the T_{WAIT} cycle.

Display Commands

Display Control Instructions

These instructions should be written into the instruction register of HD43160AH by the microcomputer. (RS0 = Low, R/W = Low)

1. Display clear

MSB — LSB

Code:								
	0	0	0	0	0	0	0	1

Operation: The screen is cleared and the cursor returns to the 1st digit.

2. Cursor return

MSB — LSB

Code:								
	0	0	0	0	0	0	1	0

Operation: The cursor returns to the 1st digit and the characters being displayed do not change.

3. Cursor on/off

MSB — LSB

Code:									
	0	0	0	0	0	1	0	0	(On)
	0	0	0	0	0	1	0	1	(Off)

Operation: The cursor appears (on) or disappears (off).

4. Set cursor position

MSB — LSB

Code:				
1 line		1		(N − 1) binary
2 lines	upper	1	0	(n − 1) binary
	lower	1	1	(m − 1) binary

N, n, m: digit number

Operation: The cursor moves to the Nth (nth, mth) digit.
N ≦ the total character number
n, m ≦ 1/2 total character number

ex 1: 1 line
Set the cursor at digit 55. The code is 10110110.

ex 2: 2 lines
Set the cursor at digit 35 of upper or lower line.
The code is 10100010 (upper).
11100010 (lower).

Display Character Command

When the character code is written into the character register of HD43160AH, the character with thiscode appears where the cursor wasdisplayed and the cursor moves to the next digit. (RS0 = High, R/W = Low)

MSB — LSB

code: (Character code)

ex. 1

before	ABCD_
after	ABCDE_

Read Busy Flag

When CS0—CS3 = High, R/W = High and E = High (RS0 = 'don't care'), the Busy/Ready signal appears on DB7.

DB 7 High: Busy
Low: Ready

Table 1 Time Length of Busy (oscillation frequency = 200 kHz)

	Min	Max	Unit
Display clear	2.0	2.05	ms
Other operations	50	100	μs

(depends on the operating frequency)

Interface to External ROM

1. Example

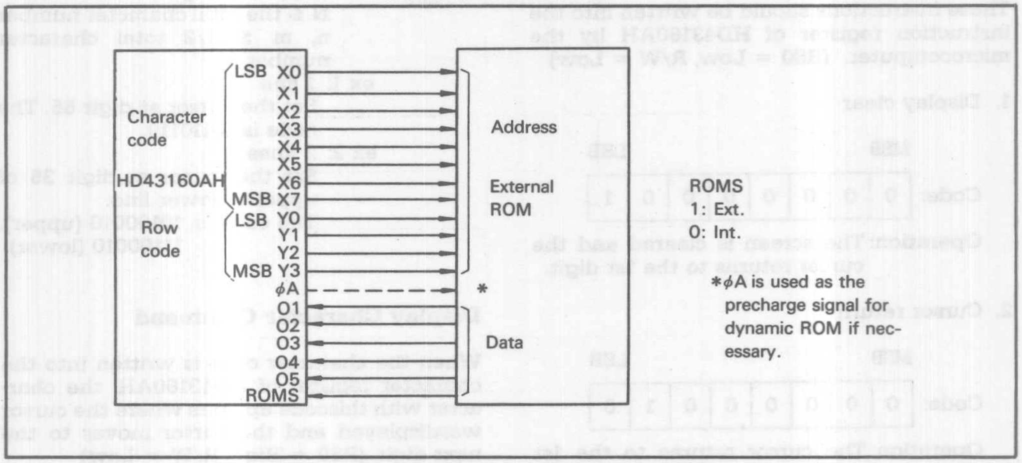


Figure 9 Interface to External ROM

2. Row code

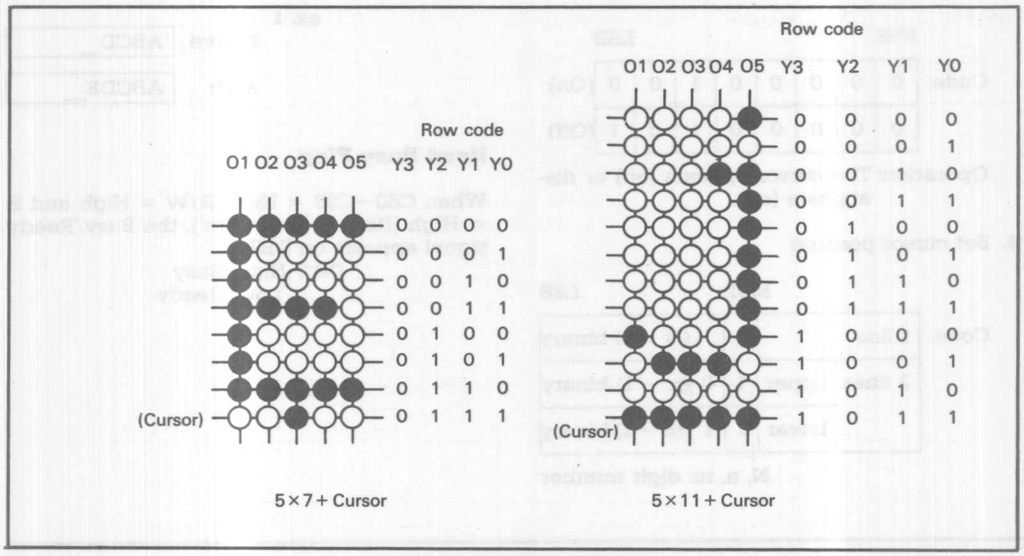


Figure 10 Row Code

3. Timing chart

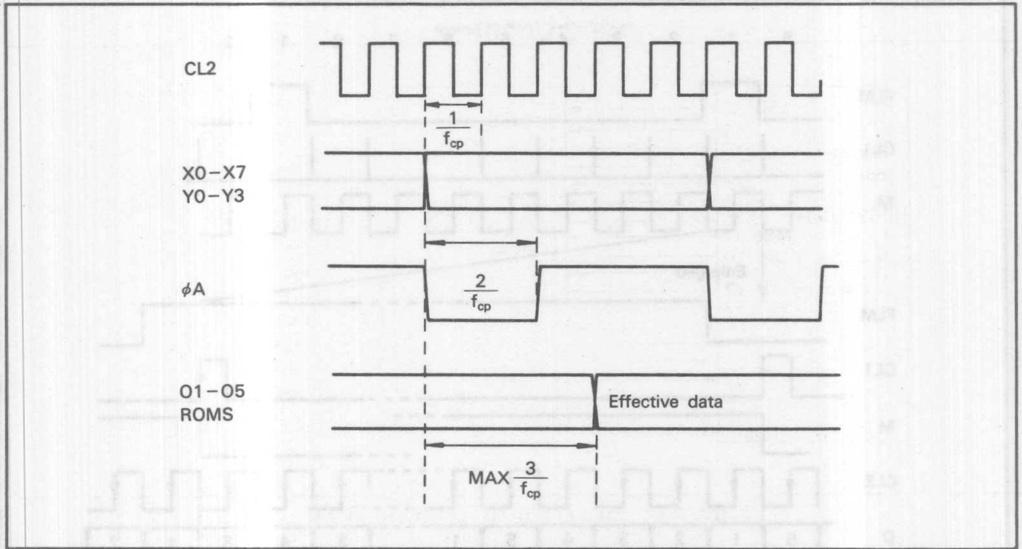


Figure 11 Display Timing

Interface to LCD Drivers

1. Example

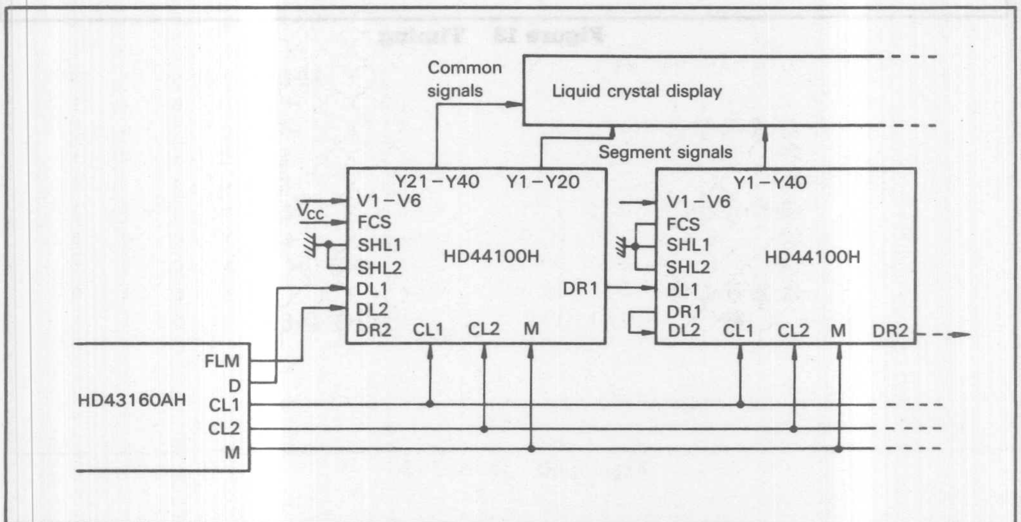


Figure 12 Interface to HD44100H

2. Waveforms (5 × 7 + Cursor 1 line)

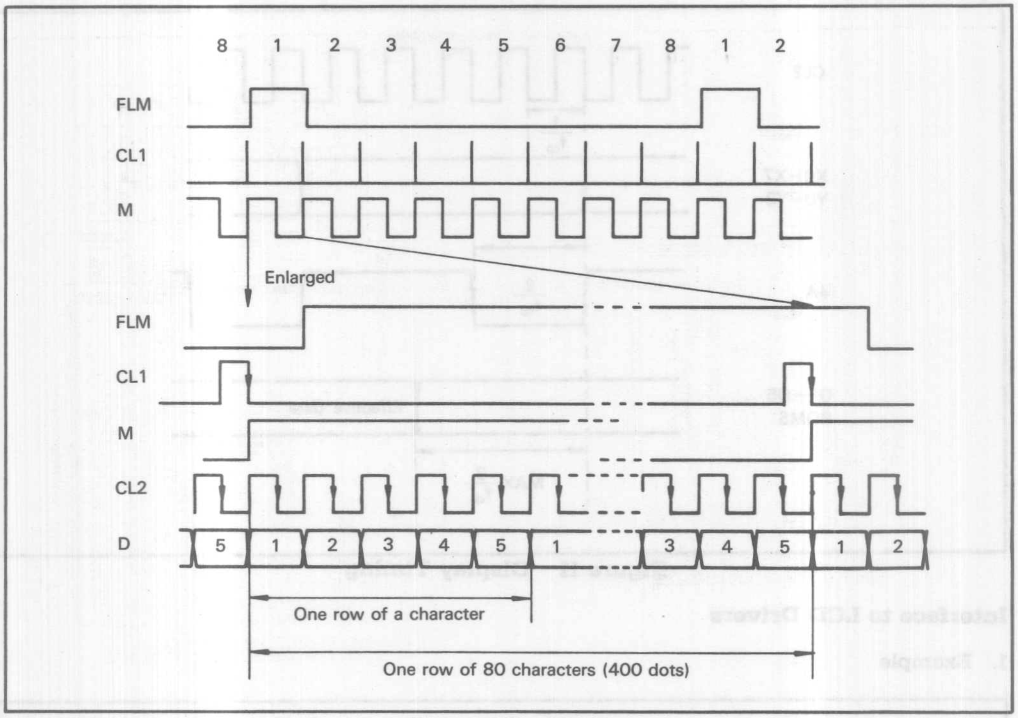


Figure 13 Timing

Dot Matrix Liquid Crystal Display System

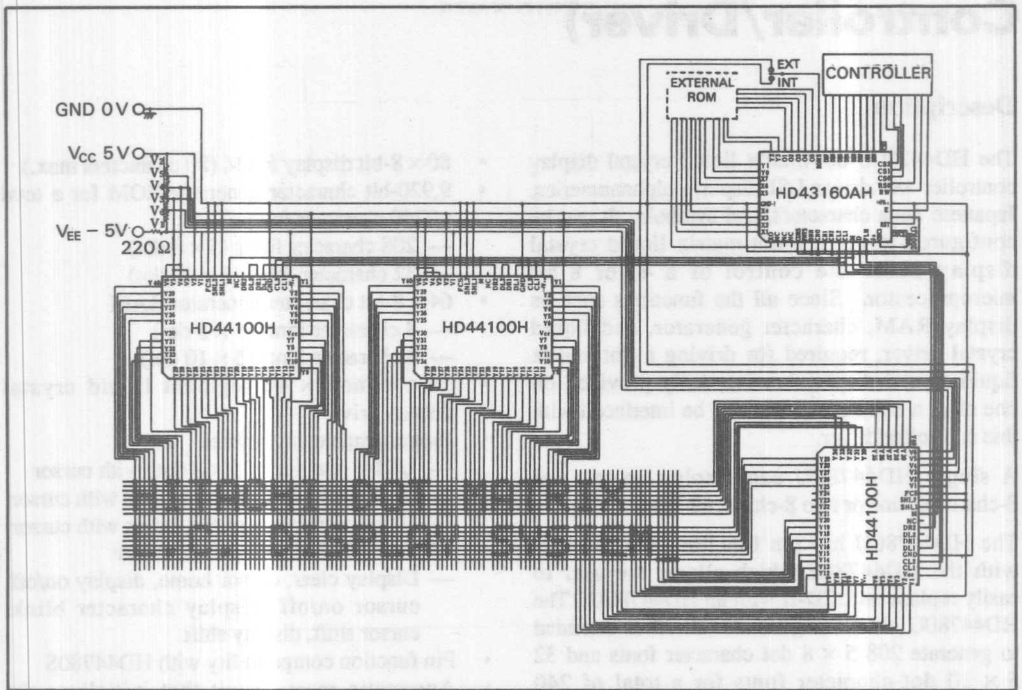


Figure 14 Typical Application 5 × 7 + Cursor, 2 Lines, 40 Characters

HD44780U (LCD-II)

(Dot Matrix Liquid Crystal Display Controller/Driver)

Description

The HD44780U dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

A single HD44780U can display up to one 8-character line or two 8-character lines.

The HD44780U has pin function compatibility with the HD44780S which allows the user to easily replace an LCD-II with an HD44780U. The HD44780U character generator ROM is extended to generate 208 5 × 8 dot character fonts and 32 5 × 10 dot character fonts for a total of 240 different character fonts.

The low power supply (2.7 V to 5.5 V) of the HD44780U is suitable for any portable battery-driven product requiring low power dissipation.

Features

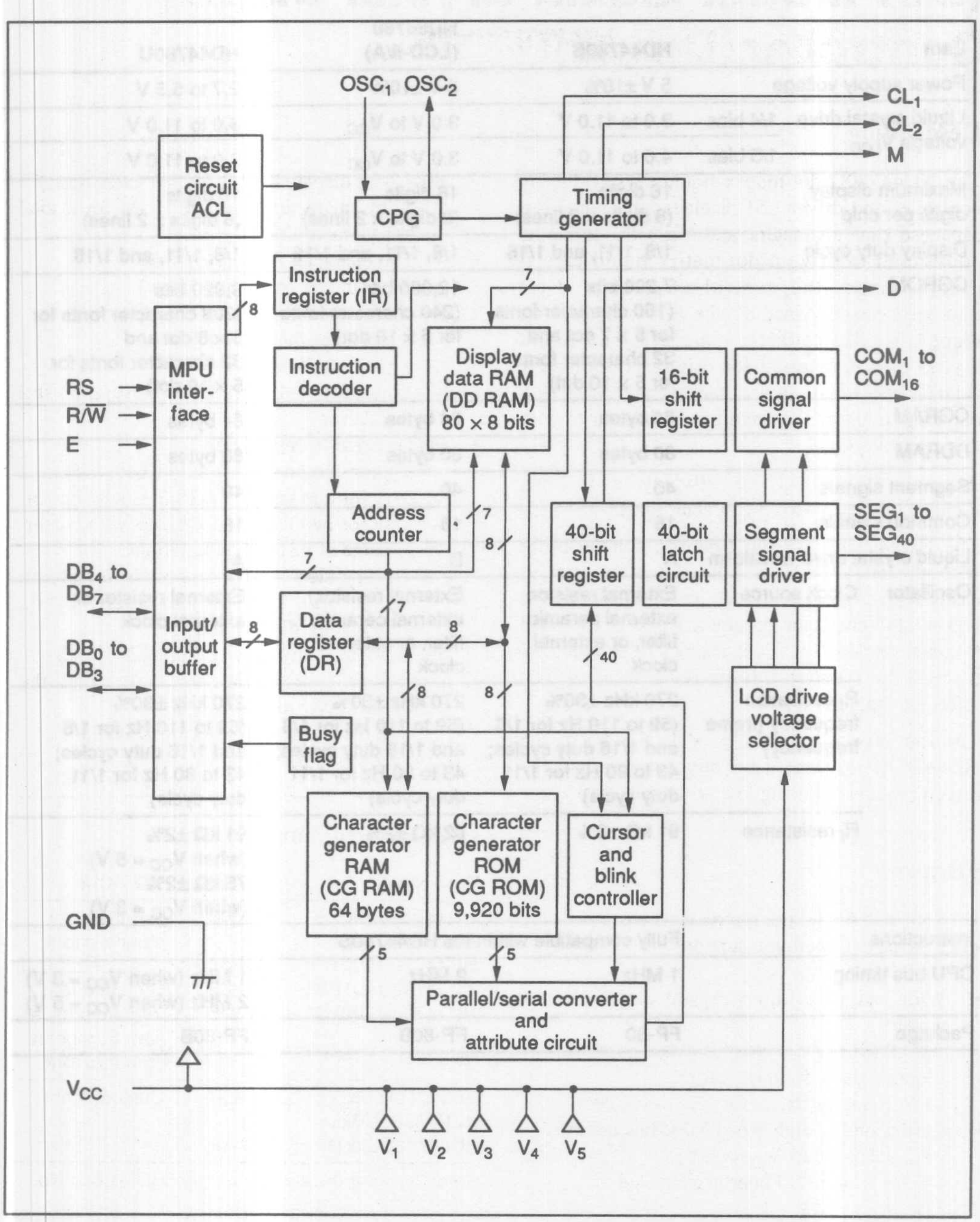
- 5 × 8 and 5 × 10 dot matrix possible
- Low power operation support:
  - — 2.7 to 5.5 V
- Wide range of liquid crystal display driver power
  - — 3.0 to 11 V
- Liquid crystal drive waveform
  - — A (One line frequency AC waveform)
- Correspond to high speed MPU bus interface
  - — 2 MHz (when V_{CC} = 5 V)
- 4-bit or 8-bit MPU interface enabled
- 80 × 8-bit display RAM (80 characters max.)
- 9,920-bit character generator ROM for a total of 240 character fonts
  - — 208 character fonts (5 × 8 dot)
  - — 32 character fonts (5 × 10 dot)
- 64 × 8-bit character generator RAM
  - — 8 character fonts (5 × 8 dot)
  - — 4 character fonts (5 × 10 dot)
- 16-common × 40-segment liquid crystal display driver
- Programmable duty cycles
  - — 1/8 for one line of 5 × 8 dots with cursor
  - — 1/11 for one line of 5 × 10 dots with cursor
  - — 1/16 for two lines of 5 × 8 dots with cursor
- Wide range of instruction functions:
  - — Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Pin function compatibility with HD44780S
- Automatic reset circuit that initializes the controller/driver after power on
- Internal oscillator with external resistors
- Low power consumption

Ordering Information

Type No.	Package	CG ROM
HD44780UA00FS	FP-80B	Japanese standard font
HCD44780UA00	Chip	
HD44780UA00TF*	TFP-80	
HD44780UA01FS*	FP-80B	Standard font for communication, European standard font
HD44780UA02FS*	FP-80B	
HD44780UBxxFS	FP-80B	Custom font
HCD44780UBxx	Chip	
HD44780UBxxTF	TFP-80	

Note: * Under development xx: ROM code No.

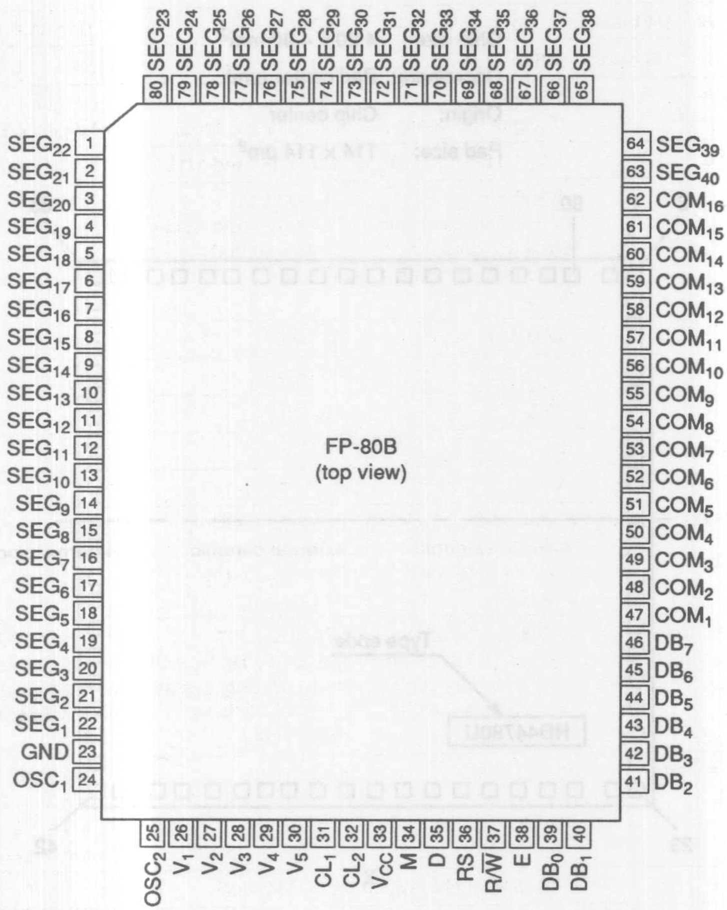
HD44780U Block Diagram



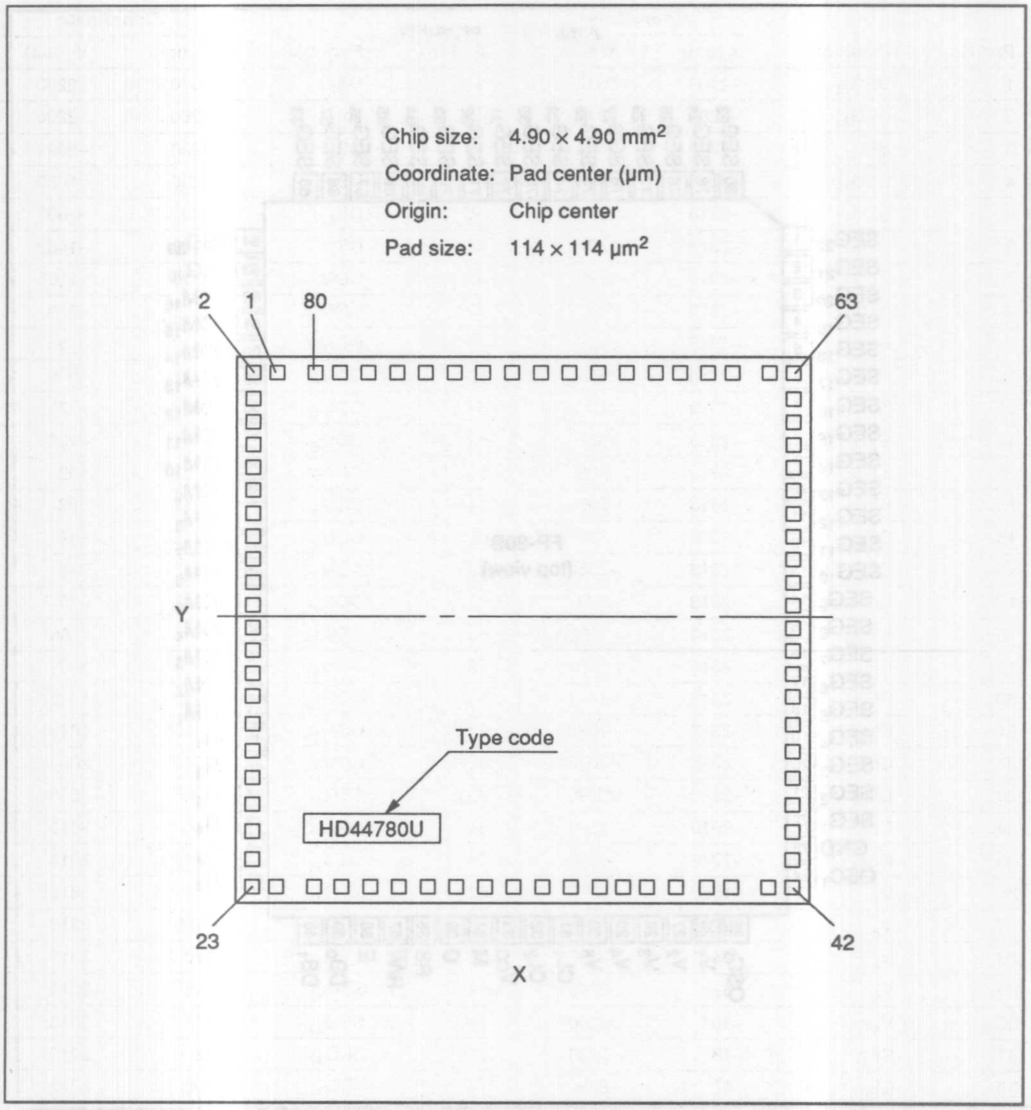
LCD-II Family Comparison

Item		HD44780S	HD66780 (LCD-II/A)	HD44780U
Power supply voltage		5 V ±10%	5 V ±10%	2.7 to 5.5 V
Liquid crystal drive voltage V_{LCD}	1/4 bias	3.0 to 11.0 V	3.0 V to V_{CC}	3.0 to 11.0 V
	1/5 bias	4.6 to 11.0 V	3.0 V to V_{CC}	3.0 to 11.0 V
Maximum display digits per chip		16 digits (8 digits × 2 lines)	16 digits (8 digits × 2 lines)	16 digits (8 digits × 2 lines)
Display duty cycle		1/8, 1/11, and 1/16	1/8, 1/11, and 1/16	1/8, 1/11, and 1/16
CGROM		7,200 bits (160 character fonts for 5 × 7 dot and 32 character fonts for 5 × 10 dot)	12,000 bits (240 character fonts for 5 × 10 dot)	9,920 bits (208 character fonts for 5 × 8 dot and 32 character fonts for 5 × 10 dot)
CGRAM		64 bytes	64 bytes	64 bytes
DDRAM		80 bytes	80 bytes	80 bytes
Segment signals		40	40	40
Common signals		16	16	16
Liquid crystal drive waveform		A	B	A
Oscillator	Clock source	External resistor, external ceramic filter, or external clock	External resistor, external ceramic filter, or external clock	External resistor or external clock
	R_f oscillation frequency (frame frequency)	270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)
	R_f resistance	91 kΩ ±2%	82 kΩ ±2%	91 kΩ ±2% (when V_{CC} = 5 V) 75 kΩ ±2% (when V_{CC} = 3 V)
Instructions		Fully compatible within the HD44780S		
CPU bus timing		1 MHz	2 MHz	1 MHz (when V_{CC} = 3 V) 2 MHz (when V_{CC} = 5 V)
Package		FP-80	FP-80B	FP-80B

HD44780U Pin Arrangement



HD44780U Pad Arrangement



HCD44780U Pad Location Coordinates

Pad No.	Function	Coordinate X (um)	Coordinate Y (um)	Pad No.	Function	Coordinate X (um)	Coordinate Y (um)
1	SEG$_{22}$	–2100	2313	41	DB$_2$	2070	–2290
2	SEG$_{21}$	–2280	2313	42	DB$_3$	2260	–2290
3	SEG$_{20}$	–2313	2089	43	DB$_4$	2290	–2099
4	SEG$_{19}$	–2313	1833	44	DB$_5$	2290	–1883
5	SEG$_{18}$	–2313	1617	45	DB$_6$	2290	–1667
6	SEG$_{17}$	–2313	1401	46	DB$_7$	2290	–1452
7	SEG$_{16}$	–2313	1186	47	COM$_1$	2313	–1186
8	SEG$_{15}$	–2313	970	48	COM$_2$	2313	–970
9	SEG$_{14}$	–2313	755	49	COM$_3$	2313	–755
10	SEG$_{13}$	–2313	539	50	COM$_4$	2313	–539
11	SEG$_{12}$	–2313	323	51	COM$_5$	2313	–323
12	SEG$_{11}$	–2313	108	52	COM$_6$	2313	–108
13	SEG$_{10}$	–2313	–108	53	COM$_7$	2313	108
14	SEG$_9$	–2313	–323	54	COM$_8$	2313	323
15	SEG$_8$	–2313	–539	55	COM$_9$	2313	539
16	SEG$_7$	–2313	–755	56	COM$_{10}$	2313	755
17	SEG$_6$	–2313	–970	57	COM$_{11}$	2313	970
18	SEG$_5$	–2313	–1186	58	COM$_{12}$	2313	1186
19	SEG$_4$	–2313	–1401	59	COM$_{13}$	2313	1401
20	SEG$_3$	–2313	–1617	60	COM$_{14}$	2313	1617
21	SEG$_2$	–2313	–1833	61	COM$_{15}$	2313	1833
22	SEG$_1$	–2313	–2073	62	COM$_{16}$	2313	2095
23	GND	–2280	–2290	63	SEG$_{40}$	2296	2313
24	OSC$_1$	–2080	–2290	64	SEG$_{39}$	2100	2313
25	OSC$_2$	–1749	–2290	65	SEG$_{38}$	1617	2313
26	V$_1$	–1550	–2290	66	SEG$_{37}$	1401	2313
27	V$_2$	–1268	–2290	67	SEG$_{36}$	1186	2313
28	V$_3$	–941	–2290	68	SEG$_{35}$	970	2313
29	V$_4$	–623	–2290	69	SEG$_{34}$	755	2313
30	V$_5$	–304	–2290	70	SEG$_{33}$	539	2313
31	CL$_1$	–48	–2290	71	SEG$_{32}$	323	2313
32	CL$_2$	142	–2290	72	SEG$_{31}$	108	2313
33	V$_{CC}$	309	–2290	73	SEG$_{30}$	–108	2313
34	M	475	–2290	74	SEG$_{29}$	–323	2313
35	D	665	–2290	75	SEG$_{28}$	–539	2313
36	RS	832	–2290	76	SEG$_{27}$	–755	2313
37	R/$\overline{\text{W}}$	1022	–2290	77	SEG$_{26}$	–970	2313
38	E	1204	–2290	78	SEG$_{25}$	–1186	2313
39	DB$_0$	1454	–2290	79	SEG$_{24}$	–1401	2313
40	DB$_1$	1684	–2290	80	SEG$_{23}$	–1617	2313

Pin Functions

Signal	No. of Lines	I/O	Device Interfaced with	Function
RS	1	I	MPU	Selects registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read)
R/$\overline{W}$	1	I	MPU	Selects read or write. 0: Write 1: Read
E	1	I	MPU	Starts data read/write
DB_4 to DB_7	4	I/O	MPU	Four high order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. DB_7 can be used as a busy flag.
DB_0 to DB_3	4	I/O	MPU	Four low order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. These pins are not used during 4-bit operation.
CL_1	1	O	HD44100	Clock to latch serial data D sent to the HD44100 driver
CL_2	1	O	HD44100	Clock to shift serial data D
M	1	O	HD44100	Switch signal for converting the liquid crystal drive waveform to AC
D	1	O	HD44100	Character pattern data corresponding to each segment signal
COM_1 to COM_{16}	16	O	LCD	Common signals that are not used are changed to non-selection waveforms. COM_9 to COM_{16} are non-selection waveforms at 1/8 duty factor and COM_{12} to COM_{16} are non-selection waveforms at 1/11 duty factor.
SEG_1 to SEG_{40}	40	O	LCD	Segment signals
V_1 to V_5	5	—	Power supply	Power supply for LCD drive $V_{CC} - V_5 = 11$ V (max)
V_{CC}, GND	2	—	Power supply	V_{CC}: 2.7 V to 5.5 V, GND: 0 V
OSC_1, OSC_2	2	—	Oscillation resistor clock	When crystal oscillation is performed, a resistor must be connected externally. When the pin input is an external clock, it must be input to OSC_1.

Function Description

Registers

The HD44780U has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can only be written from the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM and temporarily stores data to be read from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into DD RAM or CG RAM by an internal operation. The DR is also used for data storage when reading data from DD RAM or CG RAM. When address information is written into the IR, data is read and then stored into the DR from DD RAM or CG RAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. By the register selector (RS) signal, these two registers can be selected (table 1).

Busy Flag (BF)

When the busy flag is 1, the HD44780U is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/$\overline{W}$ = 1 (table 1), the busy flag is output to DB_7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to both DD RAM and CG RAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of either DD RAM or CG RAM is also determined concurrently by the instruction.

After writing into (reading from) DD RAM or CG RAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB_0 to DB_6 when RS = 0 and R/$\overline{W}$ = 1 (table 1).

Table 1 Register Selection

RS	R/$\overline{W}$	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0 to DB_6)
1	0	DR write as an internal operation (DR to DD RAM or CG RAM)
1	1	DR read as an internal operation (DD RAM or CG RAM to DR)

Display Data RAM (DD RAM)

Display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its extended capacity is 80×8 bits, or 80 characters. The area in display data RAM (DD RAM) that is not used for display can be used as general data RAM. See figure 1 for the relationships between DD RAM addresses and positions on the liquid crystal display.

The DD RAM address (A_{DD}) is set in the address counter (AC) as hexadecimal.

- 1-line display (N = 0) (figure 2)
  - — Case 1: When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the HD44780, 8 characters are displayed. See figure 3.

    When the display shift operation is performed, the DD RAM address shifts. See figure 3.
  - — Case 2: For a 16-character display, the HD44780 can be extended using one HD44100 and displayed. See figure 4.

    When the display shift operation is performed, the DD RAM address shifts. See figure 4.
  - — Case 3: The relationship between the display position and DD RAM address when the number of display digits is increased through the use of two or more HD44100s can be considered as an extension of case #2.

    Since the increase can be eight digits per additional HD44100, up to 80 digits can be displayed by externally connecting nine HD44100s. See figure 5.

	High order bits			Low order bits			
AC (hexadecimal)	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Example: DD RAM address 4E

1	0	0	1	1	1	0

Figure 1 DD RAM Address

Display position (digit)	1	2	3	4	5		79	80
DD RAM address (hexadecimal)	00	01	02	03	04	....	4E	4F

Figure 2 1-Line Display

Display position	1	2	3	4	5	6	7	8
DD RAM address	00	01	02	03	04	05	06	07
For shift left	01	02	03	04	05	06	07	08
For shift right	4F	00	01	02	03	04	05	06

Figure 3 1-Line by 8-Character Display Example

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
	HD44780 display								HD44100 display							
For shift left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
For shift right	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E

Figure 4 1-Line by 16-Character Display Example

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		73	74	75	76	77	78	79	80
DD RAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	....	48	49	4A	4B	4C	4D	4E	4F
	HD44780 display								1st HD44100 display								2nd to 8th HD44100 display					9th HD44100 display							

Figure 5 1-Line by 80-Character Display Example

- 2-line display (N = 1) (figure 6)

  Case 1: When the number of display characters is less than 40 × 2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the HD44780 is used, 8 characters × 2 lines are displayed. See figure 7.

  When display shift operation is performed, the DD RAM address shifts. See figure 7.

Display position	1	2	3	4	5		39	40
DD RAM address (hexadecimal)	00	01	02	03	04	....	26	27
	40	41	42	43	44	....	66	67

Figure 6 2-Line Display

Display position	1	2	3	4	5	6	7	8
DD RAM address	00	01	02	03	04	05	06	07
	40	41	42	43	44	45	46	47
For shift left	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48
For shift right	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

Figure 7 2-Line by 8-Character Display Example

— Case 2: For a 16-character × 2-line display, the HD44780 can be extended using one HD44100. See figure 8.

When display shift operation is performed, the DD RAM address shifts. See figure 8.

— Case 3: The relationship between the display position and DD RAM address when the number of display digits is increased by using one HD44780U and two or more HD44100s, can be considered as an extension of case #2. See figure 9.

Since the increase can be 8 digits × 2 lines for each additional HD44100, up to 40 digits × 2 lines can be displayed by externally connecting four HD44100s.

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
	HD44780U display								HD44100 display							
For shift left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50
For shift right	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

Figure 8 2-Line by 16-Character Display Example

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		33	34	35	36	37	38	39	40
DD RAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	....	20	21	22	23	24	25	26	27
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	....	60	61	62	63	64	65	66	67
	HD44780U display								1st HD44100 display								2nd and 3rd HD44100 display						4th HD44100 display							

Figure 9 2-Line by 40-Character Display Example

Character Generator ROM (CG ROM)

The character generator ROM generates 5×8 dot or 5×10 dot character patterns from 8-bit character codes (table 4). It can generate 208 5×8 dot character patterns and 32 5×10 dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CG RAM)

In the character generator RAM, the user can rewrite character patterns by program. For 5×8 dots, eight character patterns can be written, and for 5×10 dots, four character patterns can be written.

Write into DD RAM the character codes at the addresses shown as the left column of table 4 to show the character patterns stored in CG RAM.

See table 5 for the relationship between CG RAM addresses and data and display patterns.

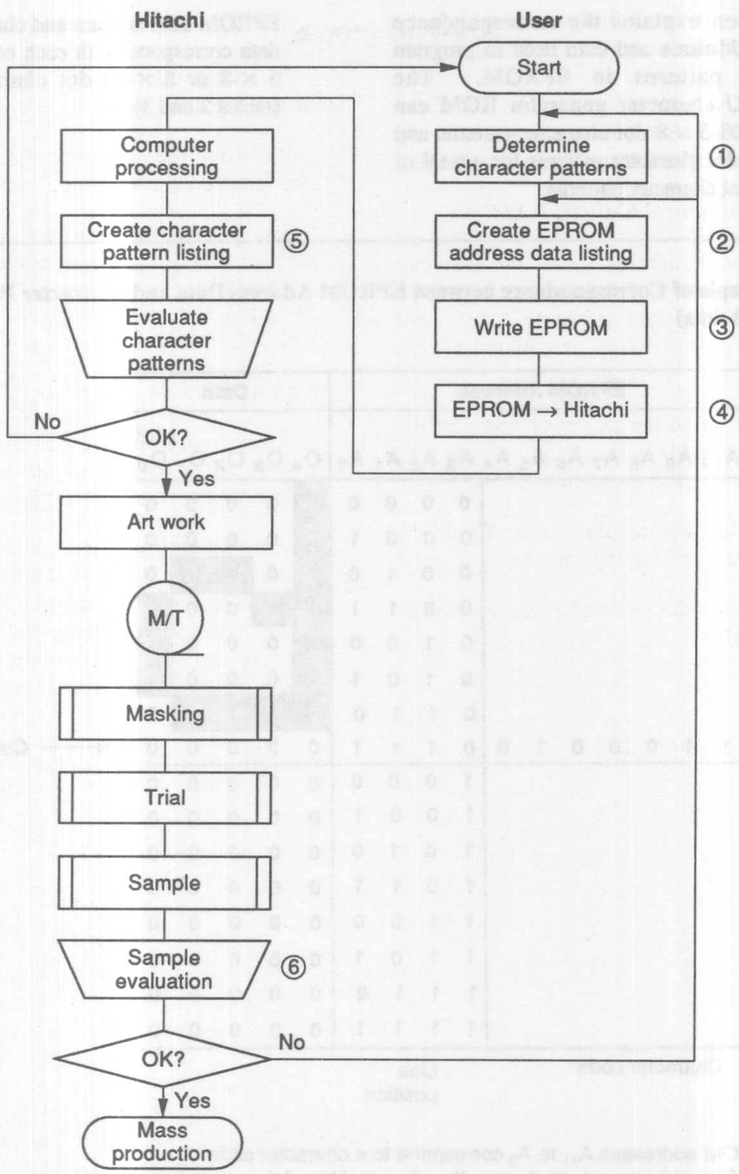
Areas that are not used for display can be used as general data RAM.

Modifying Character Patterns

- Character pattern development procedure

The following operations correspond to the numbers listed in figure 10:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into the EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing on the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI proceeds at Hitachi.



Note: For a description of the numbers used in this figure, refer to the preceding page.

Figure 10 Character Pattern Development Procedure

- Programming character patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM. The HD44780U character generator ROM can generate 208 5 × 8 dot character patterns and 32 5 × 10 dot character patterns for a total of 240 different character patterns.

— Character patterns

EPROM address data and character pattern data correspond with each other to form a 5 × 8 or 5 × 10 dot character pattern (tables 2 and 3).

Table 2 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 8 dots)

EPROM Address												Data					
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0 (LSB)	
								0	0	0	0	1	0	0	0	0	
								0	0	0	1	1	0	0	0	0	
								0	0	1	0	1	0	1	1	0	
								0	0	1	1	1	1	0	0	1	
								0	1	0	0	1	0	0	0	1	
								0	1	0	1	1	0	0	0	1	
								0	1	1	0	1	1	1	1	0	
0	1	1	0	0	0	1	0	0	1	1	1	0	0	0	0	0	← Cursor position
								1	0	0	0	0	0	0	0	0	
								1	0	0	1	0	0	0	0	0	
								1	0	1	0	0	0	0	0	0	
								1	0	1	1	0	0	0	0	0	
								1	1	0	0	0	0	0	0	0	
								1	1	0	1	0	0	0	0	0	
								1	1	1	0	0	0	0	0	0	
								1	1	1	1	0	0	0	0	0	

Character code (A_{11}–A_4) Line position (A_3–A_0)

Notes:
1. EPROM addresses A_{11} to A_3 correspond to a character code.
2. EPROM addresses A_3 to A_0 specify a line position of the character pattern.
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. EPROM data O_5 to O_7 must be specified as 0.
5. A lit display position (black) corresponds to a 1.
6. Line 9 and the following lines must be blanked with 0s for a 5 x 8 dot character fonts.

— Handling unused character patterns

1. **EPROM data outside the character pattern area:** Always input 0s.
2. **EPROM data in CG RAM area:** Always input 0s. (Input 0s to EPROM addresses 00H to FFH.)
3. **EPROM data used when the user does not use any HD44780U character pattern:** According to the user application, handled in one of the two ways listed as follows.

i. **When unused character patterns are not programmed:** If an unused character code is written into DD RAM, all its dots are lit. By not programing a character pattern, all of its bits become lit. (This is due to the EPROM being filled with 1s after it is erased.)

ii. **When unused character patterns are programmed as 0s:** Nothing is displayed even if unused character codes are written into DD RAM. (This is equivalent to a space.)

Table 3 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 10 dots)

EPROM Address												Data					
																LSB	
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0	
								0	0	0	0	0	0	0	0	0	
								0	0	0	1	0	0	0	0	0	
								0	0	1	0	0	1	1	0	1	
								0	0	1	1	1	0	0	1	1	
								0	1	0	0	1	0	0	0	1	
								0	1	0	1	1	0	0	0	1	
								0	1	1	0	0	1	1	1	1	
0	1	0	1	0	0	1	0	0	1	1	1	0	0	0	0	1	
								1	0	0	0	0	0	0	0	1	
								1	0	0	1	0	0	0	0	1	
								1	0	1	0	0	0	0	0	0	← Cursor position
								1	0	1	1	0	0	0	0	0	
								1	1	0	0	0	0	0	0	0	
								1	1	0	1	0	0	0	0	0	
								1	1	1	0	0	0	0	0	0	
								1	1	1	1	0	0	0	0	0	
Character code								Line position									

Notes: 1. EPROM addresses A_{11} to A_3 correspond to a character code.
2. EPROM addresses A_3 to A_0 specify a line position of the character pattern.
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. EPROM data O_5 to O_7 must be specified as 0.
5. A lit display position (black) corresponds to a 1.
6. Line 11 and the following lines must be blanked with 0s for a 5 x 10 dot character fonts.

Table 4 Correspondence between Character Codes and Character Patterns (ROM code: A00)

Lower 4 Bits \ Upper 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)			0	@	P	`	p				ー	タ	ミ	α	p
xxxx0001	(2)		!	1	A	Q	a	q			。	ア	チ	ム	ä	q
xxxx0010	(3)		"	2	B	R	b	r			「	イ	ツ	メ	β	θ
xxxx0011	(4)		#	3	C	S	c	s			」	ウ	テ	モ	ε	∞
xxxx0100	(5)		$	4	D	T	d	t			、	エ	ト	ヤ	μ	Ω
xxxx0101	(6)		%	5	E	U	e	u			・	オ	ナ	ユ	σ	ü
xxxx0110	(7)		&	6	F	V	f	v			ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	(8)		'	7	G	W	g	w			ァ	キ	ヌ	ラ	g	π
xxxx1000	(1)		(	8	H	X	h	x			ィ	ク	ネ	リ	√	x̄
xxxx1001	(2)		)	9	I	Y	i	y			ゥ	ケ	ノ	ル	⁻¹	y
xxxx1010	(3)		*	:	J	Z	j	z			ェ	コ	ハ	レ	j	千
xxxx1011	(4)		+	;	K	[	k	{			ォ	サ	ヒ	ロ	ˣ	万
xxxx1100	(5)		,	<	L	¥	l	|			ャ	シ	フ	ワ	¢	円
xxxx1101	(6)		-	=	M	]	m	}			ュ	ス	ヘ	ン	£	÷
xxxx1110	(7)		.	>	N	^	n	→			ョ	セ	ホ	゛	ñ	
xxxx1111	(8)		/	?	O	_	o	←			ッ	ソ	マ	゜	ö	█

Note: The user can specify any pattern for character-generator RAM.

Table 4 Correspondence between Character Codes and Character Patterns (ROM code: A01)

Lower 4 Bits \ Upper 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)	á		0	@	P	`	p	Ç	É	[illegible]	ー	タ	ミ	月	ダ
xxxx0001	(2)	í	!	1	A	Q	a	q	ü	æ	。	ア	チ	ム	日	ヂ
xxxx0010	(3)	ó	"	2	B	R	b	r	é	Æ	「	イ	ツ	×	分	ヅ
xxxx0011	(4)	ú	#	3	C	S	c	s	â	ô	」	ウ	テ	モ	円	デ
xxxx0100	(5)	ñ	$	4	D	T	d	t	ä	ö	、	エ	ト	ヤ	中	ド
xxxx0101	(6)	Ñ	%	5	E	U	e	u	à	ò	・	オ	ナ	ユ	回	バ
xxxx0110	(7)	ª	&	6	F	V	f	v	å	û	ヲ	カ	ニ	ヨ	ガ	ピ
xxxx0111	(8)	º	'	7	G	W	g	w	ç	ù	ァ	キ	ヌ	ラ	ギ	ブ
xxxx1000	(1)	¿	(	8	H	X	h	x	ê	ÿ	ィ	ク	ネ	リ	グ	ベ
xxxx1001	(2)	ß	)	9	I	Y	i	y	ë	Ö	ゥ	ケ	ノ	ル	ゲ	ボ
xxxx1010	(3)	[illegible]	*	:	J	Z	j	z	è	Ü	ェ	コ	ハ	レ	ゴ	パ
xxxx1011	(4)	¢	+	;	K	[	k	{	ï	±	ォ	サ	ヒ	ロ	ザ	ビ
xxxx1100	(5)	£	,	<	L	¥	l	|	î	[illegible]	ャ	シ	フ	ワ	ジ	プ
xxxx1101	(6)	¡	-	=	M	]	m	}	ì	[illegible]	ュ	ス	ヘ	ン	ズ	ペ
xxxx1110	(7)	«	.	>	N	^	n	→	Ä	[illegible]	ョ	セ	ホ	゛	ゼ	ポ
xxxx1111	(8)	»	/	?	O	_	o	←	Å	火	ッ	ソ	マ	゜	ゾ	█

Table 4 Correspondence between Character Codes and Character Patterns (ROM code: A02)

Lower 4 Bits \ Upper 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)	▶		0	@	P	`	p	Б	α	▮	°	À	Ð	à	ð
xxxx0001	(2)	◀	!	1	A	Q	a	q	Д	♪	¡	±	Á	Ñ	á	ñ
xxxx0010	(3)	“	"	2	B	R	b	r	Ж	Γ	¢	²	Â	Ò	â	ò
xxxx0011	(4)	”	#	3	C	S	c	s	З	π	£	³	Ã	Ó	ã	ó
xxxx0100	(5)	⏫	$	4	D	T	d	t	И	Σ	¤	₧	Ä	Ô	ä	ô
xxxx0101	(6)	⏬	%	5	E	U	e	u	Й	σ	¥	µ	Å	Õ	å	õ
xxxx0110	(7)	●	&	6	F	V	f	v	Л	♬	¦	¶	Æ	Ö	æ	ö
xxxx0111	(8)	↵	'	7	G	W	g	w	П	τ	§	·	Ç	×	ç	÷
xxxx1000	(1)	↑	(	8	H	X	h	x	У	🔔	ƒ	ω	È	Φ	è	φ
xxxx1001	(2)	↓	)	9	I	Y	i	y	Ц	Θ	©	¹	É	Ù	é	ù
xxxx1010	(3)	→	*	:	J	Z	j	z	Ч	Ω	ª	º	Ê	Ú	ê	ú
xxxx1011	(4)	←	+	;	K	[	k	{	Ш	δ	«	»	Ë	Û	ë	û
xxxx1100	(5)	≤	,	<	L	\	l	|	Щ	∞	Ю	¼	Ì	Ü	ì	ü
xxxx1101	(6)	≥	-	=	M	]	m	}	Ъ	♥	Я	½	Í	Ý	í	ý
xxxx1110	(7)	▲	.	>	N	^	n	~	Ы	ε	®	¾	Î	Þ	î	þ
xxxx1111	(8)	▼	/	?	O	_	o	⌂	Э	∩	‘	¿	Ï	ß	ï	ÿ

Table 5 Relationship between CG RAM Addresses, Character Codes (DD RAM) and Character Patterns (CG RAM data)

For 5 × 8 dot character patterns

Character Codes (DD RAM data)	CG RAM Address		Character Patterns (CG RAM data)		
7 6 5 4 3 2 1 0	5 4 3	2 1 0	7 6 5	4 3 2 1 0	
High Low	High	Low	High	Low	
0 0 0 0 * 0 0 0	0 0 0	0 0 0	* * *	1 1 1 1 0	Character pattern (1)
		0 0 1		1 0 0 0 1	
		0 1 0		1 0 0 0 1	
		0 1 1		1 1 1 1 0	
		1 0 0		1 0 1 0 0	
		1 0 1		1 0 0 1 0	
		1 1 0		1 0 0 0 1	
		1 1 1	* * *	0 0 0 0 0	Cursor position
0 0 0 0 * 0 0 1	0 0 1	0 0 0	* * *	1 0 0 0 1	Character pattern (2)
		0 0 1		0 1 0 1 0	
		0 1 0		1 1 1 1 1	
		0 1 1		0 0 1 0 0	
		1 0 0		1 1 1 1 1	
		1 0 1		0 0 1 0 0	
		1 1 0		0 0 1 0 0	
		1 1 1	* * *	0 0 0 0 0	Cursor position
		0 0 0	* * *		
		0 0 1			
0 0 0 0 * 1 1 1	1 1 1				
		1 0 0			
		1 0 1			
		1 1 0			
		1 1 1	* * *		

Notes: 1. Character code bits 0 to 2 correspond to CG RAM address bits 3 to 5 (3 bits: 8 types).
2. CG RAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.
Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CG RAM data bits 0 to 4 (bit 4 being at the left).
4. As shown table 5, CG RAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.
* Indicates no effect.

Table 5 Relationship between CG RAM Addresses, Character Codes (DD RAM) and Character Patterns (CG RAM data) (cont)

For 5 × 10 dot character patterns

Character Codes (DD RAM data)	CG RAM Address		Character Patterns (CG RAM data)		
7 6 5 4 3 2 1 0	5 4	3 2 1 0	7 6 5	4 3 2 1 0	
High / Low	High	Low	High	Low	
		0 0 0 0	* * *	0 0 0 0 0	Character pattern
		0 0 0 1		0 0 0 0 0	
		0 0 1 0		1 0 1 1 0	
		0 0 1 1		1 1 0 0 1	
		0 1 0 0		1 0 0 0 1	
0 0 0 0 * 0 0 *	0 0	0 1 0 1		1 0 0 0 1	
		0 1 1 0		1 1 1 1 0	
		0 1 1 1		1 0 0 0 0	
		1 0 0 0		1 0 0 0 0	
		1 0 0 1		1 0 0 0 0	
		1 0 1 0	* * *	0 0 0 0 0	Cursor position
		1 0 1 1	* * *	* * * * *	
		1 1 0 0			
		1 1 0 1			
		1 1 1 0			
		1 1 1 1	* * *	* * * * *	
		0 0 0 0	* * *		
		0 0 0 1			
0 0 0 0 * 1 1 *	1 1	1 0 0 1			
		1 0 1 0	* * *		
		1 0 1 1	* * *	* * * * *	
		1 1 0 0			
		1 1 0 1			
		1 1 1 0			
		1 1 1 1	* * *	* * * * *	

Notes: 1. Character code bits 1 and 2 correspond to CG RAM address bits 4 and 5 (2 bits: 4 types).
2. CG RAM address bits 0 to 3 designate the character pattern line position. The 11th line is the cursor position and its display is formed by a logical OR with the cursor.
Maintain the 11th line data corresponding to the cursor display positon at 0 as the cursor display.
If the 11th line data is "1", "1" bits will light up the 11th line regardless of the cursor presence.
Since lines 12 to 16 are not used for display, they can be used for general data RAM.
3. Character pattern row positions are the same as 5 × 8 dot character pattern positions.
4. CG RAM character patterns are selected when character code bits 4 to 7 are all 0.
However, since character code bits 0 and 3 have no effect, the P display example above can be selected by character codes 00H, 01H, 08H, and 09H.
5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.
* Indicates no effect.

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DD RAM, CG ROM and CG RAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DD RAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area. This circuit also generates timing signals for the operation of the externally connected HD44100 driver.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the HD44100 driver. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data then enables the driver to generate drive waveform outputs. The serial data can be sent to externally cascaded HD44100s used for displaying extended digit numbers.

Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD44780U drives from the head display. The rest of the display, corresponding to latter addresses, are added with each additional HD44100.

Cursor/Blink Control Circuit

The cursor/blink control circuit generates the cursor or character blinking. The cursor or the blinking will appear with the digit located at the display data RAM (DD RAM) address set in the address counter (AC).

For example (figure 11), when the address counter is 08H, the cursor position is displayed at DD RAM address 08H.

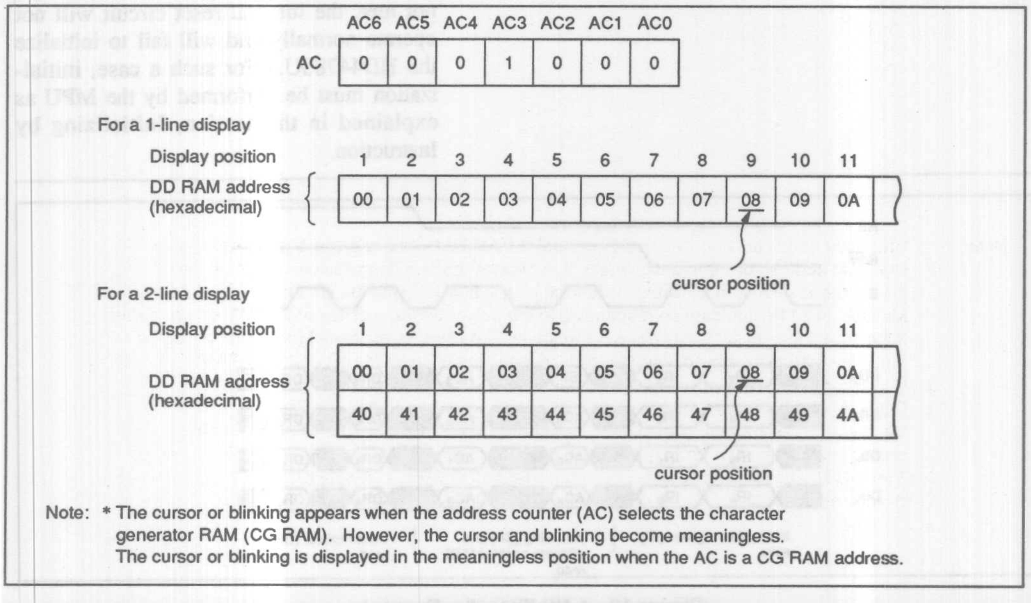


Figure 11 Cursor/Blink Display Example

Interfacing to the MPU

The HD44780U can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB_4 to DB_7) are used for transfer. Bus lines DB_0 to DB_3 are disabled. The data transfer between the HD44780U and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB_4 to DB_7) are transferred before the four low order bits (for 8-bit operation, DB_0 to DB_3).

  The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

- For 8-bit interface data, all eight bus lines (DB_0 to DB_7) are used.

Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD44780U when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 10 ms after V_{CC} rises to 4.5 V.

1. Display clear
2. Function set:
   DL = 1; 8-bit interface data
   N = 0; 1-line display
   F = 0; 5 × 8 dot character font
3. Display on/off control:
   D = 0; Display off
   C = 0; Cursor off
   B = 0; Blinking off
4. Entry mode set:
   I/D = 1; Increment by 1
   S = 0; No shift

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD44780U. For such a case, initialization must be performed by the MPU as explained in the section, Initializing by Instruction.

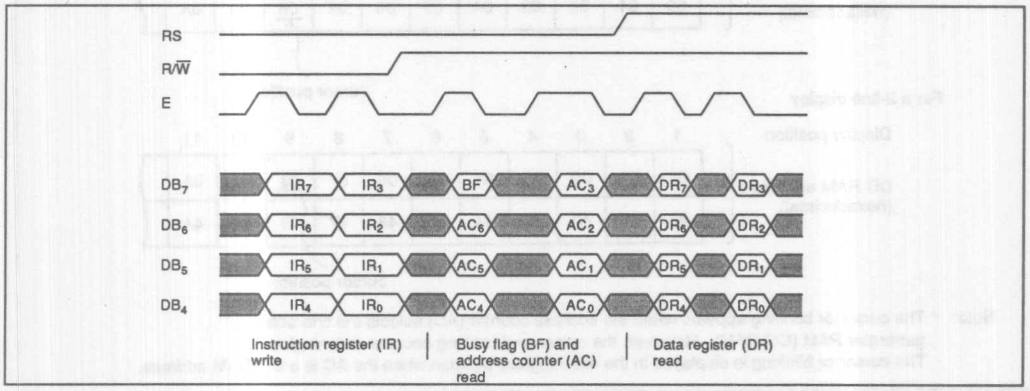


Figure 12 4-Bit Transfer Example

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD44780U can be controlled by the MPU. Before starting the internal operation of the HD44780U, control information is temporarily stored into these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD44780U is determined by signals sent from the MPU. These signals, which include register selection signal (RS), read/write signal (R/$\overline{W}$), and the data bus (DB_0 to DB_7), make up the HD44780U instructions (table 6). There are four categories of instructions that:

- Designate HD44780U functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD44780U RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (table 11) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the HD44780U is not in the busy state (BF = 0) before sending an instruction from the MPU to the HD44780U. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to table 6 for the list of each instruction execution time.

Table 6 Instructions

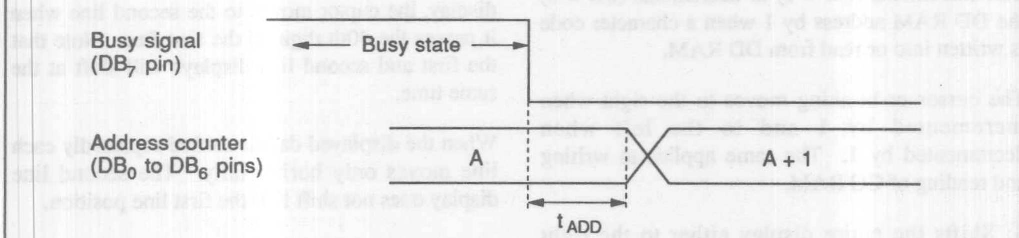
Instruction	Code										Description	Execution Time (max) (when f_{cp} or f_{OSC} is 270 kHz)
	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	15.2 ms
Return home	0	0	0	0	0	0	0	0	1	—	Sets DD RAM address 0 in address counter. Also returns display from being shifted to original position. DD RAM contents remain unchanged.	15.2 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 µs
Display on/off control	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	37 µs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DD RAM contents.	37 µs
Function set	0	0	0	0	1	DL	N	F	—	—	Sets interface data length (DL), number of display lines (N), and character font (F).	37 µs
Set CG RAM address	0	0	0	1	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	Sets CG RAM address. CG RAM data is sent and received after this setting.	37 µs
Set DD RAM address	0	0	1	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	Sets DD RAM address. DD RAM data is sent and received after this setting.	37 µs
Read busy flag & address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs

Table 6 Instructions (cont)

Instruction	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Description	Execution Time (max) (when f_{cp} or f_{OSC} is 270 kHz)
Write data to CG or DD RAM	1	0	Write data								Writes data into DD RAM or CG RAM.	37 μs t_{ADD} = 4 μs*
Read data from CG or DD RAM	1	1	Read data								Reads data from DD RAM or CG RAM.	37 μs t_{ADD} = 4 μs*
	I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits, DL = 0: 4 bits N = 1: 2 lines, N = 0: 1 line F = 1: 5 × 10 dots, F = 0: 5 × 8 dots BF = 1: Internally operating BF = 0: Instructions acceptable										DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM address A_{DD}: DD RAM address (corresponds to cursor address) AC: Address counter used for both DD and CG RAM addresses	Execution time changes when frequency changes Example: When f_{cp} or f_{OSC} is 250 kHz, $37\ \mu s \times \frac{270}{250} = 40\ \mu s$

Note: — indicates no effect.

* After execution of the CG RAM/DD RAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In figure 13, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.



Note: t_{ADD} depends on the operation frequency
$t_{ADD} = 1.5/(f_{cp}$ or $f_{OSC})$ seconds

Figure 13 Address Counter Update

Instruction Description

Clear Display

Clear display writes space code 20H (character pattern for character code 20H must be a blank pattern) into all DD RAM addresses. It then sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change.

Return Home

Return home sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DD RAM contents do not change.

The cursor or blinking go to the left edge of the display (in the first line if 2 lines are displayed).

Entry Mode Set

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from DD RAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DD RAM. Also, writing into or reading out from CG RAM does not shift the display.

Display On/Off Control

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in DD RAM, but can be displayed instantly by setting D to 1.

C: The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5 × 8 dot character font selection and in the 11th line for the 5 × 10 dot character font selection (figure 16).

B: The character indicated by the cursor blinks when B is 1 (figure 16). The blinking is displayed as switching between all blank dots and displayed characters at a speed of 409.6-ms intervals when f_{cp} or f_{OSC} is 250 kHz. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to f_{OSC} or the reciprocal of f_{cp}. For example, when f_{cp} is 270 kHz, $409.6 \times 250/270 = 379.2$ ms.)

Cursor or Display Shift

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (table 7). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. Note that the first and second line displays will shift at the same time.

When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position.

The address counter (AC) contents will not change if the only action performed is a display shift.

Function Set

DL: Sets the interface data length. Data is sent or received in 8-bit lengths (DB_7 to DB_0) when DL is 1, and in 4-bit lengths (DB_7 to DB_4) when DL is 0.

When 4-bit length is selected, data must be sent or received twice.

N: Sets the number of display lines.

F: Sets the character font.

Note: Perform the function at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, the function set instruction cannot be executed unless the interface data length is changed.

Set CG RAM Address

Set CG RAM address sets the CG RAM address binary AAAAAA into the address counter.

Data is then written to or read from the MPU for CG RAM.

		RS	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Clear display	Code	0	0	0	0	0	0	0	0	0	1	
Return home	Code	0	0	0	0	0	0	0	0	1	*	Note: * Don't care.
Entry mode set	Code	0	0	0	0	0	0	0	1	I/D	S	
Display on/off control	Code	0	0	0	0	0	0	1	D	C	B	

Figure 14

		RS	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Cursor or display shift	Code	0	0	0	0	0	1	S/C	R/L	*	*	Note: * Don't care.
Function set	Code	0	0	0	0	1	DL	N	F	*	*	Note: * Don't care.
Set CG RAM address	Code	0	0	0	1	A	A	A	A	A	A	

← Higher order bit   Lower order bit →

Figure 15

Set DD RAM Address

Set DD RAM address sets the DD RAM address binary AAAAAAA into the address counter.

Data is then written to or read from the MPU for DD RAM.

However, when N is 0 (1-line display), AAAAAAA can be 00H to 4FH. When N is 1 (2-line display), AAAAAAA can be 00H to 27H for the first line, and 40H to 67H for the second line.

Read Busy Flag and Address

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. The address contents are the same as for instructions set CG RAM address and set DD RAM address.

Table 7 Shift Function

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Table 8 Function Set

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5 × 8 dots	1/8	
0	1	1	5 × 10 dots	1/11	
1	*	2	5 × 8 dots	1/16	Cannot display two lines for 5 × 10 dot character font

Note: * Indicates don't care.

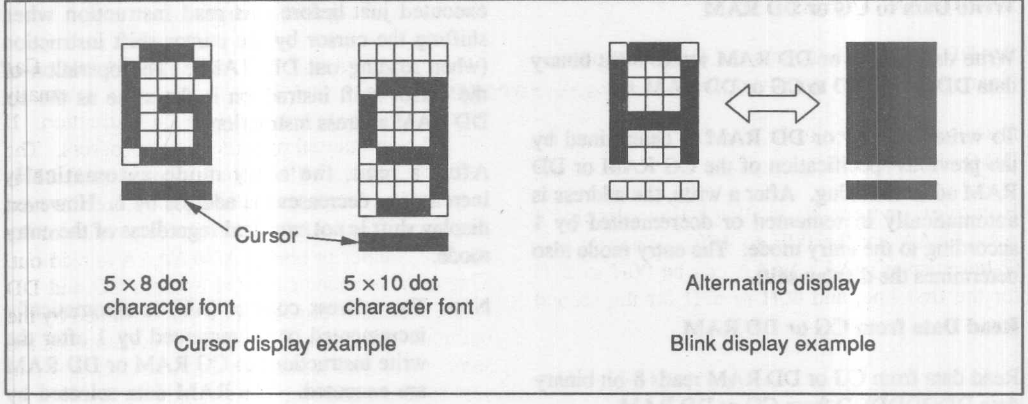


Figure 16 Cursor and Blinking

Set DD RAM address

	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	1	A	A	A	A	A	A	A

Higher order bit ← → Lower order bit

Read busy flag and address

	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	1	BF	A	A	A	A	A	A	A

Higher order bit ← → Lower order bit

Figure 17

Write Data to CG or DD RAM

Write data to CG or DD RAM writes 8-bit binary data DDDDDDDD to CG or DD RAM.

To write into CG or DD RAM is determined by the previous specification of the CG RAM or DD RAM address setting. After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift.

Read Data from CG or DD RAM

Read data from CG or DD RAM reads 8-bit binary data DDDDDDDD from CG or DD RAM.

The previous designation determines whether CG or DD RAM is to be read. Before entering this read instruction, either CG RAM or DD RAM address set instruction must be executed. If not executed, the first read data will be invalid. When serially executing read instructions, the next address data is normally read from the second read. The address set instructions need not be executed just before this read instruction when shifting the cursor by the cursor shift instruction (when reading out DD RAM). The operation of the cursor shift instruction is the same as the set DD RAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented by 1 after the write instructions to CG RAM or DD RAM are executed. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to correctly read data, execute either the address set instruction or cursor shift instruction (only with DD RAM), then just before reading the desired data, execute the read instruction from the second time the read instruction is sent.

		RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Write data to CG or DD RAM	Code	1	0	D	D	D	D	D	D	D	D

← Higher order bits   Lower order bits →

		RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Read data from CG or DD RAM	Code	1	1	D	D	D	D	D	D	D	D

← Higher order bits   Lower order bits →

Figure 18

Interfacing the HD44780U

Interface to MPUs

- Interfacing to an 8-bit MPU through a PIA

See figure 20 for an example of using a PIA or I/O port (for a single-chip microcomputer) as an interface device. The input and output of the device is TTL compatible.

In this example, PB_0 to PB_7 are connected to the data bus DB_0 to DB_7, and PA_0 to PA_2 are connected to E, R/$\overline{W}$, and RS, respectively.

Pay careful attention to the timing relationship between E and the other signals when reading or writing data using a PIA for the interface.

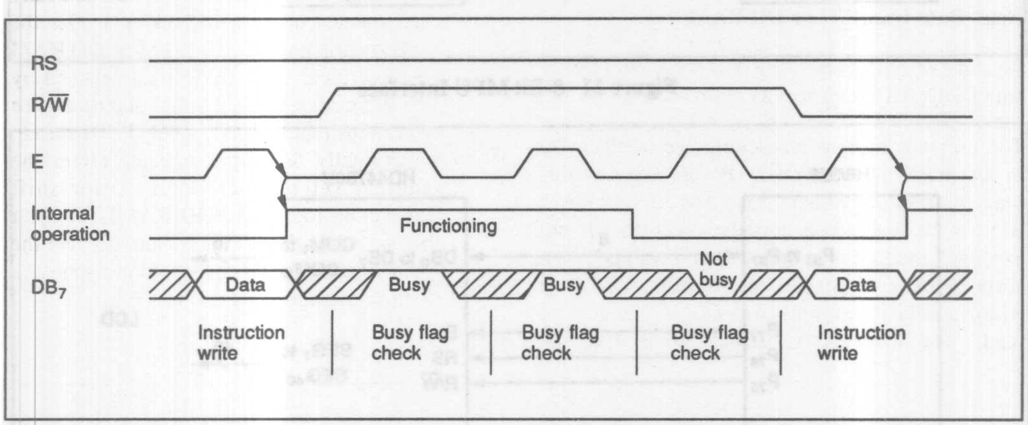


Figure 19 Example of Busy Flag Check Timing Sequence

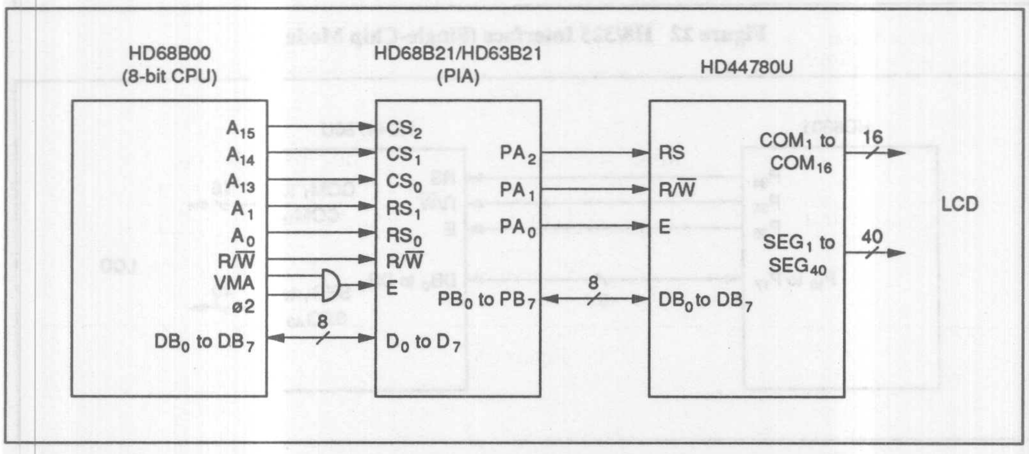


Figure 20 Example of Interface to HD68B00 Using PIA (HD68B21/HD63B21)

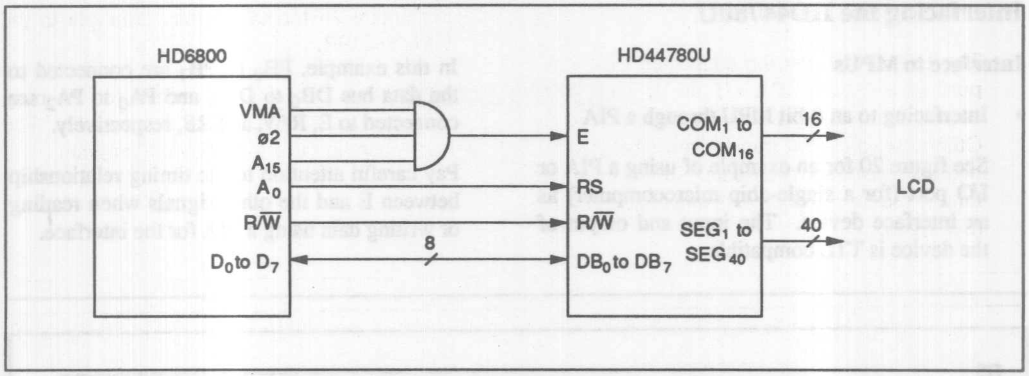


Figure 21 8-Bit MPU Interface

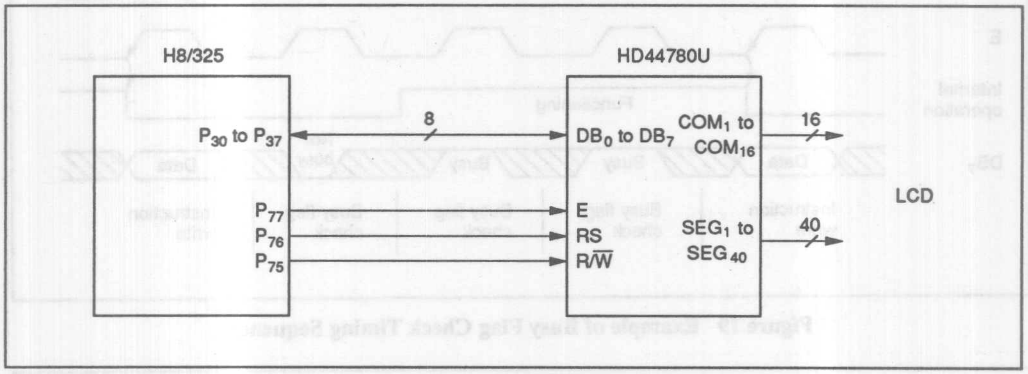


Figure 22 H8/325 Interface (Single-Chip Mode)

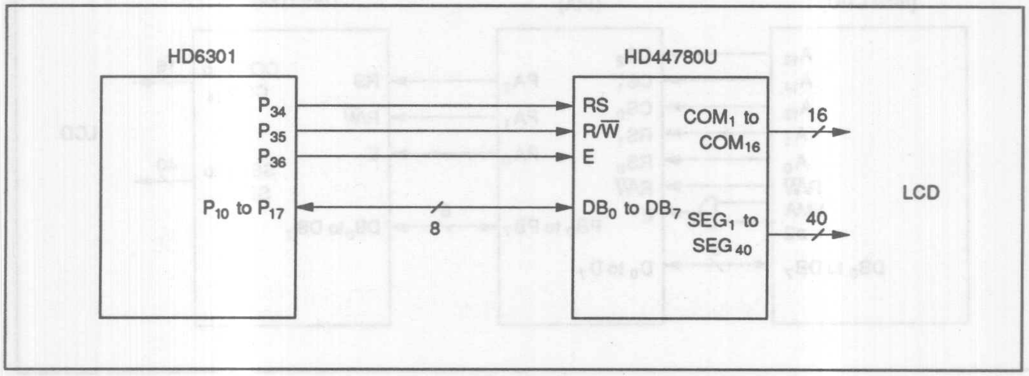


Figure 23 HD6301 Interface

- Interfacing to a 4-bit MPU

The HD44780U can be connected to the I/O port of a 4-bit MPU. If the I/O port has enough bits, 8-bit data can be transferred. Otherwise, one data transfer must be made in two operations for 4-bit data. In this case, the timing sequence becomes somewhat complex. (See figure 24.)

See figure 25 for an interface example to the HMCS4019R.

Note that two cycles are needed for the busy flag check as well as for the data transfer. The 4-bit operation is selected by the program.

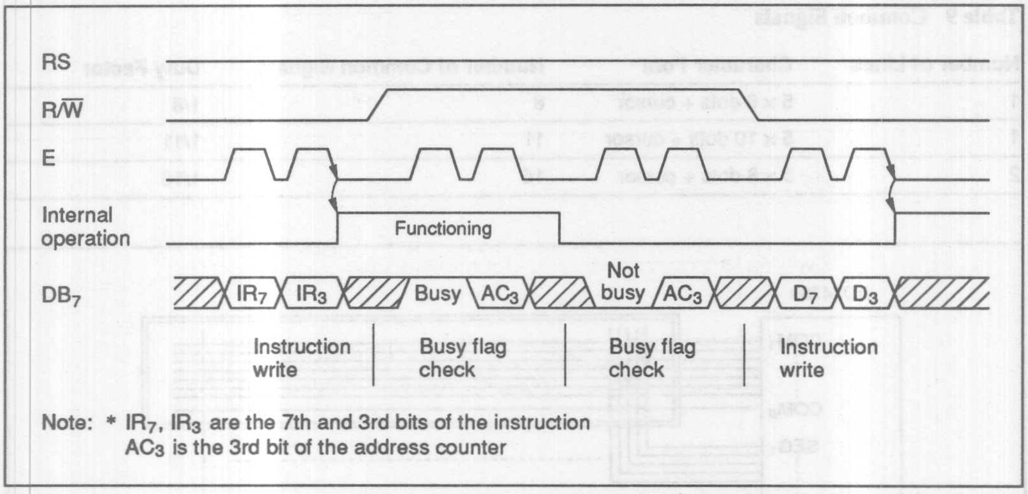


Figure 24 Example of 4-Bit Data Transfer Timing Sequence

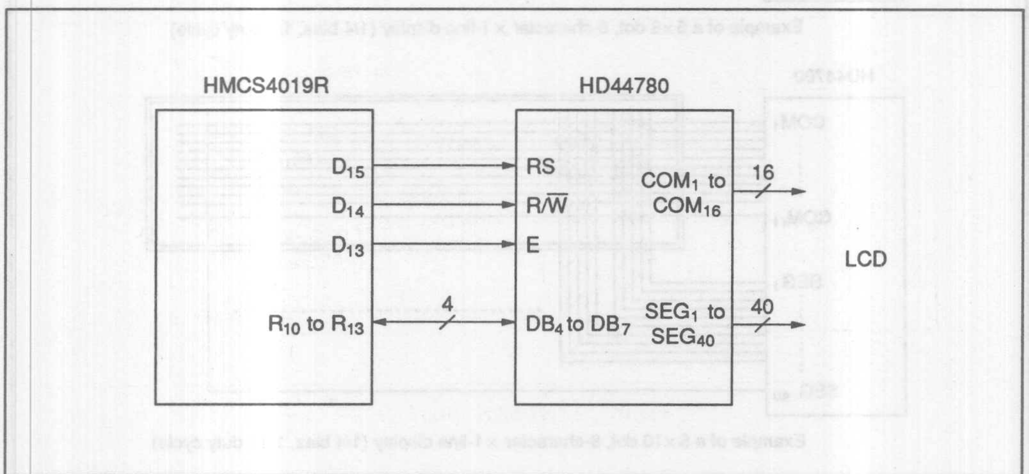


Figure 25 Example of Interface to HMCS4019R

Interface to Liquid Crystal Display

Character Font and Number of Lines: The HD44780U can perform two types of displays, 5 × 8 dot and 5 × 10 dot character fonts, each with a cursor.

Up to two lines are displayed for 5 × 8 dots and one line for 5 × 10 dots. Therefore, a total of three types of common signals are available (table 9).

The number of lines and font types can be selected by the program. (See table 6, Instructions.)

Connection to HD44780 and Liquid Crystal Display: See figure 26 for the connection examples.

Table 9 Common Signals

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 × 8 dots + cursor	8	1/8
1	5 × 10 dots + cursor	11	1/11
2	5 × 8 dots + cursor	16	1/16

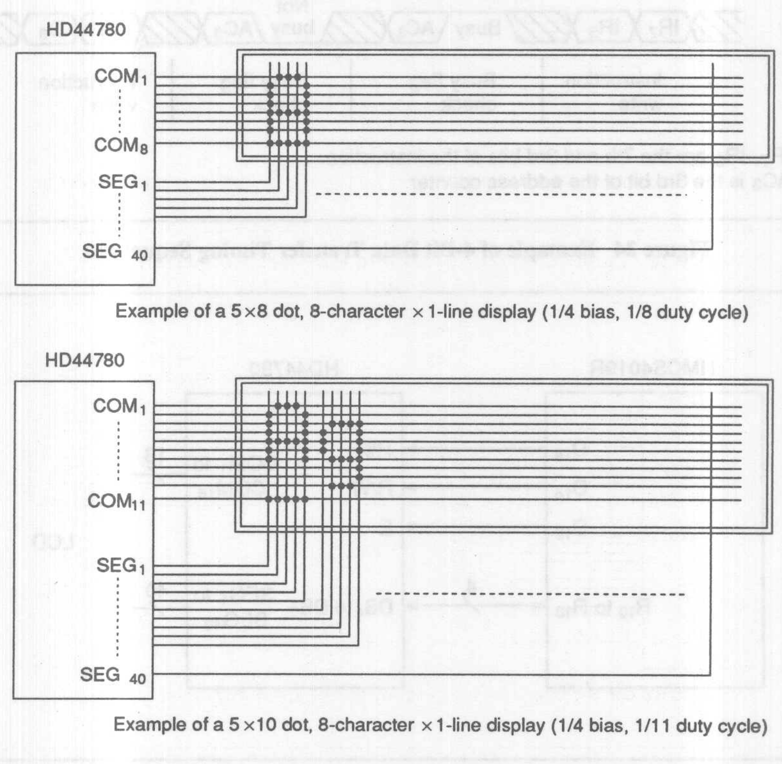
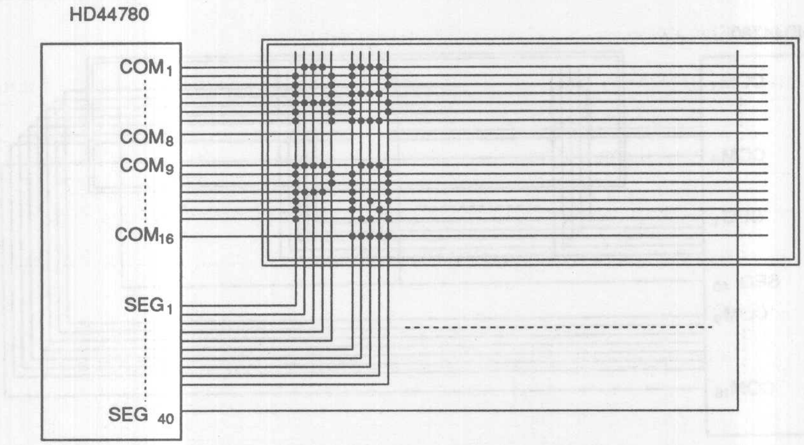


Figure 26 Liquid Crystal Display and HD44780 Connections

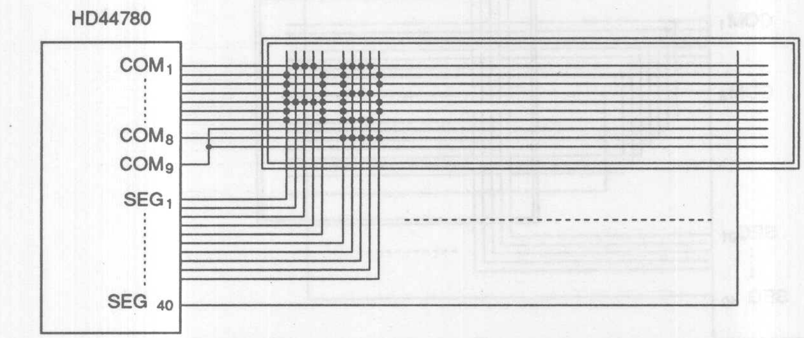
Since five segment signal lines can display one digit, one HD44780U can display up to 8 digits for a 1-line display and 16 digits for a 2-line display.

The examples in figure 26 have unused common signal pins, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, connect the extra scanning lines to these common signal pins to avoid any undesirable effects due to crosstalk during the floating state (figure 27).



Example of a 5 × 8 dot, 8-character × 2-line display (1/5 bias, 1/16 duty cycle)

Figure 26 Liquid Crystal Display and HD44780 Connections (cont)



5 × 8 dot, 8-character × 1-line display (1/4 bias, 1/8 duty cycle)

Figure 27 Using COM_9 to Avoid Crosstalk on Unneeded Scanning Line

Connection of Changed Matrix Layout: In the preceding examples, the number of lines correspond to the scanning lines. However, the following display examples (figure 28) are made possible by altering the matrix layout of the liquid crystal display panel. In either case, the only change is the layout. The display characteristics and the number of liquid crystal display characters depend on the number of common signals or on duty factor. Note that the display data RAM (DD RAM) addresses for 4 characters × 2 lines and for 16 characters × 1 line are the same as in figure 26.

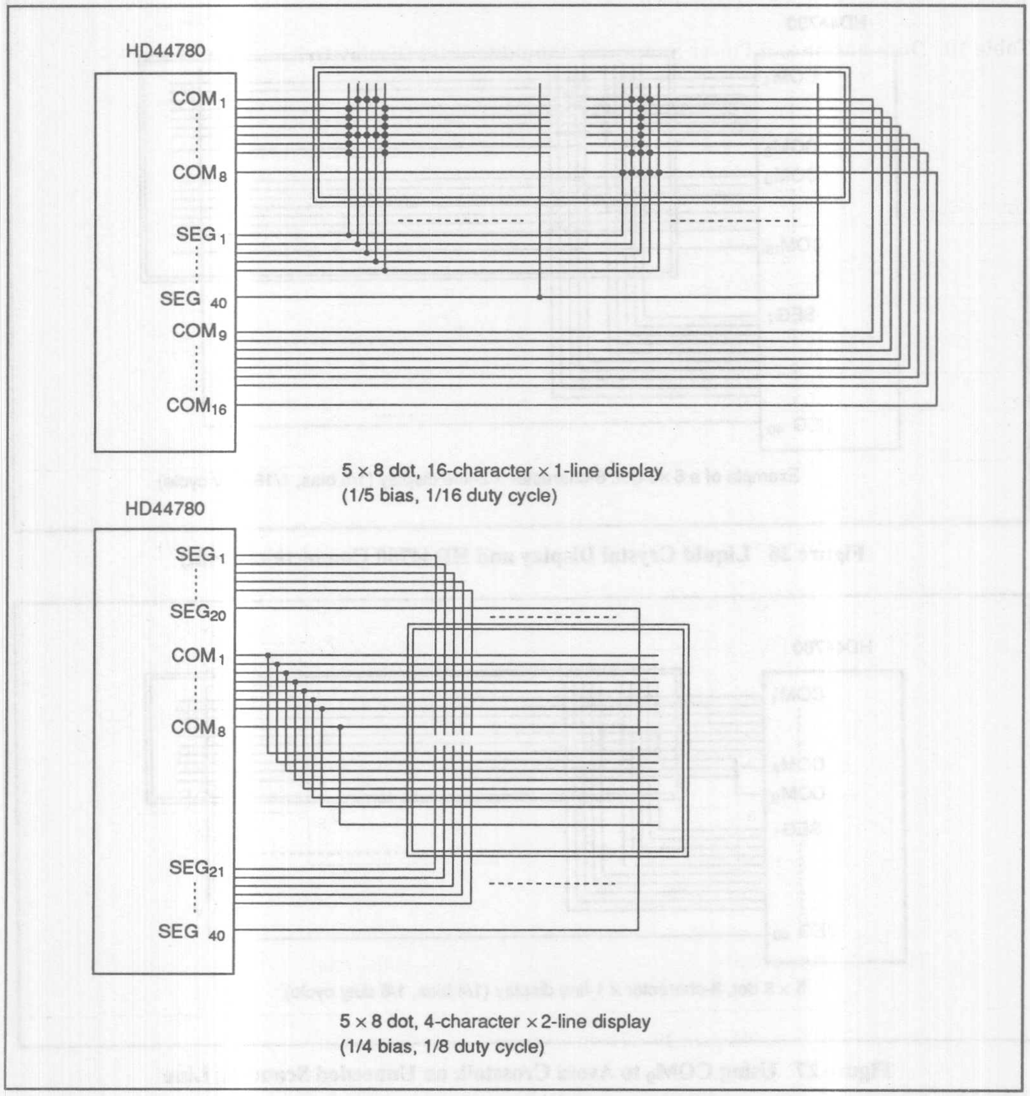


Figure 28 Changed Matrix Layout Displays

Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to pins V_1 to V_5 of the HD44780U to obtain the liquid crystal display drive waveforms. The voltages must be changed according to the duty factor (table 10).

V_{LCD} is the peak value for the liquid crystal display drive waveforms, and resistance dividing provides voltages V_1 to V_5 (figure 29).

Table 10 Duty Factor and Power Supply for Liquid Crystal Display Drive

	Duty Factor	
	1/8, 1/11	1/16
	Bias	
Power Supply	1/4	1/5
V_1	V_{CC}–1/4 V_{LCD}	V_{CC}–1/5 V_{LCD}
V_2	V_{CC}–1/2 V_{LCD}	V_{CC}–2/5 V_{LCD}
V_3	V_{CC}–1/2 V_{LCD}	V_{CC}–3/5 V_{LCD}
V_4	V_{CC}–3/4 V_{LCD}	V_{CC}–4/5 V_{LCD}
V_5	V_{CC}–V_{LCD}	V_{CC}–V_{LCD}

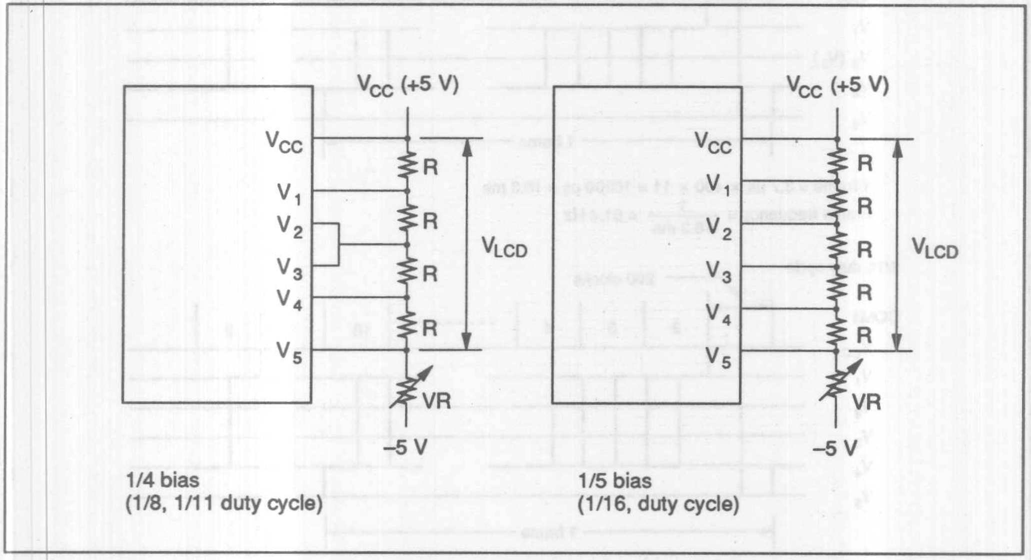


Figure 29 Drive Voltage Supply Example

Relationship between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The liquid crystal display frame frequencies of figure 30 apply only when the oscillation frequency is 270 kHz (one clock pulse of 3.7 µs).

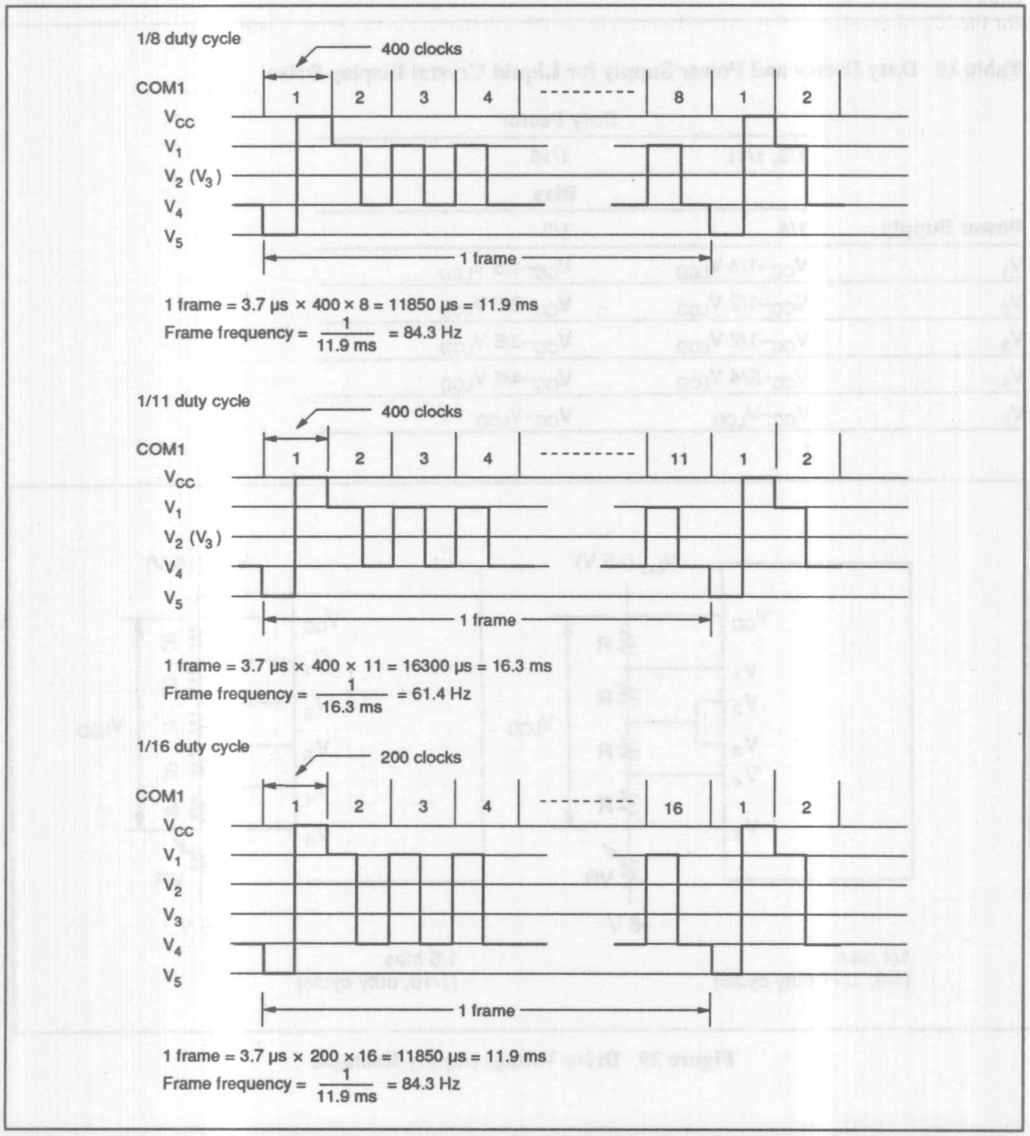


Figure 30 Frame Frequency

Connection with HD44100 Driver

By externally connecting an HD44100 liquid crystal display driver to the HD44780U, the number of display digits can be increased. The HD44100 is used as a segment signal driver when connected to the HD44780U. The HD44100 can be directly connected to the HD44780U since it supplies CL_1, CL_2, M, and D signals and power for the liquid crystal display drive (figure 31).

Caution: The connection of voltage supply pins V_1 through V_6 for the liquid crystal display drive is somewhat complicated.

Up to nine HD44100 units can be connected for a 1-line display (duty factor 1/8 or 1/11) and up to four units for a 2-line display (duty factor 1/16). The RAM size limits the HD44780U to a maximum of 80 character display digits. The connection method for both 1-line and 2-line displays or for 5 × 8 and 5 × 10 dot character fonts can remain the same (figure 26).

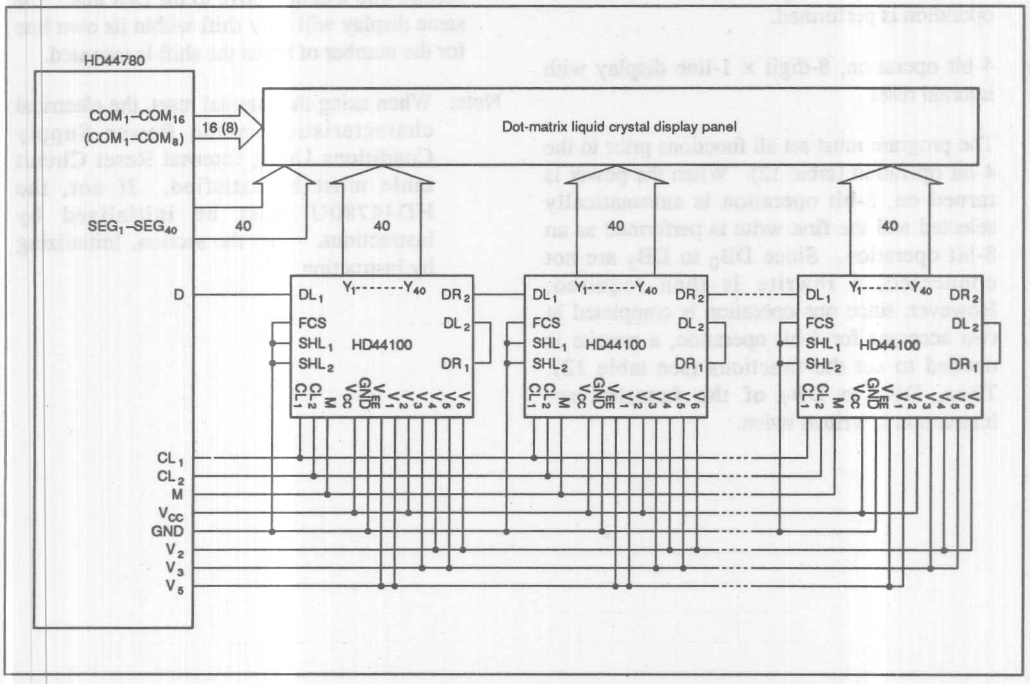


Figure 31 Example of Connecting HD44100s to HD44780

Instruction and Display Correspondence

- 8-bit operation, 8-digit × 1-line display with internal reset

  Refer to table 11 for an example of an 8-digit × 1-line display in 8-bit operation. The HD44780U functions must be set by the function set instruction prior to the display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays such as for advertising when combined with the display shift operation.

  Since the display shift operation changes only the display position with DD RAM contents unchanged, the first display data entered into DD RAM can be output when the return home operation is performed.

- 4-bit operation, 8-digit × 1-line display with internal reset

  The program must set all functions prior to the 4-bit operation (table 12). When the power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since DB_0 to DB_3 are not connected, a rewrite is then required. However, since one operation is completed in two accesses for 4-bit operation, a rewrite is needed to set the functions (see table 12). Thus, DB_4 to DB_7 of the function set instruction is written twice.

- 8-bit operation, 8-digit × 2-line display

  For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must be again set after the 8th character is completed. (See table 13.) Note that the display shift operation is performed for the first and second lines. In the example of table 13, the display shift is performed when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and second lines move together. If the shift is repeated, the display of the second line will not move to the first line. The same display will only shift within its own line for the number of times the shift is repeated.

Note: When using the internal reset, the electrical characteristics in the Power Supply Conditions Using Internal Reset Circuit table must be satisfied. If not, the HD44780U must be initialized by instructions. See the section, Initializing by Instruction.

Table 11 8-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction: RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
1	Power supply on (the HD44780U is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											
	0	0	0	0	1	1	0	0	*	*		Sets to 8-bit operation and selects 1-line display and 5 x 8 dot character font. (Number of display lines and character fonts cannot be changed after step #2.)
3	Display on/off control											
	0	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry mode set											
	0	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write data to CG RAM/DD RAM											
	1	0	0	1	0	0	1	0	0	0	H_	Writes H. DD RAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.
6	Write data to CG RAM/DD RAM											
	1	0	0	1	0	0	1	0	0	1	HI_	Writes I.
7					⋮						⋮	
8	Write data to CG RAM/DD RAM											
	1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.
9	Entry mode set											
	0	0	0	0	0	0	0	1	1	1	HITACHI_	Sets mode to shift display at the time of write.
10	Write data to CG RAM/DD RAM											
	1	0	0	0	1	0	0	0	0	0	ITACHI _	Writes a space.

Table 11 8-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/W̄	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
11	Write data to CG RAM/DD RAM										TACHI M_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
12	⋮										⋮	
13	Write data to CG RAM/DD RAM										MICROKO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
14	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
15	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
16	Write data to CG RAM/DD RAM										ICROCO	Writes C over K. The display moves to the left.
	1	0	0	1	0	0	0	0	1	1		
17	Cursor or display shift										MICROCO	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	1	1	*	*		
18	Cursor or display shift										MICROCO_	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	0	1	*	*		
19	Write data to CG RAM/DD RAM										ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
20	⋮										⋮	
21	Return home										HITACHI	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 12 4-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset

Step No.	RS	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	Display	Operation
1	Power supply on (the HD44780U is initialized by the internal reset circuit)							Initialized. No display.
2	Function set							Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
	0	0	0	0	1	0		
3	Function set							Sets 4-bit operation and selects 1-line display and 5 × 8 dot character font. 4-bit operation starts from this step and resetting is necessary. (Number of display lines and character fonts cannot be changed after step #3.)
	0	0	0	0	1	0		
	0	0	0	0	*	*		
4	Display on/off control						_	Turns on display and cursor. Entire display is in space mode because of initialization.
	0	0	0	0	0	0		
	0	0	1	1	1	0		
5	Entry mode set						_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
	0	0	0	0	0	0		
	0	0	0	1	1	0		
6	Write data to CG RAM/DD RAM						H_	Writes H. The cursor is incremented by one and shifts to the right.
	1	0	0	1	0	0		
	1	0	1	0	0	0		

Note: The control is the same as for 8-bit operation beyond step #6.

Table 13 8-Bit Operation, 8-Digit × 2-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
1	Power supply on (the HD44780U is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 8-bit operation and selects 2-line display and 5 × 8 dot character font.
	0	0	0	0	1	1	1	0	*	*		
3	Display on/off control										_	Turns on display and cursor. All display is in space mode because of initialization.
	0	0	0	0	0	0	1	1	1	0		
4	Entry mode set										_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
	0	0	0	0	0	0	0	1	1	0		
5	Write data to CG RAM/DD RAM										H_	Writes H. DD RAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.
	1	0	0	1	0	0	1	0	0	0		
6	⋮										⋮	
7	Write data to CG RAM/DD RAM										HITACHI_	Writes I.
	1	0	0	1	0	0	1	0	0	1		
8	Set DD RAM address										HITACHI _	Sets DD RAM address so that the cursor is positioned at the head of the second line.
	0	0	1	1	0	0	0	0	0	0		

Table 13 8-Bit Operation, 8-Digit × 2-Line Display Example with Internal Reset (cont)

Step No.	Instruction										Display	Operation
	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
9	Write data to CG RAM/DD RAM											Writes M.
	1	0	0	1	0	0	1	1	0	1	HITACHI M_	
10	⋮										⋮	
11	Write data to CG RAM/DD RAM											Writes O.
	1	0	0	1	0	0	1	1	1	1	HITACHI MICROCO_	
12	Entry mode set											Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1	HITACHI MICROCO_	
13	Write data to CG RAM/DD RAM											Writes M. Display is shifted to the left. The first and second lines both shift at the same time.
	1	0	0	1	0	0	1	1	0	1	ITACHI ICROCOM_	
14	⋮										⋮	
15	Return home											Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0	HITACHI MICROCOM	

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

Refer to figures 32 and 33 for the procedures on 8-bit and 4-bit initializations, respectively.

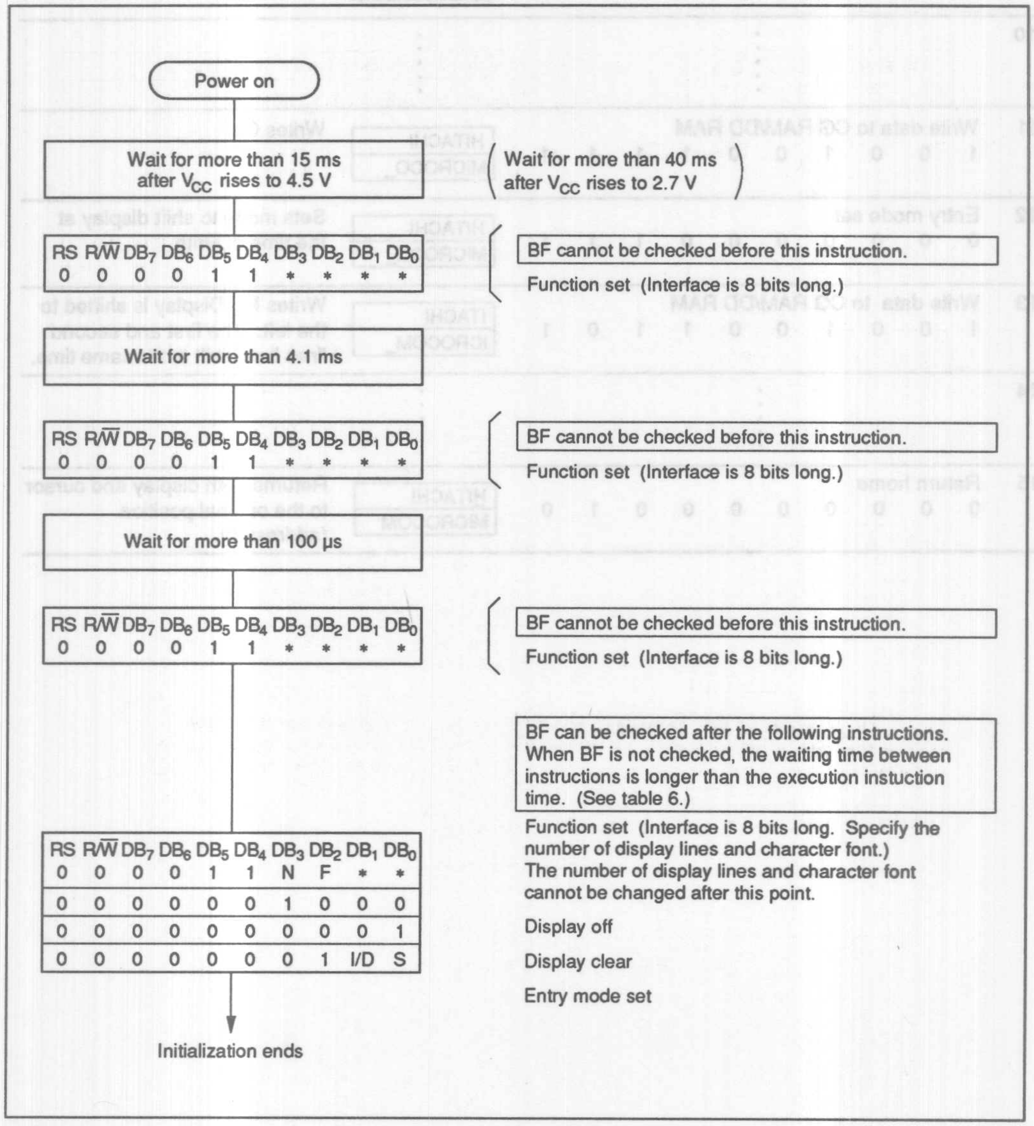


Figure 32 8-Bit Interface

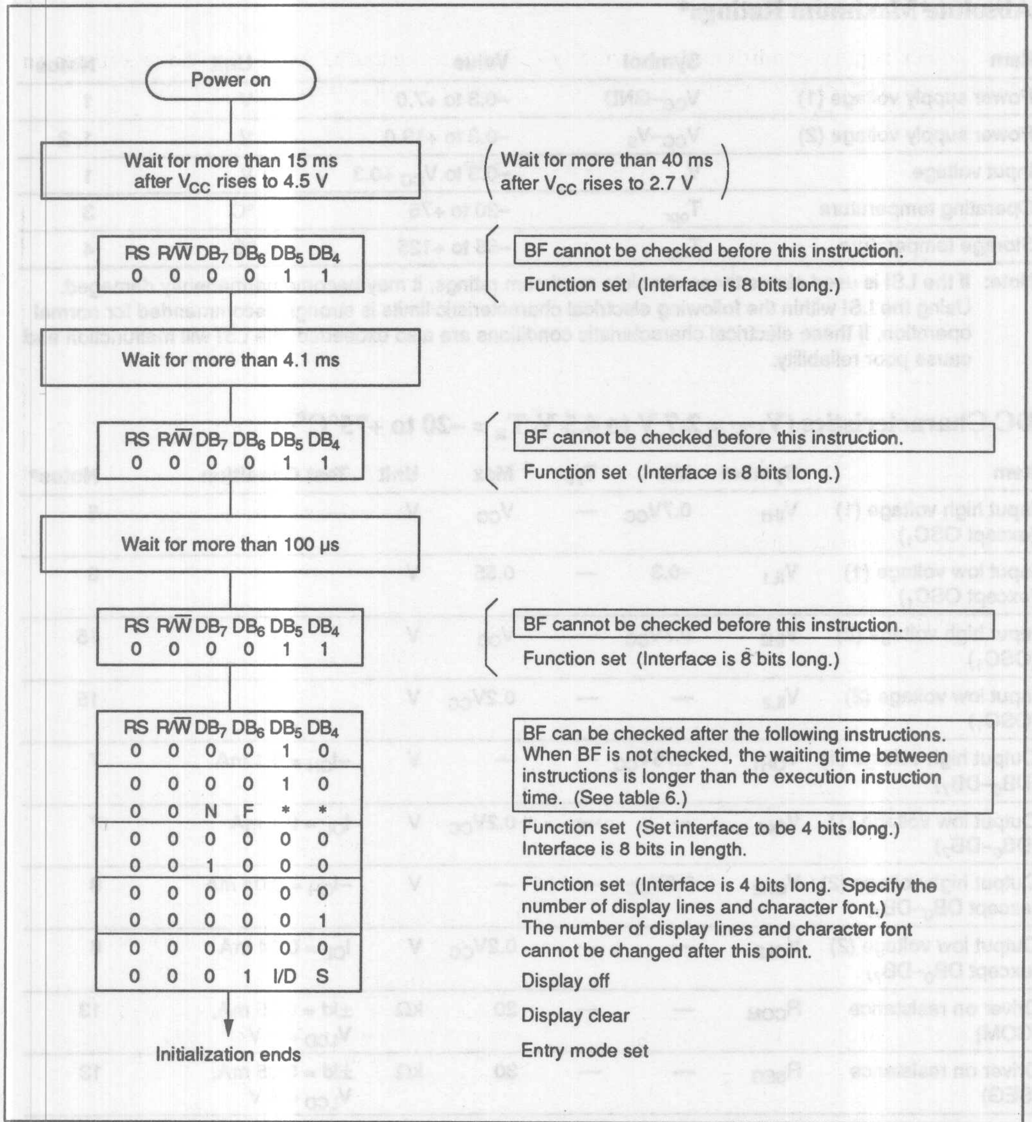


Figure 33 4-Bit Interface

Absolute Maximum Ratings*

Item	Symbol	Value	Unit	Notes
Power supply voltage (1)	V_{CC}–GND	–0.3 to +7.0	V	1
Power supply voltage (2)	V_{CC}–V_5	–0.3 to +13.0	V	1, 2
Input voltage	V_t	–0.3 to V_{CC} +0.3	V	1
Operating temperature	T_{opr}	–20 to +75	°C	3
Storage temperature	T_{stg}	–55 to +125	°C	4

Note: If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 2.7 V to 4.5 V, T_a = –20 to +75°C*3)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC_1)	V_{IH1}	$0.7V_{CC}$	—	V_{CC}	V		6
Input low voltage (1) (except OSC_1)	V_{IL1}	–0.3	—	0.55	V		6
Input high voltage (2) (OSC_1)	V_{IH2}	$0.7V_{CC}$	—	V_{CC}	V		15
Input low voltage (2) (OSC_1)	V_{IL2}	—	—	$0.2V_{CC}$	V		15
Output high voltage (1) (DB_0–DB_7)	V_{OH1}	$0.75V_{CC}$	—	—	V	$-I_{OH}$ = 0.1 mA	7
Output low voltage (1) (DB_0–DB_7)	V_{OL1}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.1 mA	7
Output high voltage (2) (except DB_0–DB_7)	V_{OH2}	$0.8V_{CC}$	—	—	V	$-I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except DB_0–DB_7)	V_{OL2}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA, V_{LCD} = 4 V	13
Driver on resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA, V_{LCD} = 4 V	13
Input leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (DB_0–DB_7, RS, R/$\overline{W}$)	–Ip	10	50	120	µA	V_{CC} = 3 V	
Power supply current	I_{CC}	—	0.15	0.30	mA	R_f oscillation, external clock V_{CC} = 3V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD1}	3.0	—	11.0	V	V_{CC}–V_5, 1/5 bias	16
	V_{LCD2}	3.0	—	11.0	V	V_{CC}–V_5, 1/4 bias	16

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 2.7 V to 4.5 V, T_a = –20 to +75°C*3)

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Note*
External clock operation	External clock frequency	f_{cp}	125	250	350	kHz		11
	External clock duty	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{fcp}	—	—	0.2	µs		
R_f oscillation	Clock oscillation frequency	f_{OSC}	190	270	350	kHz	R_f = 75 kΩ, V_{CC} = 3 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 34
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 35
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data delay time	t_{DDR}	—	—	360		
Data hold time	t_{DHR}	5	—	—		

Interface Timing Characteristics with External Driver

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 36
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	−1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	200		

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 37
Power supply off time	t_{OFF}	1	—	—		

DC Characteristics (V_{CC} = 4.5 V to 5.5 V, T_a = –20 to +75°C*3)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC_1)	V_{IH1}	2.2	—	V_{CC}	V		6
Input low voltage (1) (except OSC_1)	V_{IL1}	–0.3	—	0.6	V		6
Input high voltage (2) (OSC_1)	V_{IH2}	V_{CC}–1.0	—	V_{CC}	V		15
Input low voltage (2) (OSC_1)	V_{IL2}	—	—	1.0	V		15
Output high voltage (1) (DB_0–DB_7)	V_{OH1}	2.4	—	—	V	$-I_{OH}$ = 0.205 mA	7
Output low voltage (1) (DB_0–DB_7)	V_{OL1}	—	—	0.4	V	I_{OL} = 1.2 mA	7
Output high voltage (2) (except DB_0–DB_7)	V_{OH2}	0.9 V_{CC}	—	—	V	$-I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except DB_0–DB_7)	V_{OL2}	—	—	0.1 V_{CC}	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA, V_{LCD} = 4 V	13
Driver on resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA, V_{LCD} = 4 V	13
Input leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (DB_0–DB_7, RS, R/$\overline{W}$)	$-I_p$	50	125	250	µA	V_{CC} = 5 V	
Power supply current	I_{CC}	—	0.35	0.60	mA	R_f oscillation, external clock V_{CC} = 5 V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD1}	3.0	—	11.0	V	V_{CC}–V_5, 1/5 bias	16
	V_{LCD2}	3.0	—	11.0	V	V_{CC}–V_5, 1/4 bias	16

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 4.5 V to 5.5 V, T_a = –20 to +75°C*3)

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Note*
External clock operation	External clock frequency	f_{cp}	125	250	350	kHz		11
	External clock duty	Duty	45	50	55	%		11
	External clock rise time	t_{rcp}	—	—	0.2	µs		11
	External clock fall time	t_{fcp}	—	—	0.2	µs		11
R_f oscillation	Clock oscillation frequency	f_{OSC}	190	270	350	kHz	R_f = 91 kΩ V_{CC} = 5.0 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 34
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data set-up time	t_{DSW}	80	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 35
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data delay time	t_{DDR}	—	—	160		
Data hold time	t_{DHR}	5	—	—		

Interface Timing Characteristics with External Driver

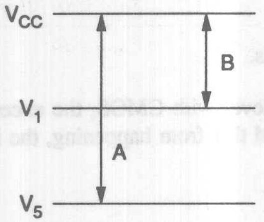
Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 36
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	−1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	100		

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 37
Power supply off time	t_{OFF}	1	—	—		

Electrical Characteristics Notes

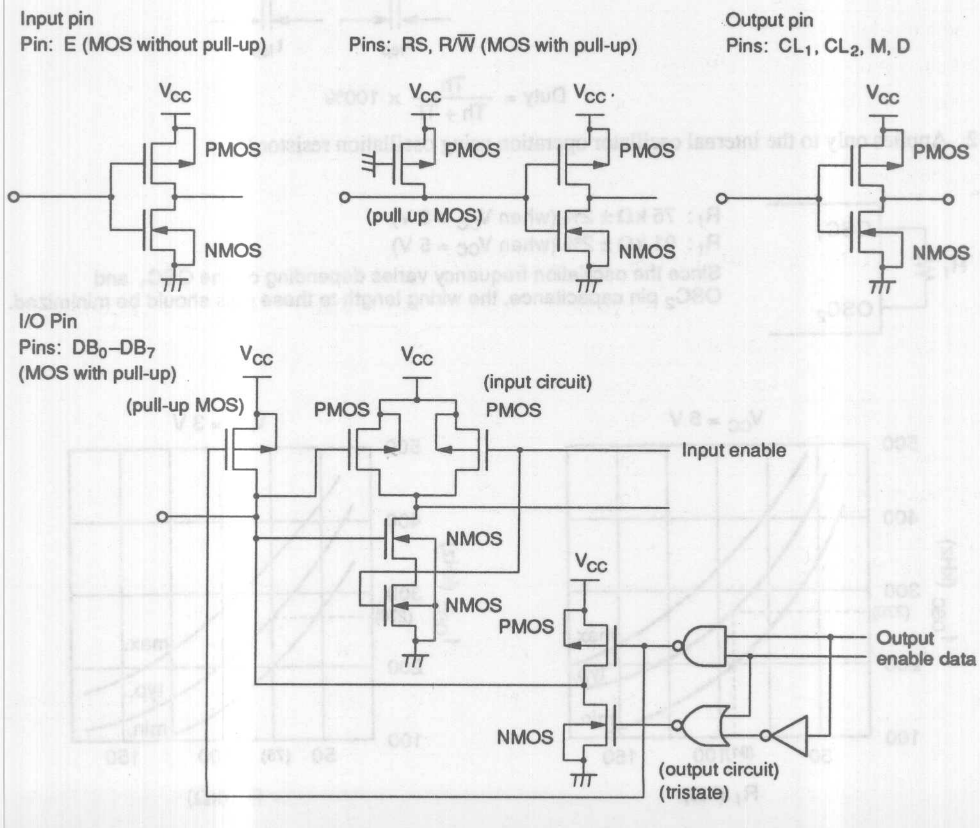
1. All voltage values are referred to GND = 0 V.



$A = V_{CC} - V_5$
$B = V_{CC} - V_1$
$A \geq 1.5$ V
$B \leq 0.25 \times A$

The conditions of V_1 and V_5 voltages are for proper operation of the LSI and not for the LCD output level. The LCD drive voltage condition for the LCD output level is specified as LCD voltage V_{LCD}.

2. $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ must be maintained.
3. For die products, specified up to 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.



6. Applies to input pins and I/O pins, excluding the OSC_1 pin.

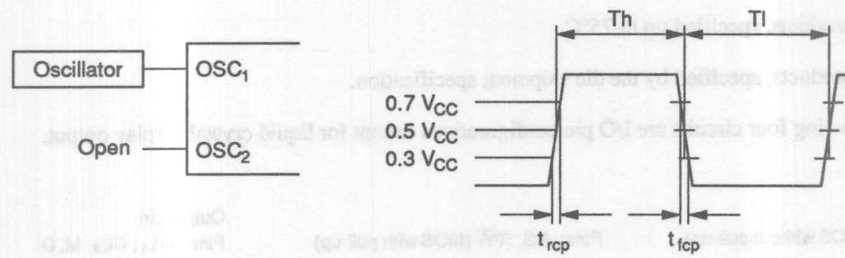
7. Applies to I/O pins.

8. Applies to output pins.

9. Current flowing through pull–up MOSs, excluding output drive MOSs.

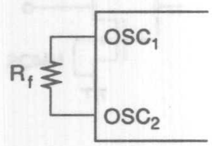
10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.

11. Applies only to external clock operation.

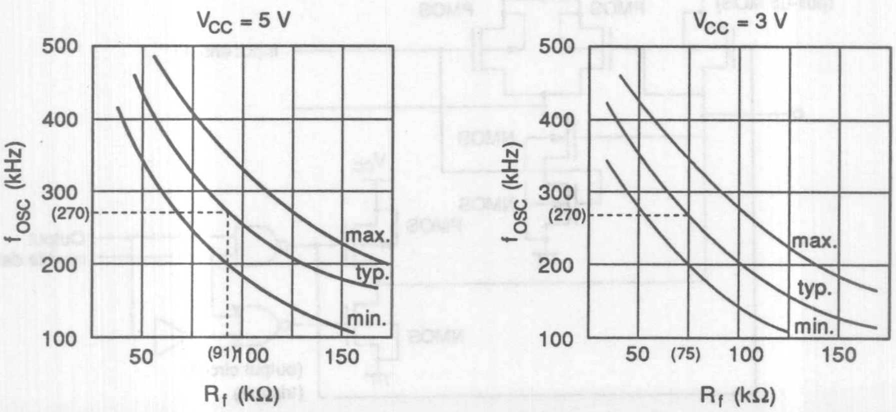


$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

12. Applies only to the internal oscillator operation using oscillation resistor R_f.



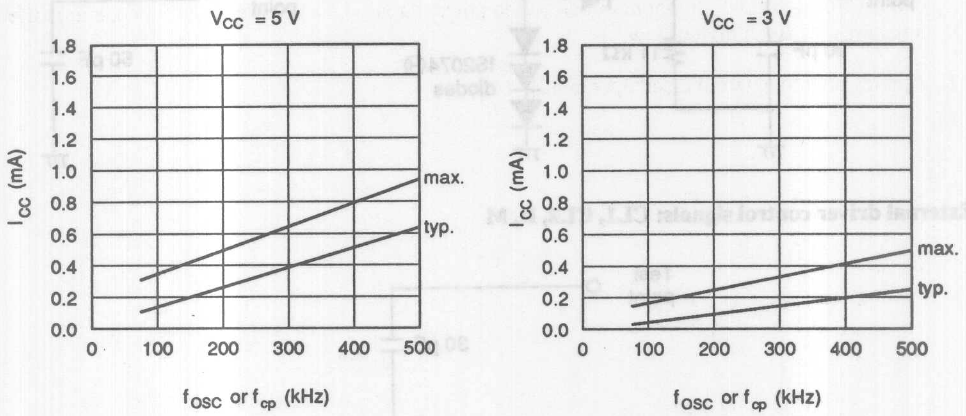
R_f: 75 kΩ ± 2% (when V_{CC} = 3 V)
R_f: 91 kΩ ± 2% (when V_{CC} = 5 V)
Since the oscillation frequency varies depending on the OSC_1 and OSC_2 pin capacitance, the wiring length to these pins should be minimized.



13. R_{COM} is the resistance between the power supply pins (V_{CC}, V_1, V_4, V_5) and each common signal pin (COM_1 to COM_{16}).

    R_{SEG} is the resistance between the power supply pins (V_{CC}, V_2, V_3, V_5) and each segment signal pin (SEG_1 to SEG_{40}).

14. The following graphs show the relationship between operation frequency and current consumption.

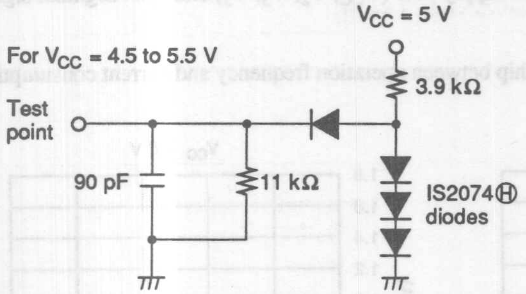


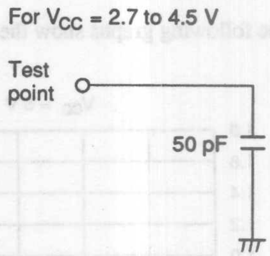
15. Applies to the OSC_1 pin.

16. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (V_{CC}, V_1, V_2, V_3, V_4, V_5) when there is no load.

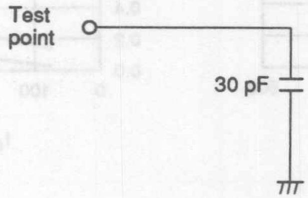
Load Circuits

Data Bus DB_0 to DB_7





External driver control signals: CL1, CL2, D, M



Timing Characteristics

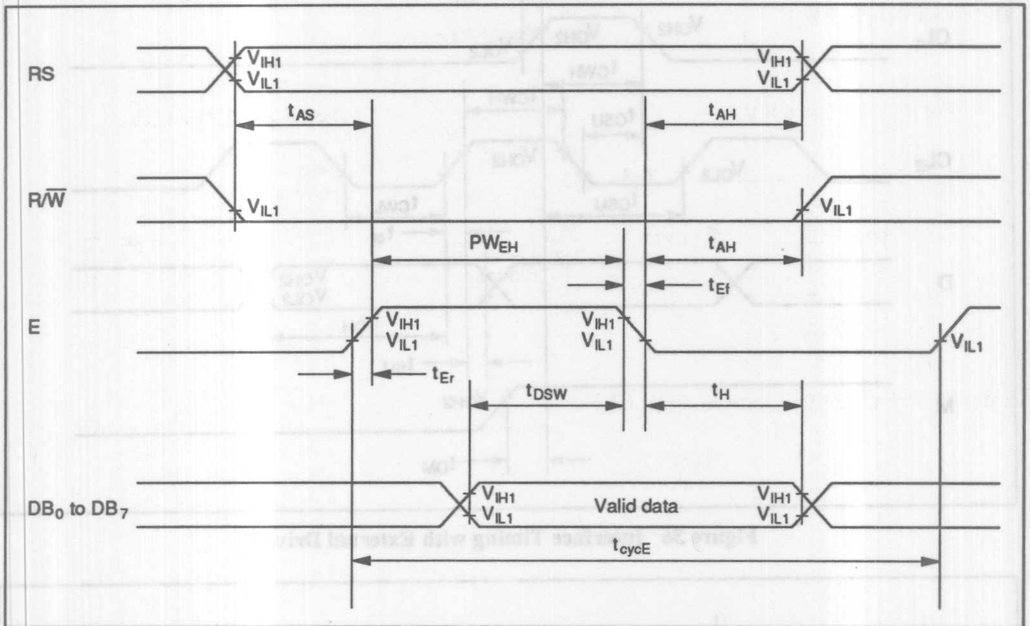
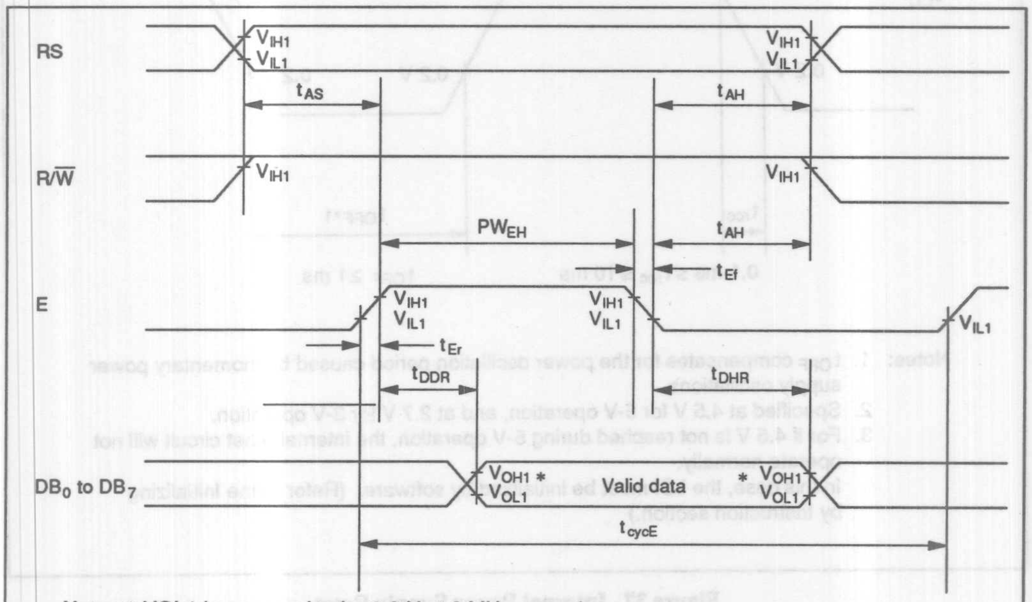


Figure 34 Write Operation



Note: * VOL1 is assumed to be 0.8 V at 2 MHz operation.

Figure 35 Read Operation

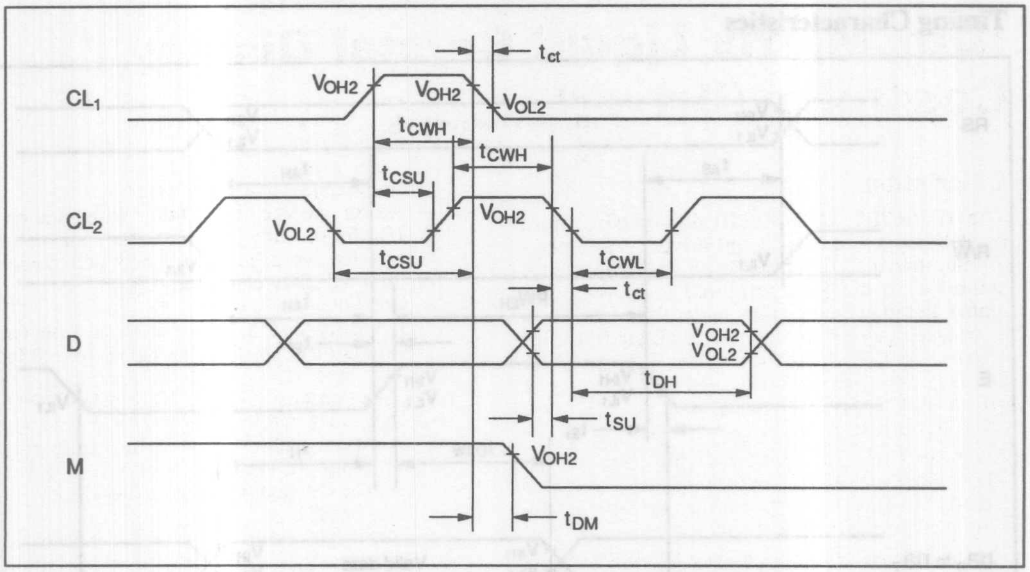
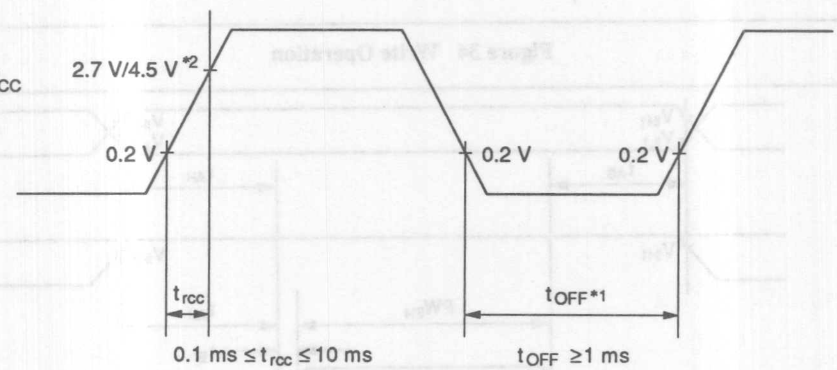


Figure 36 Interface Timing with External Driver



Notes: 1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for 5-V operation, and at 2.7 V for 3-V operation.
3. For if 4.5 V is not reached during 5-V operation, the internal reset circuit will not operate normally.
In this case, the LSI must be initialized by software. (Refer to the Initializing by Instruction section.)

Figure 37 Internal Power Supply Reset

HD66702 (LCD-II/E20)
(Dot Matrix Liquid Crystal Display Controller/Driver)

Description

The HD66702 LCD-II/E20 dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

A single LCD-II/E20 can display up to two 20-character lines. However, with the addition of HD44100 drivers, a maximum of up to two 40-character lines can be displayed.

The low 3-V power supply of the LCD-II/E20 under development is suitable for any portable battery-driven product requiring low power dissipation.

Features

- 5 × 7 and 5 × 10 dot matrix possible
- 80 × 8-bit display RAM (80 characters max.)
- 7,200-bit character generator ROM
  - — 160 character fonts (5 × 7 dot)
  - — 32 character fonts (5 × 10 dot)
- 64 × 8-bit character generator RAM
  - — 8 character fonts (5 × 7 dot)
  - — 4 character fonts (5 × 10 dot)
- 16-common × 100-segment liquid crystal display driver
- Programmable duty cycles
  - — 1/8 for one line of 5 × 7 dots with cursor
  - — 1/11 for one line of 5 × 10 dots with cursor
  - — 1/16 for two lines of 5 × 7 dots with cursor
- Maximum display characters
  - — One line:
    1/8 duty cycle, 20-char. × 1-line (no extension), 28-char. × 1-line (extended with one HD44100), 80-char. × 1-line (max. extension with eight HD44100s).
    1/11 duty cycle, 20-char. × 1-line (no extension), 28-char. × 1-line (extended with one HD44100), 80-char. × 1-line (max. extension with eight HD44100s)
  - — Two lines:
    1/16 duty cycle, 20-char. × 2-line (no extension), 28-char. × 2-line (extended with one HD44100), 40-char. × 2-line (max. extension with eight HD44100s)
- Wide range of instruction functions:
  - — Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Choice of power supply (V_{CC}): 4.5 to 5.5 V (standard), 2.7 to 5.5 V (low voltage)
- Automatic reset circuit that initializes the controller/driver after power on (standard version only)
- Independent LCD drive voltage driven off of the logic power supply (V_{CC}): 3.0 to 7.0 V

Ordering Information

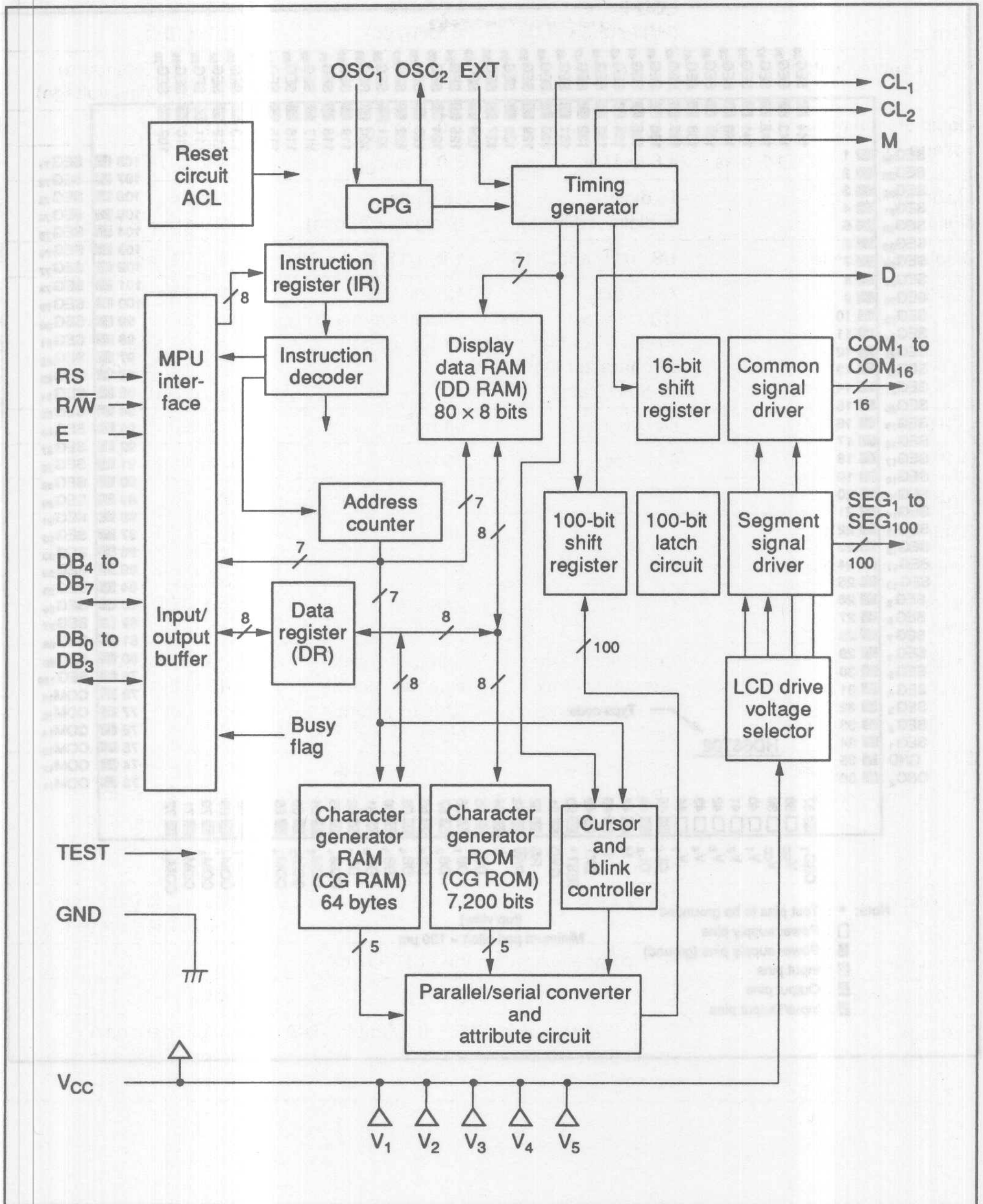
Type No.	Package	Operating Voltage	ROM Font
HCD66702RA00	Chip	4.5 to 5.5 V	Standard Japanese font
HCD66702RA00L	Chip	2.7 to 5.5 V	
HD66702RA00F	144-pin plastic QFP (FP-144A)	4.5 to 5.5 V	
HD66702RA00FL	144-pin plastic QFP (FP-144A)	2.7 to 5.5 V	
HD66702RA01F	144-pin plastic QFP (FP-144A)	4.5 to 5.5 V	Japanese font for comunication system
HD66702RA02F	144-pin plastic QFP (FP-144A)	4.5 to 5.5 V	European font
HCD66702RBxx	Chip	4.5 to 5.5 V	Custom font
HCD66702RBxxL	Chip	2.7 to 5.5 V	
HD66702RBxxF	144-pin plastic QFP (FP-144A)	4.5 to 5.5 V	
HD66702RBxxFL	144-pin plastic QFP (FP-144A)	2.7 to 5.5 V	

Note: xx: ROM code No.

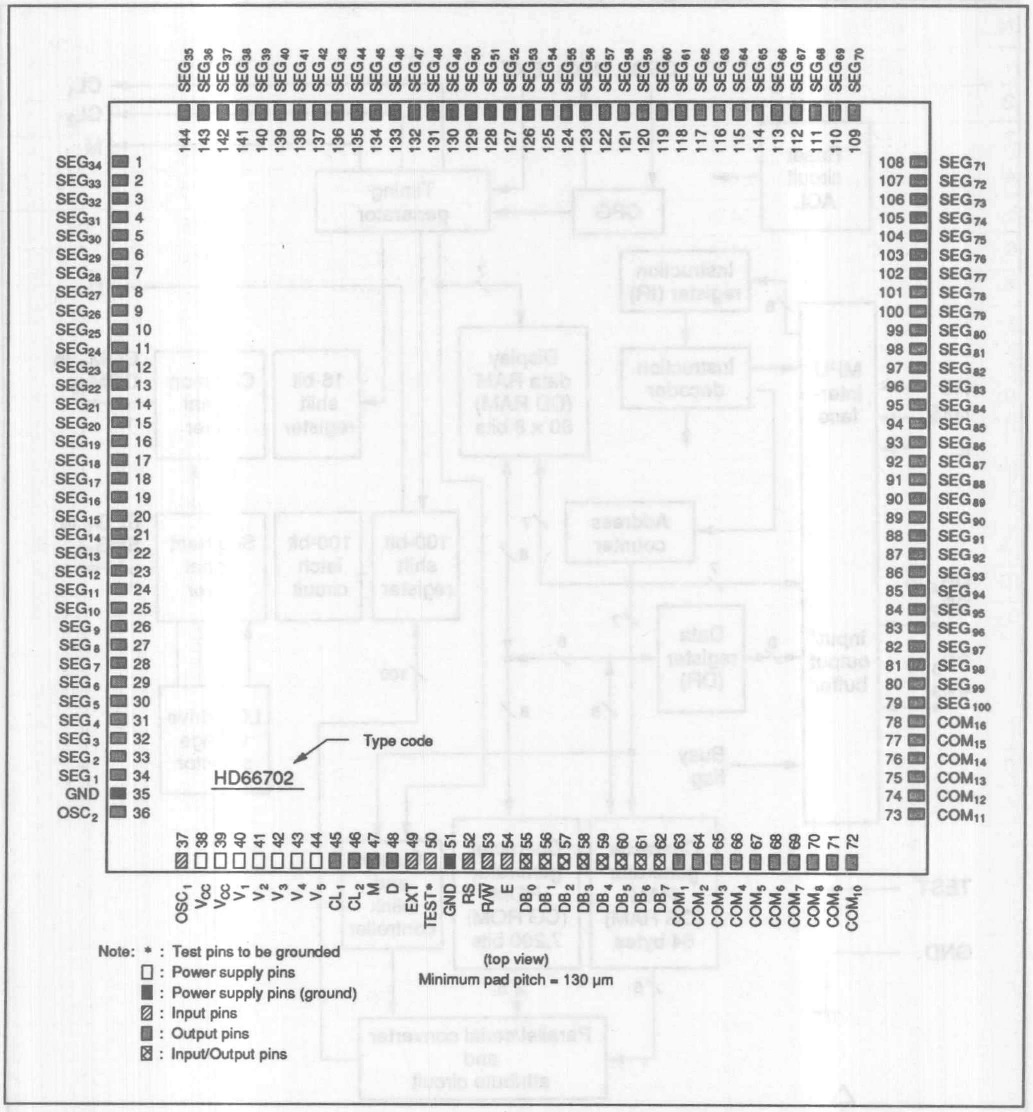
LCD-II Family Comparison

Item		LCD-II (HD44780)	LCD-II/A (HD66780)	LCD-II/E20 (HD66702)
Power supply voltage		5 V ±10%	5 V ±10%	5 V ±10% (standard) 3 V ±10% (low voltage)
Liquid crystal drive voltage V_{LCD}	1/4 bias	3.0 to 11 V	3.0 V to V_{CC}	3.0 to 6.0 V
	1/5 bias	4.6 to 11 V	3.0 V to V_{CC}	3.0 to 6.0 V
Maximum display digits per chip		16 digits (8 digits × 2 lines)	16 digits (8 digits × 2 lines)	40 digits (20 digits × 2 lines)
Display duty cycle		1/8, 1/11, and 1/16	1/8, 1/11, and 1/16	1/8, 1/11, and 1/16
CGROM		7,200 bits (160 character fonts for 5 × 7 dot and 32 character fonts for 5 × 10 dot)	12,000 bits (240 character fonts for 5 × 10 dot)	7,200 bits (160 character fonts for 5 × 7 dot and 32 character fonts for 5 × 10 dot)
CGRAM		64 bytes	64 bytes	64 bytes
DDRAM		80 bytes	80 bytes	80 bytes
Segment signals		40	40	100
Common signals		16	16	16
Liquid crystal drive waveform		A	B	B
Ladder resistor for LCD power supply		External	External	External
Clock source		External resistor, external ceramic filter, or external clock	External resistor, external ceramic filter, or external clock	External resistor or external clock
R_f oscillation frequency (frame frequency)		270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	320 kHz ±30% (69 to 128 Hz for 1/8 and 1/16 duty cycles; 50 to 93 Hz for 1/11 duty cycle)
R_f resistance		91 kΩ ±2%	83 kΩ ±2%	68 kΩ ±2% (standard) 56 kΩ ±2% (low voltage)
Instructions		Fully compatible within the LCD-II family		
CPU bus timing		1 MHz	2 MHz	1 MHz
Package		FP-80, FP-80A, and 80-pin bare chip (no package)	FP-80B and FP-80A	144-pin bare chip (no package) and FP-144A

LCD-II/E20 Block Diagram



LCD-II/E20 Pad Arrangement



HCD66702 Pad Location Coordinates

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
1	SEG_{34}	–2475	2350	31	SEG_4	–2475	–1600
2	SEG_{33}	–2475	2205	32	SEG_3	–2475	–1735
3	SEG_{32}	–2475	2065	33	SEG_2	–2475	–1870
4	SEG_{31}	–2475	1925	34	SEG_1	–2475	–2010
5	SEG_{30}	–2475	1790	35	GND	–2475	–2180
6	SEG_{29}	–2475	1655	36	OSC_2	–2475	–2325
7	SEG_{28}	–2475	1525	37	OSC_1	–2445	–2475
8	SEG_{27}	–2475	1395	38	V_{CC}	–2305	–2475
9	SEG_{26}	–2475	1265	39	V_{CC}	–2165	–2475
10	SEG_{25}	–2475	1135	40	V_1	–2025	–2475
11	SEG_{24}	–2475	1005	41	V_2	–1875	–2475
12	SEG_{23}	–2475	875	42	V_3	–1745	–2475
13	SEG_{22}	–2475	745	43	V_4	–1595	–2475
14	SEG_{21}	–2475	615	44	V_5	–1465	–2475
15	SEG_{20}	–2475	485	45	CL_1	–1335	–2475
16	SEG_{19}	–2475	355	46	CL_2	–1185	–2475
17	SEG_{18}	–2475	225	47	M	–1055	–2475
18	SEG_{17}	–2475	95	48	D	–905	–2475
19	SEG_{16}	–2475	–35	49	EXT	–775	–2475
20	SEG_{15}	–2475	–165	50	TEST	–625	–2475
21	SEG_{14}	–2475	–295	51	GND	–495	–2475
22	SEG_{13}	–2475	–425	52	RS	–345	–2475
23	SEG_{12}	–2475	–555	53	$R/\overline{W}$	–195	–2475
24	SEG_{11}	–2475	–685	54	E	–45	–2475
25	SEG_{10}	–2475	–815	55	DB_0	85	–2475
26	SEG_9	–2475	–945	56	DB_1	235	–2475
27	SEG_8	–2475	–1075	57	DB_2	365	–2475
28	SEG_7	–2475	–1205	58	DB_3	515	–2475
29	SEG_6	–2475	–1335	59	DB_4	645	–2475
30	SEG_5	–2475	–1465	60	DB_5	795	–2475

HCD66702 Pad Location Coordinates (cont)

Pad No.	Pad Name	X (µm)	Y (µm)
61	DB_6	925	–2475
62	DB_7	1075	–2475
63	COM_1	1205	–2475
64	COM_2	1335	–2475
65	COM_3	1465	–2475
66	COM_4	1595	–2475
67	COM_5	1725	–2475
68	COM_6	1855	–2475
69	COM_7	1990	–2475
70	COM_8	2125	–2475
71	COM_9	2265	–2475
72	COM_{10}	2410	–2475
73	COM_{11}	2475	–2290
74	COM_{12}	2475	–2145
75	COM_{13}	2475	–2005
76	COM_{14}	2475	–1865
77	COM_{15}	2475	–1730
78	COM_{16}	2475	–1595
79	SEG_{100}	2475	–1465
80	SEG_{99}	2475	–1335
81	SEG_{98}	2475	–1205
82	SEG_{97}	2475	–1075
83	SEG_{96}	2475	–945
84	SEG_{95}	2475	–815
85	SEG_{94}	2475	–685
86	SEG_{93}	2475	–555
87	SEG_{92}	2475	–425
88	SEG_{91}	2475	–295
89	SEG_{90}	2475	–165
90	SEG_{89}	2475	–35

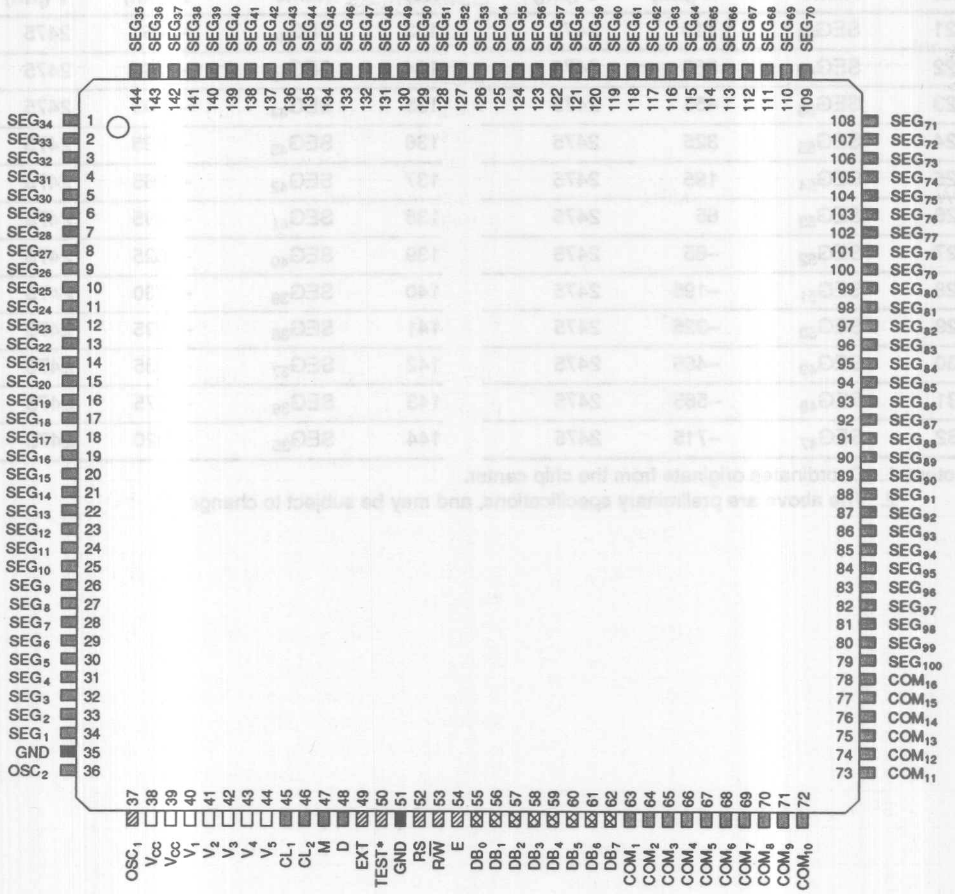
Pad No.	Pad Name	X (µm)	Y (µm)
91	SEG_{88}	2475	95
92	SEG_{87}	2475	225
93	SEG_{86}	2475	355
94	SEG_{85}	2475	485
95	SEG_{84}	2475	615
96	SEG_{83}	2475	745
97	SEG_{82}	2475	875
98	SEG_{81}	2475	1005
99	SEG_{80}	2475	1135
100	SEG_{79}	2475	1265
101	SEG_{78}	2475	1395
102	SEG_{77}	2475	1525
103	SEG_{76}	2475	1655
104	SEG_{75}	2475	1790
105	SEG_{74}	2475	1925
106	SEG_{73}	2475	2065
107	SEG_{72}	2475	2205
108	SEG_{71}	2475	2350
109	SEG_{70}	2320	2475
110	SEG_{69}	2175	2475
111	SEG_{68}	2035	2475
112	SEG_{67}	1895	2475
113	SEG_{66}	1760	2475
114	SEG_{65}	1625	2475
115	SEG_{64}	1495	2475
116	SEG_{63}	1365	2475
117	SEG_{62}	1235	2475
118	SEG_{61}	1105	2475
119	SEG_{60}	975	2475
120	SEG_{59}	845	2475

HCD66702 Pad Location Coordinates (cont)

Pad No.	Pad Name	X (µm)	Y (µm)	Pad No.	Pad Name	X (µm)	Y (µm)
121	SEG_{58}	715	2475	133	SEG_{46}	–845	2475
122	SEG_{57}	585	2475	134	SEG_{45}	–975	2475
123	SEG_{56}	455	2475	135	SEG_{44}	–1105	2475
124	SEG_{55}	325	2475	136	SEG_{43}	–1235	2475
125	SEG_{54}	195	2475	137	SEG_{42}	–1365	2475
126	SEG_{53}	65	2475	138	SEG_{41}	–1495	2475
127	SEG_{52}	–65	2475	139	SEG_{40}	–1625	2475
128	SEG_{51}	–195	2475	140	SEG_{39}	–1760	2475
129	SEG_{50}	–325	2475	141	SEG_{38}	–1895	2475
130	SEG_{49}	–455	2475	142	SEG_{37}	–2035	2475
131	SEG_{48}	–585	2475	143	SEG_{36}	–2175	2475
132	SEG_{47}	–715	2475	144	SEG_{35}	–2320	2475

Notes: 1. Coordinates originate from the chip center.
2. The above are preliminary specifications, and may be subject to change.

HD66702 Pin Arrangement



Note: * : Test pins to be grounded
□ : Power supply pins
■ : Power supply pins (ground)
▨ : Input pins
▦ : Output pins
⊠ : Input/Output pins

FP-144A
(top view)

Pin Functions

Table 1 Pin Functional Description

Signal	I/O	Device Interfaced with	Function
RS	I	MPU	Selects registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read)
$R/\overline{W}$	I	MPU	Selects read or write. 0: Write 1: Read
E	I	MPU	Starts data read/write
DB_4 to DB_7	I/O	MPU	Four high order bidirectional tristate data bus pins. Used for data transfer between the MPU and the LCD-II/E20. DB_7 can be used as a busy flag.
DB_0 to DB_3	I/O	MPU	Four low order bidirectional tristate data bus pins. Used for data transfer between the MPU and the LCD-II/E20. These pins are not used during 4-bit operation.
CL_1	O	HD44100	Clock to latch serial data D sent to the HD44100H driver
CL_2	O	HD44100	Clock to shift serial data D
M	O	HD44100	Switch signal for converting the liquid crystal drive waveform to AC
D	O	HD44100	Character pattern data corresponding to each segment signal
COM_1 to COM_{16}	O	LCD	Common signals that are not used are changed to non-selection waveforms. COM_9 to COM_{16} are non-selection waveforms at 1/8 duty factor and COM_{12} to COM_{16} are non-selection waveforms at 1/11 duty factor.
SEG_1 to SEG_{100}	O	LCD	Segment signals
V_1 to V_5	—	Power supply	Power supply for LCD drive
V_{CC}, GND	—	Power supply	V_{CC}: +5 V or +3 V, GND: 0 V
TEST	I	—	Test pin, which must be grounded
EXT	I	—	0: Enables extension driver control signals CL_1, CL_2, M, and D to be output from its corresponding pins. 1: Drives CL_1, CL_2, M, and D as tristate, lowering power dissipation.
OSC_1, OSC_2	—	—	Pins for connecting the registers of the internal clock oscillation. When the pin input is an external clock, it must be input to OSC_1.

Function Description

Registers

The HD66702 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can only be written from the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into DD RAM or CG RAM by an internal operation. The DR is also used for data storage when reading data from DD RAM or CG RAM. When address information is written into the IR, data is read and then stored into the DR from DD RAM or CG RAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. By the register selector (RS) signal, these two registers can be selected (table 2).

Busy Flag (BF)

When the busy flag is 1, the HD66702 is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/$\overline{W}$ = 1 (table 2), the busy flag is output to DB_7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to both DD RAM and CG RAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of either DD RAM or CG RAM is also determined concurrently by the instruction.

After writing into (reading from) DD RAM or CG RAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB_0 to DB_6 when RS = 0 and R/$\overline{W}$ = 1 (table 2).

Table 2 Register Selection

RS	R/$\overline{W}$	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0 to DB_6)
1	0	DR write as an internal operation (DR to DD RAM or CG RAM)
1	1	DR read as an internal operation (DD RAM or CG RAM to DR)

Display Data RAM (DD RAM)

Display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its extended capacity is 80×8 bits, or 80 characters. The area in display data RAM (DD RAM) that is not used for display can be used as general data RAM. See figure 1 for the relationships between DD RAM addresses and positions on the liquid crystal display.

The DD RAM address (A_{DD}) is set in the address counter (AC) as hexadecimal.

- 1-line display (N = 0) (figure 2)

  — Case 1: When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the HD66702, 20 characters are displayed. See figure 3.

  When the display shift operation is performed, the DD RAM address shifts. See figure 3.

  — Case 2: For a 28-character display, the HD66702 can be extended using one HD44100 and displayed. See figure 4.

  When the display shift operation is performed, the DD RAM address shifts. See figure 4.

  — Case 3: The relationship between the display position and DD RAM address when the number of display digits is increased through the use of two or more HD44100s can be considered as an extension of case #2.

  Since the increase can be eight digits per additional HD44100, up to 80 digits can be displayed by externally connecting eight HD44100s. See figure 5.

	High order bits			Low order bits			
AC (hexadecimal)	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Example: DD RAM address 4E

1	0	0	1	1	1	0

Figure 1 DD RAM Address

Display position (digit)	1	2	3	4	5		79	80
DD RAM address (hexadecimal)	00	01	02	03	04	....	4E	4F

Figure 2 1-Line Display

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
DD RAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
For shift left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
For shift right	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12

Figure 3 1-Line by 20-Character Display Example

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
DD RAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B
	LCD-II/E20 display																				HD44100 display							
For shift left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
For shift right	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A

Figure 4 1-Line by 28-Character Display Example

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28		77	78	79	80
DD RAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	....	4C	4D	4E	4F
	LCD-II/E20 display																				1st HD44100 display									8th HD44100 display			

Figure 5 1-Line by 80-Character Display Example

- 2-line display (N = 1) (figure 6)
  - — Case 1: When the number of display characters is less than 40 × 2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the HD66702 is used, 20 characters × 2 lines are displayed. See figure 7.

    When display shift operation is performed, the DD RAM address shifts. See figure 7.

Display position	1	2	3	4	5		39	40
DD RAM address (hexadecimal)	00	01	02	03	04	....	26	27
	40	41	42	43	44	....	66	67

Figure 6 2-Line Display

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
DD RAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
For shift left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54
For shift right	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52

Figure 7 2-Line by 20-Character Display Example

— Case 2: For a 28-character × 2-line display, the HD66702 can be extended using one HD44100. See figure 8.

When display shift operation is performed, the DD RAM address shifts. See figure 8.

— Case 3: The relationship between the display position and DD RAM address when the number of display digits is increased by using two or more HD44100s, can be considered as an extension of case #2. See figure 9.

Since the increase can be 8 digits × 2 lines for each additional HD44100, up to 40 digits × 2 lines can be displayed by externally connecting three HD44100s.

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
DD RAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B
	LCD-II/E20 display																				HD44100 display							
For shift left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C
For shift right	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A

Figure 8 2-Line by 28-Character Display Example

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28		37	38	39	40
DD RAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	....	24	25	26	27
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	....	64	65	66	67
	LCD-II/E20 display																				1st HD44100 display									3rd HD44100 display			

Figure 9 2-Line by 40-Character Display Example

Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 7 dot or 5 × 10 dot character patterns from 8-bit character codes (table 5). It can generate 160 5 × 7 dot character patterns and 32 5 × 10 dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CG RAM)

In the character generator RAM, the user can rewrite character patterns by program. For 5 × 7 dots, eight character patterns can be written, and for 5 × 10 dots, four character patterns can be written.

Write the character codes at the addresses shown as the left column of table 5 to show the character patterns stored in CG RAM.

See table 6 for the relationship between CG RAM addresses and data and display patterns.

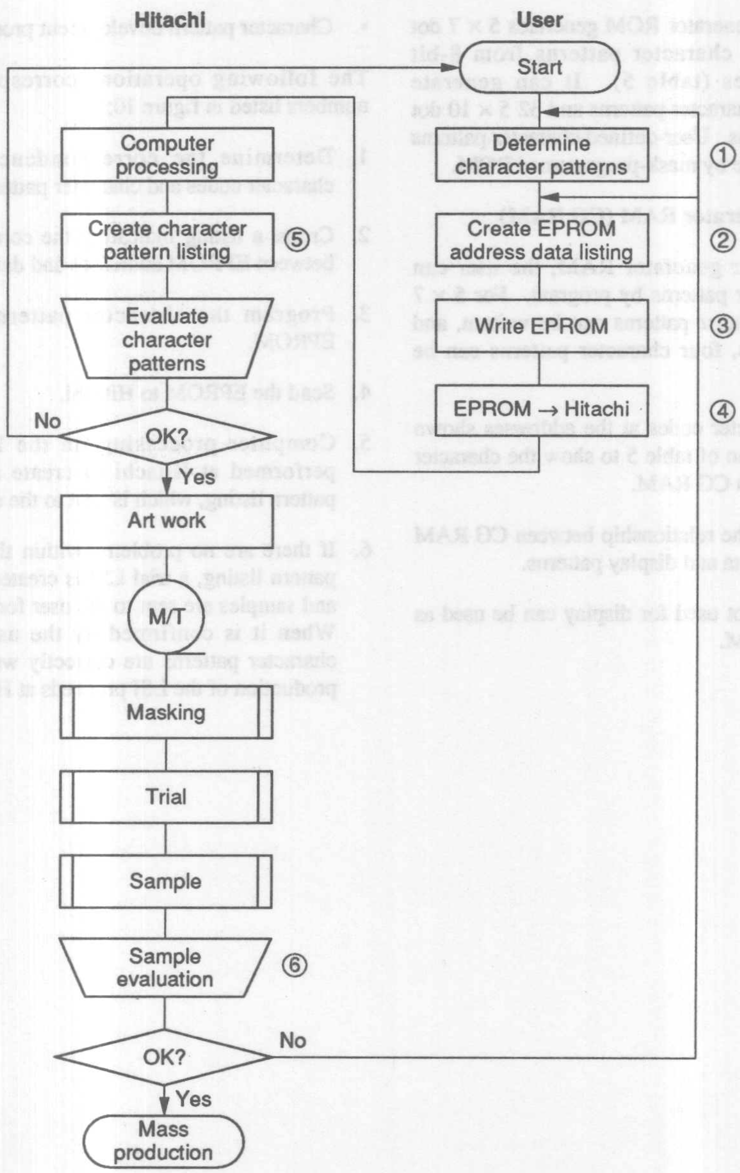
Areas that are not used for display can be used as general data RAM.

Modifying Character Patterns

- Character pattern development procedure

The following operations correspond to the numbers listed in figure 10:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into the EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing on the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI proceeds at Hitachi.



Note: For a description of the numbers used in this figure, refer to the preceding page.

Figure 10 Character Pattern Development Procedure

- Programming character patterns

  This section explains the correspondence between addresses and data used to program character patterns in EPROM. The LCD-II/E20 character generator ROM can generate 160 5 × 7 dot character patterns and 32 5 × 10 dot character patterns for a total of 192 different character patterns.

— 5 × 7 dot character pattern

EPROM address data and character pattern data correspond with each other to form a 5 × 7 dot character pattern (table 3).

Table 3 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 7 dots)

EPROM Address											Data				
															LSB
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0
0	1	0	1	0	0	1	0	0	0	0	1	1	1	1	0
								0	0	1	1	0	0	0	1
								0	1	0	1	0	0	0	1
								0	1	1	1	1	1	1	0
								1	0	0	1	0	1	0	0
								1	0	1	1	0	0	1	0
								1	1	0	1	0	0	0	1
								1	1	1	0	0	0	0	0 ← Fill line 8 (cursor position) with 0s
Character code								Line position							

Notes: 1. EPROM addresses A_{10} to A_3 correspond to a character code.
2. EPROM addresses A_2 to A_0 specify a line position of the character pattern.
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. A lit display position (black) corresponds to a 1.
5. Line 8 (cursor position) of the character pattern must be blanked with 0s.
6. EPROM data O_5 to O_7 are not used.

— 5 × 10 dot character pattern

EPROM address data and character pattern data correspond with each other to form a 5 × 10 dot character pattern (table 4).

— Handling unused character patterns

1. **EPROM data outside the character pattern area:** Ignored by the character generator ROM for display operation so 0 or 1 is arbitrary.

2. **EPROM data in CG RAM area:** Ignored by the character generator ROM for display operation so 0 or 1 is arbitrary.

3. **EPROM data used when the user does not use any HD66702 character pattern:** According to the user application, handled in one of the two ways listed as follows.

   i. **When unused character patterns are not programmed:** If an unused character code is written into DD RAM, all its dots are lit. By not programing a character pattern, all of its bits become lit. (This is due to the EPROM being filled with 1s after it is erased.)

   ii. **When unused character patterns are programmed as 0s:** Nothing is displayed even if unused character codes are written into DD RAM. (This is equivalent to a space.)

Table 4 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 10 dots)

EPROM Address											Data				LSB
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0
								0	0	0	0	0	0	0	0
								0	0	1	0	0	0	0	0
								0	1	0	0	1	1	0	1
1	1	1	1	0	0	0	1	0	1	1	1	0	0	1	1
								1	0	0	1	0	0	0	1
								1	0	1	1	0	0	0	1
								1	1	0	0	1	1	1	1
								1	1	1	0	0	0	0	1
1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0 ← Fill line 11 (cursor position) with 0s

Character code — Line position

Notes: 1. EPROM addresses A_{10} to A_3 correspond to a character code. Set A_8 and A_9 of character pattern lines 9, 10, and 11 to 0s.
2. EPROM addresses A_2 to A_0 specify a line position of the character pattern.
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. A lit display position (black) corresponds to a 1.
5. Blank out line 11 (cursor position) of the character pattern with 0s.
6. EPROM data O_5 to O_7 are not used.

Table 5 Correspondence between Character Codes and Character Patterns (ROM code: A00)

Lower 4 Bits \ Upper 4 Bits	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)		0	@	P	`	p		ー	タ	ミ	α	p
xxxx0001	(2)	!	1	A	Q	a	q	。	ア	チ	ム	ä	q
xxxx0010	(3)	"	2	B	R	b	r	「	イ	ツ	メ	β	θ
xxxx0011	(4)	#	3	C	S	c	s	」	ウ	テ	モ	ε	∞
xxxx0100	(5)	$	4	D	T	d	t	、	エ	ト	ヤ	μ	Ω
xxxx0101	(6)	%	5	E	U	e	u	・	オ	ナ	ユ	σ	ü
xxxx0110	(7)	&	6	F	V	f	v	ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	(8)	'	7	G	W	g	w	ァ	キ	ヌ	ラ	g	π
xxxx1000	(1)	(	8	H	X	h	x	ィ	ク	ネ	リ	√	x̄
xxxx1001	(2)	)	9	I	Y	i	y	ゥ	ケ	ノ	ル	⁻¹	y
xxxx1010	(3)	*	:	J	Z	j	z	ェ	コ	ハ	レ	j	千
xxxx1011	(4)	+	;	K	[	k	{	ォ	サ	ヒ	ロ	ˣ	万
xxxx1100	(5)	,	<	L	¥	l	|	ャ	シ	フ	ワ	¢	円
xxxx1101	(6)	-	=	M	]	m	}	ュ	ス	ヘ	ン	£	÷
xxxx1110	(7)	.	>	N	^	n	→	ョ	セ	ホ	゛	ñ	
xxxx1111	(8)	/	?	O	_	o	←	ッ	ソ	マ	゜	ö	█

Note: The user can specify any pattern for character-generator RAM.

Table 5 Correspondence between Character Codes and Character Patterns (ROM code: A01)

Lower 4 Bits \ Upper 4 Bits	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)		0	@	P	`	p	[illegible]	ー	タ	ミ	α	p
xxxx0001	(2)	!	1	A	Q	a	q	。	ア	チ	ム	ä	q
xxxx0010	(3)	"	2	B	R	b	r	「	イ	ツ	メ	β	θ
xxxx0011	(4)	#	3	C	S	c	s	」	ウ	テ	モ	ε	∞
xxxx0100	(5)	$	4	D	T	d	t	、	エ	ト	ヤ	μ	Ω
xxxx0101	(6)	%	5	E	U	e	u	・	オ	ナ	ユ	σ	ü
xxxx0110	(7)	&	6	F	V	f	v	ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	(8)	'	7	G	W	g	w	ァ	キ	ヌ	ラ	g	π
xxxx1000	(1)	(	8	H	X	h	x	ィ	ク	ネ	リ	√	x̄
xxxx1001	(2)	)	9	I	Y	i	y	ゥ	ケ	ノ	ル	$^{-1}$	y
xxxx1010	(3)	*	:	J	Z	j	z	ェ	コ	ハ	レ	j	千
xxxx1011	(4)	+	;	K	[	k	{	ォ	サ	ヒ	ロ	ˣ	万
xxxx1100	(5)	,	<	L	¥	l	|	ャ	シ	フ	ワ	¢	円
xxxx1101	(6)	-	=	M	]	m	}	ュ	ス	ヘ	ン	£	÷
xxxx1110	(7)	.	>	N	^	n	→	ョ	セ	ホ	゛	ñ	[illegible]
xxxx1111	(8)	/	?	O	_	o	←	ッ	ソ	マ	゜	ö	█

Table 5 Correspondence between Character Codes and Character Patterns (ROM code: A02)

Upper 4 Bits / Lower 4 Bits	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)		0	@	P	`	p	▪	“	À	Ð	à	ð
xxxx0001	(2)	!	1	A	Q	a	q	¡	”	Á	Ñ	á	ñ
xxxx0010	(3)	"	2	B	R	b	r	¢	Σ	Â	Ò	â	ò
xxxx0011	(4)	#	3	C	S	c	s	£	Ω	Ã	Ó	ã	ó
xxxx0100	(5)	$	4	D	T	d	t	¤	α	Ä	Ô	ä	ô
xxxx0101	(6)	%	5	E	U	e	u	¥	[illegible]	Å	Õ	å	õ
xxxx0110	(7)	&	6	F	V	f	v	¦	∃	Æ	Ö	æ	ö
xxxx0111	(8)	'	7	G	W	g	w	¶	ʊ	Ç	×	ç	÷
xxxx1000	(1)	(	8	H	X	h	x	§	ă	È	Ø	è	ø
xxxx1001	(2)	)	9	I	Y	i	y	→	Ŏ	É	Ù	é	ù
xxxx1010	(3)	*	:	J	Z	j	z	←	Ĕ	Ê	Ú	ê	ú
xxxx1011	(4)	+	;	K	[	k	{	«	Ă	Ë	Û	ë	û
xxxx1100	(5)	,	<	L	¥	l	|	»	š	Ì	Ü	ì	ü
xxxx1101	(6)	-	=	M	]	m	}	↑	ž	Í	Ý	í	ý
xxxx1110	(7)	.	>	N	^	n	~	↓	ş	Î	Þ	î	þ
xxxx1111	(8)	/	?	O	_	o	±	'	¿	Ï	ß	ï	ÿ

Table 6 Relationship between CG RAM Addresses, Character Codes (DD RAM) and Character Patterns (CG RAM data)

For 5 × 7 dot character patterns

Character Codes (DD RAM data)	CG RAM Address		Character Patterns (CG RAM data)		
7 6 5 4 3 2 1 0 High Low	5 4 3 2 1 0 High Low		7 6 5 4 3 2 1 0 High Low		
0 0 0 0 * 0 0 0	0 0 0	0 0 0	* * *	1 1 1 1 0	Character pattern
		0 0 1		1 0 0 0 1	
		0 1 0		1 0 0 0 1	
		0 1 1		1 1 1 1 0	
		1 0 0		1 0 1 0 0	
		1 0 1		1 0 0 1 0	
		1 1 0		1 0 0 0 1	
		1 1 1	* * *	0 0 0 0 0	Cursor position
0 0 0 0 * 0 0 1	0 0 1	0 0 0	* * *	1 0 0 0 1	
		0 0 1		0 1 0 1 0	
		0 1 0		1 1 1 1 1	
		0 1 1		0 0 1 0 0	
		1 0 0		1 1 1 1 1	
		1 0 1		0 0 1 0 0	
		1 1 0		0 0 1 0 0	
		1 1 1	* * *	0 0 0 0 0	
		0 0 0	* * *		
		0 0 1			
0 0 0 0 * 1 1 1	1 1 1				
		1 0 0			
		1 0 1			
		1 1 0			
		1 1 1	* * *		

Notes:
1. Character code bits 0 to 2 correspond to CG RAM address bits 3 to 5 (3 bits: 8 types).
2. CG RAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.
   Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CG RAM data bits 0 to 4 (bit 4 being at the left).
   Since CG RAM data bits 5 to 7 are not used for display, they can be used for general data RAM.
4. As shown tables 5 and 6, CG RAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.

* Indicates no effect.

Table 6 Relationship between CG RAM Addresses, Character Codes (DD RAM) and Character Patterns (CG RAM data) (cont)

For 5 × 10 dot character patterns

Character Codes (DD RAM data) 7 6 5 4 3 2 1 0 (High → Low)	CG RAM Address 5 4 (High)	CG RAM Address 3 2 1 0 (Low)	Character Patterns (CG RAM data) 7 6 5 (High)	Character Patterns (CG RAM data) 4 3 2 1 0 (Low)	
		0 0 0 0	* * *	0 0 0 0 0	Character pattern
		0 0 0 1		0 0 0 0 0	
		0 0 1 0		1 0 1 1 0	
		0 0 1 1		1 1 0 0 1	
		0 1 0 0		1 0 0 0 1	
0 0 0 0 * 0 0 *	0 0	0 1 0 1		1 0 0 0 1	
		0 1 1 0		1 1 1 1 0	
		0 1 1 1		1 0 0 0 0	
		1 0 0 0		1 0 0 0 0	
		1 0 0 1		1 0 0 0 0	
		1 0 1 0	* * *	0 0 0 0 0	Cursor position
		1 0 1 1	* * *	* * * * *	
		1 1 0 0			
		1 1 0 1			
		1 1 1 0			
		1 1 1 1	* * *	* * * * *	
		0 0 0 0	* * *		
		0 0 0 1			
…	…	…	…	…	
0 0 0 0 * 1 1 *	1 1	1 0 0 1			
		1 0 1 0	* * *		
		1 0 1 1	* * *	* * * * *	
		1 1 0 0			
		1 1 0 1			
		1 1 1 0			
		1 1 1 1	* * *	* * * * *	

Notes: 1. Character code bits 1 and 2 correspond to CG RAM address bits 4 and 5 (2 bits: 4 types).
2. CG RAM address bits 0 to 3 designate the character pattern line position. The 11th line is the cursor position and its display is formed by a logical OR with the cursor.
Maintain the 11th line data corresponding to the cursor display positon at 0 as the cursor display.
If the 11th line data is 1, 1 bits will light up the 11th line regardless of the cursor presence.
Since lines 12 to 16 are not used for display, they can be used for general data RAM.
3. Character pattern row positions are the same as 5 × 7 dot character pattern positions.
4. CG RAM character patterns are selected when character code bits 4 to 7 are all 0.
However, since character code bits 0 and 3 have no effect, the P display example above can be selected by character codes 00H, 01H, 08H, and 09H.
5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.
* Indicates no effect.

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DD RAM, CG ROM and CG RAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DD RAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area. This circuit also generates timing signals for the operation of the externally connected HD44100 driver.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 100 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the HD44100 driver. Character pattern data is sent serially through a 100-bit shift register and latched when all needed data has arrived. The latched data then enables the driver to generate drive waveform outputs. The serial data can be sent to externally cascaded HD44100s used for displaying extended digit numbers.

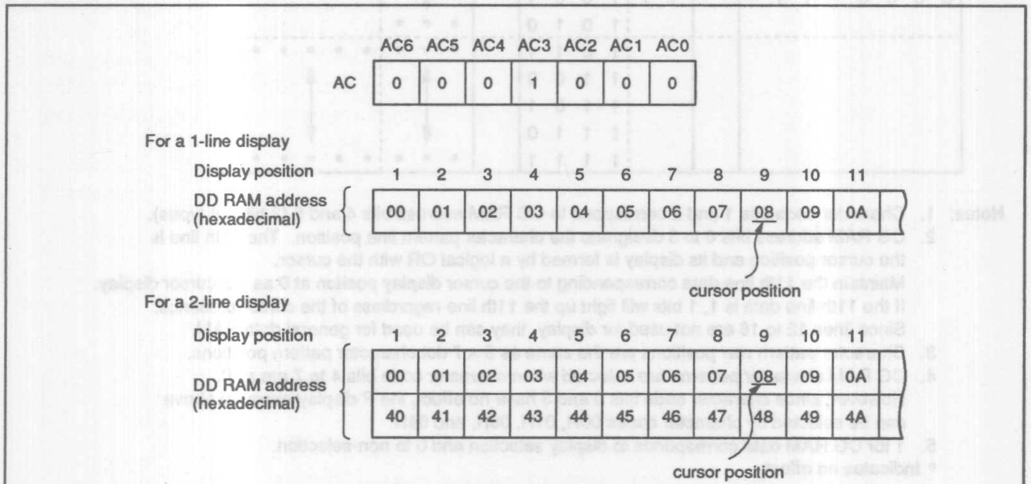
Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD66702 drives from the head display. The rest of the display, corresponding to latter addresses, are added with each additional HD44100.

Cursor/Blink Control Circuit

The cursor/blink control circuit generates the cursor or character blinking. The cursor or the blinking will appear with the digit located at the display data RAM (DD RAM) address set in the address counter (AC).

For example (figure 11), when the address counter is 08H, the cursor position is displayed at DD RAM address 08H.



Note: * The cursor or blinking appears when the address counter (AC) selects the character generator RAM (CG RAM). However, the cursor and blinking become meaningless. The cursor or blinking is displayed in the meaningless position when the AC is a CG RAM address.

Figure 11 Cursor/Blink Display Example

Interfacing to the MPU

The HD66702 can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB_4 to DB_7) are used for transfer. Bus lines DB_0 to DB_3 are disabled. The data transfer between the HD66702 and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB_4 to DB_7) are transferred before the four low order bits (for 8-bit operation, DB_0 to DB_3).

  The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

- For 8-bit interface data, all eight bus lines (DB_0 to DB_7) are used.

Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD66702 when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 10 ms after V_{CC} rises to 4.5 V.

1. Display clear
2. Function set:
   DL = 1; 8-bit interface data
   N = 0; 1-line display
   F = 0; 5 × 7 dot character font
3. Display on/off control:
   D = 0; Display off
   C = 0; Cursor off
   B = 0; Blinking off
4. Entry mode set:
   I/D = 1; Increment by 1
   S = 0; No shift

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD66702. For such a case, initialization must be performed by the MPU as explained in the section, Initializing by Instruction.

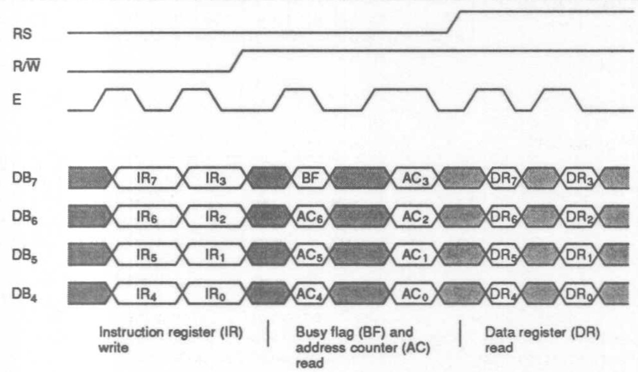


Figure 12 4-Bit Transfer Example

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66702 can be controlled by the MPU. Before starting the internal operation of the HD66702, control information is temporarily stored into these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD66702 is determined by signals sent from the MPU. These signals, which include register selection (RS), read/write ($R/\overline{W}$), and the data bus (DB_0 to DB_7), make up the HD66702 instructions (table 7). There are four categories of instructions that:

- Designate HD66702 functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66702 RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (table 12) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the HD66702 is not in the busy state (BF = 0) before sending an instruction from the MPU to the HD66702. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to table 7 for the list of each instruction execution time.

Table 7 Instructions

	Code											
Instruction	**RS**	**R/$\overline{W}$**	**DB_7**	**DB_6**	**DB_5**	**DB_4**	**DB_3**	**DB_2**	**DB_1**	**DB_0**	**Description**	**Execution Time (max) (when f_{cp} or f_{OSC} is 320 kHz)**
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.28 ms
Return home	0	0	0	0	0	0	0	0	1	—	Sets DD RAM address 0 in address counter. Also returns display from being shifted to original position. DD RAM contents remain unchanged.	1.28 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	31 µs
Display on/off control	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	31 µs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DD RAM contents.	31 µs
Function set	0	0	0	0	1	DL	N	F	—	—	Sets interface data length (DL), number of display lines (L), and character font (F).	31 µs
Set CG RAM address	0	0	0	1	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	Sets CG RAM address. CG RAM data is sent and received after this setting.	31 µs
Set DD RAM address	0	0	1	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	Sets DD RAM address. DD RAM data is sent and received after this setting.	31 µs
Read busy flag & address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs

Table 7 Instructions (cont)

Instruction	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Description	Execution Time (max) (when f_{cp} or f_{OSC} is 320 kHz)
			Code									
Write data to CG or DD RAM	1	0	Write data								Writes data into DD RAM or CG RAM.	31 µs t_{ADD} = 4.7 µs*
Read data from CG or DD RAM	1	1	Read data								Reads data from DD RAM or CG RAM.	31 µs t_{ADD} = 4.7 µs*
	I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits, DL = 0: 4 bits N = 1: 2 lines, N = 0: 1 line F = 1: 5 × 10 dots, F = 0: 5 × 7 dots BF = 1: Internally operating BF = 0: Instructions acceptable										DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM address A_{DD}: DD RAM address (corresponds to cursor address) AC: Address counter used for both DD and CG RAM addresses	Execution time changes when frequency changes Example: When f_{cp} or f_{OSC} is 270 kHz, $31\ \mu s \times \frac{320}{270} = 37\ \mu s$

Note: — indicates no effect.

* After execution of the CG RAM/DD RAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In figure 13, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

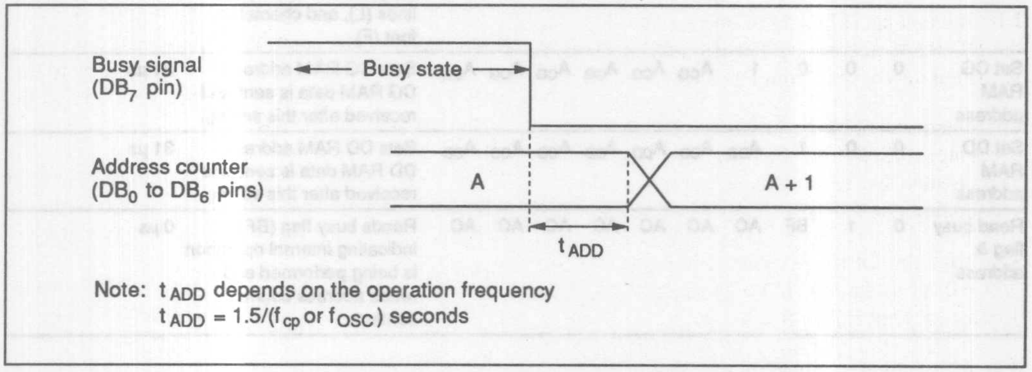


Figure 13 Address Counter Update

Instruction Description

Clear Display

Clear display writes space code 20H (character pattern for character code 20H must be a blank pattern) into all DD RAM addresses. It then sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change.

Return Home

Return home sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DD RAM contents do not change.

The cursor or blinking go to the left edge of the display (in the first line if 2 lines are displayed).

Entry Mode Set

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from DD RAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DD RAM. Also, writing into or reading out from CG RAM does not shift the display.

Display On/Off Control

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in DD RAM, but can be displayed instantly by setting D to 1.

C: The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5×7 dot character font selection and in the 11th line for the 5×10 dot character font selection (figure 16).

B: The character indicated by the cursor blinks when B is 1 (figure 16). The blinking is displayed as switching between all blank dots and displayed characters at a speed of 320-ms intervals when f_{cp} or f_{OSC} is 320 kHz. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to f_{OSC} or the reciprocal of f_{cp}. For example, when f_{cp} is 270 kHz, $320 \times 320/270 = 379.2$ ms.)

Cursor or Display Shift

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (table 8). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. Note that the first and second line displays will shift at the same time.

When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position.

The address counter (AC) contents will not change if the only action performed is a display shift.

Function Set

DL: Sets the interface data length. Data is sent or received in 8-bit lengths (DB_7 to DB_0) when DL is 1, and in 4-bit lengths (DB_7 to DB_4) when DL is 0.

When 4-bit length is selected, data must be sent or received twice.

N: Sets the number of display lines.

F: Sets the character font.

Note: Perform the function at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, the function set instruction cannot be executed unless the interface data length is changed.

Set CG RAM Address

Set CG RAM address sets the CG RAM address binary AAAAAA into the address counter.

Data is then written to or read from the MPU for CG RAM.

		RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Clear display	Code	0	0	0	0	0	0	0	0	0	1	
Return home	Code	0	0	0	0	0	0	0	0	1	*	Note: * Don't care.
Entry mode set	Code	0	0	0	0	0	0	0	1	I/D	S	
Display on/off control	Code	0	0	0	0	0	0	1	D	C	B	

Figure 14

		RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Cursor or display shift	Code	0	0	0	0	0	1	S/C	R/L	*	*	Note: * Don't care.
Function set	Code	0	0	0	0	1	DL	N	F	*	*	Note: * Don't care.
Set CG RAM address	Code	0	0	0	1	A	A	A	A	A	A	
						Highest order bit					Lowest order bit	

Figure 15

Set DD RAM Address

Set DD RAM address sets the DD RAM address binary AAAAAAA into the address counter.

Data is then written to or read from the MPU for DD RAM.

However, when N is 0 (1-line display), AAAAAAA can be 00H to 4FH. When N is 1 (2-line display), AAAAAAA can be 00H to 27H for the first line, and 40H to 67H for the second line.

Read Busy Flag and Address

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. The address contents are the same as for instructions set CG RAM address and set DD RAM address.

Table 8 Shift Function

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Table 9 Function Set

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5 × 7 dots	1/8	
0	1	1	5 × 10 dots	1/11	
1	*	2	5 × 7 dots	1/16	Cannot display two lines for 5 × 10 dot character font

Note: * Indicates don't care.

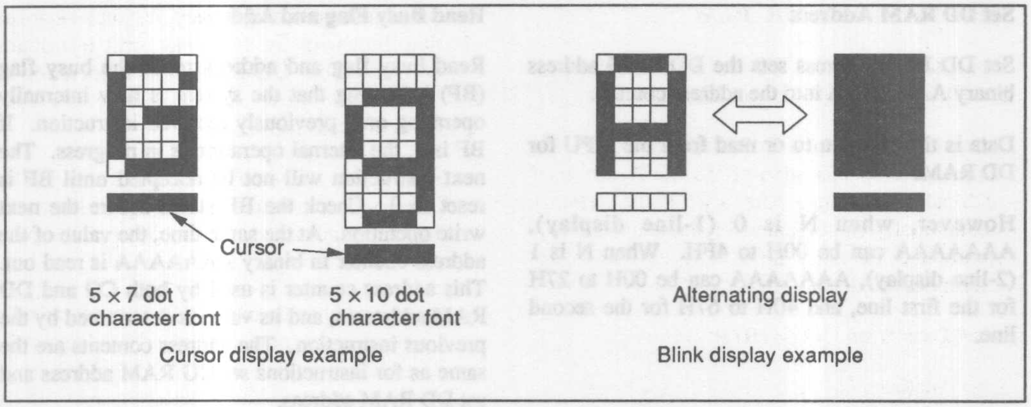


Figure 16 Cursor and Blinking

Set DD RAM address

	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	1	A	A	A	A	A	A	A
				Highest order bit						Lowest order bit

Read busy flag and address

	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	1	BF	A	A	A	A	A	A	A
				Highest order bit						Lowest order bit

Figure 17

Write Data to CG or DD RAM

Write data to CG or DD RAM writes 8-bit binary data DDDDDDDD to CG or DD RAM.

To write into CG or DD RAM is determined by the previous specification of the CG RAM or DD RAM address setting. After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift.

Read Data from CG or DD RAM

Read data from CG or DD RAM reads 8-bit binary data DDDDDDDD from CG or DD RAM.

The previous designation determines whether CG or DD RAM is to be read. Before entering this read instruction, either CG RAM or DD RAM address set instruction must be executed. If not executed, the first read data will be invalid. When serially executing read instructions, the next address data is normally read from the second read. The address set instructions need not be executed just before this read instruction when shifting the cursor by the cursor shift instruction (when reading out DD RAM). The operation of the cursor shift instruction is the same as the set DD RAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented by 1 after the write instructions to CG RAM or DD RAM are executed. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to correctly read data, execute either the address set instruction or cursor shift instruction (only with DD RAM), then just before reading the desired data, execute the read instruction from the second time the read instruction is sent.

Write data to CG or DD RAM

	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	D	D	D	D	D	D	D	D

← Higher order bits   Lower order bits →

Read data from CG or DD RAM

	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	1	D	D	D	D	D	D	D	D

← Higher order bits   Lower order bits →

Figure 18

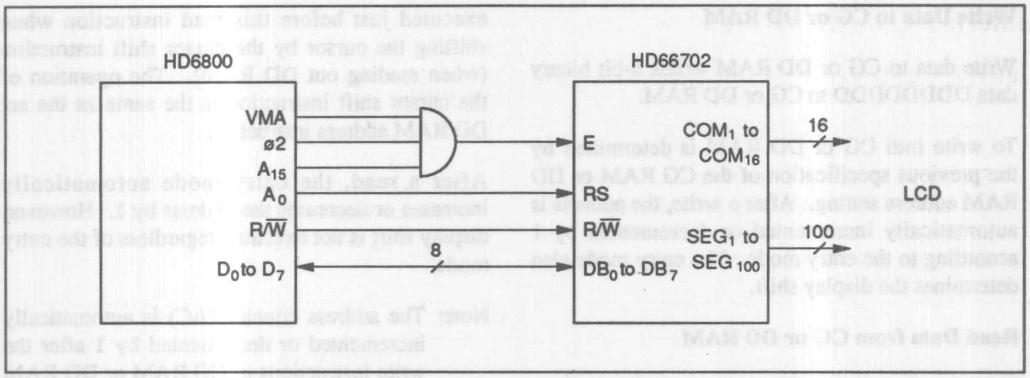


Figure 19 8-Bit MPU Interface

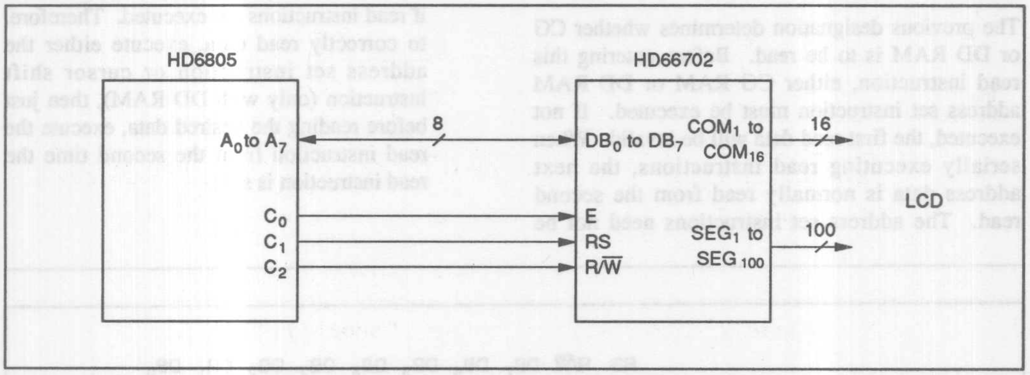


Figure 20 HD6805 Interface

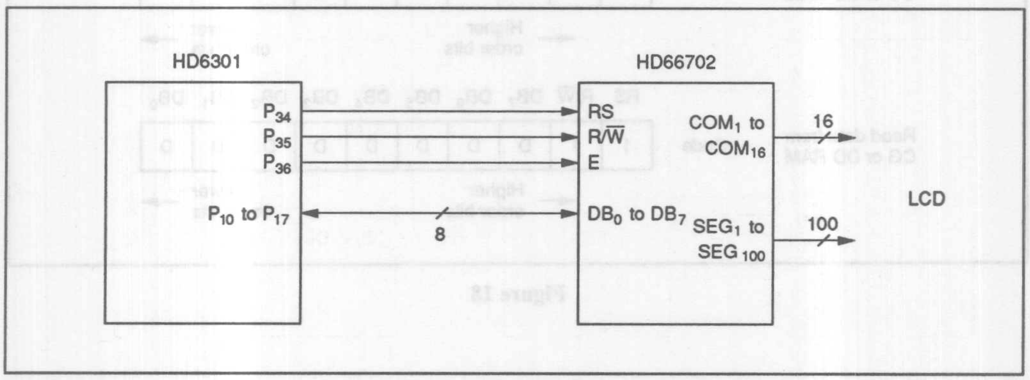


Figure 21 HD6301 Interface

Interfacing the HD66702

Interface to MPUs

- Interfacing to an 8-bit MPU through a PIA

  See figure 23 for an example of using a PIA or I/O port (for a single-chip microcomputer) as an interface device. The input and output of the device is TTL compatible.

  In this example, PB_0 to PB_7 are connected to the data bus DB_0 to DB_7, and PA_0 to PA_2 are connected to E, R/W, and RS, respectively.

  Pay careful attention to the timing relationship between E and the other signals when reading or writing data using a PIA for the interface.

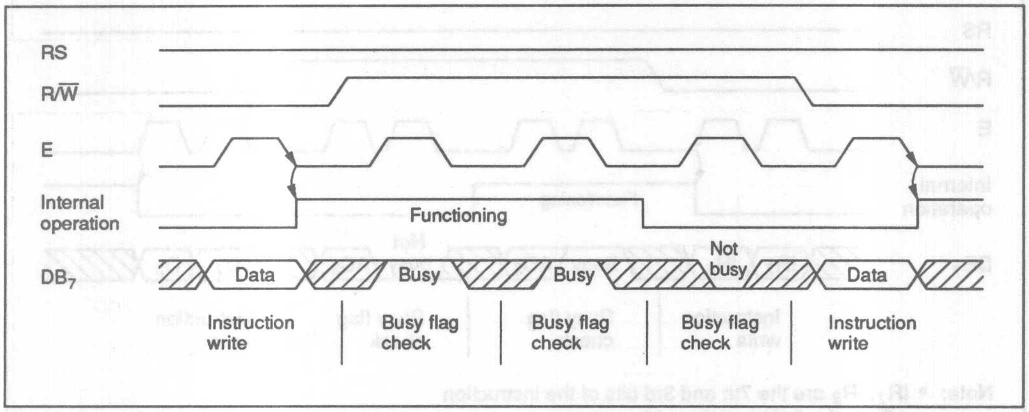


Figure 22 Example of Busy Flag Check Timing Sequence

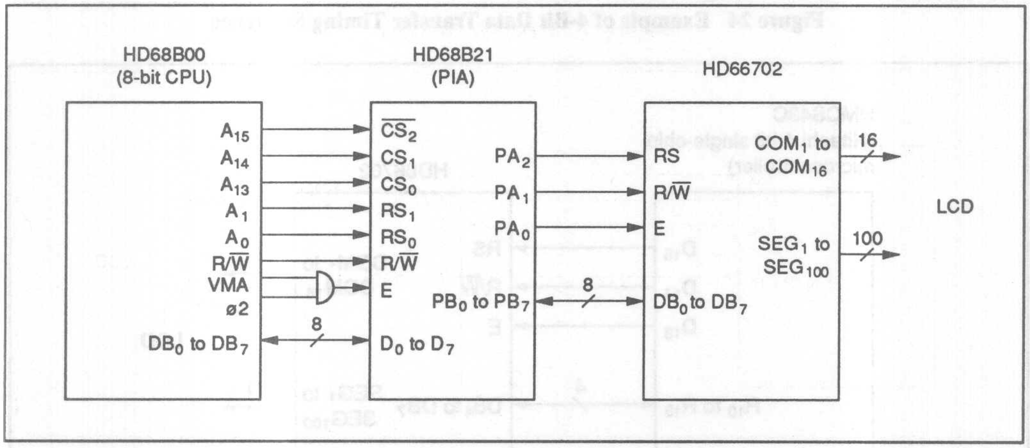


Figure 23 Example of Interface to HD68B00 Using PIA (HD68B21)

- Interfacing to a 4-bit MPU

The HD66702 can be connected to the I/O port of a 4-bit MPU. If the I/O port has enough bits, 8-bit data can be transferred. Otherwise, one data transfer must be made in two operations for 4-bit data. In this case, the timing sequence becomes somewhat complex. (See figure 24.)

See figure 25 for an interface example to the HMCS43C.

Note that two cycles are needed for the busy flag check as well as for the data transfer. The 4-bit operation is selected by the program.

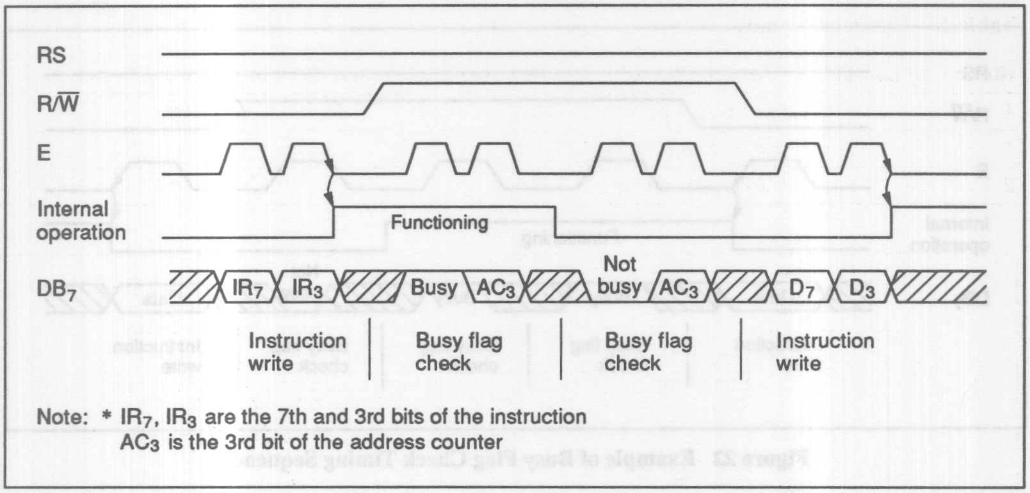


Figure 24 Example of 4-Bit Data Transfer Timing Sequence

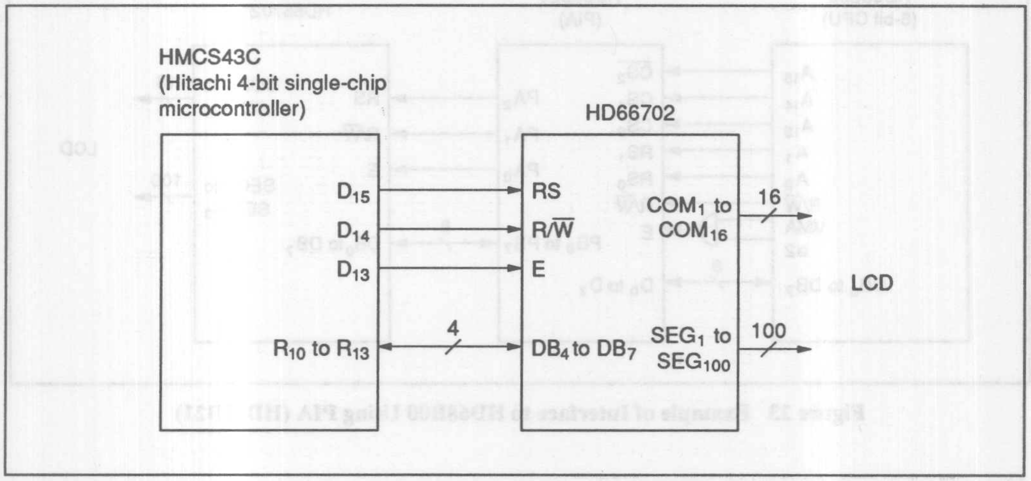


Figure 25 Example of Interface to HMCS43C

Interface to Liquid Crystal Display

Character Font and Number of Lines: The HD66702 can perform two types of displays, 5 × 7 dot and 5 × 10 dot character fonts, each with a cursor.

Up to two lines are displayed for 5 × 7 dots and one line for 5 × 10 dots. Therefore, a total of three types of common signals are available (table 10).

The number of lines and font types can be selected by the program. (See table 7, Instructions.)

Connection to HD66702 and Liquid Crystal Display: See figure 26 for the connection examples.

Table 10 Common Signals

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 × 7 dots + cursor	8	1/8
1	5 × 10 dots + cursor	11	1/11
2	5 × 7 dots + cursor	16	1/16

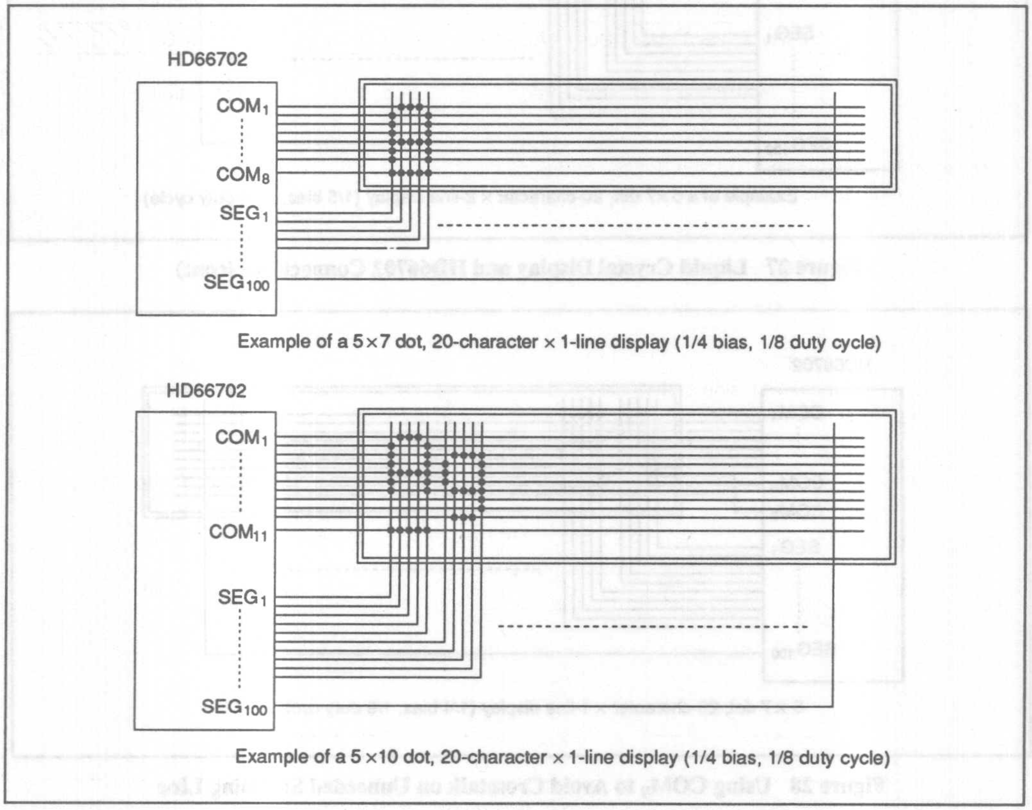
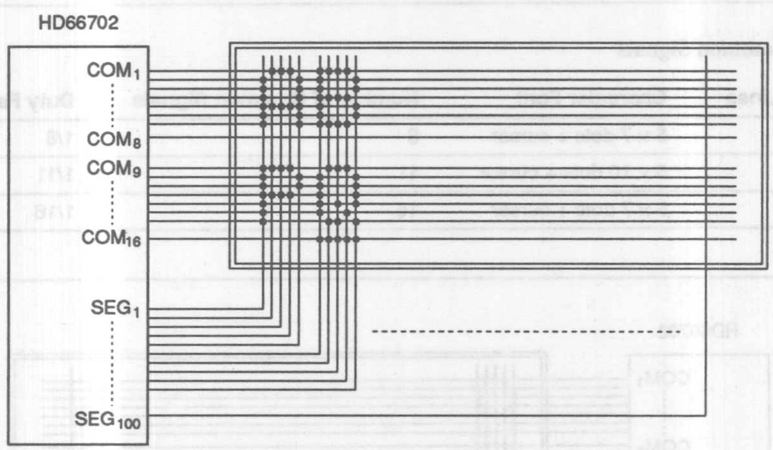


Figure 26 Liquid Crystal Display and HD66702 Connections

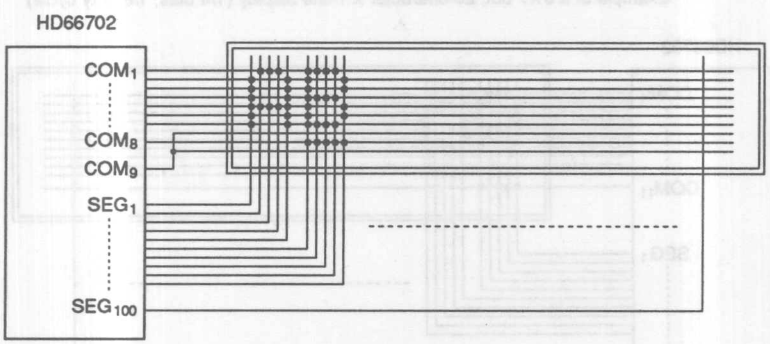
Since five segment signal lines can display one digit, one HD66702 can display up to 20 digits for a 1-line display and 40 digits for a 2-line display.

The examples in figure 26 have unused common signal pins, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, connect the extra scanning lines to these common signal pins to avoid any undesirable effects due to crosstalk during the floating state (figure 28).



Example of a 5 × 7 dot, 20-character × 2-line display (1/5 bias, 1/16 duty cycle)

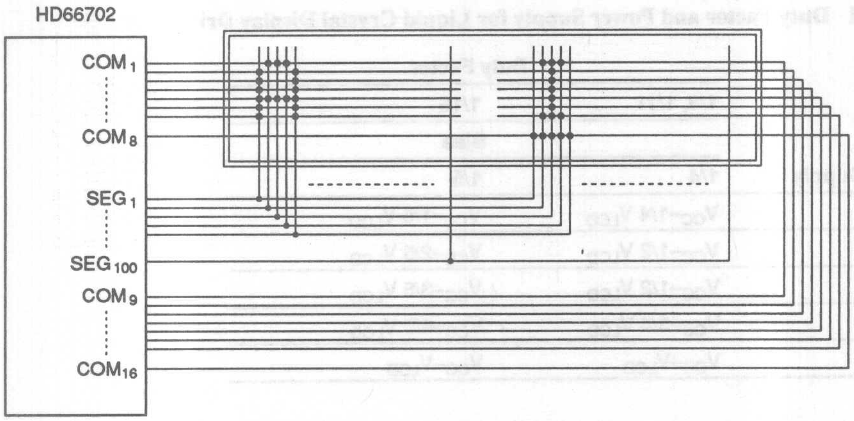
Figure 27 Liquid Crystal Display and HD66702 Connections (cont)



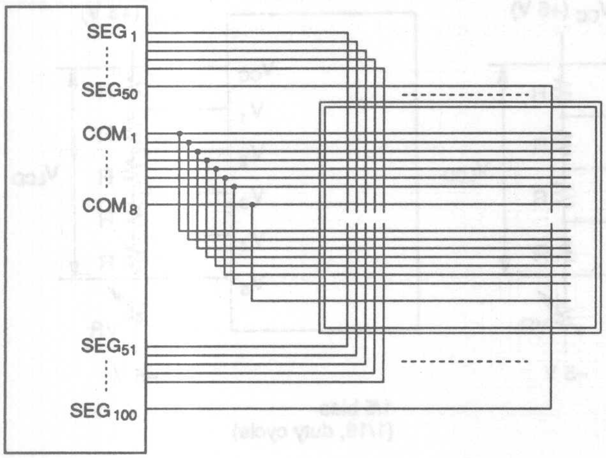
5 × 7 dot, 20-character × 1-line display (1/4 bias, 1/8 duty cycle)

Figure 28 Using COM_9 to Avoid Crosstalk on Unneeded Scanning Line

Connection of Changed Matrix Layout: In the preceding examples, the number of lines correspond to the scanning lines. However, the following display examples (figure 29) are made possible by altering the matrix layout of the liquid crystal display panel. In either case, the only change is the layout. The display characteristics and the number of liquid crystal display characters depend on the number of common signals or on duty factor. Note that the display data RAM (DD RAM) addresses for 10 characters × 2 lines and for 40 characters × 1 line are the same as in figure 27.



5 × 7 dot, 40-character × 1-line display
(1/5 bias, 1/16 duty cycle)



5 × 7 dot, 10-character × 2-line display
(1/4 bias, 1/8 duty cycle)

Figure 29 Changed Matrix Layout Displays

Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to pins V_1 to V_5 of the HD66702 to obtain the liquid crystal display drive waveforms. The voltages must be changed according to the duty factor (table 11).

V_{LCD} is the peak value for the liquid crystal display drive waveforms, and resistance dividing provides voltages V_1 to V_5 (figure 30).

Table 11 Duty Factor and Power Supply for Liquid Crystal Display Drive

	Duty Factor	
	1/8, 1/11	1/16
	Bias	
Power Supply	1/4	1/5
V_1	V_{CC}–1/4 V_{LCD}	V_{CC}–1/5 V_{LCD}
V_2	V_{CC}–1/2 V_{LCD}	V_{CC}–2/5 V_{LCD}
V_3	V_{CC}–1/2 V_{LCD}	V_{CC}–3/5 V_{LCD}
V_4	V_{CC}–3/4 V_{LCD}	V_{CC}–4/5 V_{LCD}
V_5	V_{CC}–V_{LCD}	V_{CC}–V_{LCD}

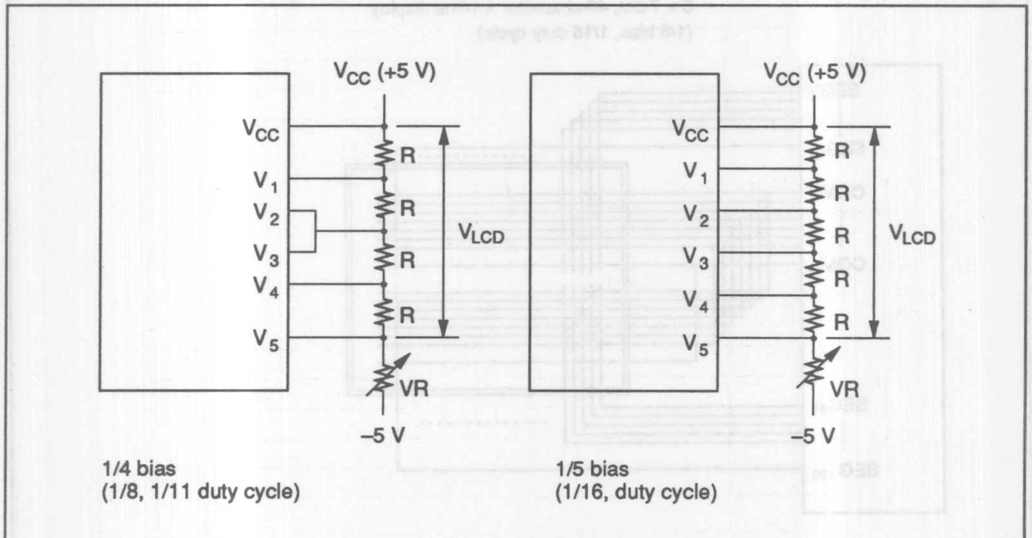


Figure 30 Drive Voltage Supply Example

Relationship between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The liquid crystal display frame frequencies of figure 31 apply only when the oscillation frequency is 320 kHz (one clock pulse of 3.125 µs).

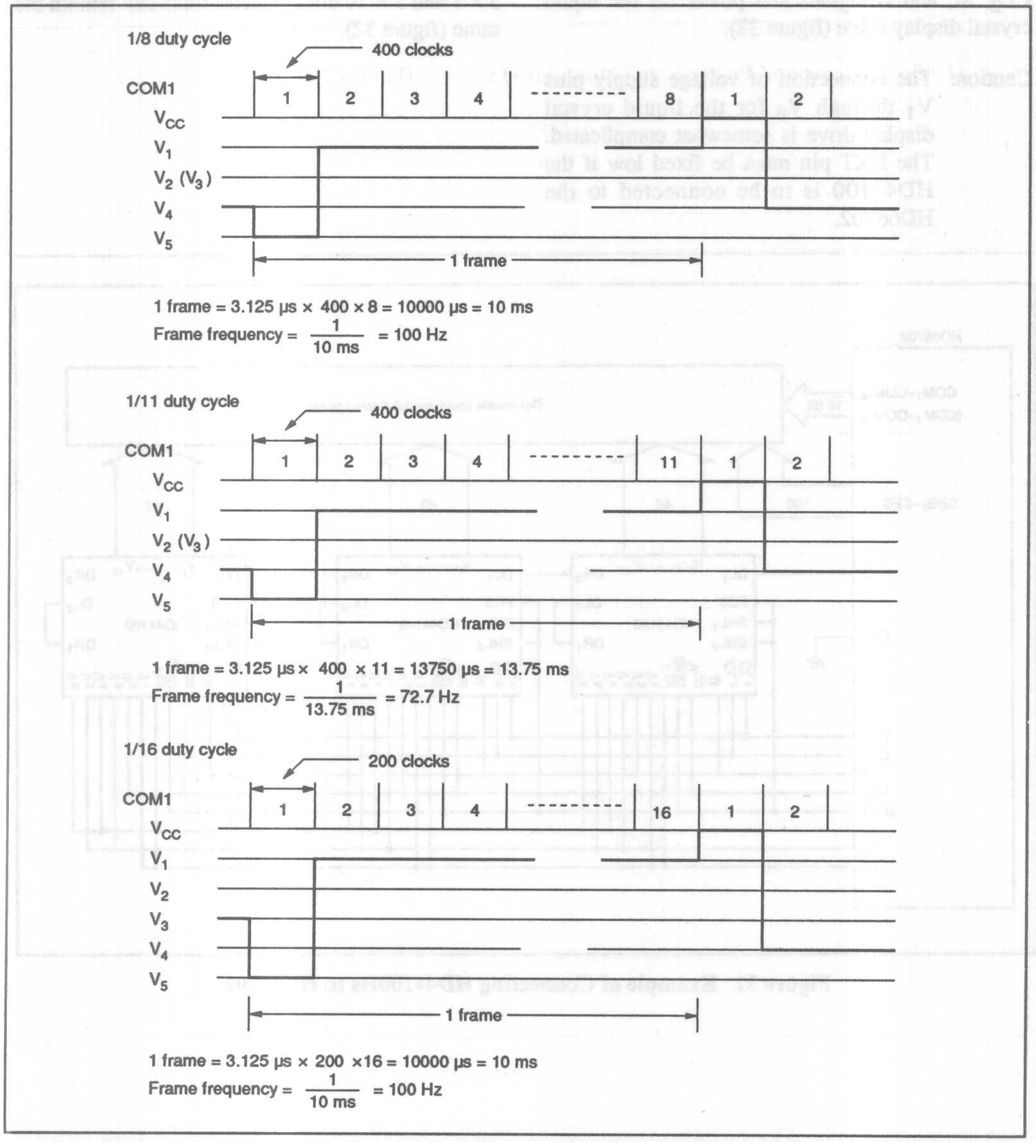


Figure 31 Frame Frequency

Connection with HD44100 Driver

By externally connecting an HD44100 liquid crystal display driver to the HD66702, the number of display digits can be increased. The HD44100 is used as a segment signal driver when connected to the HD66702. The HD44100 can be directly connected to the HD66702 since it supplies CL_1, CL_2, M, and D signals and power for the liquid crystal display drive (figure 32).

Caution: The connection of voltage supply pins V_1 through V_6 for the liquid crystal display drive is somewhat complicated. The EXT pin must be fixed low if the HD44100 is to be connected to the HD66702.

Up to eight HD44100 units can be connected for a 1-line display (duty factor 1/8 or 1/11) and up to three units for a 2-line display (duty factor 1/16). The RAM size limits the HD66702 to a maximum of 80 character display digits. The connection method for both 1-line and 2-line displays or for 5 × 7 and 5 × 10 dot character fonts can remain the same (figure 32).

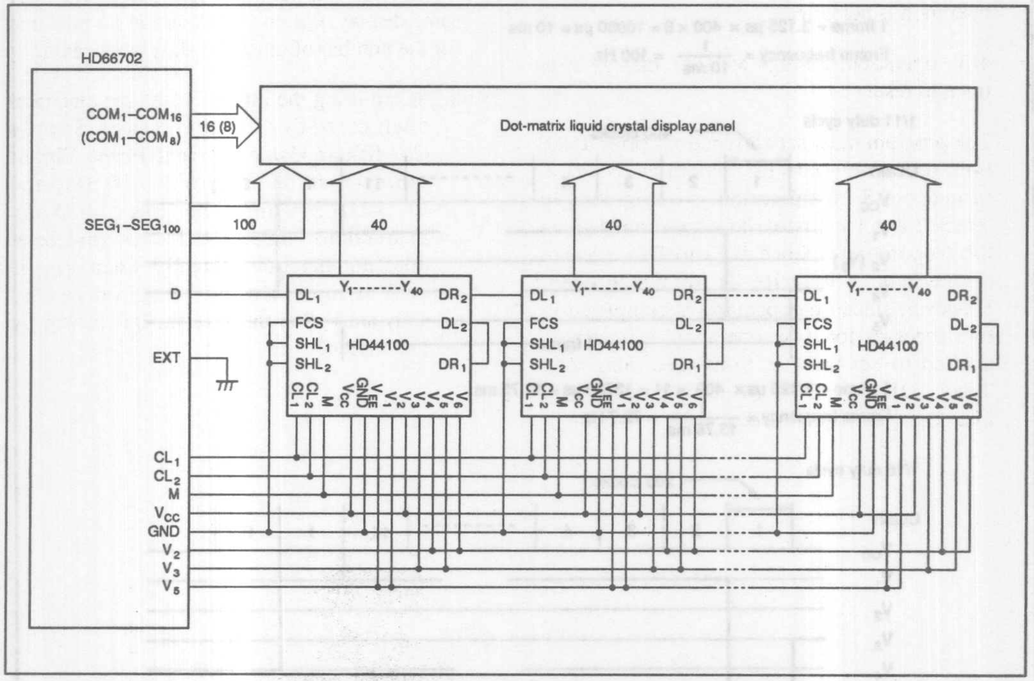


Figure 32 Example of Connecting HD44100Hs to HD66702

HITACHI

Instruction and Display Correspondence

- 8-bit operation, 20-digit × 1-line display with internal reset

  Refer to table 12 for an example of an 8-bit × 1-line display in 8-bit operation. The HD66702 functions must be set by the function set instruction prior to the display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays such as for advertising when combined with the display shift operation.

  Since the display shift operation changes only the display position with DD RAM contents unchanged, the first display data entered into DD RAM can be output when the return home operation is performed.

- 4-bit operation, 20-digit × 1-line display with internal reset

  The program must set all functions prior to the 4-bit operation (table 13). When the power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since DB_0 to DB_3 are not connected, a rewrite is then required. However, since one operation is completed in two accesses for 4-bit operation, a rewrite is needed to set the functions (see table 13). Thus, DB_4 to DB_7 of the function set instruction is written twice.

- 8-bit operation, 20-digit × 2-line display

  For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 20 characters in the first line, the DD RAM address must be again set after the 20th character is completed. (See table 14.) Note that the display shift operation is performed for the first and second lines. In the example of table 14, the display shift is performed when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and second lines move together. If the shift is repeated, the display of the second line will not move to the first line. The same display will only shift within its own line for the number of times the shift is repeated.

Note: When using the internal reset, the electrical characteristics in the Power Supply Conditions Using Internal Reset Circuit table must be satisfied. If not, the LCD-II/E20 must be initialized by instructions. (Because the internal reset does not function correctly when V_{CC} is 3 V, it must always be initialized by software.) See the section, Initializing by Instruction.

Table 12 8-Bit Operation, 20-Digit × 1-Line Display Example with Internal Reset

Step No.	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
1	Power supply on (the HD66702 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 8-bit operation and selects 1-line display and character font. (Number of display lines and character fonts cannot be changed after step #2.)
	0	0	0	0	1	1	0	0	*	*		
3	Display on/off control											Turns on display and cursor. Entire display is in space mode because of initialization.
	0	0	0	0	0	0	1	1	1	0	_	
4	Entry mode set											Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
	0	0	0	0	0	0	0	1	1	0	_	
5	Write data to CG RAM/DD RAM											Writes H. DD RAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.
	1	0	0	1	0	0	1	0	0	0	H_	
6	Write data to CG RAM/DD RAM											Writes I.
	1	0	0	1	0	0	1	0	0	1	HI_	
7	⋮											
8	Write data to CG RAM/DD RAM											Writes I.
	1	0	0	1	0	0	1	0	0	1	HITACHI_	
9	Entry mode set											Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1	HITACHI_	
10	Write data to CG RAM/DD RAM											Writes a space.
	1	0	0	0	1	0	0	0	0	0	ITACHI _	

Table 12 8-Bit Operation, 20-Digit × 1-Line Display Example with Internal Reset (cont)

Step No.	Instruction										Display	Operation
	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
11	Write data to CG RAM/DD RAM											
	1	0	0	1	0	0	1	1	0	1	TACHI M_	Writes M.
12	⋮										⋮	
13	Write data to CG RAM/DD RAM											
	1	0	0	1	0	0	1	1	1	1	MICROKO_	Writes O.
14	Cursor or display shift											
	0	0	0	0	0	1	0	0	*	*	MICROKO	Shifts only the cursor position to the left.
15	Cursor or display shift											
	0	0	0	0	0	1	0	0	*	*	MICROKO	Shifts only the cursor position to the left.
16	Write data to CG RAM/DD RAM											
	1	0	0	1	0	0	0	0	1	1	ICROCO	Writes C over K. The display moves to the left.
17	Cursor or display shift											
	0	0	0	0	0	1	1	1	*	*	MICROCO	Shifts the display and cursor position to the right.
18	Cursor or display shift											
	0	0	0	0	0	1	0	1	*	*	MICROCO_	Shifts the display and cursor position to the right.
19	Write data to CG RAM/DD RAM											
	1	0	0	1	0	0	1	1	0	1	ICROCOM_	Writes M.
20	⋮										⋮	
21	Return home											
	0	0	0	0	0	0	0	0	1	0	HITACHI	Returns both display and cursor to the original position (address 0).

Table 13 4-Bit Operation, 20-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction (RS R/$\overline{W}$ DB_7 DB_6 DB_5 DB_4)	Display	Operation
1	Power supply on (the HD66702 is initialized by the internal reset circuit)		Initialized. No display.
2	Function set 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function set 0 0 0 0 1 0 0 0 0 0 * *		Sets 4-bit operation and selects 1-line display and 5 × 7 dot character font. 4-bit operation starts from this step and resetting is necessary. (Number of display lines and character fonts cannot be changed after step #3.)
4	Display on/off control 0 0 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry mode set 0 0 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
6	Write data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H_	Writes H. The cursor is incremented by one and shifts to the right.

Note: The control is the same as for 8-bit operation beyond step #6.

Table 14 8-Bit Operation, 20-Digit × 2-Line Display Example with Internal Reset

Stop No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
1	Power supply on (the HD66702 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 8-bit operation and selects 2-line display and 5 × 7 dot character font.
	0	0	0	0	1	1	1	0	*	*		
3	Display on/off control										_	Turns on display and cursor. All display is in space mode because of initialization.
	0	0	0	0	0	0	1	1	1	0		
4	Entry mode set										_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
	0	0	0	0	0	0	0	1	1	0		
5	Write data to CG RAM/DD RAM										H_	Writes H. DD RAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.
	1	0	0	1	0	0	1	0	0	0		
6	⋮										⋮	
7	Write data to CG RAM/DD RAM										HITACHI_	Writes I.
	1	0	0	1	0	0	1	0	0	1		
8	Set DD RAM address										HITACHI _	Sets RAM address so that the cursor is positioned at the head of the second line.
	0	0	1	1	0	0	0	0	0	0		

Table 14 8-Bit Operation, 20-Digit × 2-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/W̄	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
9	Write data to CG RAM/DD RAM										HITACHI M_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
10	⋮										⋮	
11	Write data to CG RAM/DD RAM										HITACHI MICROCO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
12	Entry mode set										HITACHI MICROCO_	Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1		
13	Write data to CG RAM/DD RAM										ITACHI ICROCOM_	Writes M. Display is shifted to the right. The first and second lines both shift at the same time.
	1	0	0	1	0	0	1	1	0	1		
14	⋮										⋮	
15	Return home										HITACHI MICROCOM	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

Refer to figures 33 and 34 for the procedures on 8-bit and 4-bit initializations, respectively.

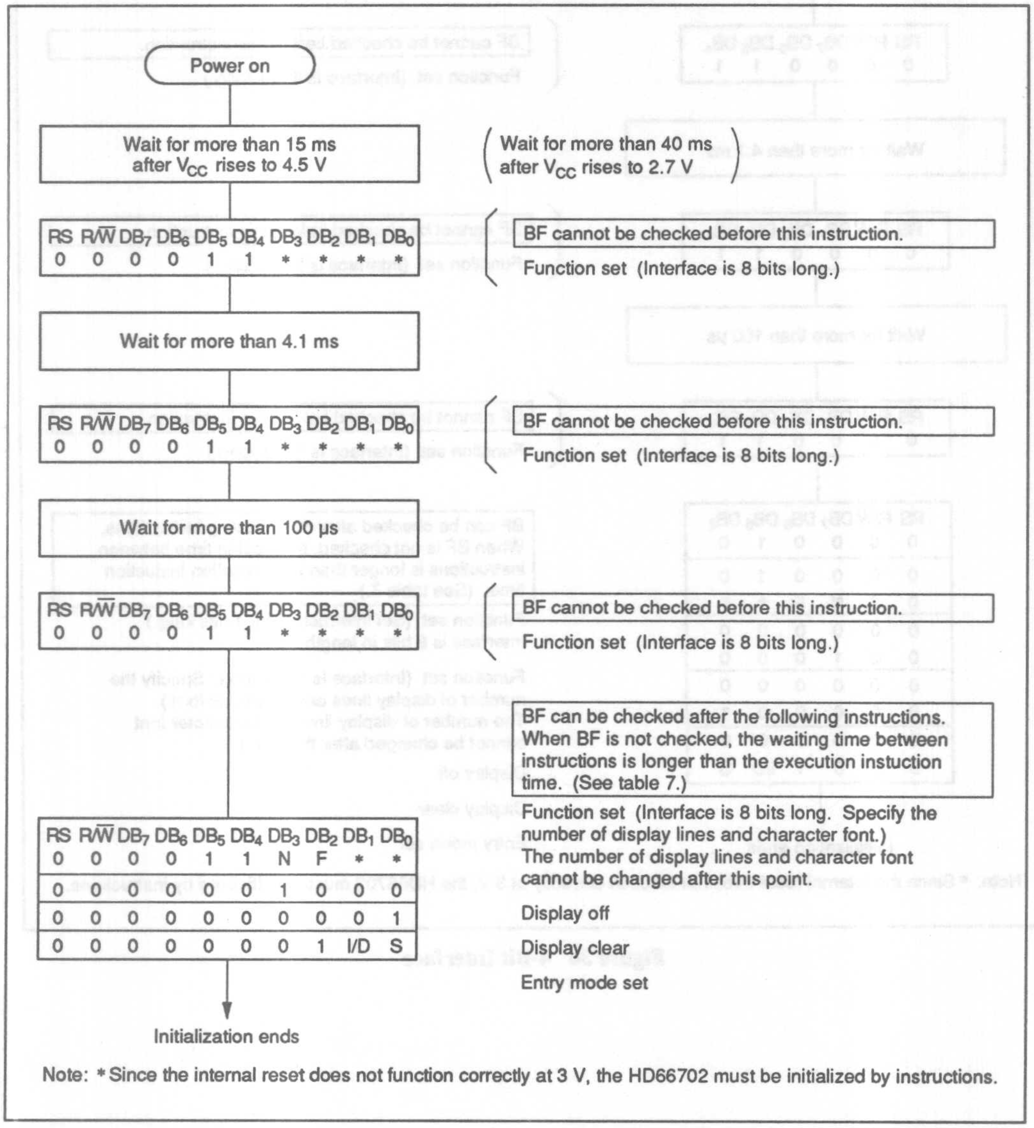


Figure 33 8-Bit Interface

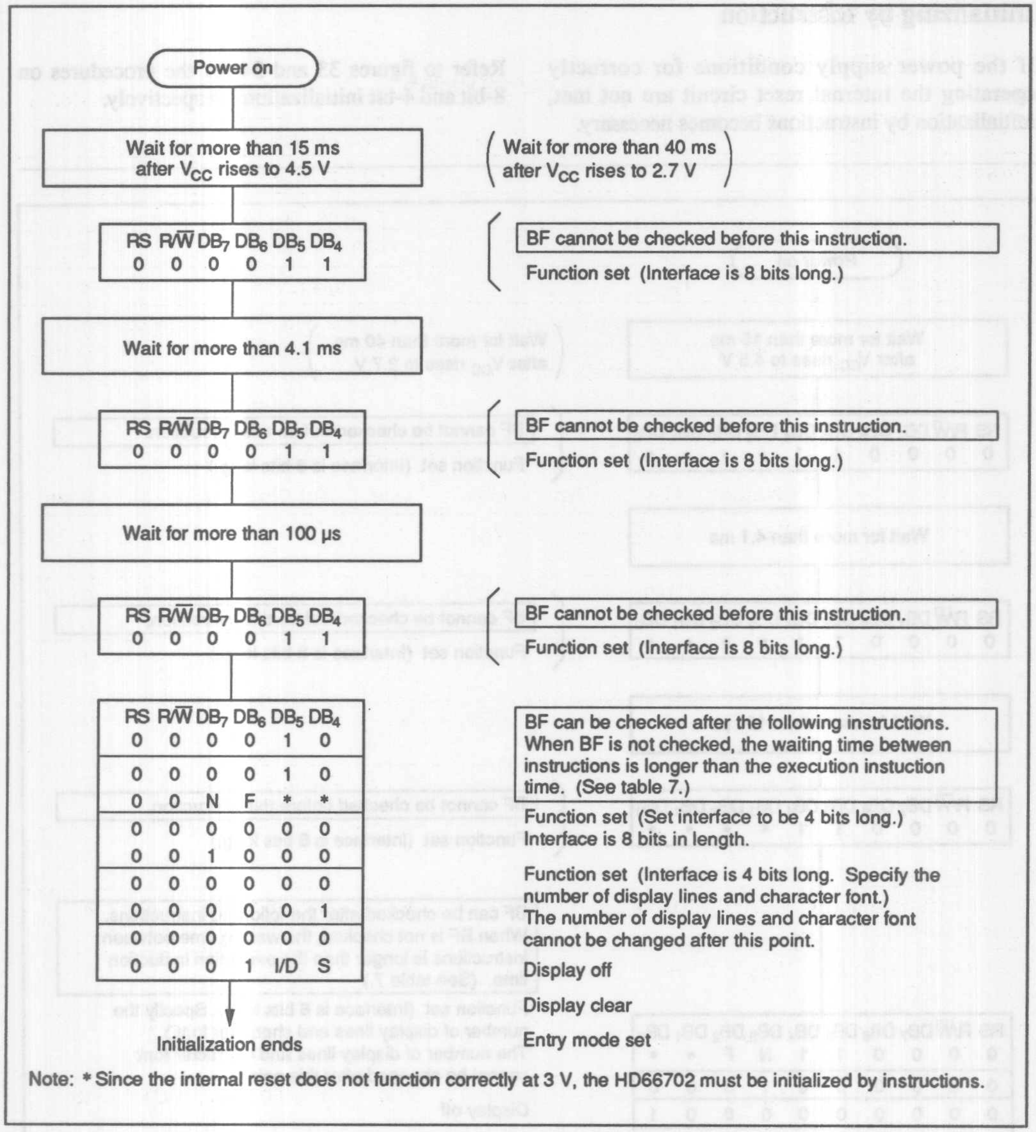


Figure 34 4-Bit Interface

[Low voltage version]

Absolute Maximum Ratings*

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	1
Power supply voltage (2)	V_{CC}–V_5	V	–0.3 to +7.0	2
Input voltage	V_t	V	–0.3 to V_{CC} +0.3	1
Operating temperature	T_{opr}	°C	–20 to +75	3
Storage temperature	T_{stg}	°C	–55 to +125	4

Note: If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 2.7 to 5.5 V, T_a = –20 to +75°C*3)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC_1)	V_{IH1}	$0.7V_{CC}$	—	V_{CC}	V		6, 17
Input low voltage (1) (except OSC_1)	V_{IL1}	–0.3	—	0.55	V		6, 17
Input high voltage (2) (OSC_1)	V_{IH2}	$0.7V_{CC}$	—	V_{CC}	V		15
Input low voltage (2) (OSC_1)	V_{IL2}	—	—	$0.2V_{CC}$	V		15
Output high voltage (1) (D_0–D_7)	V_{OH1}	$0.75V_{CC}$	—	—	V	$-I_{OH}$ = 0.1 mA	7
Output low voltage (1) (D_0–D_7)	V_{OL1}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.1 mA	7
Output high voltage (2) (except D_0–D_7)	V_{OH2}	$0.8V_{CC}$	—	—	V	$-I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except D_0–D_7)	V_{OL2}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA (COM)	13
Driver on resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA (SEG)	13
Input leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (RS, R/$\overline{W}$)	–Ip	10	50	120	µA	V_{CC} = 3 V	
Power supply current	I_{CC}	—	0.15	0.30	mA	R_f oscillation, external clock V_{CC} = 3V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD1}	3.0	—	7.0	V	V_{CC}–V_5, 1/5 bias	16
	V_{LCD2}	3.0	—	7.0	V	V_{CC}–V_5, 1/4 bias	16

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 3 V ±10%, T_a = –20 to +75°C*3)

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	125	270	410	kHz		11
	External clock duty	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{fcp}	—	—	0.2	µs		
R_f oscillation	Clock oscillation frequency	f_{OSC}	220	320	420	kHz	R_f = 56 kΩ	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 35
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	20	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 36
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	20	—	—		
Data delay time	t_{DDR}	—	—	350		
Data hold time	t_{DHR}	20	—	—		

Interface Timing Characteristics with External Driver

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 37
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	200		

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 38
Power supply off time	t_{OFF}	1	—	—		

[Standard voltage version]

Absolute Maximum Ratings*

Item	Symbol	Unit	Value	Note
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	1
Power supply voltage (2)	$V_{CC}–V_5$	V	–0.3 to +7.0	2
Input voltage	V_t	V	–0.3 to V_{CC} +0.3	1
Operating temperature	T_{opr}	°C	–20 to +75	3
Storage temperature	T_{stg}	°C	–55 to +125	4

Note: If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability. Refer to the Electrical Characteristics Notes section following these tables.

DC Characteristics (V_{CC} = 5 V ±10%, T_a = –20 to +75°C*3)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC_1)	V_{IH1}	2.2	—	V_{CC}	V		6, 17
Input low voltage (1) (except OSC_1)	V_{IL1}	–0.3	—	0.6	V		6, 17
Input high voltage (2) (OSC_1)	V_{IH2}	V_{CC}–1.0	—	V_{CC}	V		15
Input low voltage (2) (OSC_1)	V_{IL2}	—	—	1.0	V		15
Output high voltage (1) (D_0–D_7)	V_{OH1}	2.4	—	—	V	$-I_{OH}$ = 0.205 mA	7
Output low voltage (1) (D_0–D_7)	V_{OL1}	—	—	0.4	V	I_{OL} = 1.6 mA	7
Output high voltage (2) (except D_0–D_7)	V_{OH2}	0.9 V_{CC}	—	—	V	$-I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except D_0–D_7)	V_{OL2}	—	—	0.1 V_{CC}	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA (COM)	13
Driver on resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA (SEG)	13
Input leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (RS, R/$\overline{W}$)	$-I_p$	50	125	250	µA	V_{CC} = 5 V	
Power supply current	I_{CC}		0.35	0.60	mA	R_f oscillation, external clock V_{CC} = 5 V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD1}	3.0	—	7.0	V	V_{CC}–V_5, 1/5 bias	16
	V_{LCD2}	3.0	—	7.0	V	V_{CC}–V_5, 1/4 bias	16

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 5 V ±10%, T_a = –20 to +75°C*3)

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	125	270	410	kHz		11
	External clock duty	Duty	45	50	55	%		11
	External clock rise time	t_{rcp}	—	—	0.2	µs		11
	External clock fall time	t_{fcp}	—	—	0.2	µs		11
R_f oscillation	Clock oscillation frequency	f_{OSC}	220	320	420	kHz	R_f = 68 kΩ	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 35
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 36
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data delay time	t_{DDR}	—	—	320		
Data hold time	t_{DHR}	20	—	—		

Interface Timing Characteristics with External Driver

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 37
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	100		

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 38
Power supply off time	t_{OFF}	1	—	—		

Electrical Characteristics Notes

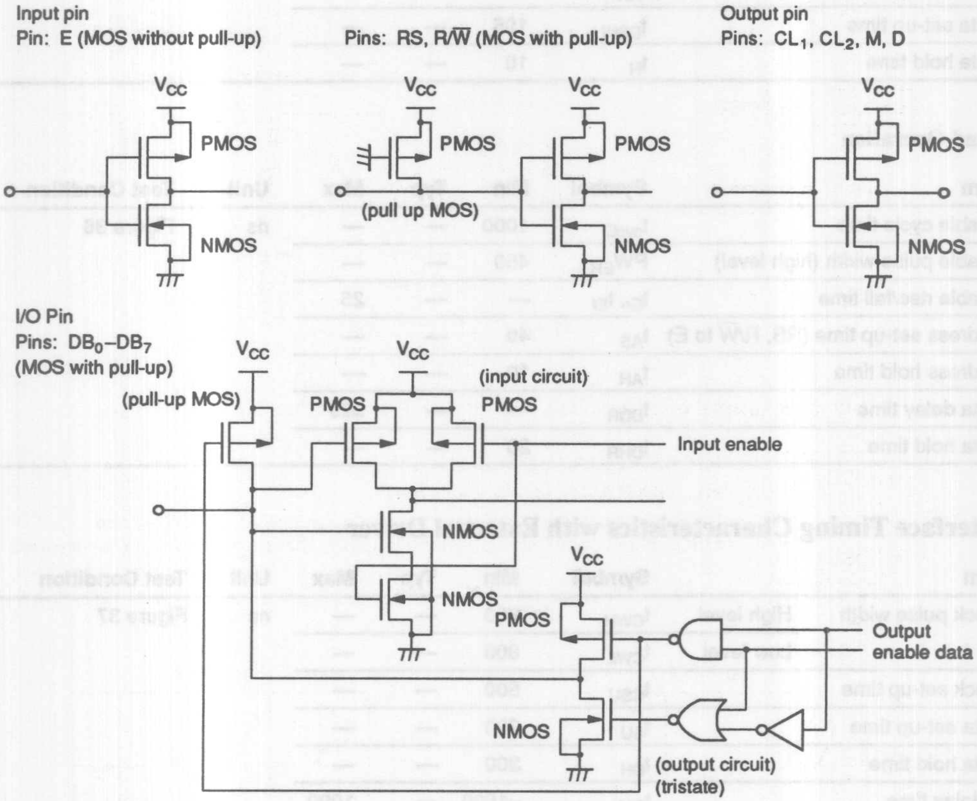
1. All voltage values are referred to GND = 0 V.

2. $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ must be maintained.

3. For die products, specified up to 75°C.

4. For die products, specified by the die shipment specification.

5. The following four circuits are I/O pin configurations except for liquid crystal display output.



6. Applies to input pins and I/O pins, excluding the OSC_1 pin.

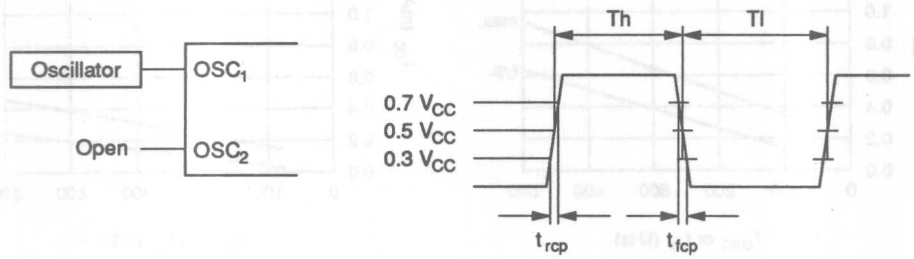
7. Applies to I/O pins.

8. Applies to output pins.

9. Current flowing through pull–up MOSs, excluding output drive MOSs.

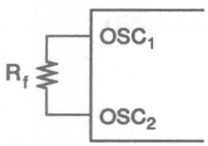
10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.

11. Applies only to external clock operation.

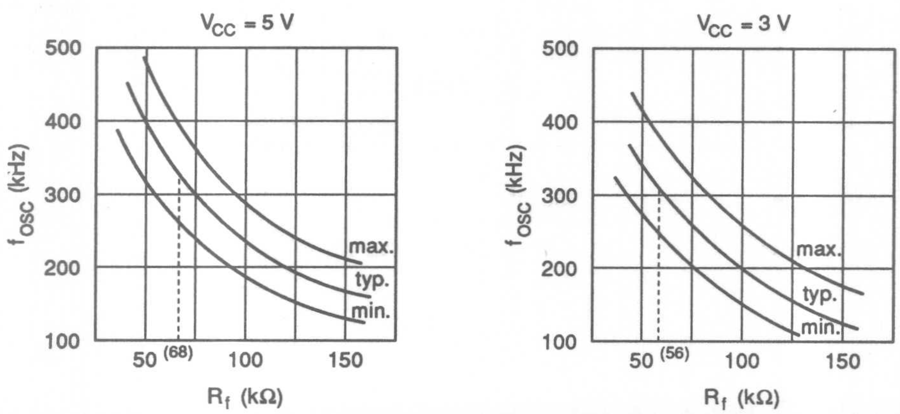


$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

12. Applies only to the internal oscillator operation using oscillation resistor R_f.



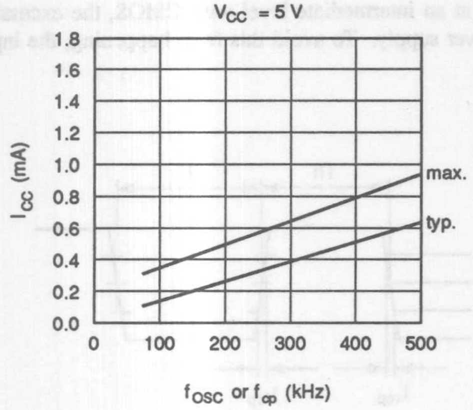
R_f: 56 kΩ ± 2% (when V_{CC} = 3 V)
R_f: 68 kΩ ± 2% (when V_{CC} = 5 V)
Since the oscillation frequency varies depending on the OSC_1 and OSC_2 pin capacitance, the wiring length to these pins should be minimized.

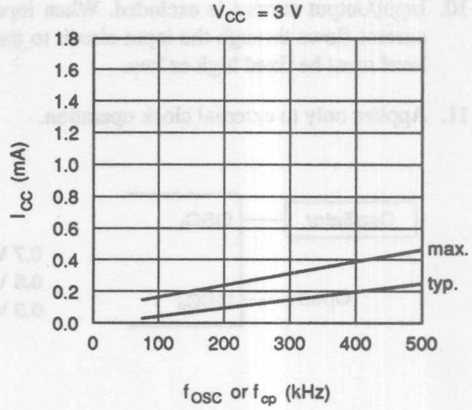


13. R_{COM} is the resistance between the power supply pins (V_{CC}, V_1, V_4, V_5) and each common signal pin (COM_1 to COM_{16}).

    R_{SEG} is the resistance between the power supply pins (V_{CC}, V_2, V_3, V_5) and each segment signal pin (SEG_1 to SEG_{100}).

14. The following graphs show the relationship between operation frequency and current consumption.





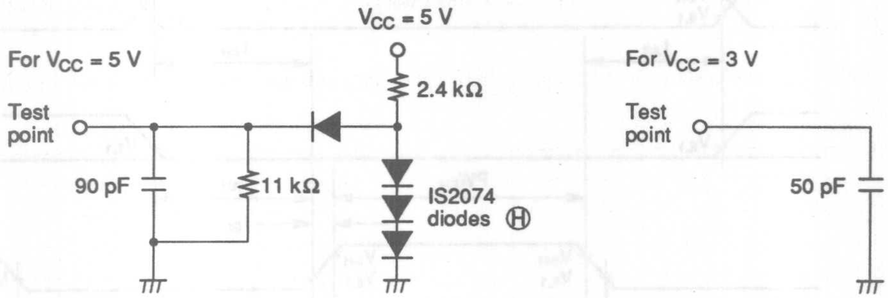
15. Applies to the OSC_1 pin.

16. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (V_{CC}, V_1, V_2, V_3, V_4, V_5) when there is no load.

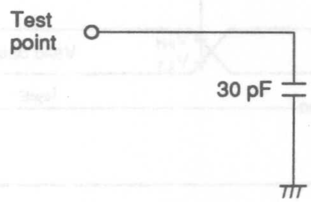
17. The TEST pin should be fixed to GND and the EXT pin should be fixed to V_{CC} or GND.

Load Circuits

Data Bus DB_0 to DB_7



Segment Extension Signals



Timing Characteristics

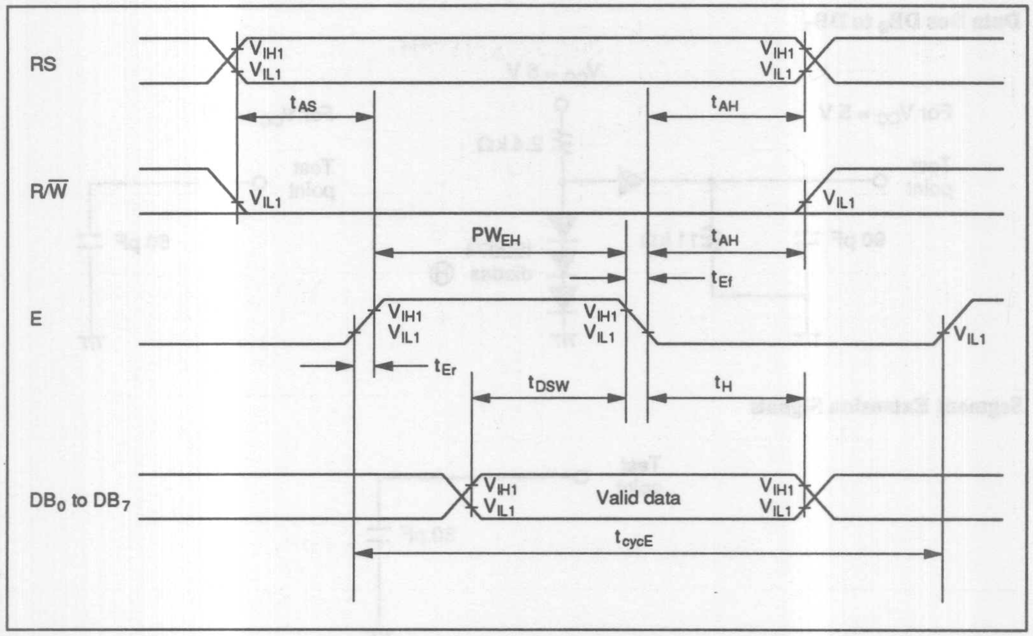


Figure 35 Write Operation

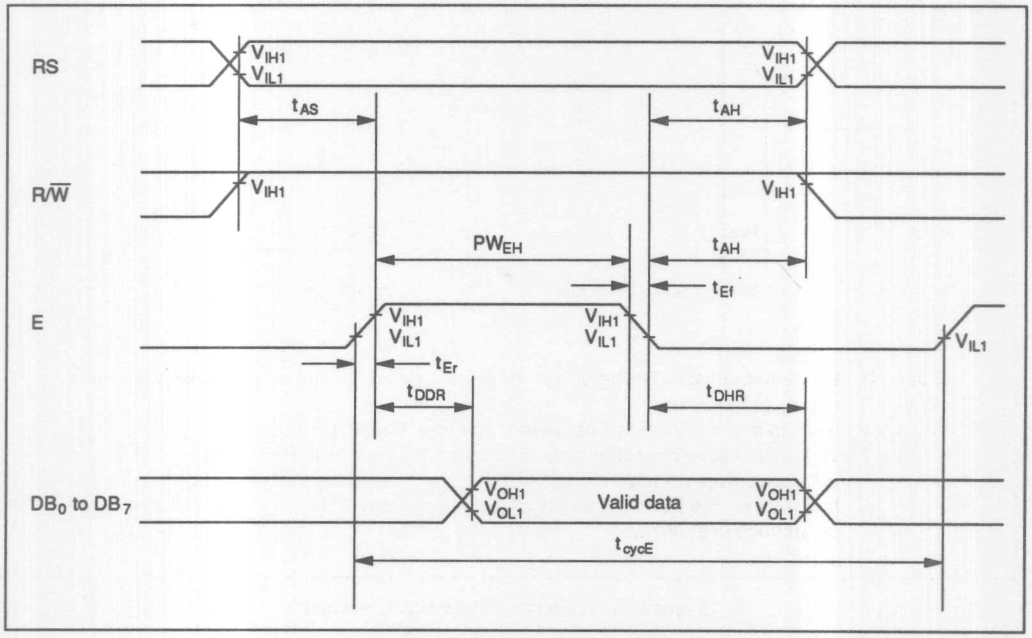


Figure 36 Read Operation

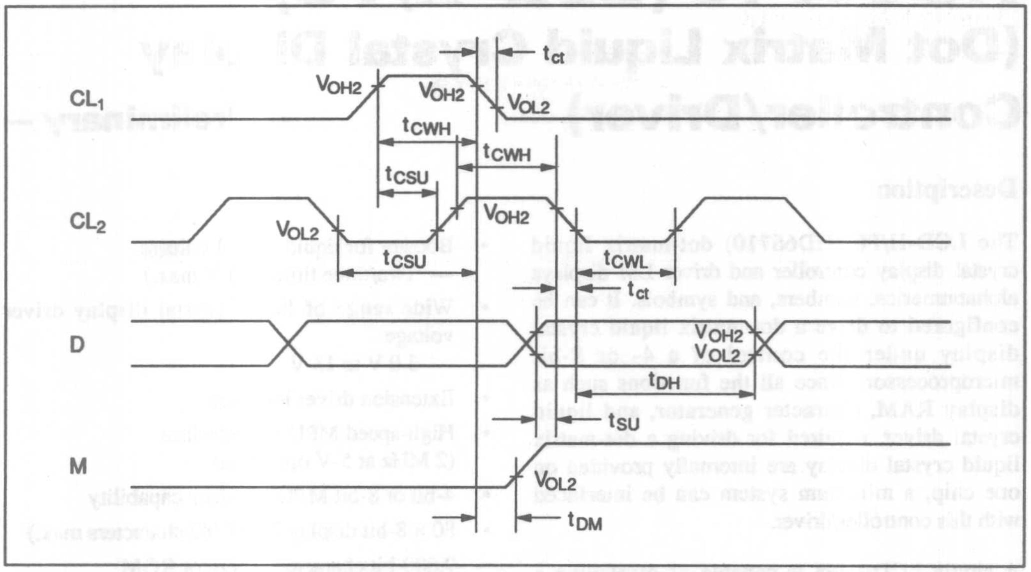
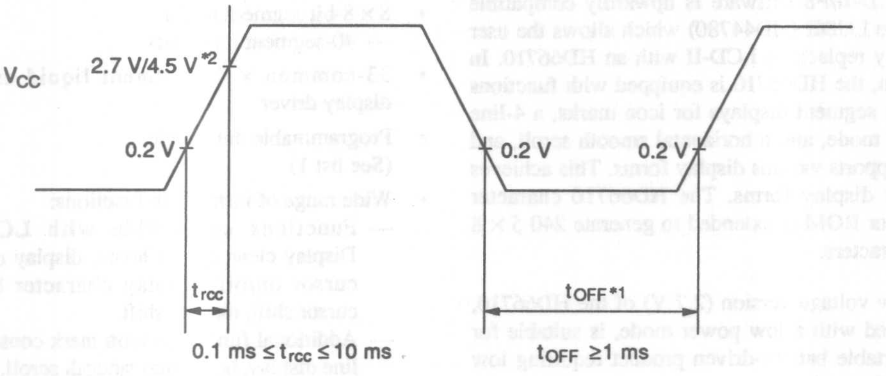


Figure 37 Interface Timing with External Driver



Notes: 1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for 5-V operation, and at 2.7 V for 3-V operation.
3. When the above condition cannot be satisfied, the internal reset circuit will not operate normally.
In this case, the LSI must be initialized by software. (Refer to the Initializing by Instruction section.)

Figure 38 Internal Power Supply Reset

HD66710 (LCD-II/F8)

(Dot Matrix Liquid Crystal Display Controller/Driver)

— Preliminary —

Description

The LCD-II/F8 (HD66710) dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, numbers, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimum system can be interfaced with this controller/driver.

A single LCD-II/F8 is capable of displaying a single16-character line, two 16-character lines, or up to four 8-character lines.

The LCD-II/F8 software is upwardly compatible with the LCDII (HD44780) which allows the user to easily replace an LCD-II with an HD66710. In addition, the HD66710 is equipped with functions such as segment displays for icon marks, a 4-line display mode, and a horizontal smooth scroll, and thus supports various display forms. This achieves various display forms. The HD66710 character generator ROM is extended to generate 240 5 × 8 dot characters.

The low voltage version (2.7 V) of the HD66710, combined with a low power mode, is suitable for any portable battery-driven product requiring low power dissipation.

Features

- 5 × 8 dot matrix possible
- Low power operation support:
  - — 2.7 V to 5.5 V (low voltage)
- Booster for liquid crystal voltage
  - — Two/three times (13 V max.)
- Wide range of liquid crystal display driver voltage
  - — 3.0 V to 13 V
- Extension driver interface
- High-speed MPU bus interface (2 MHz at 5-V operation)
- 4-bit or 8-bit MPU interface capability
- 80 × 8-bit display RAM (80 characters max.)
- 9,600-bit character generator ROM
  - — 240 characters (5 × 8 dot)
- 64 × 8-bit character generator RAM
  - — 8 characters (5 × 8 dot)
- 8 × 8-bit segment RAM
  - — 40-segment icon mark
- 33-common × 40-segment liquid crystal display driver
- Programmable duty cycle (See list 1)
- Wide range of instruction functions:
  - — Functions compatible with LCD-II: Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
  - — Additional functions: Icon mark control, 4-line display, horizontal smooth scroll, 6-dot character width control, white-black inverting blinking cursor.
- Software upwardly compatible with HD44780.
- Automatic reset circuit that initializes the controller/driver after power on
- Internal oscillator with an external resistor
- Low power consumption

List 1 Programmable Duty Cycles

Number of Lines	Duty Ratio	Displayed Character	Maximum Number of Displayed Characters: Single-chip Operation	Maximum Number of Displayed Characters: With Extention Driver
1	1/17	5 × 8-dot	One 16-character line + 40 segments	One 50-character line + 40 segments
2	1/33	5 × 8-dot	Two 16-character lines + 40 segments	Two 30-character lines + 40 segments
4	1/33	5 × 8-dot	Four 8-character lines + 40 segments	Four 20-character lines + 40 segments

Ordering Information

Type No.	Package
HD66710***FS	100-pin plastic QFP (FP-100A)
HCD66710***	Chip

Note: *** = ROM code No.

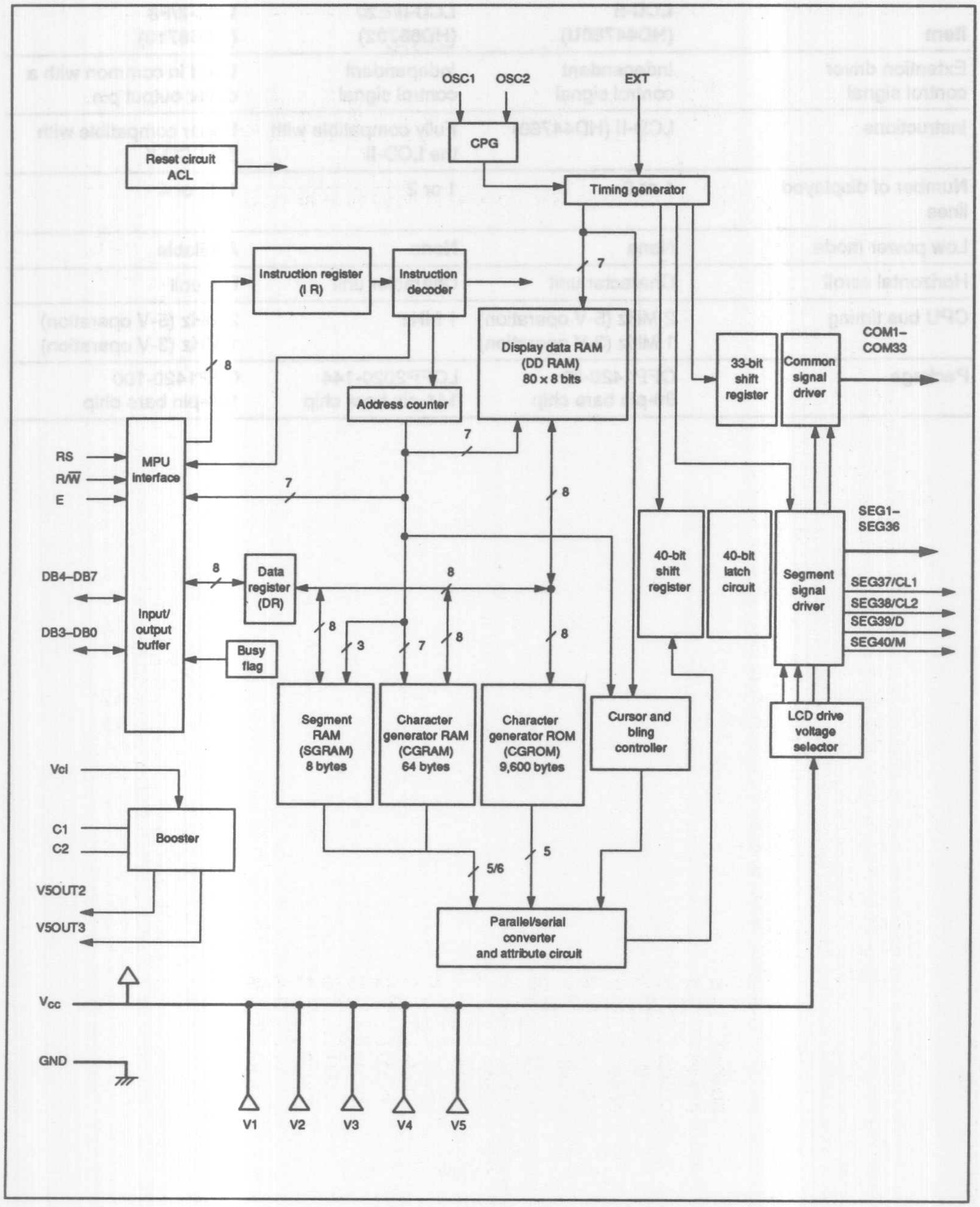
LCD-II Family Comparison

Item	LCD-II (HD44780U)	LCD-II/E20 (HD66702)	LCD-II/F8 (HD66710)
Power supply voltage	2.7 V to 5.5 V	5 V ±10 % (standard) 2.7 V to 5.5 V (low voltage)	2.7 V to 5.5 V
Liquid crystal drive voltage V_{LCD}	3.0 V to 11 V	3.0 V to 7.0 V	3.0 V to 13.0 V
Maximum display digits per chip	8 characters × 2 lines	20 characters × 2 lines	16 characters × 2 lines/ 8 characters × 4 lines
Segment display	None	None	40 segments
Display duty cycle	1/8, 1/11, and 1/16	1/8, 1/11, and 1/16	1/17 and 1/33
CGROM	9,920 bits (208: 5 × 8 dot characters and 32: 5 × 10 dot characters)	7,200 bits (160: 5 × 7 dot characters and 32: 5 × 10 dot characters)	9,600 bits (240: 5 × 8 dot characters)
CGRAM	64 bytes	64 bytes	64 bytes
DDRAM	80 bytes	80 bytes	80 bytes
SEGRAM	None	None	8 bytes
Segment signals	40	100	40
Common signals	16	16	33
Liquid crystal drive waveform	A	B	B
Bleeder resistor for LCD power supply	External (adjustable)	External (adjustable)	External (adjustable)
Clock source	External resistor, or external clock	External resistor or external clock	External resistor or external clock
R_f oscillation frequency (frame frequency)	270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	320 kHz ±30% (70 to 130 Hz for 1/8 and 1/16 duty cycles; 51 to 95 Hz for 1/11 duty cycle)	270 kHz ±30% (56 to 103 Hz for 1/17 duty cycle; 57 to 106 Hz for 1/33 duty cycle)
R_f resistance	91 kΩ (5-V operation) 75 kΩ (3-V operation)	68 kΩ (5-V operation) 56 kΩ (3-V operation)	91 kΩ (5-V operation) 75 kΩ (3-V operation)
Liquid crystal voltage booster circuit	None	None	2-3 times step-up circuit

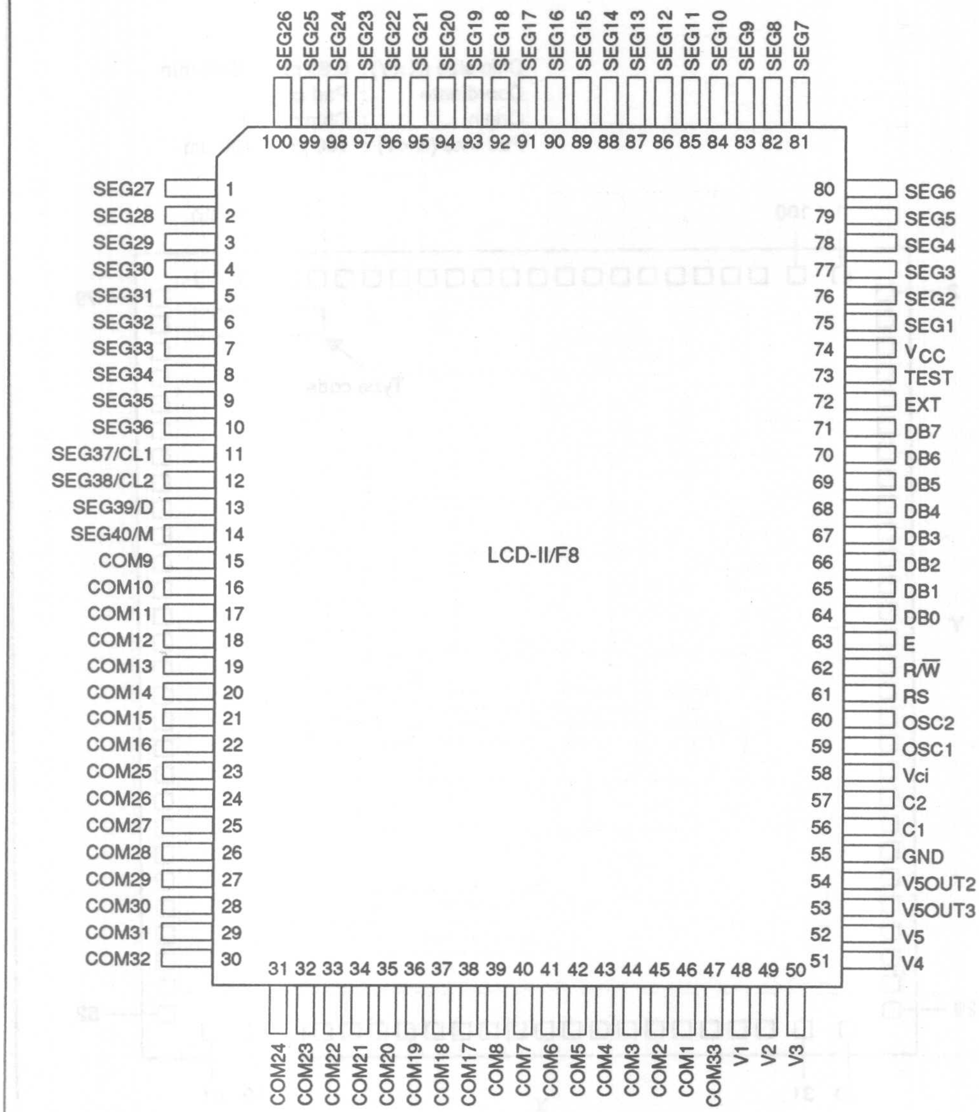
LCD-II Family Comparison (cont)

Item	LCD-II (HD44780U)	LCD-II/E20 (HD66702)	LCD-II/F8 (HD66710)
Extention driver control signal	Independent control signal	Independent control signal	Used in common with a driver output pin
Instructions	LCD-II (HD44780)	Fully compatible with the LCD-II	Upper compatible with the LCD-II
Number of displayed lines	1 or 2	1 or 2	1, 2, or 4
Low power mode	None	None	Available
Horizontal scroll	Character unit	Character unit	Dot unit
CPU bus timing	2 MHz (5-V operation) 1 MHz (3-V operation)	1 MHz	2 MHz (5-V operation) 1 MHz (3-V operation)
Package	QFP1420-80 80-pin bare chip	LQFP2020-144 144-pin bare chip	QFP1420-100 100-pin bare chip

HD66710 Block Diagram

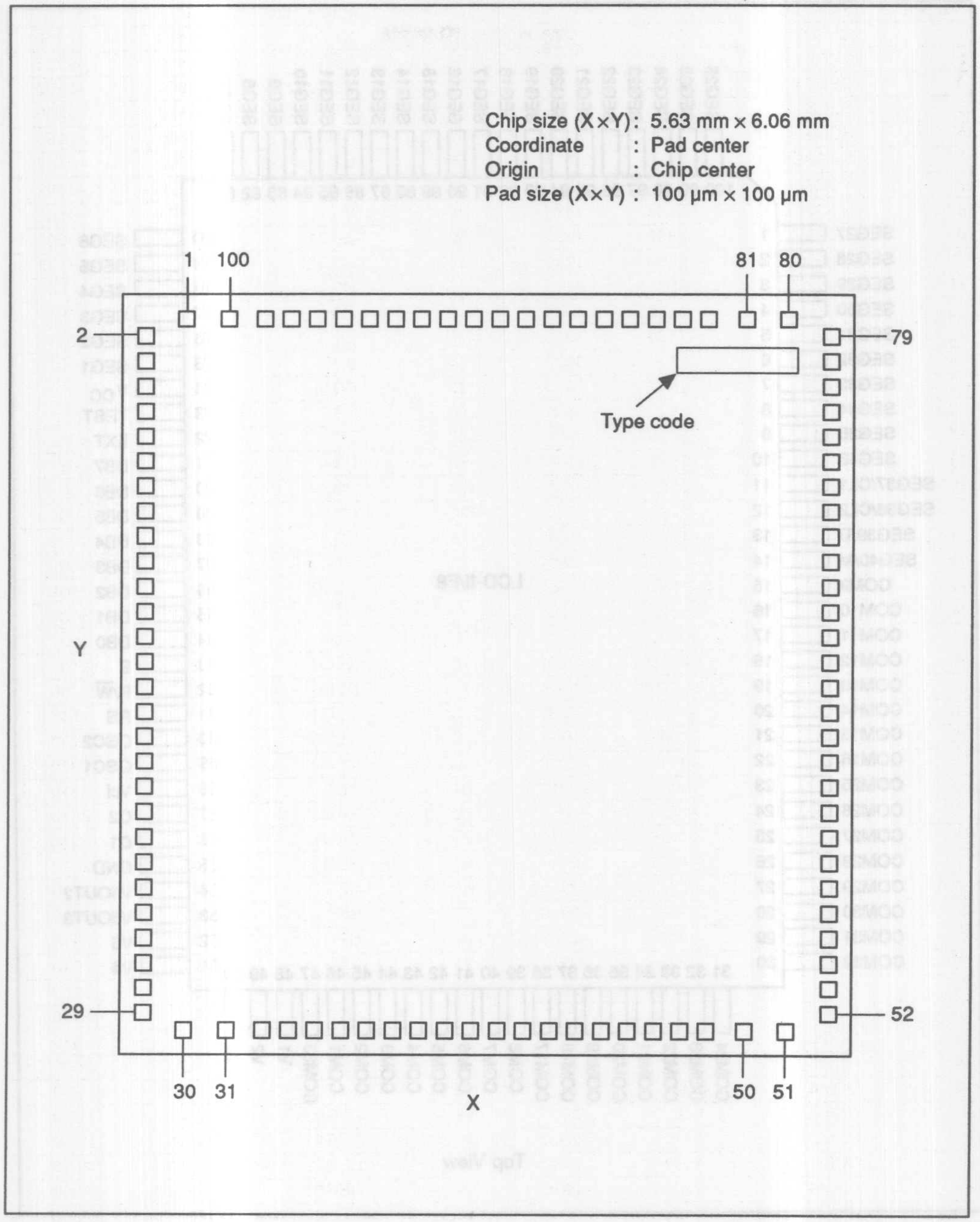


HD66710 Pin Arrangement



Top View

HD66710 Pad Arrangement



HD66710 Pad Location Coordinates

Pin No.	Pad Name	X	Y	Pin No.	Pad Name	X	Y
1	SEG27	–2495	2910	51	V4	2458	–2910
2	SEG28	–2695	2730	52	V5	2660	–2731
3	SEG29	–2695	2499	53	V5OUT3	2660	–2500
4	SEG30	–2695	2300	54	V5OUT2	2660	–2300
5	SEG31	–2695	2100	55	GND	2640	–2090
6	SEG32	–2695	1901	56	C1	2650	–1887
7	SEG33	–2695	1698	57	C2	2675	–1702
8	SEG34	–2695	1498	58	Vci	2675	–1502
9	SEG35	–2695	1295	59	OSC1	2675	–1303
10	SEG36	–2695	1099	60	OSC2	2675	–1103
11	SEG37	–2695	900	61	RS	2675	–900
12	SEG38	–2695	700	62	R/$\overline{W}$	2675	–701
13	SEG39	–2695	501	63	E	2675	–501
14	SEG40	–2695	301	64	DB0	2675	–302
15	COM9	–2695	98	65	DB1	2675	–99
16	COM10	–2695	–113	66	DB2	2675	98
17	COM11	–2695	–302	67	DB3	2675	301
18	COM12	–2695	–501	68	DB4	2675	501
19	COM13	–2695	–701	69	DB5	2675	700
20	COM14	–2695	–900	70	DB6	2675	900
21	COM15	–2695	–1100	71	DB7	2675	1099
22	COM16	–2695	–1303	72	EXT	2675	1299
23	COM25	–2695	–1502	73	TEST	2675	1502
24	COM26	–2695	–1702	74	V_{CC}	2695	1698
25	COM27	–2695	–1901	75	SEG1	2695	1901
26	COM28	–2695	–2101	76	SEG2	2695	2104
27	COM29	–2695	–2300	77	SEG3	2695	2300
28	COM30	–2695	–2500	78	SEG4	2695	2503
29	COM31	–2695	–2731	79	SEG5	2695	2730
30	COM32	–2495	–2910	80	SEG6	2495	2910
31	COM24	–2051	–2910	81	SEG7	2049	2910
32	COM23	–1701	–2910	82	SEG8	1699	2910
33	COM22	–1498	–2910	83	SEG9	1499	2910
34	COM21	–1302	–2910	84	SEG10	1300	2910
35	COM20	–1102	–2910	85	SEG11	1100	2910
36	COM19	–899	–2910	86	SEG12	901	2910
37	COM18	–700	–2910	87	SEG13	701	2910
38	COM17	–500	–2910	88	SEG14	502	2910
39	COM8	–301	–2910	89	SEG15	299	2910
40	COM7	–101	–2910	90	SEG16	99	2910
41	COM6	99	–2910	91	SEG17	–101	2910
42	COM5	302	–2910	92	SEG18	–301	2910
43	COM4	502	–2910	93	SEG19	–500	2910
44	COM3	698	–2910	94	SEG20	–700	2910
45	COM2	887	–2910	95	SEG21	–899	2910
46	COM1	1077	–2910	96	SEG22	–1099	2910
47	COM33	1266	–2910	97	SEG23	–1302	2910
48	V1	1488	–2910	98	SEG24	–1501	2910
49	V2	1710	–2910	99	SEG25	–1701	2910
50	V3	2063	–2910	100	SEG26	–2051	2910

Pin Functions

Table 1 Pin Functional Description

Signal	I/O	Device Interfaced with	Function
RS	I	MPU	Selects registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read)
R/W	I	MPU	Selects read or write. 0: Write 1: Read
E	I	MPU	Starts data read/write
DB4 to DB7	I/O	MPU	Four high order bidirectional tristate data bus pins. Used for data transfer between the MPU and the HD66710. DB7 can be used as a busy flag.
DB0 to DB3	I/O	MPU	Four low order bidirectional tristate data bus pins. Used for data transfer between the MPU and the HD66710. These pins are not used during 4-bit operation.
COM1 to COM33	O	LCD	Common signals; those are not used become non-selected waveforms. At 1/17 duty rate, COM1 to COM16 are used for character display, COM17 for icon display, and COM18 to COM33 become non-selected waveforms. At 1/33 duty rate, COM1 to COM32 are used for character display, and COM33 for icon display.
SEG1 to SEG35	O	LCD	Segment signals
SEG36	O	LCD	Segment signal. When EXT = high, the same data as that of the first dot of the extension driver is output.
SEG37/CL1	O	LCD/ Extension driver	Segment signal when EXT = low. When EXT = high, outputs the extension driver latch pulse.
SEG38/CL2	O	LCD/ Extension driver	Segment signal when EXT = low. When EXT = high, outputs the extension driver shift clock.
SEG39/D	O	LCD/ Extension driver	Segment signal at EXT = low. At EXT = high, the extension driver data. Data on and after the 36th dot is output.
SEG40/M	O	LCD/ Extension driver	Segment signal when EXT = low. When EXT = high, outputs the extension driver AC signal.
EXT	I	—	Extension driver enable signal. When EXT = high, SEG37 to SEG40 become extension driver interface signals. At this time, make sure that V5 level is lower than GND level (0 V). V5 (low) ≤ GND (high).
V1 to V5	—	Power supply	Power supply for LCD drive V_{CC} – V5 = 13 V (max)

Table 1 Pin Functional Description (cont)

Signal	I/O	Device Interfaced with	Function
V_{CC}, GND	—	Power supply	V_{CC}: +2.7 V to 5.5 V, GND: 0 V
OSC1, OSC2	—	Oscillation resistor clock	When CR oscillation is performed, a resistor must be connected externally. When the pin input is an external clock, it must be input to OSC1.
Vci	I	—	Input voltage to the booster, from which the liquid crystal display drive voltage is generated. Vci: 2.5 V to 4.5 V
V5OUT2	O	V5 pin/ Booster capacitance	Voltage input to the Vci pin is boosted twice and output When the voltage is boosted three times, the same capacity as that of C1–C2 should be connected.
V5OUT3	O	V5 pin	Voltage input to the Vci pin is boosted three times and output.
C1/C2	—	Booster capacitance	External capacitance should be connected when using the booster.
TEST	I	—	Test pin. Should be wired to ground.

Function Description

Registers

The HD66710 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for the display data RAM (DD RAM), the character generator RAM (CG RAM), and the segment RAM (SEG RAM). The MPU can only write to IR, and cannot be read from.

The DR temporarily stores data to be written into DD RAM, CG RAM, or SEG RAM. Data written into the DR from the MPU is automatically written into DD RAM, CG RAM, or SEG RAM by an internal operation. The DR is also used for data storage when reading data from DD RAM, CG RAM, or SEG RAM. When address information is written into the IR, data is read and then stored into the DR from DD RAM, CG RAM, or SEG RAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DD RAM, CG RAM, or SEGRAM at the next address is sent to the DR for the next read from the MPU.

By the register selector (RS) signal, these two registers can be selected (table 2).

Busy Flag (BF)

When the busy flag is 1, the HD66710 is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/$\overline{W}$ = 1 (table 2), the busy flag is output from DB_7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to DD RAM, CG RAM, or SEG RAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of DD RAM, CG RAM, and SEG RAM is also determined concurrently by the instruction.

After writing into (reading from) DD RAM, CG RAM, or SEG RAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB_0 to DB_6 when RS = 0 and R/$\overline{W}$ = 1 (table 2).

Table 2 Register Selection

RS	R/$\overline{W}$	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0 to DB_6)
1	0	DR write as an internal operation (DR to DD RAM, CG RAM, or SEGRAM)
1	1	DR read as an internal operation (DD RAM, CG RAM, or SEGRAM to DR)

Display Data RAM (DD RAM)

Display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 × 8 bits, or 80 characters. The area in display data RAM (DD RAM) that is not used for display can be used as general data RAM. See figure 1 for the relationships between DD RAM addresses and positions on the liquid crystal display.

The DD RAM address (A_{DD}) is set in the address counter (AC) as hexadecimal.

- 1-line display (N = 0) (figure 2)
  - — Case 1: When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the HD66710, 16 characters are displayed. See figure 3.

    When the display shift operation is performed, the DD RAM address shifts. See figure 3.
  - — Case 2: Figure 4 shows the case where the EXT pin is fixed high, and the HD66710 and the 40-output extension driver are used to extend the number of display characters. In this case, the start address from COM9 to COM16 of the LCD-II/F8 is 0AH. To display 24 characters, addresses starting at SEG11 should be used.

    When a display shift operation is performed, the DD RAM address shifts. See figure 4.

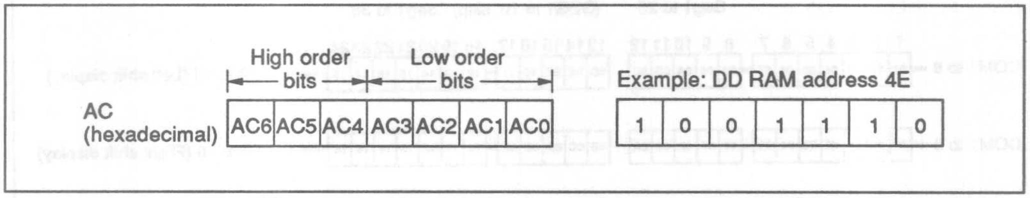


Figure 1 DD RAM Address

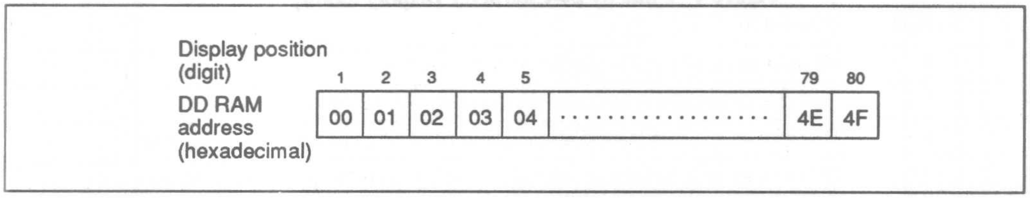


Figure 2 1-Line Display

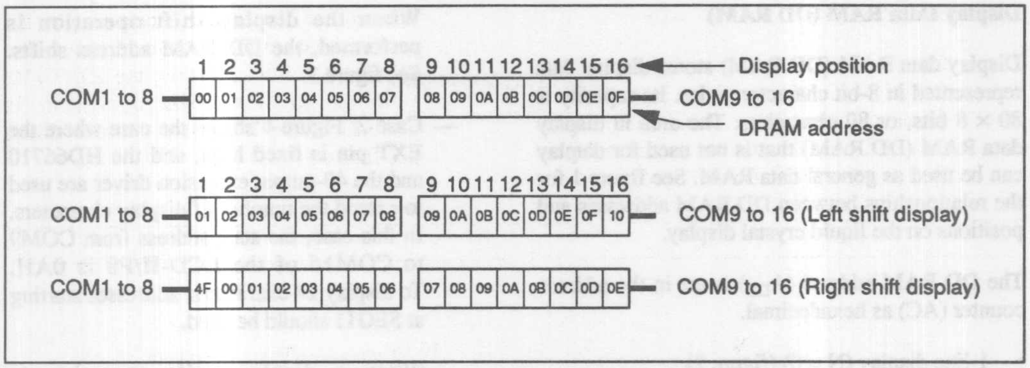


Figure 3 1-line by 16-Character Display Example

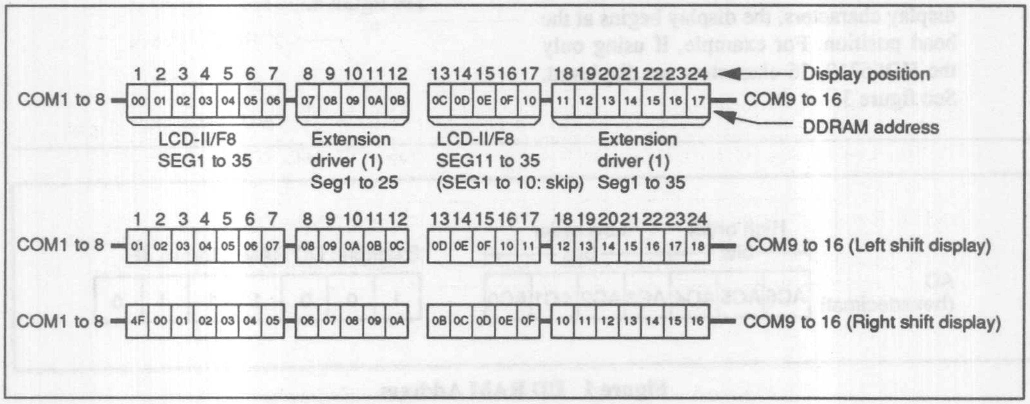


Figure 4 1-line by 24-Character Display Example

- 2-line display (N = 1, and NW = 0)
  - — Case 1: The first line is displayed from COM1 to COM16, and the second line is displayed from COM17 to COM32. Care is required because the end address of the first line and the start address of the second line are not consecutive. For example, the case is shown in figure 6 where 16 × 2-line display is performed using the HD66710. When a display shift operation is performed, the DD RAM address shifts. See figure 5.

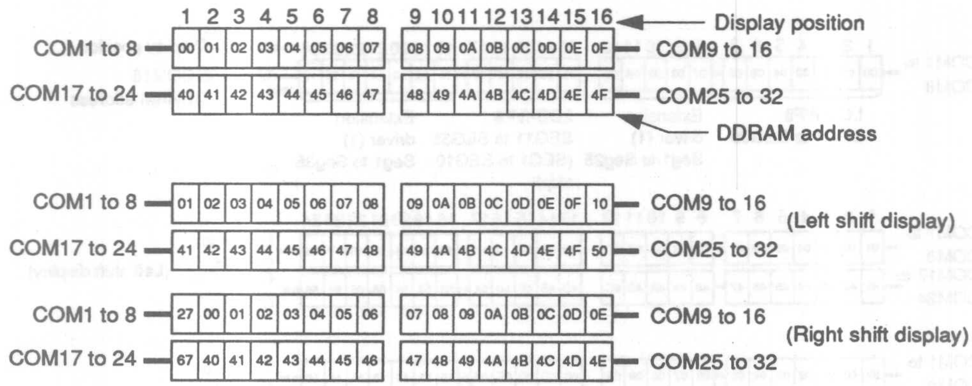


Figure 5 2-line by 16-Character Display Example

— Case 2: Figure 6 shows the case where the EXT pin is fixed to high, the HD66710 and the 40-output extension driver are used to extend the number of display characters.

In this case, the start address from COM9 to COM16 of the HD66710 is 0AH, and that from COM25 to COM32 of the HD66710 is 4AH. To display 24 characters, the addresses starting at SEG11 should be used.

When a display shift operation is performed, the DD RAM address shifts. See figure 6.

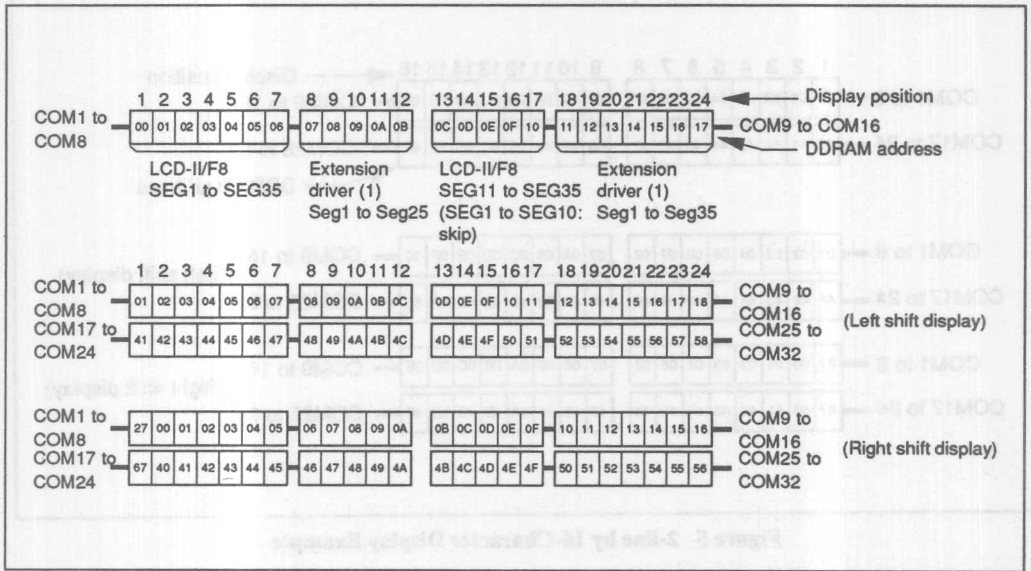


Figure 6 2-Line by 24 Character Display Example

- 4-line display (NW = 1)
  - — Case 1: The first line is displayed from COM1 to COM8, the second line is displayed from COM9 to COM16, the third line is displayed from COM17 to COM24, and the fourth line is displayed from COM25 to COM32. Care is required because the DD RAM addresses of each line are not consecutive. For example, the case is shown in figure 7 where 8 × 4-line display is performed using the HD66710.

When a display shift operation is performed, the DD RAM address shifts. See figure 7.

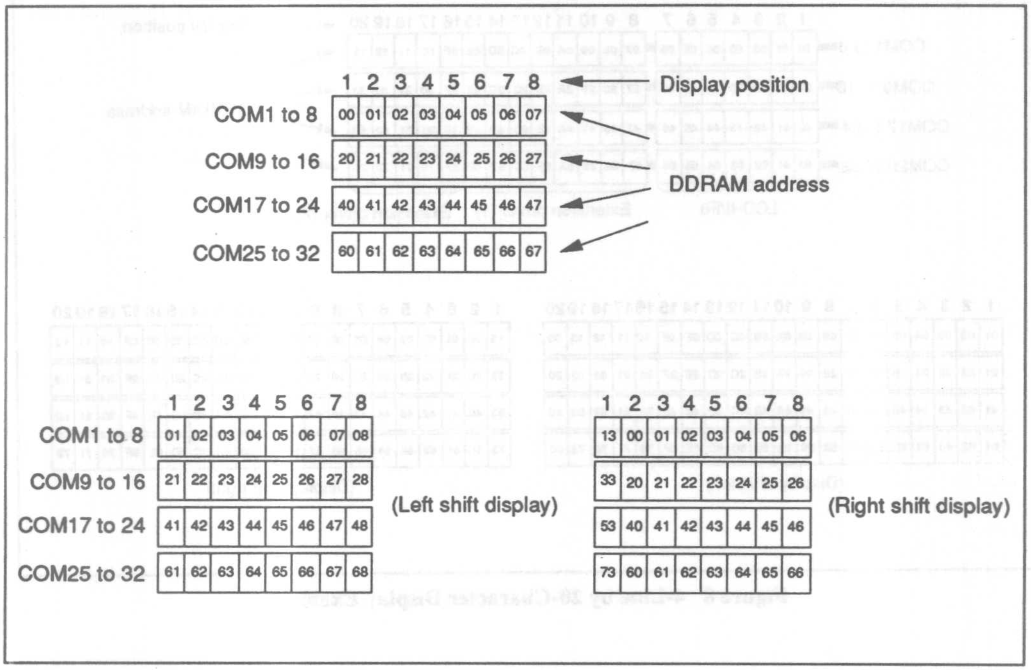


Figure 7 4-Line Display

— Case 2: The case is shown in figure where the EXT pin is fixed high, and the HD66710 and the 40-output extension driver are used to extend the number of display characters.

When a display shift operation is performed, the DD RAM address shifts. See figure 8.

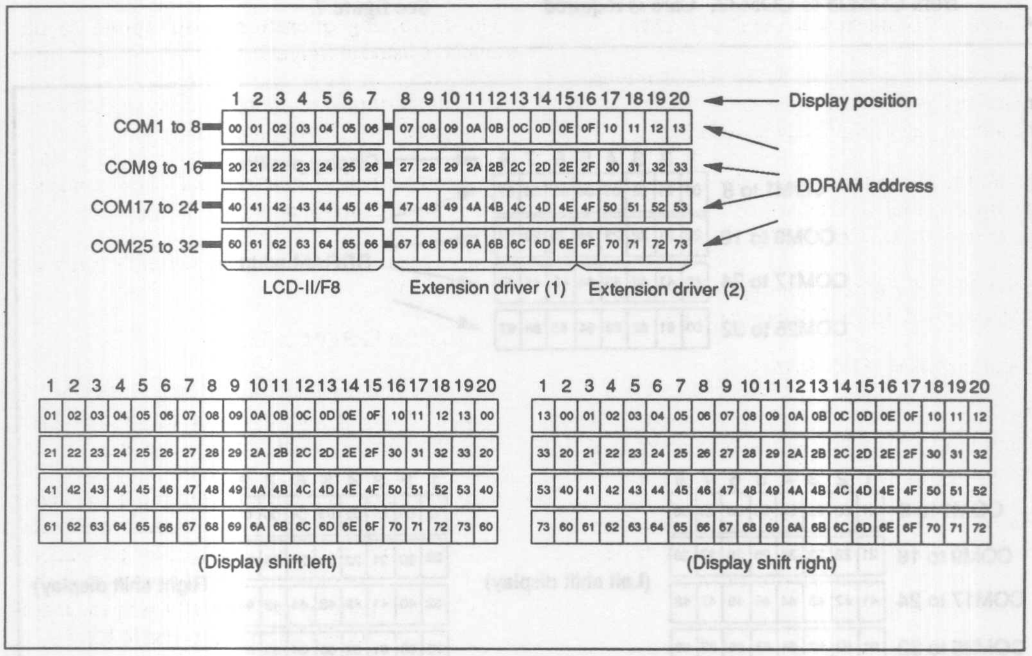


Figure 8 4-Line by 20-Character Display Example

Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 8 dot character patterns from 8-bit character codes (table 3). It can generate 240 5 × 8 dot character patterns. User-defined character patterns are also available using a mask-programmed ROM.

Character Generator RAM (CG RAM)

The character generator RAM allows the user to redefine the character patterns. In the case of 5 × 8 characters, up to eight may be redefined.

Write the character codes at the addresses shown as the left column of table 3 to show the character patterns stored in CG RAM.

See table 5 for the relationship between CG RAM addresses and data and display patterns.

Segment RAM (SEG RAM)

The segment RAM (SEG RAM) is used to enable control of segments such as an icon and a mark by the user program.

For a 1-line display, SEG RAM is read from the COM17 output, and as for 2- or 4-line displays, it is from the COM33 output, to performs 40-segment display.

As shown in table 6, bits in SEG RAM corresponding to segments to be displayed are directly set by the MPU, regardless of the contents of DD RAM and CG RAM.

SEG RAM data is stored in eight bits. The lower six bits control the display of each segment, and the upper two bits control segment blinking.

Modifying Character Patterns

- Character pattern development procedure

The following operations correspond to the numbers listed in figure 9:

1. Determine the correspondence between character codes and character patterns.

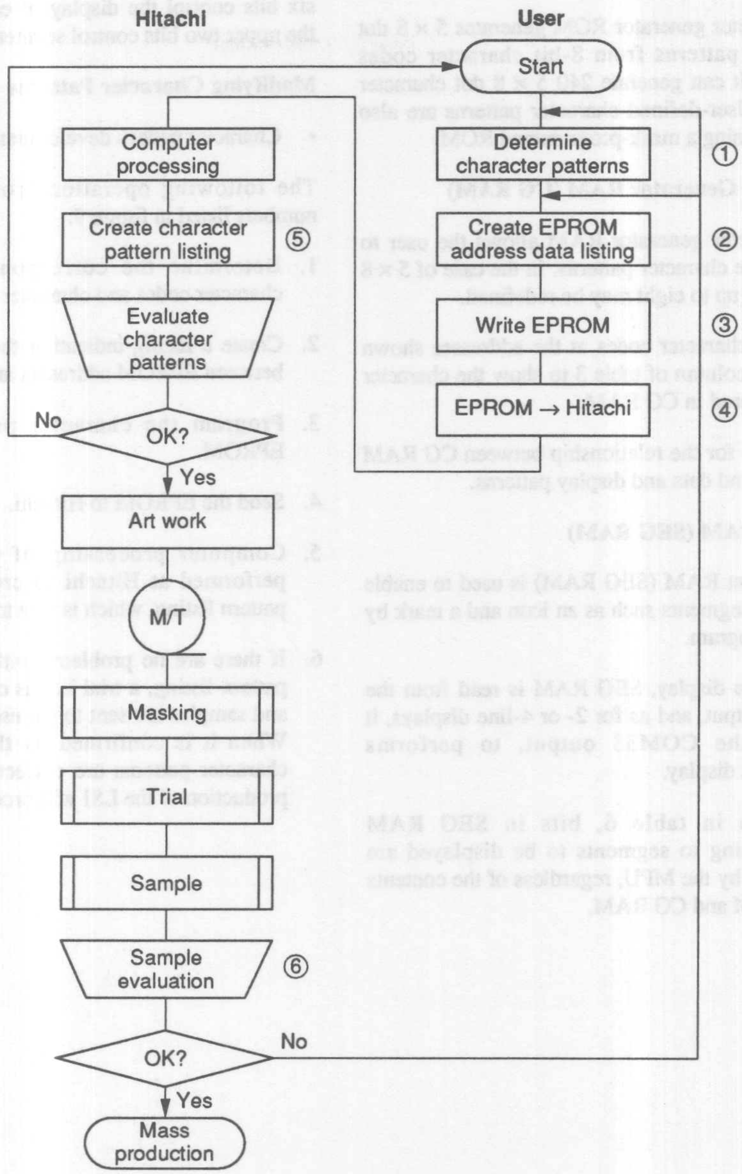
2. Create a listing indicating the correspondence between EPROM addresses and data.

3. Program the character patterns into an EPROM.

4. Send the EPROM to Hitachi.

5. Computer processing of the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.

6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI will proceed at Hitachi.



Note: For a description of the numbers used in this figure, refer to the preceding page.

Figure 9 Character Pattern Development Procedure

Table 3 Correspondence between Character Codes and Character Patterns (Hitachi standard HD66710)

Lower 4 Bits \ Upper 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)			0	@	P	`	p				ｰ	ﾀ	ﾐ	α	p
xxxx0001	(2)		!	1	A	Q	a	q			｡	ｱ	ﾁ	ﾑ	ä	q
xxxx0010	(3)		"	2	B	R	b	r			｢	ｲ	ﾂ	ﾒ	β	θ
xxxx0011	(4)		#	3	C	S	c	s			｣	ｳ	ﾃ	ﾓ	ε	∞
xxxx0100	(5)		$	4	D	T	d	t			､	ｴ	ﾄ	ﾔ	μ	Ω
xxxx0101	(6)		%	5	E	U	e	u			･	ｵ	ﾅ	ﾕ	σ	ü
xxxx0110	(7)		&	6	F	V	f	v			ｦ	ｶ	ﾆ	ﾖ	ρ	Σ
xxxx0111	(8)		'	7	G	W	g	w			ｧ	ｷ	ﾇ	ﾗ	g	π
xxxx1000	(1)		(	8	H	X	h	x			ｨ	ｸ	ﾈ	ﾘ	√	x̄
xxxx1001	(2)		)	9	I	Y	i	y			ｩ	ｹ	ﾉ	ﾙ	⁻¹	y
xxxx1010	(3)		*	:	J	Z	j	z			ｪ	ｺ	ﾊ	ﾚ	j	千
xxxx1011	(4)		+	;	K	[	k	{			ｫ	ｻ	ﾋ	ﾛ	ˣ	万
xxxx1100	(5)		,	<	L	¥	l	|			ｬ	ｼ	ﾌ	ﾜ	¢	円
xxxx1101	(6)		-	=	M	]	m	}			ｭ	ｽ	ﾍ	ﾝ	£	÷
xxxx1110	(7)		.	>	N	^	n	→			ｮ	ｾ	ﾎ	ﾞ	ñ	
xxxx1111	(8)		/	?	O	_	o	←			ｯ	ｿ	ﾏ	ﾟ	ö	█

Note: The user can specify any pattern in the character-generator RAM.

- Programming character patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM. The HD66710 character generator ROM can generate 240 5 × 8 dot character patterns.

— Character patterns

EPROM address data and character pattern data correspond with each other to form a 5 × 8 dot character pattern (table 4).

Table 4 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 8 dots)

EPROM Address												Data (MSB)				(LSB)
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0
0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
								0	0	0	1	1	0	0	0	1
								0	0	1	0	1	0	0	0	1
								0	0	1	1	0	1	0	1	0
								0	1	0	0	0	0	1	0	0
								0	1	0	1	0	0	1	0	0
								0	1	1	0	0	0	1	0	0
								0	1	1	1	0	0	0	0	0

Character code (A_{11}–A_4) "0" (A_3) Line position (A_2–A_0)

Notes: 1. EPROM addresses A_{11} to A_4 correspond to a character code.
2. EPROM addresses A_2 to A_0 specify a line position of the character pattern. EPROM address A3 should be set to 0.
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. Area which are lit (indicated by shading) are stored as 1, and unlit are as 0.
5. The eighth line is also stored in the CGROM, and should also be programmed. If the eighth line is used for a cursor, this data should all be set to zero.
6. EPROM data bits O_7 to O_5 are invalid. 0 should be written in all bits.

— Handling unused character patterns

1. **EPROM data outside the character pattern area:** This is ignored by the character generator ROM for display operation so any data is acceptable.

2. **EPROM data in CG RAM area:** Always fill with zeros. (EPROM addresses 00H to FFH.)

3. **Treatment of unused user patterns in the HD66710 EPROM:** According to the user application, these are handled in either of two ways:

i. **When unused character patterns are not programmed:** If an unused character code is written into DD RAM, all its dots are lit, because the EPROM is filled with 1s after it is erased.

ii. **When unused character patterns are programmed as 0s:** Nothing is displayed even if unused character codes are written into DD RAM. (This is equivalent to a space.)

Table 5 Example of Correspondence between Character Code and Character Pattern (5 × 8 dots) in CGRAM

a) When character pattern in 5 × 8 dots

Character code (DDRAM data)								CGRAM address						MSB CGRAM data LSB								
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	*	1	0	0	0	1	Character pattern (1)
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				0	1	0	1	0	
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	0	1	0	0	
											1	1	1				0	0	0	0	0	
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	*	1	0	0	0	1	Character pattern (8)
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				0	1	0	1	0	
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	0	1	0	0	
											1	1	1				0	0	0	0	0	

Table 5 Example of Correspondence between Character Code and Character Pattern (5 × 8 dots) in CGRAM (cont)

b) When character pattern is 6 × 8 dots

Character code (DDRAM data)								CGRAM address						CGRAM data (MSB … LSB)								
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	O7	O6	O5	O4	O3	O2	O1	O0	
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	0	1	0	0	0	1	Character pattern (1)
											0	0	1			0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
											0	1	1			0	0	1	0	1	0	
											1	0	0			0	0	0	1	0	0	
											1	0	1			0	0	0	1	0	0	
											1	1	0			0	0	0	1	0	0	
											1	1	1			0	0	0	0	0	0	
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	0	1	0	0	0	1	Character pattern (8)
											0	0	1			0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
											0	1	1			0	0	1	0	1	0	
											1	0	0			0	0	0	1	0	0	
											1	0	1			0	0	0	1	0	0	
											1	1	0			0	0	0	1	0	0	
											1	1	1			0	0	0	0	0	0	

Notes:

1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.
3. The character data is stored with the rightmost character element in bit 0, as shown in table 5. Characters with 5 dots in width (FW = 0) are stored in bits 0 to 4, and characters with 6 dots in width (FW = 1) are stored in bits 0 to 5.
4. When the upper four bits (bits 7 to 4) of the character code are 0, CGRAM is selected. Bit 3 of the character code is invalid (*). Therefore, for example, the character codes 00 (hexadecimal) and 08 (hexadecimal) correspond to the same CGRAM address.
5. A set bit in the CGRAM data corresponds to display selection, and 0 to non-selection.
6. When the BE bit of the function set register is 1, pattern blinking control of the lower six bits is controlled using the upper two bits (bits 7 and 6) in CGRAM. When bit 7 is 1, of the lower six bits, only those which are set are blinked on the display. When bit 6 is 1, a bit 4 pattern can be blinked as for a 5-dot font width, and a bit 5 pattern can be blinked as for a 6-dot font width.

* Indicates no effect.

Table 6 Relationships between SEGRAM Addresses and Display Patterns

SEGRAM address			SEGRAM data a) 5-dot font width								SEGRAM data b) 6-dot font width							
A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	B1	B0	*	S1	S2	S3	S4	S5	B1	B0	S1	S2	S3	S4	S5	S6
0	0	1	B1	B0	*	S6	S7	S8	S9	S10	B1	B0	S7	S8	S9	S10	S11	S12
0	1	0	B1	B0	*	S11	S12	S13	S14	S15	B1	B0	S13	S14	S15	S16	S17	S18
0	1	1	B1	B0	*	S16	S17	S18	S19	S20	B1	B0	S19	S20	S21	S22	S23	S24
1	0	0	B1	B0	*	S21	S22	S23	S24	S25	B1	B0	S25	S26	S27	S28	S29	S30
1	0	1	B1	B0	*	S26	S27	S28	S29	S30	B1	B0	S31	S32	S33	S34	S35	S36
1	1	0	B1	B0	*	S31	S32	S33	S34	S35	B1	B0	S37	S38	S39	S40	S41	S42
1	1	1	B1	B0	*	S36	S37	S38	S39	S40	B1	B0	S43	S44	S45	S46	S47	S48
			Blinking control			Pattern on/off					Blinking control		Pattern on/off					

Notes: 1. Data set to SEGRAM is output when COM17 is selected, as for a 1-line display, and output when COM33 is selected, as for a 2-line or a 4-line display.
2. S1 to S48 are pin numbers of the segment output driver.
S1 is positioned to the left of the monitor.
S37 to S48 are extension driver outputs for a 6-dot character width.
3. After S40 output at 5-dot font and S48 output at 6-dot font, S1 output is repeated again.
4. As for a 5-dot font width, lower five bits (D4 to D0) are display on.off information of each segment. For a 6-dot character width, the lower six bits (D5 to D0) are the display information for each segment.
5. When the BE bit of the function set register is 1, pattern blinking of the lower six bits is controlled using the upper two bits (bits 7 and 6) in SEGRAM.
When bit 7 is 1, only a bit set to "1" of the lower six bits is blinked on the display.
When bit 6 is 1, only a bit 4 pattern can be blinked as for a 5-dot font width, and only a bit 5 pattern can be blinked as for 6-dot font width.
6. Bit 5 (D5) is invalid for a 5-dot font width.
7. Set bits in the CGRAM data correspond to display selection, and zeros to non-selection.

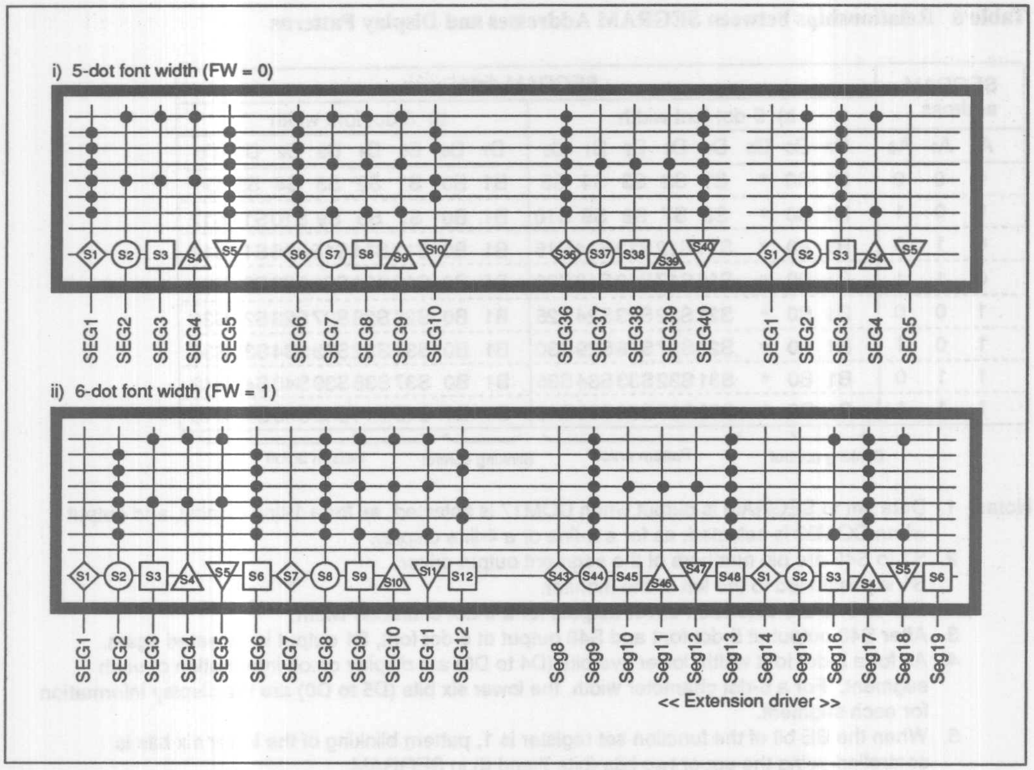


Figure 10 Relationships between SEGRAM Data and Display

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DD RAM, CG ROM, CG RAM, and SEGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DD RAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 33 common signal drivers and 40 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data then enables the driver to generate drive waveform outputs.

Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD66710 drives from the head display.

Cursor/Blink Control Circuit

The cursor/blink (or white-black inversion) control is used to produce a cursor or a flashing area on the display at a position corresponding to the location in stored in the address counter (AC).

For example (figure 11), when the address counter is 08H, a cursor is displayed at a position corresponding to DDRAM address 08H.

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
AC	0	0	0	1	0	0	0

For a 1-line display

Display position	1	2	3	4	5	6	7	8	9	10	11
DD RAM address (hexadecimal)	00	01	02	03	04	05	06	07	08	09	0A

Cursor position

For a 2-line display

Display position	1	2	3	4	5	6	7	8	9	10	11
DD RAM address (hexadecimal)	00	01	02	03	04	05	06	07	08	09	0A
	40	41	42	43	44	45	46	47	48	49	4A

Cursor position

Note: Even if the address counter (AC) points to an address in the character generator RAM (CGRAM) or segment RAM (SEGRAM), cursor/blink black-white inversion will still occur, although it will produce meaningless results.

Figure 11 Cursor/Blink Display Example

Interfacing to the MPU

The HD66710 can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB_4 to DB_7) are used for transfer. Bus lines DB_0 to DB_3 are disabled. The data transfer between the HD66710 and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB_4 to DB_7) are transfered before the four low order bits (for 8-bit operation, DB_0 to DB_3).

  The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

- For 8-bit interface data, all eight bus lines (DB_0 to DB_7) are used.

Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD66710 when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 15 ms after V_{CC} rises to 4.5 V or 40 ms after the Vcc rises to 2.7 V.

1. Display clear
2. Function set:
   DL = 1; 8-bit interface data
   N = 0; 1-line display
   RE = 0: Extension register write disable
3. Display on/off control:
   D = 0; Display off
   C = 0; Cursor off
   B = 0; Blinking off
   BE = 0: CGRAM/SEGRAM blinking off
   LP = 0: Not in low power mode
4. Entry mode set:
   I/D = 1; Increment by 1
   S = 0; No shift
5. Extension function set
   FW = 0; 5-dot character width
   B/W = 0; Normal cursor (eighth line)
   NW = 0; 1- or 2-line display (depending on N)
6. SEGRAM address set
   HDS = 000; No scroll

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD66710. For such a case, initialization must be performed by the MPU as explained in the section, Initializing by Instruction.

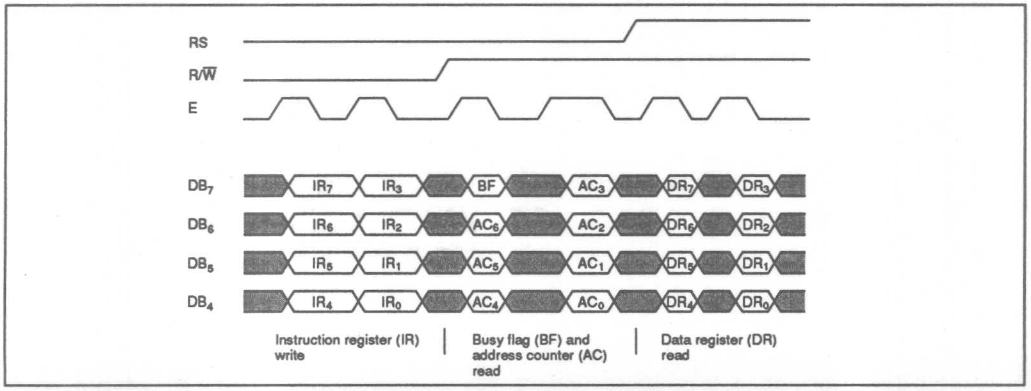


Figure 12 4-Bit Transfer Example

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66710 can be controlled by the MPU. Before starting internal operation of the HD66710, control information is temporarily stored in these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD66710 is determined by signals sent from the MPU. These signals, which include register selection (RS), read/write (R/$\overline{W}$), and the data bus (DB0 to DB7), make up the HD66710 instructions (table 7). There are four categories of instructions that:

- Designate HD66710 functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66710 RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (table 7) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the HD66710 is not in the busy state (BF = 1) before sending an instruction from the MPU to the HD66710. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to table 7 for the list of each instruction execution time.

Table 7 Instructions

Instruction	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Description	Execution Time (max) (when f_{cp} or f_{OSC} is 270 kHz)
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.52 ms
Return home	0	0	0	0	0	0	0	0	1	—	Sets DD RAM address 0 in address counter. Also returns display from being shifted to original position. DD RAM contents remain unchanged.	1.52 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 µs
Display on/off control (RE = 0)	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	37 µs
Extension function set (RE = 1)	0	0	0	0	0	0	1	FW	B/W	NW	Sets a font width, a black-white inverting cursor (B/W), a 6-dot font width (FW), and a 4-line display (NW).	37 µs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DD RAM contents.	37 µs
Function set (RE = 0)	0	0	0	0	1	DL	N	RE	—	—	Sets interface data length (DL), number of display lines (N), and extension register write enable (RE)).	37 µs
(RE = 1)	0	0	0	0	1	DL	N	RE	BE	LP	Sets CGRAM/SEGRAM blinking enable (BE), and low power mode (LP). LP is available when the EXT pin is low.	37 µs
Set CGRAM address (RE = 0)	0	0	0	1	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	Sets CG RAM address. CG RAM data is sent and received after this setting.	37 µs
Set DDRAM address (RE = 0)	0	0	1	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	Sets DD RAM address. DD RAM data is sent and received after this setting.	37 µs
Set SEGRAM address (RE = 1)	0	0	1	HDS	HDS	HDS	*—	ASG	ASG	ASG	Sets SEGRAM address. DDRAM data is sent and received after this setting. Also sets a horizontal dot scroll quantity (HDS).	37 µs

Table 7 Instructions (cont)

Instruction	Code RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Description	Execution Time (max) (when f_{cp} or f_{OSC} is 270 kHz)
Read busy flag & address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs
Write data to RAM (RE = 0/1)	1	0	Write data								Writes data into DD RAM, CG RAM, or SEGRAM. To write data to DD RAM CG RAM, clear RE to 0; or to write data to SEG RAM, set RE to 1.	37 µs t_{ADD} = 5.5 µs*
Read data from RAM (RE = 0/1)	1	1	Read data								Reads data from DD RAM, CG RAM, or SEGRAM. To read data from DD RAM or CG RAM, clear RE to 0; to read data from SEG RAM, set RE to 1.	37 µs t_{ADD} = 5.5 µs*

I/D = 1: Increment
I/D = 0: Decrement
S = 1: Accompanies display shift
D = 1: Display on
C = 1: Cursor on
B = 1: Blink on
FW = 1: 6-dot font width
B/W = 1: Black-white inverting cursor on
NW = 1: Four lines
NW = 0: One or two lines
S/C = 1: Display shift
S/C = 0: Cursor move
R/L = 1: Shift to the right
R/L = 0: Shift to the left
DL = 1: 8 bits, DL = 0: 4 bits
N = 1: 2 lines, N = 0: 1 line
RE = 1: Extension register access enable
BE = 1: CGRAM/SEGRAM blinking enable
LP = 1: Low power mode
BF = 1: Internally operating
BF = 0: Instructions acceptable

DD RAM: Display data RAM
CG RAM: Character generator RAM
SEGRAM: Segment RAM

A_{CG}: CG RAM address
A_{DD}: DD RAM address (corresponds to cursor address)
ASEG: Segment RAM address
HDS: Horizontal dot scroll quantity
AC: Address counter used for both DD, CG, and SEG RAM addresses.

Notes: 1. — indicates no effect.
* After execution of the CG RAM/DD RAM/SEGRAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In figure 13, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

2. Extension time changes as frequency changes. For example, when f is 300 kHz, the execution time is: 37 µs x 270/300 = 33 µs.

3. Execution time in a low power mode (LP = 1 & EXT = low) becomes four times as long as for a 1-line mode, and twice as long as for a 2- or 4-line mode.

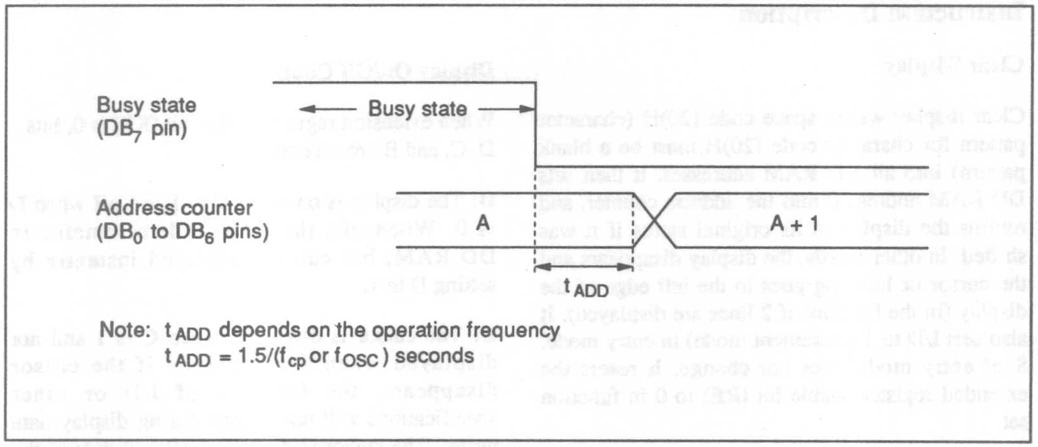


Figure 13 Address Counter Update

Instruction Description

Clear Display

Clear display writes space code (20)H (character pattern for character code (20)H must be a blank pattern) into all DD RAM addresses. It then sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change. It resets the extended register enable bit (RE) to 0 in function set.

Return Home

Return home sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DD RAM contents do not change.

The cursor or blinking go to the left edge of the display (in the first line if 2 lines are displayed). It resets the extended register enable bit (RE) to 0 in function set.

Entry Mode Set

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from DD RAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM and SEG RAM.

S: Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1 during DD RAM write. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DD RAM. Also, writing into or reading out from CG RAM and SEG RAM does not shift the display. In a low power mode (LP = 1), do not set S = 1 because the whole display does not normally shift.

Display On/Off Control

When extension register enable bit (RE) is 0, bits D, C, and B are accessed.

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in DD RAM, but can be displayed instantly by setting D to 1.

C: The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5 × 8 dot character font.

B: The character indicated by the cursor blinks when B is 1 (figure 14). The blinking is displayed as switching between all blank dots and displayed characters at a speed of 370-ms intervals when f_{cp} or f_{OSC} is 270 kHz. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to f_{OSC} or the reciprocal of f_{cp}. For example, when f_{cp} is 300 kHz, 370 × 270/300 = 333 ms.)

Extended Function Set

When the extended register enable bit (RE) is 1, FW, B/W, and NW bit shown below are accessed. Once these registers are accessed, the set values are held even if the RE bit is set to zero.

FW: When FW is 1, each displayed character is controlled with a 6-dot width. The user font in CG RAM is displayed with a 6-bit character width from bits 5 to 0. As for fonts stored in CG ROM, no display area is assigned to the leftmost bit, and the font is displayed with a 5-bit character width. If the FW bit is changed, data in DD RAM and CG RAM SEG RAM is destroyed. Therefore, set FW before data is written to RAM. When font width is set to 6 dots, the frame frequency decreases to 5/6 compared to 5-dot time. See "Oscillator Circuit" for details.

B/W: When B/W is 1, the character at the cursor position is cyclically displayed with black-white invertion. At this time, bits C and B in display on/off control register are "Don't care". When f_{CP} or f_{OSC} is 270 kHz, display is changed by switching every 370 ms.

NW: When NW is 1, 4-line display is performed. At this time, bit N in the function set register is "Don't care".

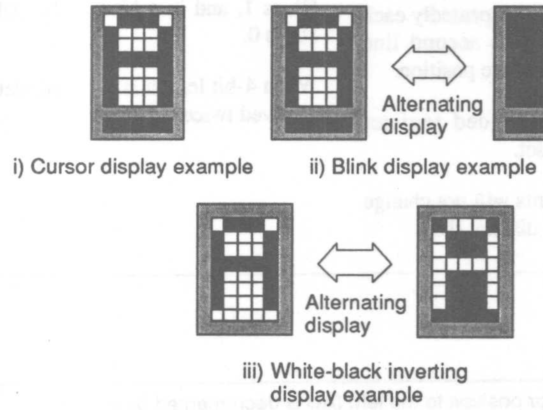


Figure 14 Cursor Blink Width Control

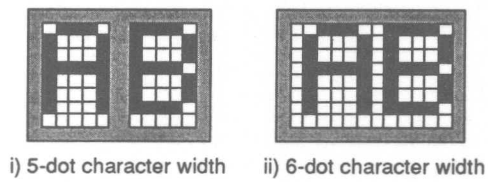


Figure 15 Character Width Control

Cursor or Display Shift

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (table 8). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. In a 4-line display, the cursor moves to the second line when it passes the 20th character of the line. Note that, all line displays will shift at the same time. When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position.

These instruction reset the extended register enable bit (RE) to 0 in function set.

The address counter (AC) contents will not change if the only action performed is a display shift.

In low power mode (LP = 1), whole-display shift cannot be normally performed.

Function Set

Only when the extended register enable bit (RE) is 1, the BE bit shown below can be accessed. Bits DL and N can be accessed regardless of RE.

DL: Sets the interface data length. Data is sent or received in 8-bit lengths (DB_7 to DB_0) when DL is 1, and in 4-bit lengths (DB_7 to DB_4) when DL is 0.

When 4-bit length is selected, data must be sent or received twice.

Table 8 Shift Function

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

N: When bit NW in the extended function set is 0, a 1- or a 2-line display is set. When N is 0, 1-line display is selected; when N is 1, 2-line display is selected. When NW is 1, a 4-line display is set. At this time, N is "Don't care".

RE: When the RE bit is 1, bit BE and LP in the extended function set registe, the SEGRAM address set register, and the extended function set register can be accessed. When bit RE is 0, the registers described above cannot be accessed, and the data in these registers is held.

To maintain compatibility with the HD44780, the RE bit should be fixed to 0.

Clear display, return home and cursor or display shift instruction a reset the RE bit to 0.

BE: When the RE bit is 1, this bit can be rewritten. When this bit is 1, the user font in CGRAM and the segment in SEGRAM can be blinked according to the upper two bits of CGRAM and SEGRAM.

LP: When the RE bit is 1, this bit can be rewritten. When LP is set to 1 and the EXT pin is low (without an extended driver), the HD66710 operates in low power mode. In 1-line display mode, the HD66710 operates on a 4-division clock, and in a 2-line or a 4-line display mode, the HD66710 operates on a 2-division clock. According to these operations, instruction execution takes four times or twice as long. Notice that in a low power mode, display shift cannot be performed.

Note: Perform the DL, N, NW, FW functions at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, if bit N, NW, or FW is changed after other instructions are executed, RAM contents may be lost.

Set CG RAM Address

A CG RAM address can be set while the RE bit is cleared to 0. Set CG RAM address sets the CG RAM address binary AAAAAA into the address counter.

Data is then written to or read from the MPU for CG RAM.

Table 9 Display Line Set

N	NW	No. of Display Lines	Character Font	Duty Factor	Maximum Number of Characters/ 1 Line with Extended Drivers
0	0	1	5 × 8 dots	1/17	50 characters
1	0	2	5 × 8 dots	1/33	30 characters
*	1	4	5 × 8 dots	1/33	20 characters

Note: * Indicates don't care.

Set DD RAM Address

Set DD RAM address sets the DD RAM address binary AAAAAAA into the address counter while the RE bit is cleared to 0.

Data is then written to or read from the MPU for DD RAM.

However, when N and NW is 0 (1-line display), AAAAAAA can be 00H to 4FH. When N is 1 and NW is 0 (2-line display), AAAAAAA is (00)H to (27)H for the first line, and (40)H to (67)H for the second line. When NW is 1 (4-line display), AAAAAAA is (00)H to (13)H for the first line, (20)H to (33)H for the second line, (40)H to (53)H for the third line, and (60)H to (73)H for the fourth line.

Set SEGRAM Address

Only when the extended register enable bit (RE) is 1, HS2 to HS0 and the SEGRAM address can be set.

The SEGRAM address in the binary form AAA is set to the address counter. SEGRAM can then be written to or read from by the MPU.

Note: When performing a horizontal scroll is described above by connecting an extended driver, the maximum number of characters per line decreases by one. In other words, 49 characters, 29 characters, and 19 characters are displayed in 1-line, 2-line, and 4-line modes, respectively. Notice that in low power mode (LP = 1), the display shift and scroll cannot be performed.

Read Busy Flag and Address

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by all CG, DD, and SEGRAM addresses, and its value is determined by the previous instruction. The address contents are the same as for CG RAM, DD RAM, and SEGRAM address set instructions.

Table 10 HS2 to HS0 Settings

HS2	HS1	HS0	Description
0	0	0	No shift
0	0	1	Shift the display position to the left by one dot.
0	1	0	Shift the display position to the left by two dots.
0	1	1	Shift the display position to the left by three dots.
1	0	0	Shift the display position to the left by four dots.
1	0	1	Shift the display position to the left by five dots.
1	1	0 or 1	No shift.

Clear display — Code

RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	0	0	0	0	1

Return home — Code

RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	0	0	0	1	*

Note: * Don't care.

Entry mode set — Code

RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	0	0	1	I/D	S

Display on/off control — Code

RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	0	1	D	C	B

Extended function set — RE = 1 Code

RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	0	1	FW	B/W	NW

Cursor or display shift — Code

RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	1	S/C	R/L	*	*

Note: * Don't care.

Function set — Code

RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	DL	N	RE	BE*	LP*

Note: * BE and LP can be rewritten while RE = 1.

Set CG RAM address — RE = 0 Code

RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	1	A	A	A	A	A	A

Highest order bit (DB_5) … Lowest order bit (DB_0)

Figure 16 Character Width Control

Set DDRAM address

	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
RE = 0	0	0	1	A	A	A	A	A	A	A
				Highest order bit						Lowest order bit

Set SEGRAM address

	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
RE = 1	0	0	1	HS_2	HS_1	HS_0	*	A	A	A

Read busy flag and address

	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	1	BF	A	A	A	A	A	A	A
				Highest order bit						Lowest order bit

Figure 16 Character Width Control (cont)

Write Data to CG, DD, or SEG RAM

This instruction writes 8-bit binary data DDDDDDDD to CG, DD or SEGRAM. If the RE bit is cleared, CG or DD RAM is selected, as determined by the previous specification of the address set instruction; if the RE bit is set, SEG RAM is selected. After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift direction.

Read Data from CG, DD, or SEG RAM

This instruction reads 8-bit binary data DDDDDDDD from CG, DD, or SEG RAM. If the RE bit is cleared, CG or DD RAM is selected, as determined by the previous specification of the address set instruction; if the RE bit is set, SEG RAM is selected. If no address is specified, the first data read will be invalid. When executing serial read instructions, the next address is normally read from the next address. An address set instruction need not be executed just before this read instruction when shifting the cursor by a cursor shift instruction (when reading from DD RAM). A cursor shift instruction is the same as a set DD RAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, a display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented after write instructions to CG, DD or SEG RAM. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to read data correctly, execute either an address set instruction or a cursor shift instruction (only with DD RAM), or alternatively, execute a preliminary read instruction to ensure the address is correctly set up before accessing the data.

		RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Write data to CG, DD, or SEG RAM	RE = 0/1 Code	1	0	D	D	D	D	D	D	D	D

← Higher order bits Lower order bits →

		RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Read data from CG, DD, or SEG RAM	RE = 0/1 Code	1	1	D	D	D	D	D	D	D	D

← Higher order bits Lower order bits →

Figure 16 Character Width Control (cont)

Interfacing the HD66710

1) Interface to 8-Bit MPUs

HD66710 can interface to 8-bit MPU directly with E clock, or to 8-bit MCU through I/O port. When number of I/O port in MCU, or interfacing bus width, 4-bit interface function is useful.

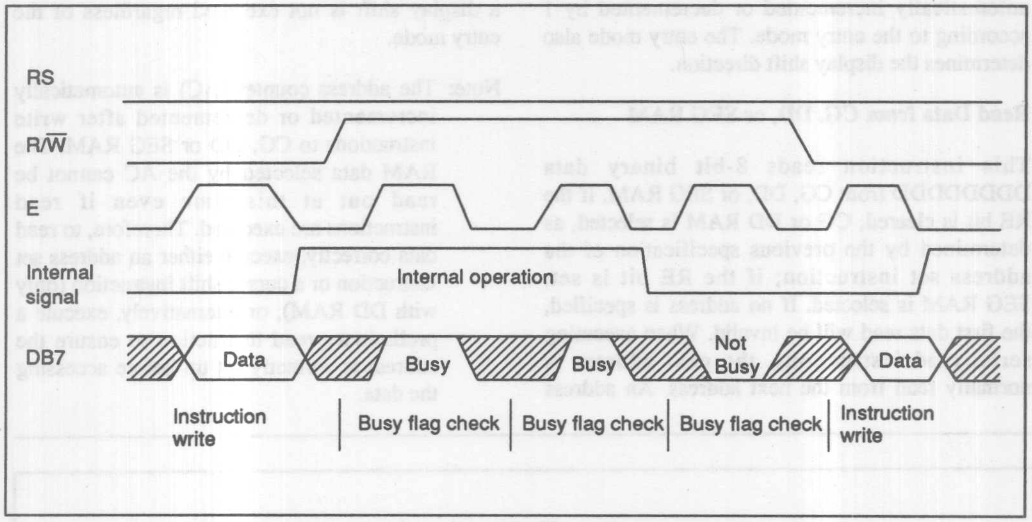


Figure 17 Example of 8-Bit Data Transfer Timing Sequence

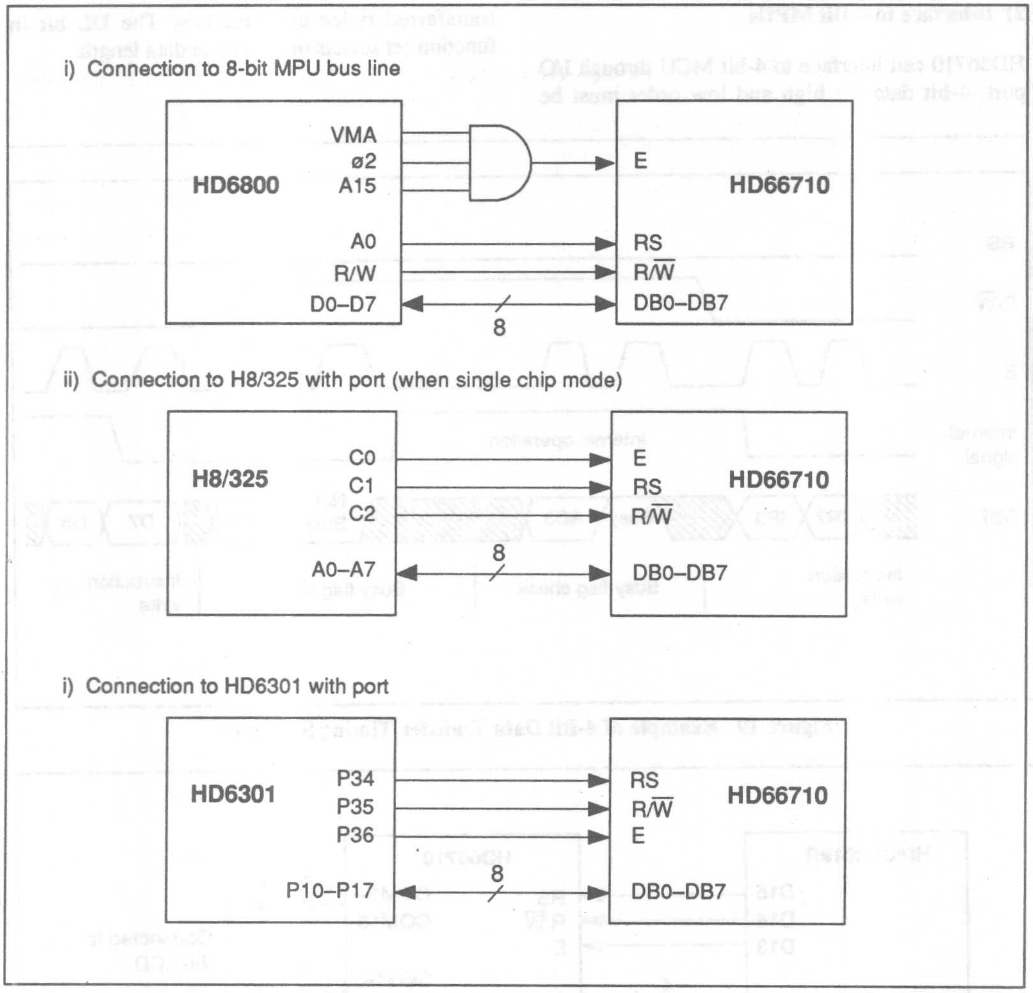


Figure 18 8-Bit MPU Interface

2) Interface to 4-Bit MPUs

HD66710 can interface to 4-bit MCU through I/O port. 4-bit data for high and low order must be transferred twice continuously. The DL bit in function set selects the interface data length.

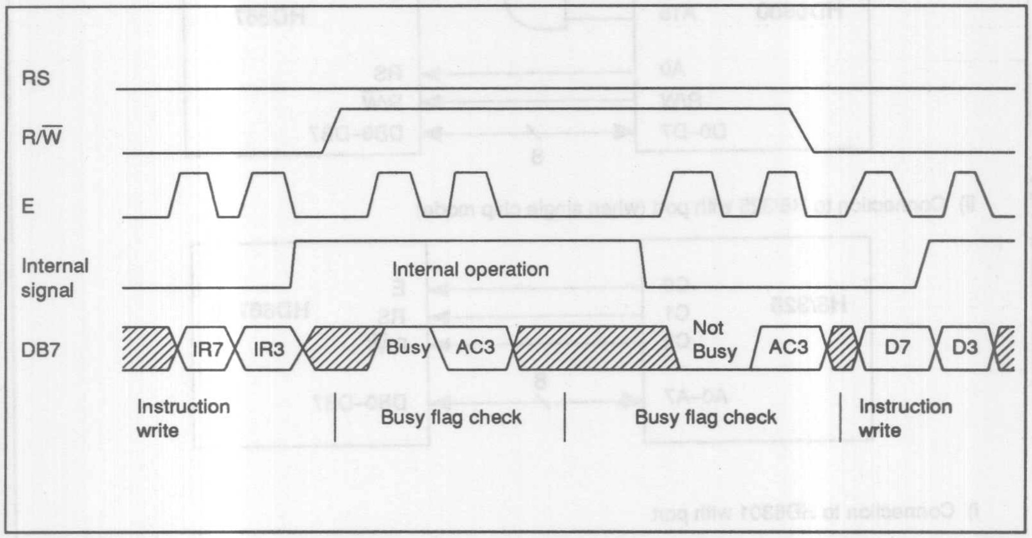


Figure 19 Example of 4-Bit Data Transfer Timing Sequence

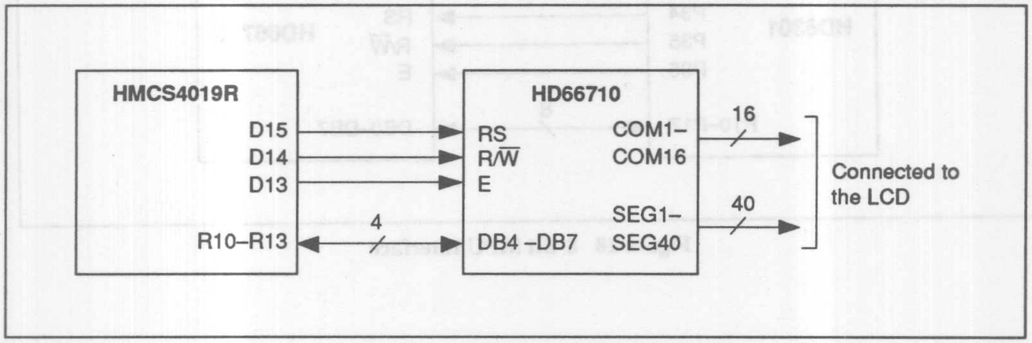
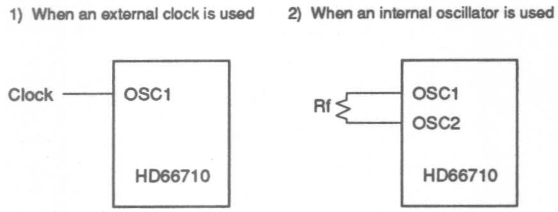


Figure 20 Interface to HMCS4019R

Oscillator Circuit

- Relationship Between Oscillation frequency and Liquid Crystal Display Frame Frequency

  The liquid crystal display frame frequencies of figure 22 apply only when the oscillation frequency is 270 kHz (one clock period: 3.7 μs).

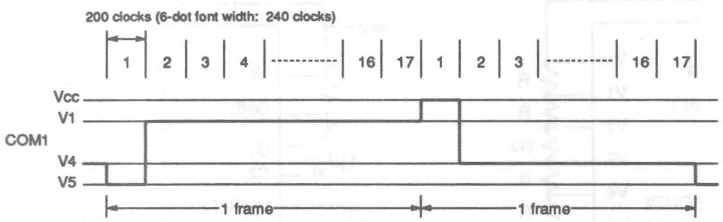


The oscillator frequency can be adjusted by oscillator resistance (Rf). If Rf is increased or power supply voltage is decreased, the oscillator frequency decreases. The recommended oscillator resistor is as follows.

- Rf = 91 kΩ ± 2% (Vcc = 5 V)
- Rf = 75 kΩ ± 2% (Vcc = 3 V)

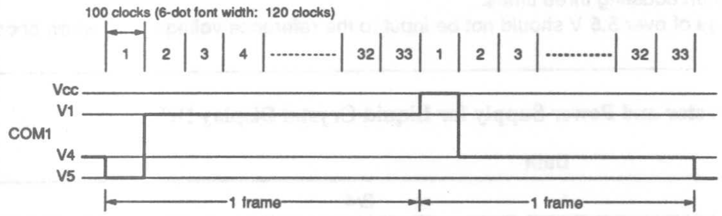
Figure 21 Oscillator Circuit

(1) 1 /17 duty cycle



Item	Normal Display Mode (LP = 0) 5-Dot Font Width	6-Dot Font Width	Low Power Mode (LP = 1) 5-Dot Font Width	6-Dot Font Width
Line selection period	200 clocks	240 clocks	50 clocks	60 clocks
Frame frequency	79.4 Hz	66.2 Hz	79.4 Hz	66.2 Hz

(2) 1 /33 duty cycle

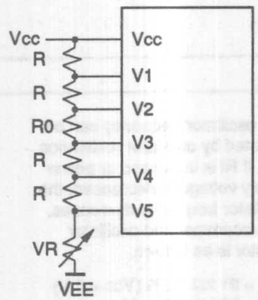


Item	Normal Display Mode (LP = 0) 5-Dot Font Width	6-Dot Font Width	Low Power Mode (LP = 1) 5-Dot Font Width	6-Dot Font Width
Line selection period	100 clocks	120 clocks	50 clocks	60 clocks
Frame frequency	81.8 Hz	68.2 Hz	81.8 Hz	68.2 Hz

Figure 22 Frame Frequency

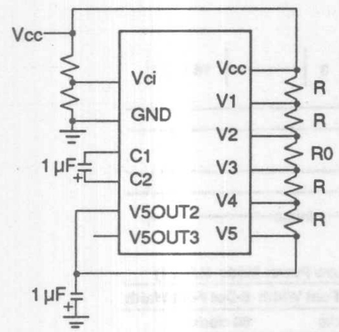
Power Supply for Liquid Crystal Display Drive

1) When an external power supply is used

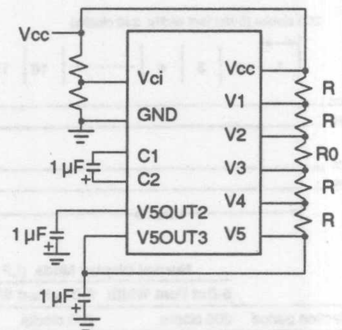


2) When an internal booster is used

(Boosting twice)



(Boosting three times)



Notes: 1. Boosted output voltage should not exceed the maximum value (13 V) of the liquid crystal power supply voltage. Especially, a voltage of over 4.3 V should not be input to the reference voltage (Vci) when boosting three times.

2. A voltage of over 5.5 V should not be input to the reference voltage (Vci) when boosting twice.

Table 11 Duty Factor and Power Supply for Liquid Crystal Display Drive

Item		Data	
Number of Lines		1	2/4
Duty factor		1/17	1/33
Bias		1/5	1/6.7
Divided resistance	R	R	R
	R0	R	2.7R

Note: R changes depending on the size of liquid crystal penel. Normally, R must be 2 kΩ to 10 kΩ.

Extension Driver LSI Interface

By bringing the EXT pin high, segment driver pins (SEG37 to SEG40) functions as the extended driver interface outputs. From these pins, a latch pulse (CL1), a shift clock (CL2), data (D), and an AC signal (M) are output. The same data is output from the SEG36 pin of the HD66710 and the start segment pin (Seg1) of the extension driver. Due to the character baundary, the Seg1 output is used for the 5-dot font width. For the 6-dot font width, the SEG36 output is used, and the Seg1 output of the extension driver must not be used. When the extension driver LSI interface is used, ground level (GND) must be higher than the V5 level.

Table 12 Required Number of 40-Output Extension Driver

Controller	HD66710*		HD44780	HD66702
Display Line	5-Dot Width	6-Dot Width	5-Dot Width	5-Dot Width
16 × 2 lines	Not required	1	1	Not required
20 × 2 lines	1	1	2	Not required
24 × 2 lines	1	2	2	1
40 × 2 lines	Disabled	Disabled	4	3
12 × 4 lines	1	1	Disabled	Disabled
16 × 4 lines	2	2	Disabled	Disabled
20 × 4 lines	2	3	Disabled	Disabled

Note: * The number of display lines can be extended to 30 × 2 lines or 20 × 4 lines.

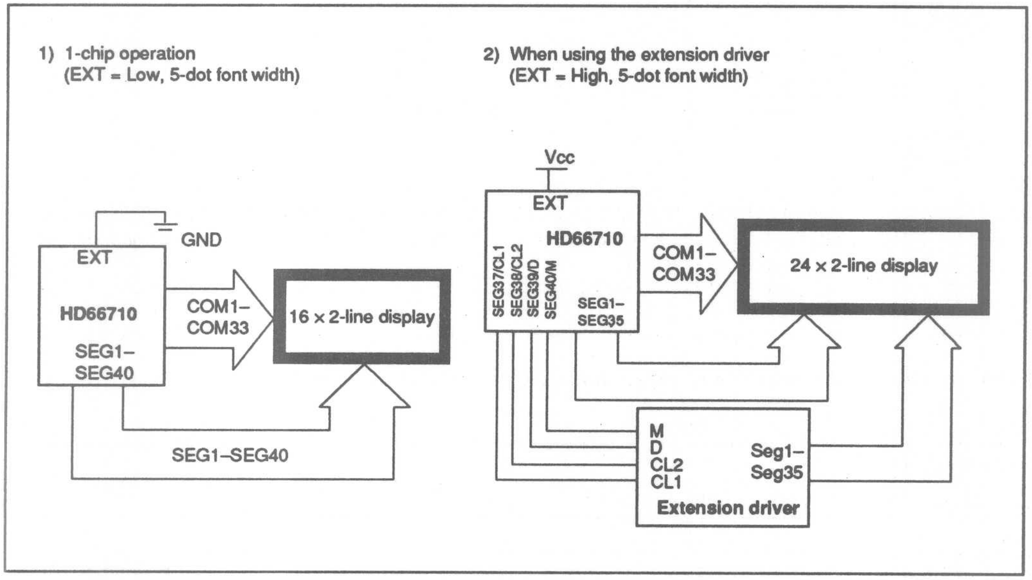


Figure 23 HD66710 and the Extension Driver Connection

When using one HD66710, the start address of COM9–COM16/COM25–COM33 is calculated by adding 8 to the start address of COM9–COM16 COM25–COM32. When extending the address, the start address is calculated by adding A(10) to COM9–COM16/COM25 to COM32. The relationship betweenmodes and display start addresses is shown below.

Table 13 Display Start Address in Each Mode

	Number of Lines				
	1-Line Mode		2-Line Mode		4-Line Mode
Output	EXT Low	EXT High	EXT Low	EXT High	EXT Low/High
COM1–COM8	D00±1	D00±1	D00±1	D00±1	D00±1
COM9–COM16	D08±1	D0A±1	D08±1	D0A±1	D20±1
COM17–COM24	—	—	D40±1	D40±1	D40±1
COM25–COM32	—	—	D48±1	D4A±1	D60±1
COM17	S00	S00	—	—	—
COM33	—	—	S00	S00	S00

Notes: 1. When an EXT pin is low, the extension driver is not used; otherwise, the extension driver is used.
2. D** is the start address of display data RAM (DDRAM) for each display line.
3. S** is the start address of segment RAM (SEGRAM).
4. ±1 following D** indicates increment or decrement at display shift.

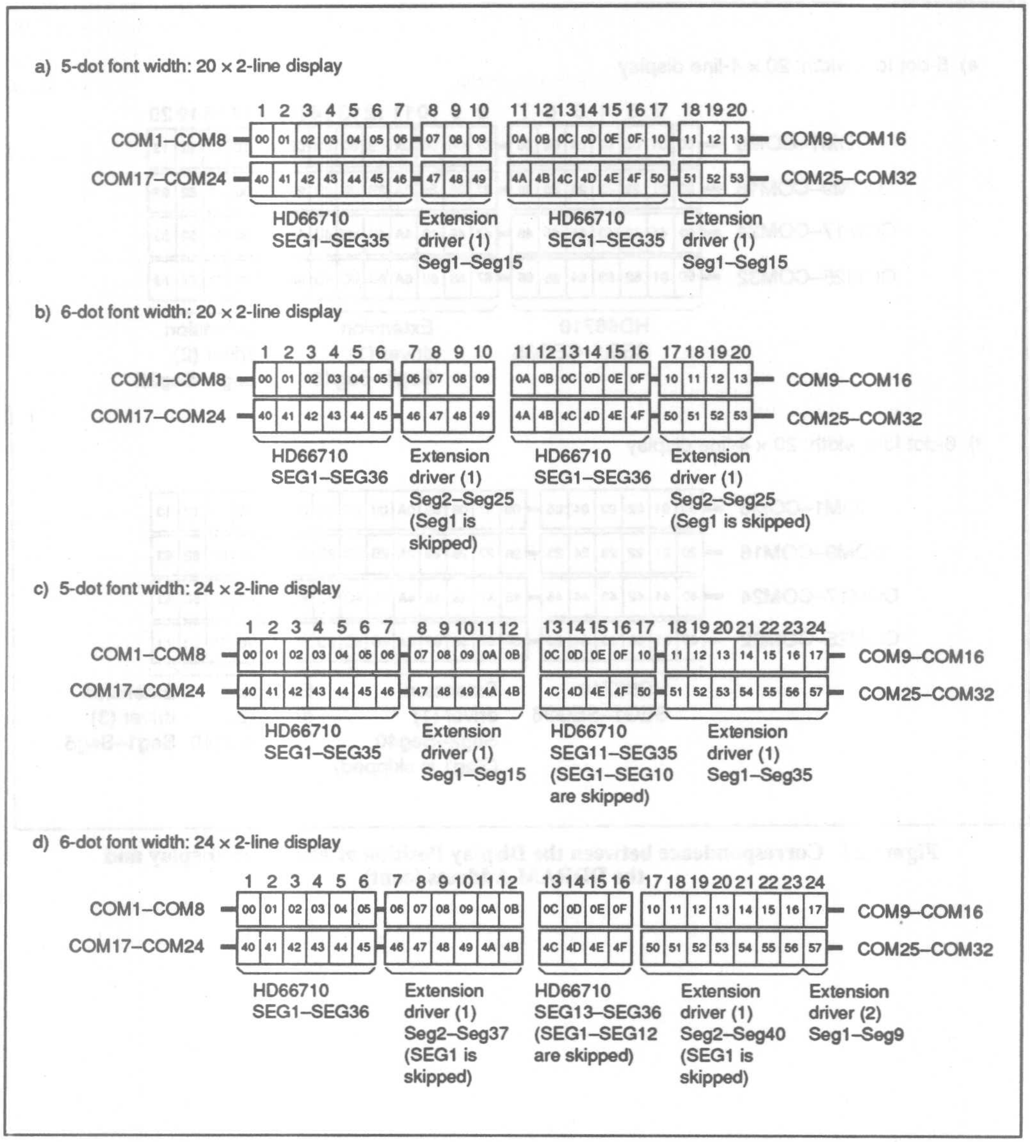


Figure 24 Correspondence between the Display Position at Extension Display and the DDRAM Address

e) 5-dot font width: 20 × 4-line display

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
COM1–COM8	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
COM9–COM16	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	60	61	62	63
COM17–COM24	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
COM25–COM32	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73

HD66710 SEG1–SEG35 (positions 1–7); Extension driver (1) Seg1–Seg40; Extension driver (2) Seg1–Seg25

f) 6-dot font width: 20 × 4-line display

COM1–COM8	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
COM9–COM16	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	60	61	62	63
COM17–COM24	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
COM25–COM32	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73

HD66710 SEG1–SEG36; Extension driver (1) Seg2–Seg40 (Seg1 is skipped); Extension driver (2) Seg1–Seg40; Extension driver (3) Seg1–Seg5

Figure 24 Correspondence between the Display Position at Extension Display and the DDRAM Address (cont)

Interface to Liquid Crystal Display

Set the extended driver interface, the number of display lines, and the font width with the EXT pin, an extended register NW, and the FW bit, respectively. The relationship between the EXT pin, register set value, and the display lines are given below.

Table 14 Relationship between EXT, Register Setting, and Display Lines

No of Lines	No. of Charactrers	EXT Pin	Extended Driver	5-Dot Font				EXT Pin	Extended Driver	6-Dot Font				Duty
				N	RE	NW	FW			N	RE	NW	FW	
1	16	L	—	0	0	0	0	H	1	0	1	0	1	1/17
	20	H	1	0	0	0	0	H	1	0	1	0	1	1/17
	24	H	1	0	0	0	0	H	2	0	1	0	1	1/17
2	16	L	—	1	0	0	0	H	1	1	1	0	1	1/33
	20	H	1	1	0	0	0	H	1	1	1	0	1	1/33
	24	H	1	1	0	0	0	H	2	1	1	0	1	1/33
4	16	H	1	*	1	1	0	H	1	*	1	1	1	1/33
	20	H	2	*	1	1	0	H	2	*	1	1	1	1/33
	24	H	2	*	1	1	0	H	3	*	1	1	1	1/33

Note: — means not required.

• Example of 5-dot font width connection

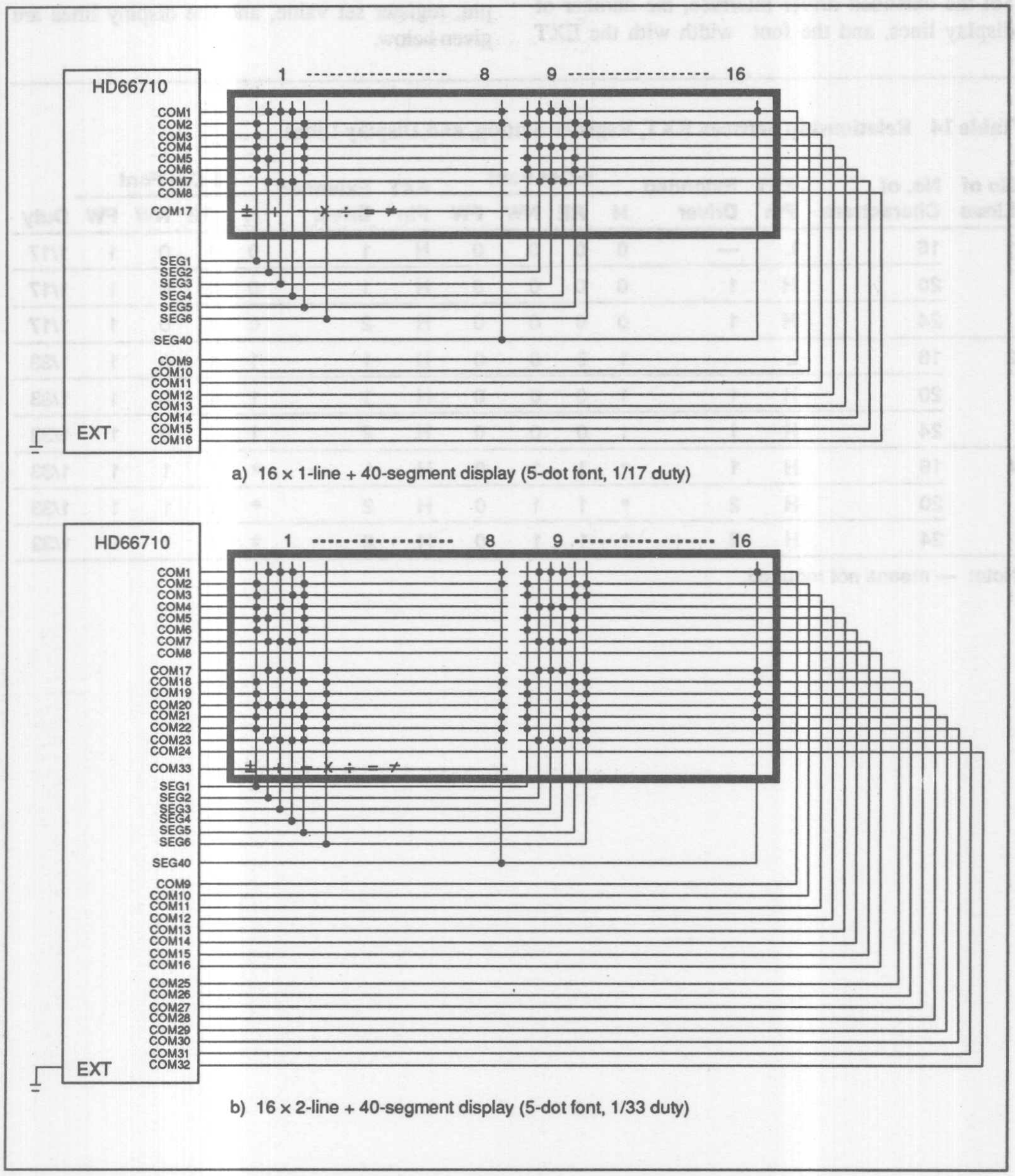


Figure 25 Liquid Crystal Display and HD66710 Connections (Single-Chip Operation)

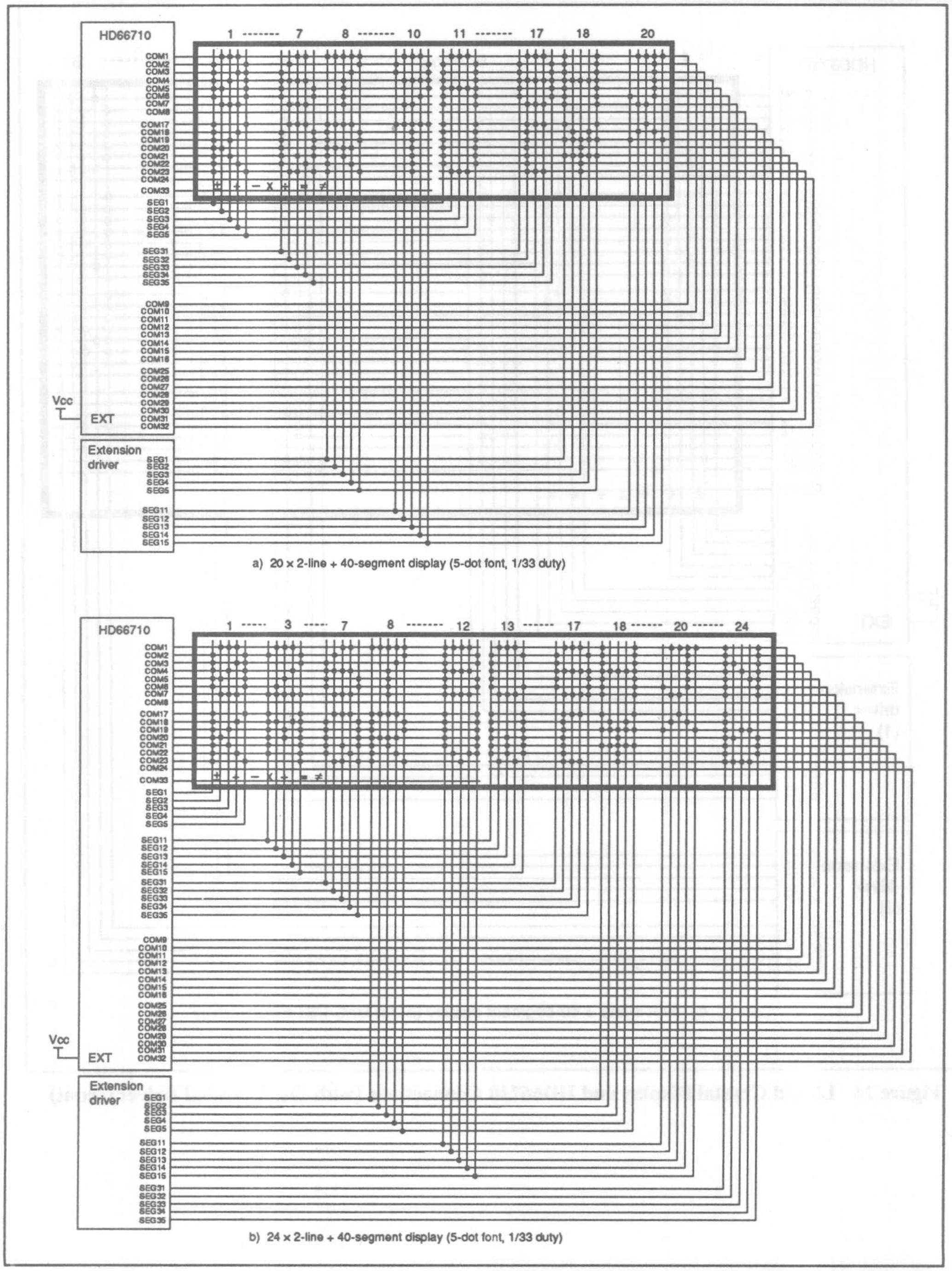
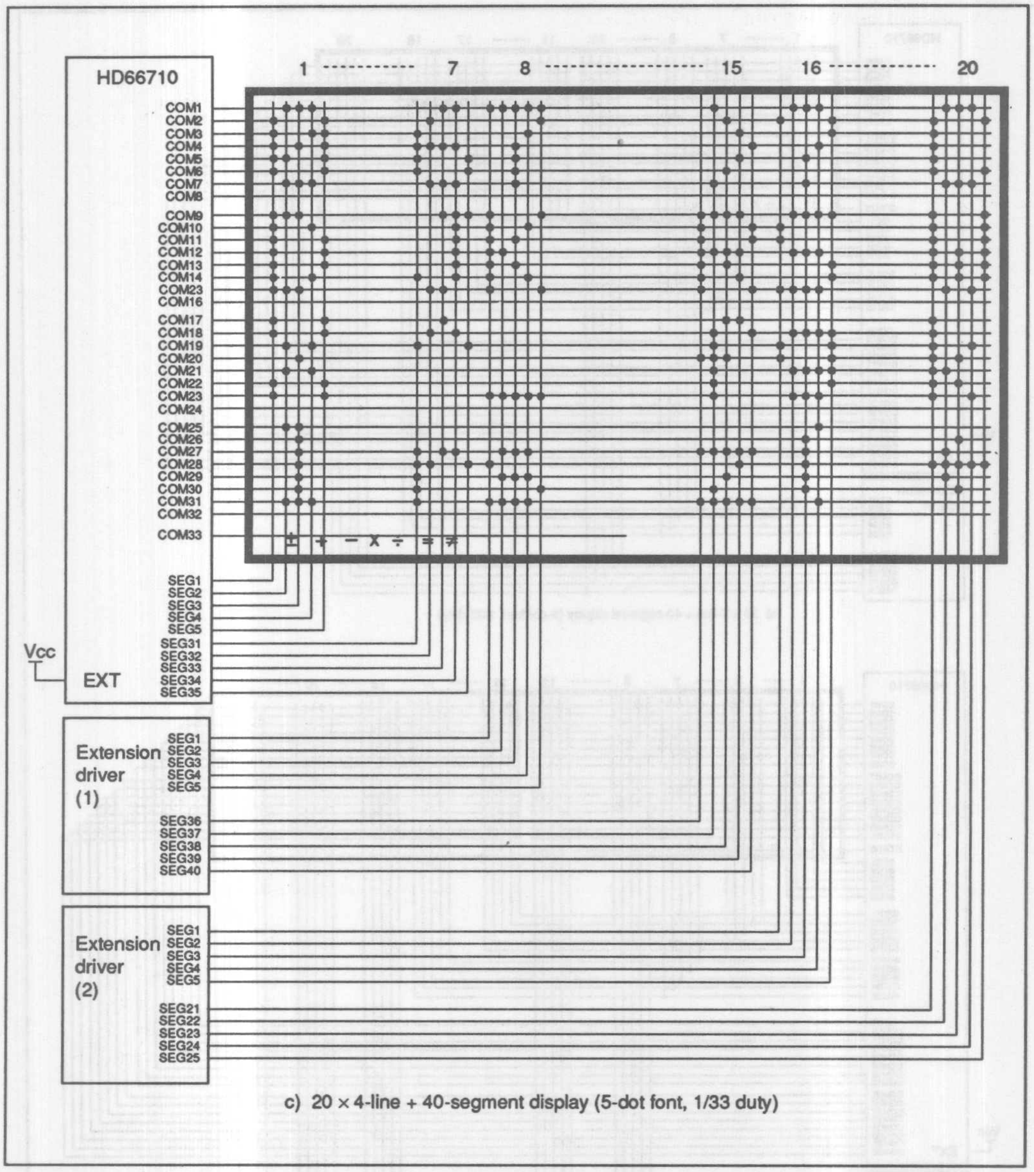


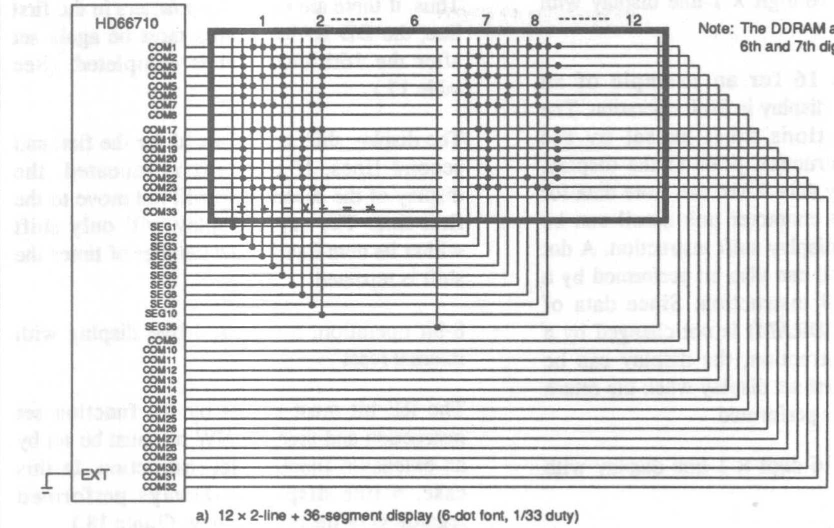
Figure 26 Liquid Crystal Display and HD66710 Connections (with the Extended Driver)



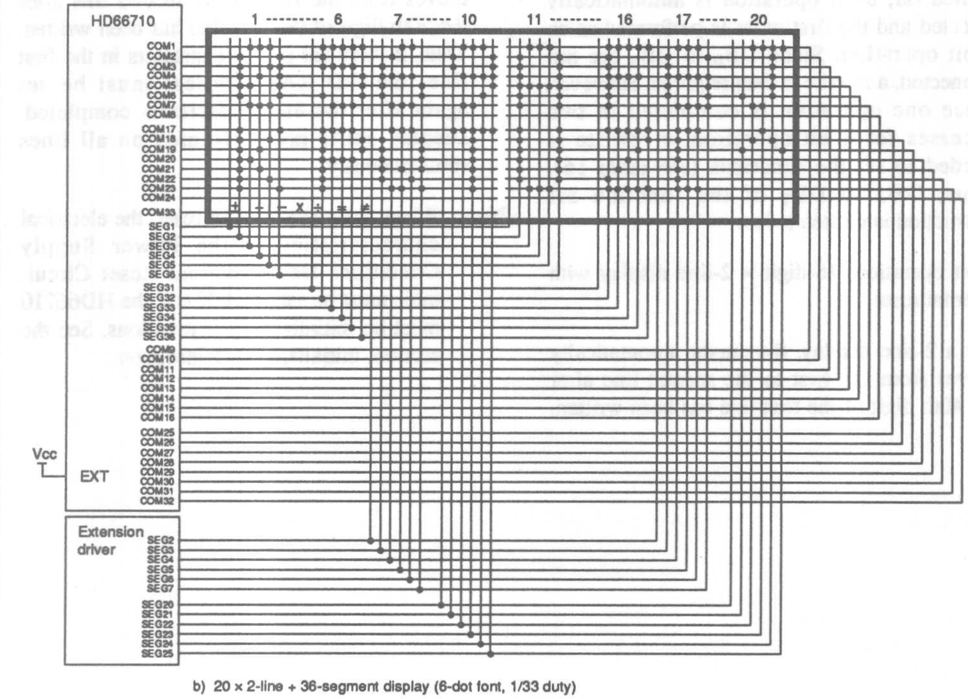
c) 20 × 4-line + 40-segment display (5-dot font, 1/33 duty)

Figure 26 Liquid Crystal Display and HD66710 Connections (with the Extended Driver) (cont)

- Example of 6-dot font width connection



a) 12 × 2-line + 36-segment display (6-dot font, 1/33 duty)



b) 20 × 2-line + 36-segment display (6-dot font, 1/33 duty)

Figure 27 Liquid Crystal Display and HD66710 Connections (6-Dot Font Width)

Instruction and Display Correspondence

- 8-bit operation, 16-digit × 1-line display with internal reset

Refer to table 16 for an example of an 16-digit × 1-line display in 8-bit operation. The HD66710 functions must be set by the function set instruction prior to the display. Since the display data RAM can store data for 80 characters, a character unit scroll can be performed by a display shift instruction. A dot unit smooth scroll can also be performed by a horizontal scroll instruction. Since data of display RAM (DDRAM) is not changed by a display shift instruction, the display can be returned to the first set display when the return home operation.is performed.

- 4-bit operation, 16-digit × 1-line display with internal reset

The program must set all functions prior to the 4-bit operation (table 16). When the power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since DB_0 to DB_3 are not connected, a rewrite is then required. However, since one operation is completed in two accesses for 4-bit operation, a rewrite is needed to set the functions (see table 16). Thus, DB_4 to DB_7 of the function set instruction is written twice.

- 8-bit operation, 16-digit × 2-line display with internal reset

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 16 characters in the first line, the DD RAM address must be again set after the 16th character is completed. (See table 17.)

The display shift is performed for the first and second lines. If the shift is repeated, the display of the second line will not move to the first line. The same display will only shift within its own line for the number of times the shift is repeated.

- 8-bit operation, 8-digit × 4-line display with internal reset

The RE bit must be set by the function set instruction and then the NW bit must be set by an extension function set instruction. In this case, 4-line display is always performed regardless of the N bit setting. (Table 18.)

In a 4-line display, the cursor automatically moves from the first to the second line after the 20th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must be set again after the 8th character is completed. Display shifts are performed on all lines simultaneously.

Note: When using the internal reset, the electrical characteristics in the Power Supply Conditions Using Internal Reset Circuit table must be satisfied. If not, the HD66710 must be initialized by instructions. See the section, Initializing by Instruction.

Table 15 8-Bit Operation, 16-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction: RS	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Display	Operation
1	Power supply on (the HD66710 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 8-bit operation and selects 1-line display. Bit 2 must always be cleared.
	0	0	0	0	1	1	0	0	*	*		
3	Display on/off control										_	Turns on display and cursor. Entire display is in space mode because of initialization.
	0	0	0	0	0	0	1	1	1	0		
4	Entry mode set										_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
	0	0	0	0	0	0	0	1	1	0		
5	Write data to CG RAM/DD RAM										H_	Writes H. DD RAM has already been selected by initialization when the power was turned on.
	1	0	0	1	0	0	1	0	0	0		
6	Write data to CG RAM/DD RAM										HI_	Writes I.
	1	0	0	1	0	0	1	0	0	1		
7	⋮										⋮	
8	Write data to CG RAM/DD RAM										HITACHI_	Writes I.
	1	0	0	1	0	0	1	0	0	1		
9	Entry mode set										HITACHI_	Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1		
10	Write data to CG RAM/DD RAM										ITACHI _	Writes a space.
	1	0	0	0	1	0	0	0	0	0		

Table 15 8-Bit Operation, 16-Digit × 1-Line Display Example with Internal Reset (cont)

Step No.	RS	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Display	Operation
	Instruction											
11	Write data to CG RAM/DD RAM										TACHI M_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
12	⋮										⋮	
13	Write data to CG RAM/DD RAM										MICROKO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
14	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
15	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
16	Write data to CG RAM/DD RAM										ICROCO	Writes C over K. The display moves to the left.
	1	0	0	1	0	0	0	0	1	1		
17	Cursor or display shift										MICROCO	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	1	1	*	*		
18	Cursor or display shift										MICROCO_	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	0	1	*	*		
19	Write data to CG RAM/DD RAM										ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
20	⋮										⋮	
21	Return home										HITACHI	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 16 4-Bit Operation, 16-Digit × 1-Line Display Example with Internal Reset

Step No.	RS	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Display	Operation
1	Power supply on (the HD66710 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 4-bit operation. Clear bit 2. In this case, operation is handled as 8 bits by initialization.
	0	0	0	0	1	0	–	–	–	–		
	–	–	–	–	–	–	–	–	–	–		
3	Function set											Sets 4-bit operation and selects 1-line display. Clear bit 2. 4-bit operation starts from this step.
	0	0	0	0	1	0	–	–	–	–		
	0	0	0	0	*	*	–	–	–	–		
4	Display on/off control										_	Turns on display and cursor. Entire display is in space mode because of initialization.
	0	0	0	0	0	0	–	–	–	–		
	0	0	1	1	1	0	–	–	–	–		
5	Entry mode set										_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
	0	0	0	0	0	0	–	–	–	–		
	0	0	0	1	1	0	–	–	–	–		
6	Write data to CG RAM/DD RAM										H_	Writes H. DDRAM has already been selected by initialization.
	1	0	0	1	0	0	–	–	–	–		
	1	0	1	0	0	0	–	–	–	–		

Note: The control is the same as for 8-bit operation beyond step #6.

Table 17 8-Bit Operation, 16-Digit × 2-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Display	Operation
1	Power supply on (the HD66710 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											
	0	0	0	0	1	1	1	0	*	*		Sets to 8-bit operation and selects 1-line display. Clear bit 2.
3	Display on/off control											
	0	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. All display is in space mode because of initialization.
4	Entry mode set											
	0	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
5	Write data to CG RAM/DD RAM											
	1	0	0	1	0	0	1	0	0	0	H_	Writes H. DD RAM has already been selected by initialization when the power was turned on.
6					⋮						⋮	
7	Write data to CG RAM/DD RAM											
	1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.
8	Set DD RAM address											
	0	0	1	1	0	0	0	0	0	0	HITACHI _	Sets RAM address so that the cursor is positioned at the head of the second line.

Table 17 8-Bit Operation, 16-Digit × 2-Line Display Example with Internal Reset (cont)

Step No.	RS	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Display	Operation
9	Write data to CG RAM/DD RAM											Writes a space.
	1	0	0	1	0	0	1	1	0	1	HITACHI M_	
10	⋮										⋮	
11	Write data to CG RAM/DD RAM											Writes O.
	1	0	0	1	0	0	1	1	1	1	HITACHI MICROCO_	
12	Entry mode set											Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1	HITACHI MICROCO_	
13	Write data to CG RAM/DD RAM											Writes M.
	1	0	0	1	0	0	1	1	0	1	ITACHI ICROCOM_	
14	⋮										⋮	
15	Return home											Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0	HITACHI MICROCOM	

Table 18 8-Bit Operation, 8-Digit × 4-Line Display Example with Internal Reset

Step No.	Instruction	RS	$R/\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Display	Operation
1	Power supply on (the HD66710 is initialized by the internal reset circuit)												Initialized. No display.
2	Function set	0	0	0	0	1	1	0	1	*	*		Sets to 8 bit operation and the extended register enable bit.
3	4-line mode set	0	0	0	0	0	0	1	0	0	1		Sets 4-line display.
4	Function set Clear extended register enable bit	0	0	0	0	1	1	0	0	*	*		Clears the extended register enable bit. Setting the N bit is "don't care".
5	Display on/off control	0	0	0	0	0	0	1	1	1	0	_	Turn on display and cursor. Entire display is in space mode because of initialization.
6	Entry mode set	0	0	0	0	0	0	0	1	1	0	_	Set mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
7	Write data to CGRAM/DDRAM	1	0	0	1	0	0	1	0	0	0	H_	Write H. DDRAM has already been selected by initialization when the power was turned on.
8	—												

Table 18 8-Bit Operation, 8-Digit × 4-Line Display Example with Internal Reset (cont)

Step No.	RS	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Display	Operation
9	Write data to CGRAM/DDRAM											Write I.
	1	0	0	1	0	0	1	0	0	1	HITACHI_	
10	Set DDRAM address											Sets RAM address so that the cursor is positioned at the head of the second line.
	0	0	1	0	1	0	0	0	0	0	HITACHI _	
11	Write data to CGRAM/DDRAM											Write 0.
	1	0	0	0	1	1	0	0	0	0	HITACHI 0_	

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

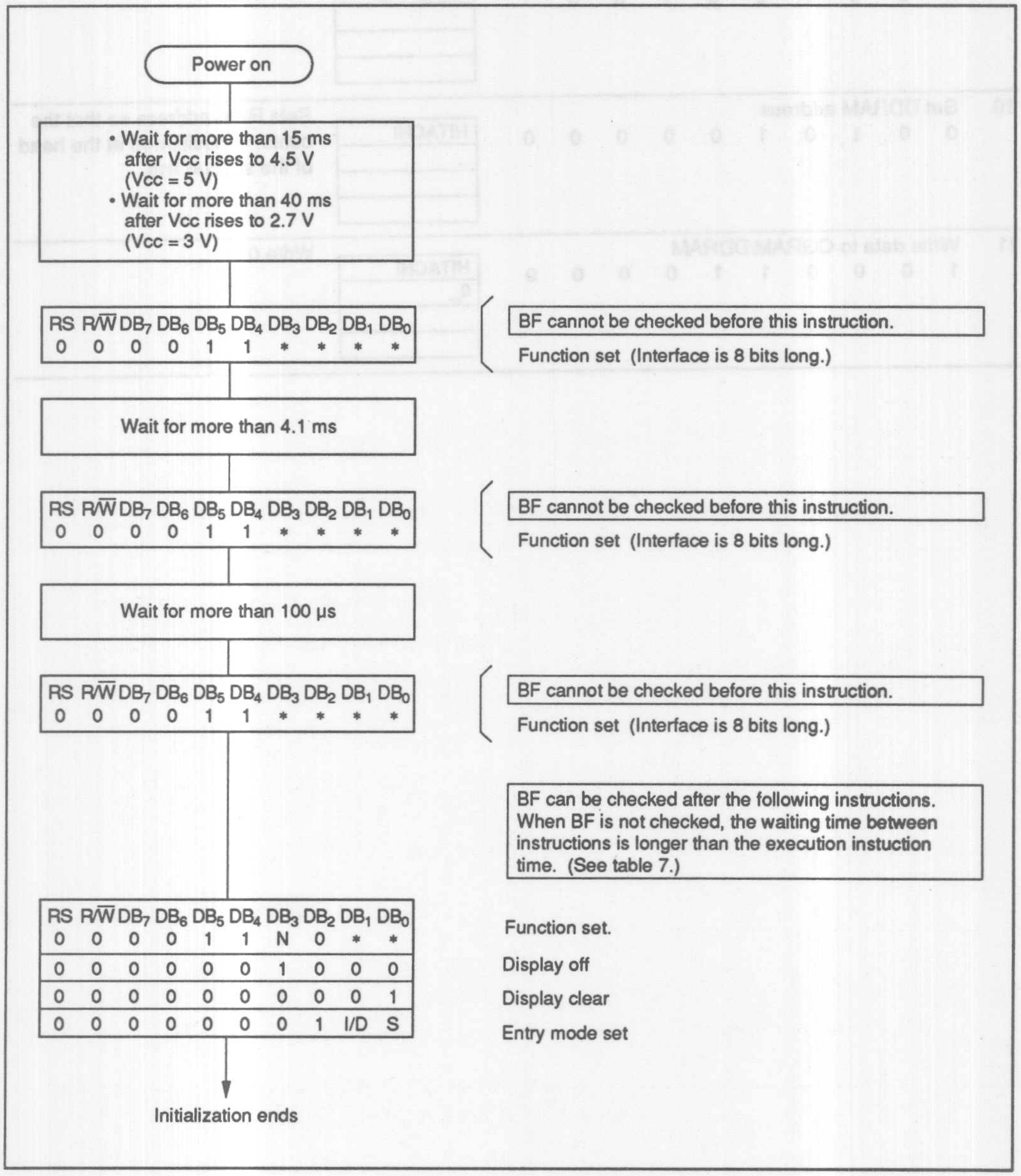


Figure 28 8-Bit Interface

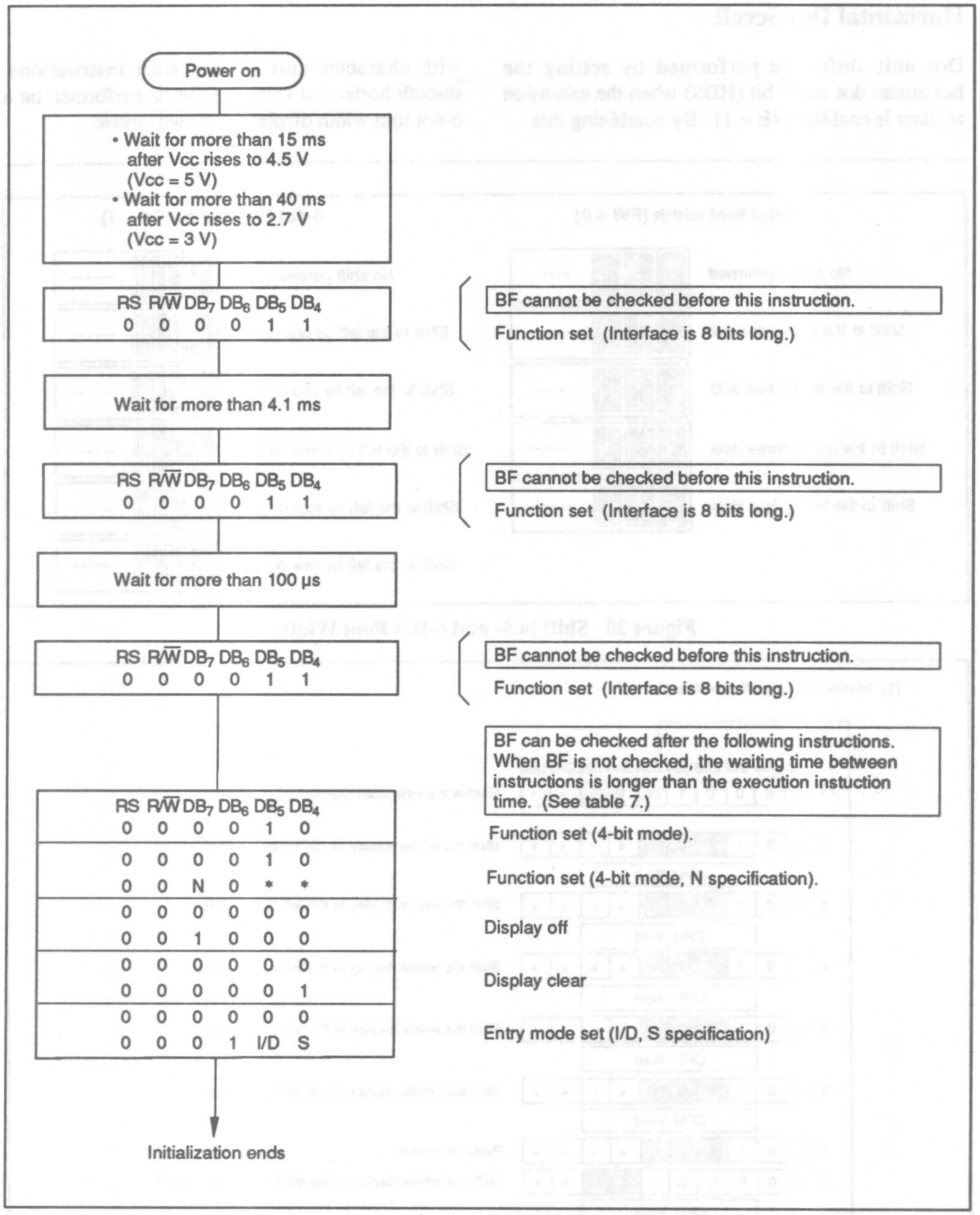


Figure 29 4-Bit Interface

Horizontal Dot Scroll

Dot unit shifts are performed by setting the horizontal dot scroll bit (HDS) when the extension register is enabled (RE = 1). By combining this with character unit display shift instructions, smooth horizontal scrolling can be performed on a 6-dot font width display as shown below.

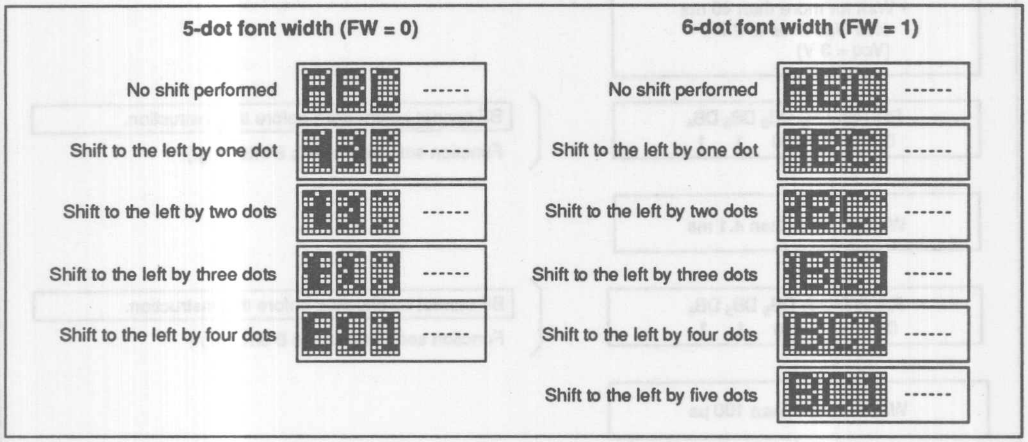


Figure 30 Shift in 5- and 6-Dot Font Width

(1) Method of smooth scroll to the left

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	0	0	0	1	DL	N	1	*	*	Enable the extension register
2	0	0	1	0	0	1	*	*	*	*	Shift the whole display to the left by one dot
			CPU Wait								
3	0	0	1	0	1	0	*	*	*	*	Shift the whole display to the left by two dots
			CPU Wait								
4	0	0	1	0	1	1	*	*	*	*	Shift the whole display to the left by three dots
			CPU Wait								
5	0	0	1	1	0	0	*	*	*	*	Shift the whole display to the left by four dots
			CPU Wait								
6	0	0	1	1	0	1	*	*	*	*	Shift the whole display to the left by five dots*1
			CPU Wait								
7	0	0	1	0	0	0	*	*	*	*	Perform no shift
8	0	0	0	0	0	1	1	0	*	*	Shift the whole display to the left by one character*2
			CPU Wait								

Notes: 1. When the font width is five (FW = 0), this step is skipped.
2. The extended register enable bit (RE) is cleared.

Figure 31 Smooth Scroll to the Left

(2) Method of smooth scroll to the right

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	0	0	0	0	1	1	1	*	*	Shift the whole display to the right by one character *2
2	0	0	0	0	1	DL	N	1	*	*	Enable the extension register
			CPU Wait								
3	0	0	1	1	0	1	*	*	*	*	Shift the whole display to the left by five dots *1
			CPU Wait								
4	0	0	1	1	0	0	*	*	*	*	Shift the whole display to the left by four dots
			CPU Wait								
5	0	0	1	0	1	1	*	*	*	*	Shift the whole display to the left by three dots
			CPU Wait								
6	0	0	1	0	1	0	*	*	*	*	Shift the whole display to the left by two dots
			CPU Wait								
7	0	0	1	0	0	1	*	*	*	*	Shift the whole display to the left by one dot
			CPU Wait								
8	0	0	1	0	0	0	*	*	*	*	Perform no shift

Notes: 1. When the font width is five (FW = 0), this step is skipped.
2. The extended register enable bit (RE) is cleared.

Figure 31 Smooth Scroll to the Left (cont)

Low Power Mode

When LP bit is 1 and the EXT pin is low (without an extended driver), the HD66710 operates in low power mode. In 1-line display mode, the HD66710 operates on a 4-division clock, and in 2-line or 4-line display mode, it operates on 2-division clock. So, instruction execution takes four times or twice as long. Notice that in this mode, display shift and scroll cannot be performed. Clear display shift with the return home instruction, and the horizontal scroll quantity.

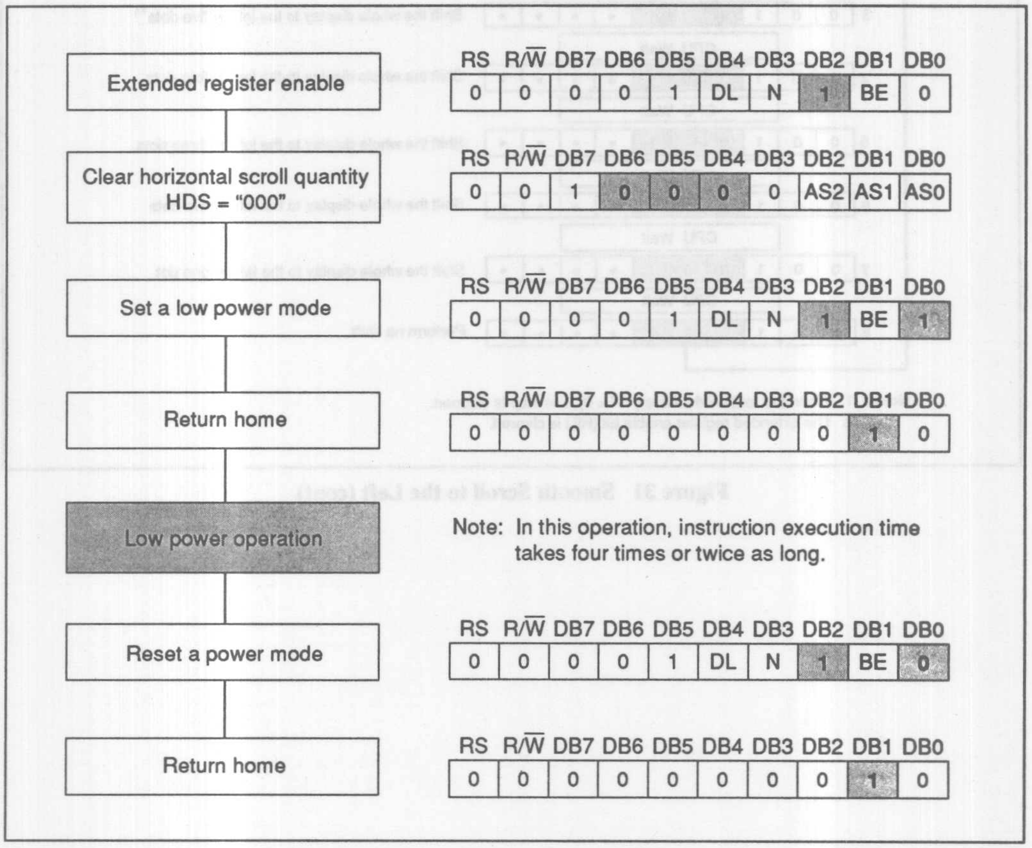


Figure 32 Low Power Mode Operation

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes*
Power supply voltage (1)	V_{CC}	–0.3 to +7.0	V	1
Power supply voltage (2)	$V_{CC}–V_5$	–0.3 to +15.0	V	1, 2
Input voltage	V_t	–0.3 to V_{CC} +0.3	V	1
Operating temperature	T_{opr}	–20 to +75	°C	3
Storage temperature	T_{stg}	–55 to +125	°C	4

Notes: If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

* Refer to the Electrical Characteristics Notes section following these tables.

DC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20°C to +75°C*3)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC_1)	V_{IH1}	$0.7V_{CC}$	—	V_{CC}	V		6
Input low voltage (1) (except OSC_1)	V_{IL1}	–0.3	—	$0.2V_{CC}$	V		6
		–0.3	—	0.6			
Input high voltage (2) (OSC_1)	V_{IH2}	$0.7V_{CC}$	—	V_{CC}	V		15
Input low voltage (2) (OSC_1)	V_{IL2}	—	—	$0.2V_{CC}$	V		15
Output high voltage (1) ($D_0–D_7$)	V_{OH1}	$0.75V_{CC}$	—	—	V	$–I_{OH}$ = 0.1 mA	7
Output low voltage (1) ($D_0–D_7$)	V_{OL1}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.1 mA	7
Output high voltage (2) (except $D_0–D_7$)	V_{OH2}	$0.8V_{CC}$	—	—	V	$–I_{OH}$ = 0.04 mA	8
Output low voltage (2) ($D_0–D_7$)	V_{OL2}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA (COM)	13
Driver on resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA (SEG)	13
I/O leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current ($D_0–D_7$, RS, R/$\overline{W}$)	–Ip	10	50	120	µA	V_{CC} = 3 V	
Power supply current	IST	—	TBD	TBD	mA	R_f oscillation, external clock V_{CC} = 3V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD1}	3.0	—	13.0	V	$V_{CC}–V_5$, 1/5 bias	16
	V_{LCD2}	3.0	—	13.0	V	$V_{CC}–V_5$, 1/4 bias	16

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Output voltage (V5OUT2 pin)	V_{UP2}	—	TBD	—	V	V_{ci} = 4.5 V, I_0 = 0.5 mA, T_a = 25°C	18
Output voltage (V5OUT3 pin)	V_{UP3}	—	TBD	—	V	V_{ci} = 3 V, I_0 = 0.3 mA, T_a = 25°C	18
Input voltage	V_{Ci}	2.5	—	4.5	V		18

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20°C to +75°C*3)

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	125	270	410	kHz		11
	External clock duty	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{fcp}	—	—	0.2	µs		
R_f oscillation	Clock oscillation frequency	f_{OSC}	190	270	350	kHz	R_f = 75 kΩ, Vcc = 3 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics (1) (V_{CC} = 2.7 V to 4.5 V, T_a = –20°C to +75°C*3)

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 33
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 34
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data delay time	t_{DDR}	—	—	360		
Data hold time	t_{DHR}	5	—	—		

Bus Timing Characteristics (2) (V_{CC} = 4.5 V to 5.5 V, T_a = –20°C to +75°C*3)

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 33
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data set-up time	t_{DSW}	60	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 34
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data delay time	t_{DDR}	—	—	160		
Data hold time	t_{DHR}	5	—	—		

Segment Extension Signal Timing (V_{CC} = 2.7 V to 5.5 V, T_a = –20°C to +75°C*3)

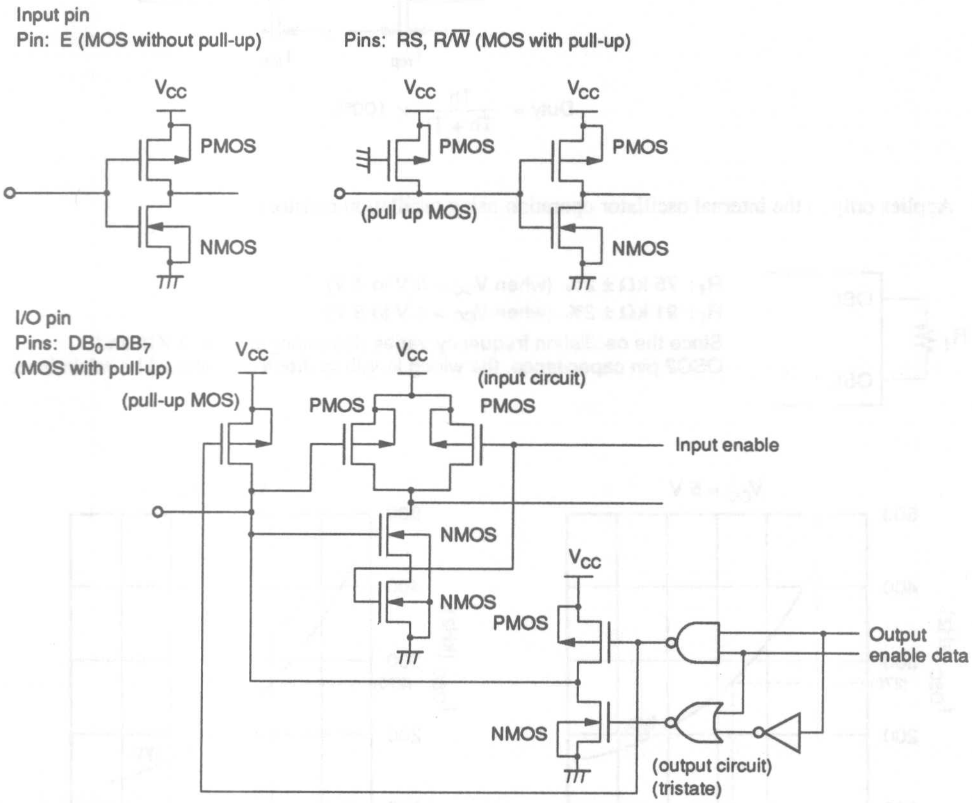
Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 35
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	TBD		

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 36
Power supply off time	t_{OFF}	1	—	—		

Electrical Characteristics Notes

1. All voltage values are referred to GND = 0 V. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.
2. $V_{CC} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ must be maintained. In addition, if the SEG37/CL1, SEG38/CL2, SEG39/D, and SEG40/M are used as extension driver interface signals (EXT = high), GND ≥ V5 must be maintained.
3. For die products, specified up to 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.



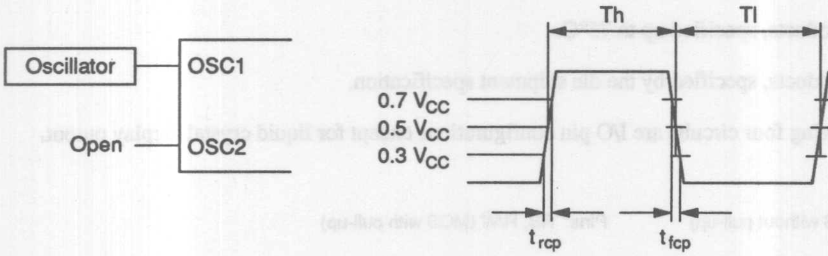
6. Applies to input pins and I/O pins, excluding the OSC_1 pin.
7. Applies to I/O pins.

8. Applies to output pins.

9. Current flowing through pull–up MOSs, excluding output drive MOSs.

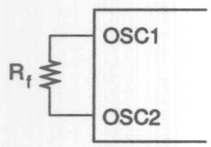
10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.

11. Applies only to external clock operation.

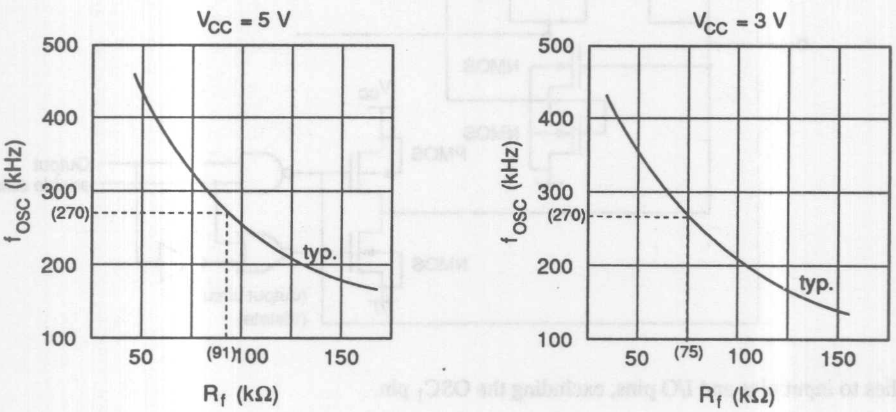


$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

12. Applies only to the internal oscillator operation using oscillation resistor R_f.



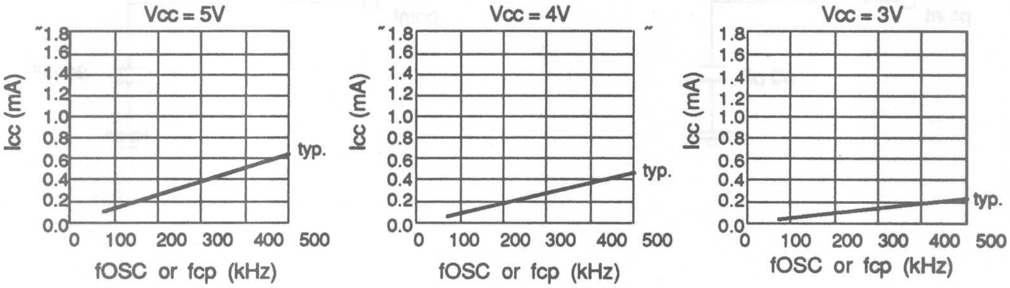
R_f: 75 kΩ ± 2% (when V_{CC} = 3 V to 4 V)
R_f: 91 kΩ ± 2% (when V_{CC} = 4 V to 5 V)
Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.



13. R_{COM} is the resistance between the power supply pins (V_{CC}, V1, V4, V5) and each common signal pin (COM1 to COM33).

    R_{SEG} is the resistance between the power supply pins (V_{CC}, V2, V3, V5) and each segment signal pin (SEG1 to SEG40).

14. The following graphs show the relationship between operation frequency and current consumption.



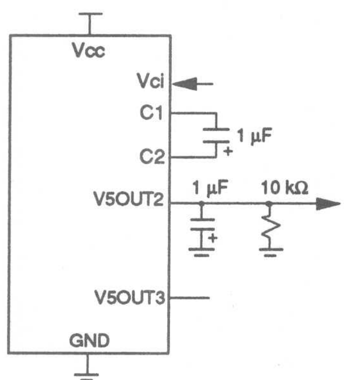
15. Applies to the OSC1 pin.

16. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (V_{CC}, V1, V2, V3, V4, V5) when there is no load.

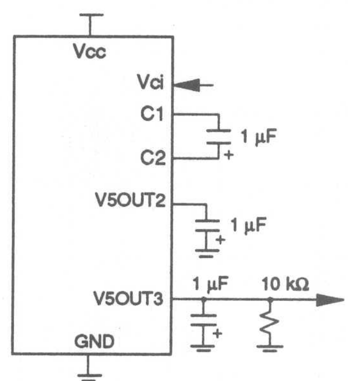
17. The TEST pin must be fixed to the ground, and the EXT or Vcc pin must also be connected to the ground.

18. Booster characteristics test circuits are shown below.

Boosting twice



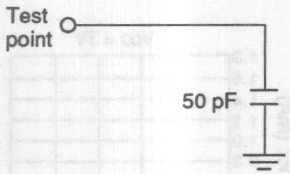
Boosting three times



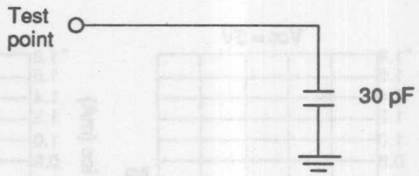
Load Circuits

AC Characteristics Test Load Circuits

Data bus: DB0–DB7



Segment extension signals: CL1, CL2, D, M



Timing Characteristics

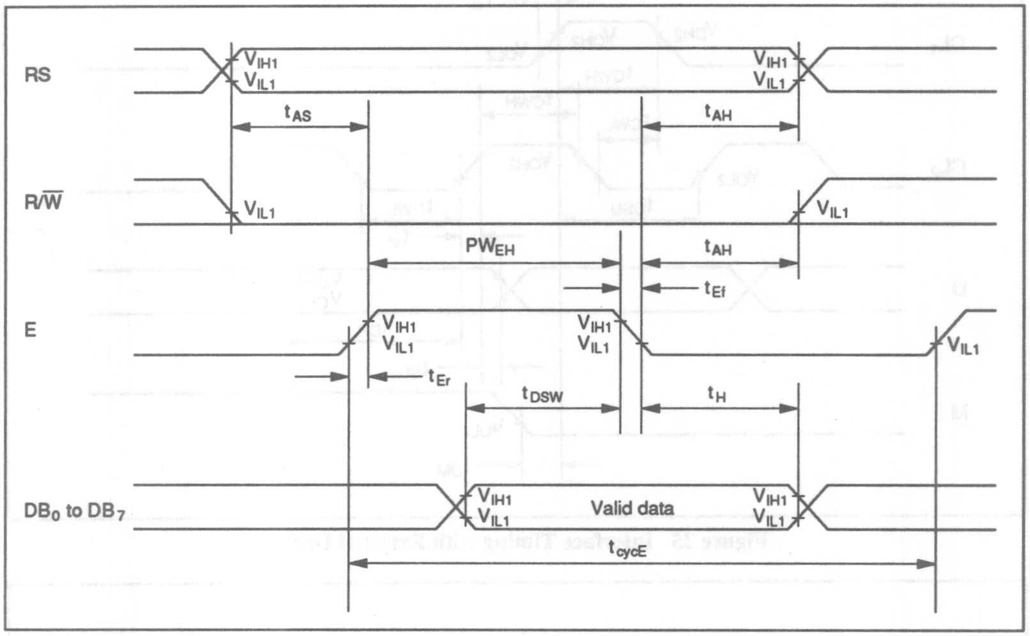


Figure 33 Write Operation

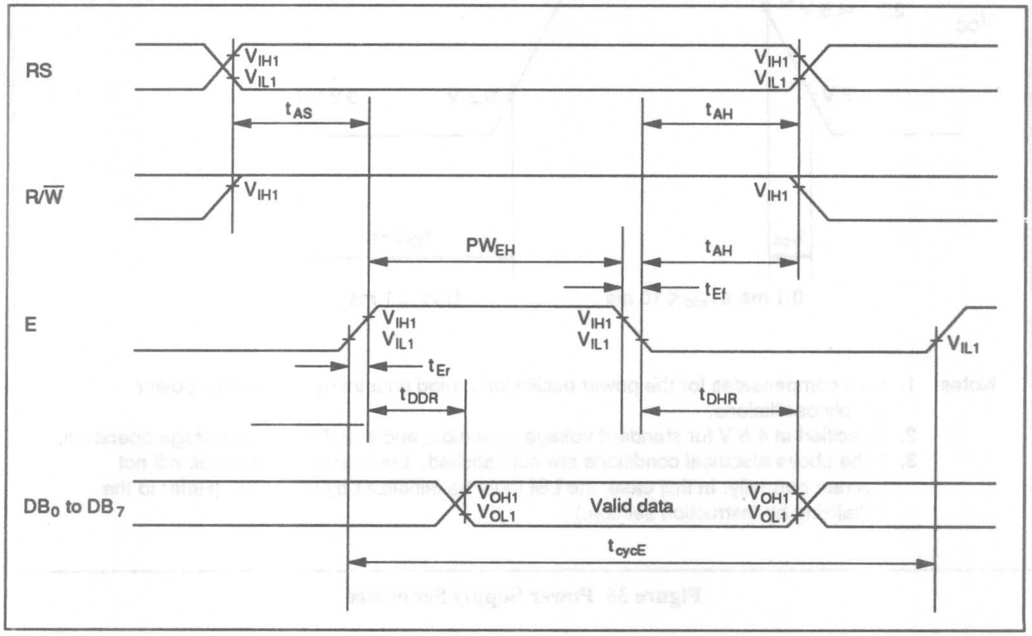


Figure 34 Read Operation

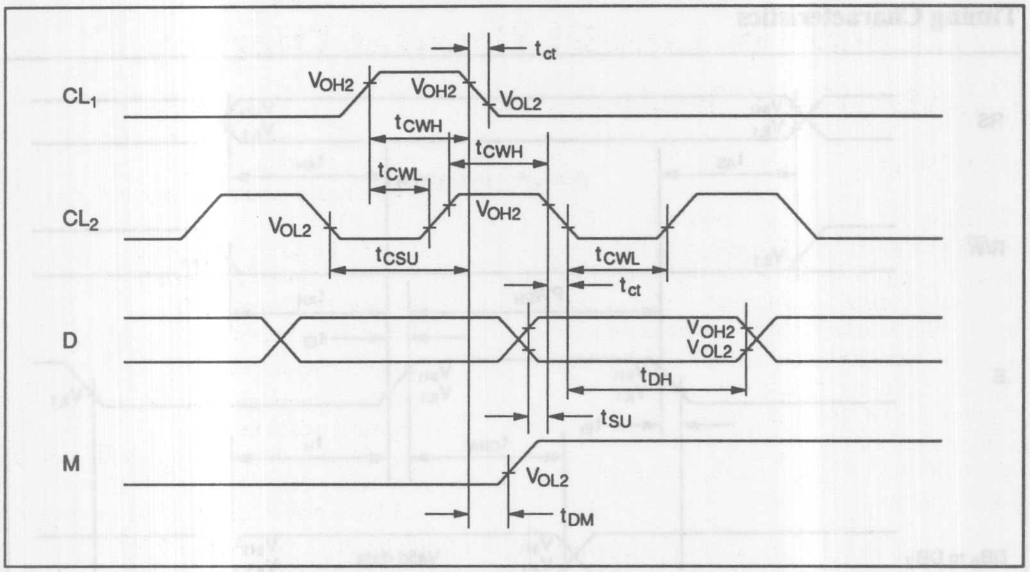
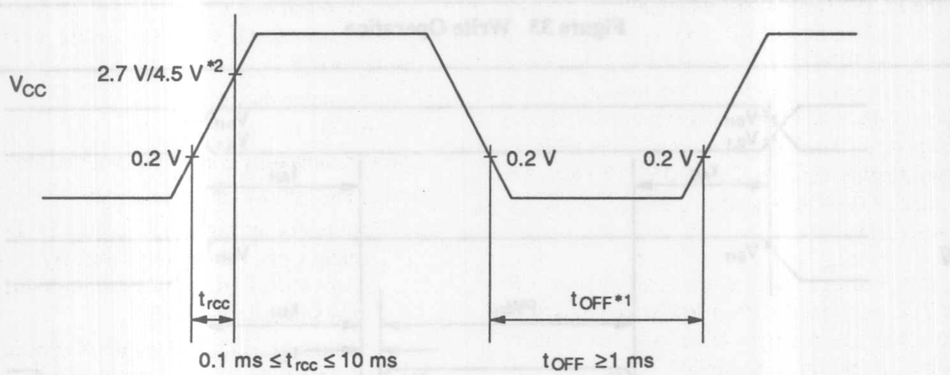


Figure 35 Interface Timing with External Driver



Notes: 1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for standard voltage operation, and at 2.7 V for low voltage operation.
3. If the above electrical conditions are not satisfied, the internal reset circuit will not operate normally. In this case, the LSI must be initialized by software. (Refer to the Initializing by Instruction section.)

Figure 36 Power Supply Sequemce

HD66712(LCD-II/F12)
(Dot Matrix Liquid Crystal Display Controller/Driver)

Description

The HD66712 dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, numbers, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a serial or a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimum system can be interfaced with this controller/driver.

A single HD66712 is capable of displaying a single 24-character line, two 24-character lines, or four 12-character lines.

The HD66712 software is upwardly compatible with the LCDII (HD44780) which allows the user to easily replace an LCD-II with an HD66712. In addition, the HD66712 is equipped with functions such as segment displays for icon marks, a 4-line display mode, and a horizontal smooth scroll, and thus supports various display forms. This achieves various display forms. The HD66712 character generator ROM is extended to generate 240 5 x 8 dot characters.

The low-voltage operation (2.7 V) of the HD66712, combined with a low-power mode, is suitable for any portable battery-driven product requiring low power consumption.

Features

- 5 × 8 dot matrix possible
- Clock-synchronized serial interface capability; can interface with 4- or 8-bit MPU
- Low-power operation support:
  - — 2.7 to 5.5 V (low voltage)
  - — Wide liquid-crystal voltage range: 3.0 to 13.0 V max.
- Booster for liquid crystal voltage
  - — Two/three times (13 V max.)
- High-speed MPU bus interface (2MHz at 5-V operation)
- Extension driver interface
- Character display and independent 60-icon mark display possible
- Horizontal smooth scroll by 6-dot font width display possible
- 80 × 8-bit display RAM (80 characters max.)
- 9,600-bit character generator ROM
  - — 240 characters (5 × 8 dot)
- 64 × 8-bit character generator RAM
  - — 8 characters (5 × 8 dot)
- 16 × 8-bit segment icon mark
  - — 96-segment icon mark
- 34-common × 60-segment liquid crystal display driver
- Programmable duty cycle (See list 1)
- Software upwardly compatible with HD44780.
- Wide range of instruction functions:
  - — Functions compatible with LCD-II: Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
  - — Additional functions: Icon mark control, 4-line display, horizontal smooth scroll, 6-dot character width control, white-black inverting blinking cursor.
- Automatic reset circuit that initializes the controller/driver after power on (standard version only)
- Internal oscillator with an external resistor

- Low power consumption
- QFP 1420-128 pin, TCP-128 pin, bare-chip.

List 1 Programmable duty cycles

5-dot font width

		Single-chip Operation		With Extension Driver	
Number of Lines	Duty Ratio	Displayed Characters	Icons	Displayed Characters	Icons
1	1/17	One 24-character line	60	One 52-character line	80
2	1/33	Two 24-character lines	60	Two 32-character lines	80
4	1/33	Four 24-character lines	60	Four 20-character lines	80

6-dot font width

		Single-chip Operation		With Extension Driver	
Number of Lines	Duty Ratio	Displayed Characters	Icons	Displayed Characters	Icons
1	1/17	One 20-character line	60	One 50-character line	96
2	1/33	Two 20-character lines	60	Two 30-character lines	96
4	1/33	Four 10-character lines	60	Four 20-character lines	96

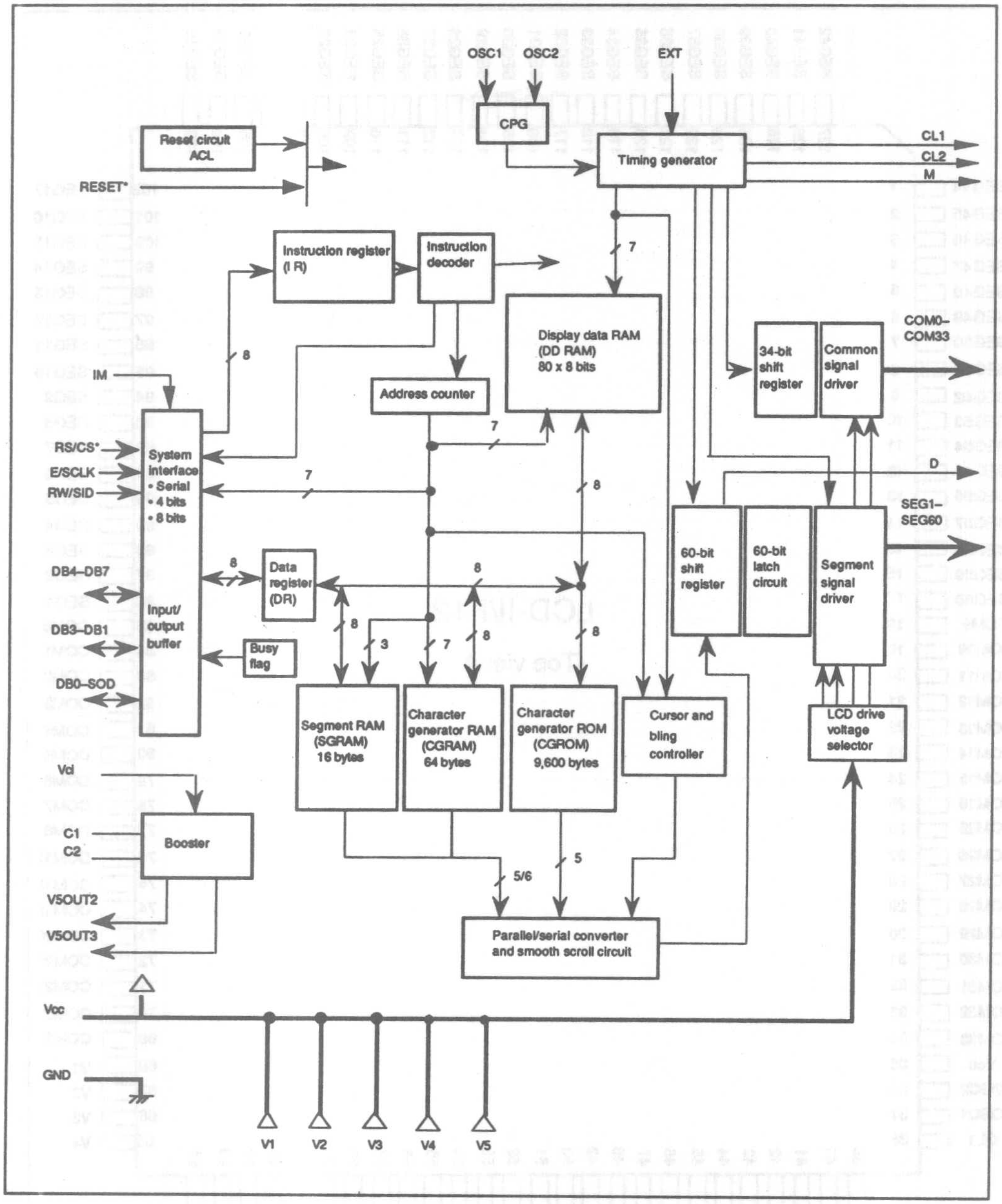
LCD-II Family Comparison

Item	LCD-II (HD44780U)	LCD-II/E20 (HD66702)	LCD-II/F8 (HD66710)	LCD-II/F12 HD66712
Power supply voltage	2.7 V to 5.5 V	5 V ±10 % (standard) 2.7 V to 5.5 V (low voltage)	2.7 V to 5.5 V	2.7 V to 5.5 V
Liquid crystal drive voltage	3.0 to 11 V	3.0 V to 7.0 V	3.0 to 13.0 V	3.0 to 13.0 V
Maximum display digits per chip	8 characters × 2 lines	20 characters × 2 lines	16 characters × 2 lines/ 8 characters x 4 lines	24 characters × 2 lines/ 12 characters x 4 lines
Segment display	None	None	40 segments	60 segments
Display duty cycle	1/8, 1/11, and 1/16	1/8, 1/11, and 1/16	1/17 and 1/33	1/17 and 1/33
CGROM	9,920 bits (208 5 × 8 dot characters and 32 5 × 10 dot characters)	7,200 bits (160 5 × 7 dot characters and 32 5 × 10 dot characters)	9,600 bits (240 5 × 8 dot characters)	9,600 bits (240 5 × 8 dot characters)
CGRAM	64 bytes	64 bytes	64 bytes	64 bytes
DDRAM	80 bytes	80 bytes	80 bytes	80 bytes
SEGRAM	None	None	8 bytes	16 bytes
Segment signals	40	100	40	60
Common signals	16	16	33	34
Liquid crystal drive waveform	A	B	B	B
Bleeder resistor for LCD power supply	External (adjustable)	External (adjustable)	External (adjustable)	External (adjustable)
Clock source	External resistor or external clock	External resistor or external clock	External resistor or external clock	External resistor or external clock
R_f oscillation frequency (frame frequency)	270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycle; 43 to 80 Hz for 1/11 duty cycle)	320 kHz ±30% (70 to 130 Hz for 1/8 and 1/16 duty cycle; 51 to 95 Hz for 1/11 duty cycle)	270 kHz ±30% (56 to 103 Hz for 1/17 duty cycle; 57 to 106 Hz for 1/33 duty cycle)	270 kHz ±30% (56 to 103 Hz for 1/17 duty cycle; 57 to 106 Hz for 1/33 duty cycle)
R_f resistance	91 kΩ: 5-V operation; 75 kΩ: 3-V operation	68 kΩ: 5-V operation 56 kΩ: (3-V operation)	91 kΩ: 5-V operation; 75 kΩ: 3-V operation	91 kΩ: 5-V operation; 75 kΩ: 3-V operation

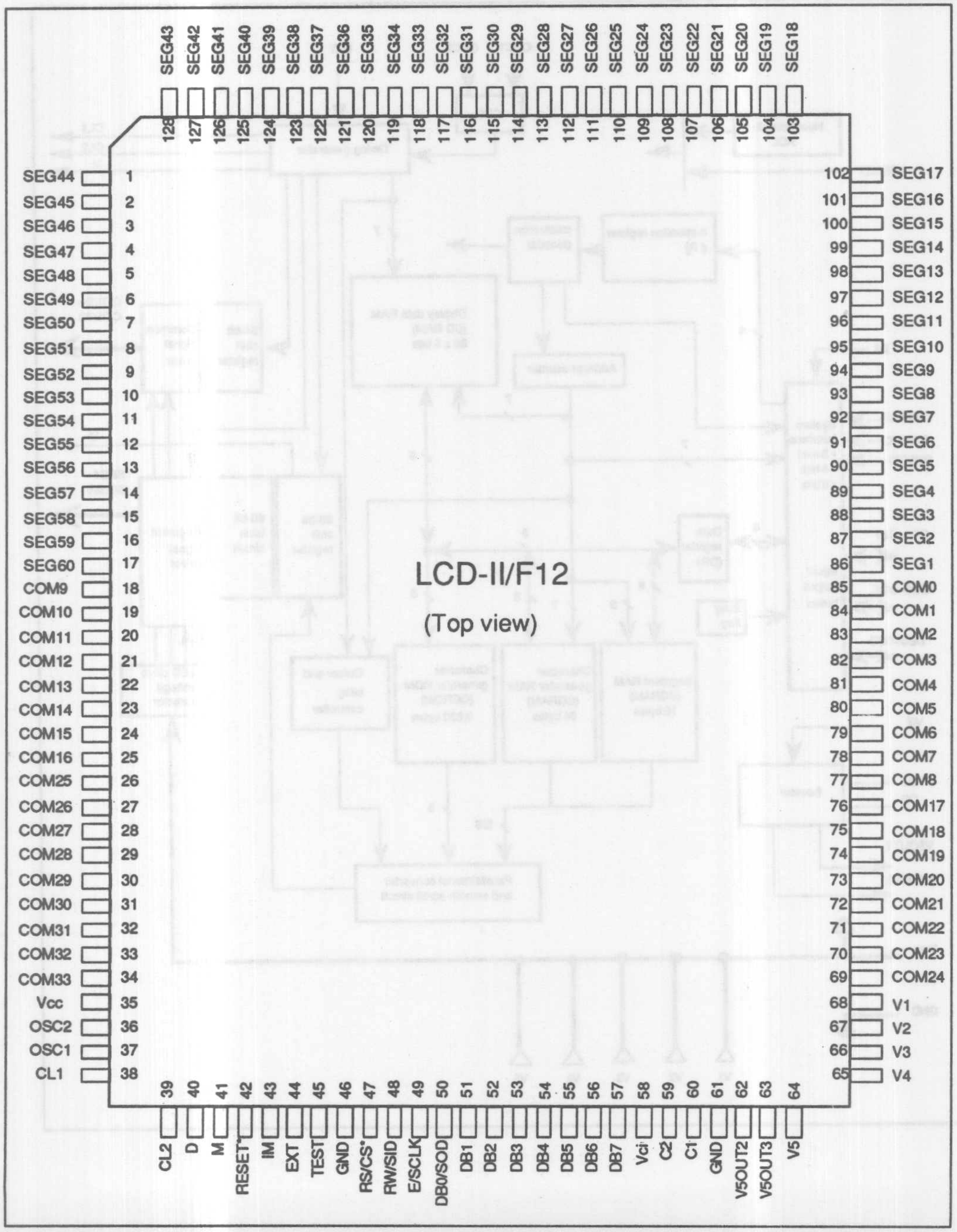
LCD-II Family Comparison (cont)

Item	LCD-II (HD44780U)	LCD-II/E20 (HD66702)	LCD-II/F8 (HD66710)	LCD-II/F12 HD66712
Liquid crystal voltage booster circuit	None	None	2-3 times step-up circuit	2-3 times step-up circuit
Extension driver control signal	Independent control signal	Independent control signal	Used in common with a driver output pin	Independent control signal
Reset function	Power on automatic reset	Power on automatic reset	Power on automatic reset	Power on automatic reset or Reset input
Instructions	LCD-II (HD44780)	Fully compatible with the LCD-II	Upper compatible with the LCD-II	Upper compatible with the LCD-II
Number of displayed lines	1 or 2	1 or 2	1, 2, or 4	1, 2, or 4
Low power mode	None	None	Available	Available
Horizontal scroll	Character unit	Character unit	Dot unit	Dot unit
Bus interface	4 bits/8 bits	4 bits/8 bits	4 bits/8 bits	Serial; 4 bits/8 bits
CPU bus timing	2 MHz: 5-V operation; 1 MHz: 3-V operation	1 MHz	2 MHz: 5-V operation; 1 MHz: 3-V operation	2 MHz: 5-V operation; 1 MHz: 3-V operation
Package	QFP-1420-80 80-pin bare chip	LQFP-2020–144 144-pin bare chip	QFP-1420-100 100-pin bare chip	QFP-1420-128 TCP-128 128-pin bare chip

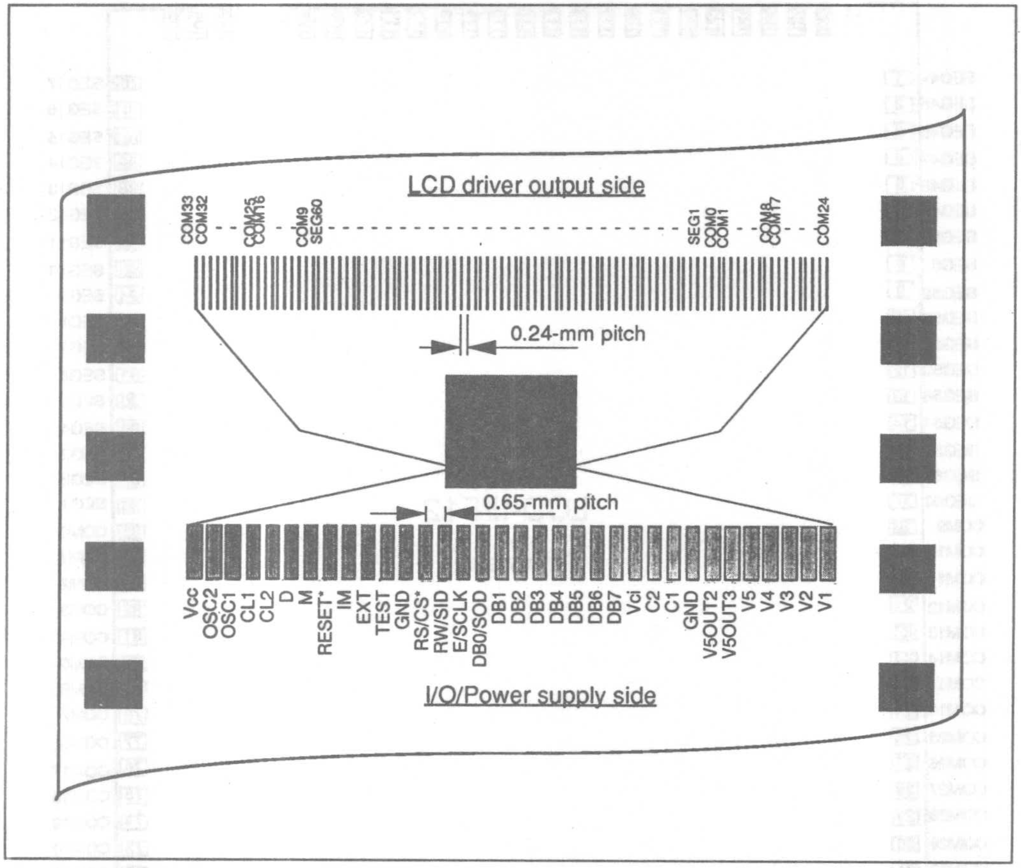
HD66712 Block Diagram



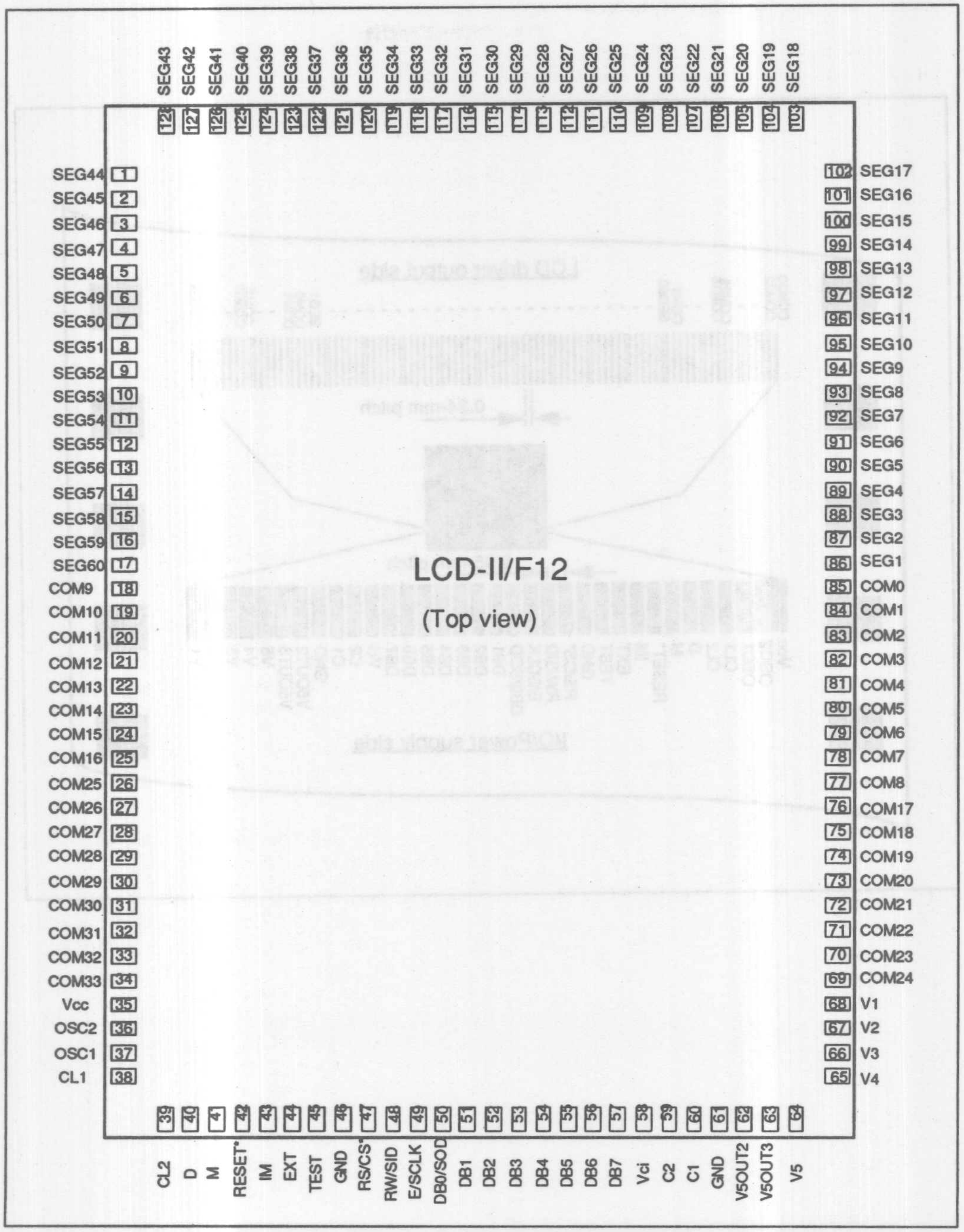
HD66712 Pin Arrangement



TCP Dimensions



HD66712 Pad Arrangement



Pin Functions

Table 1 Pin Functional Description

Signal	Number of pins	I/O	Device Interfaced with	Function
IM	1	I	—	Selects interface mode with the MPU; Low: Serial mode High: 4-bit/8-bit bus mode (Bus width is specified by instruction.)
RS/CS*	1	I	MPU	Selects registers during bus mode: Low: Instruction register (write); Busy flag, address counter (read) High: Data register (write/read) Acts as chip-select during serial mode: Low: Select (access enable) High: Not selected (access disable)
RW/SID	1	I	MPU	Selects read/write during bus mode; Low: Write High: Read Inputs serial data during serial mode.
E/SCLK	1	I	MPU	Starts data read/write during bus mode; Inputs (Receives) serial clock during serial mode.
DB_4 to DB_7	4	I/O	MPU	Four high-order bidirectional tristate data bus pins. Used for data transfer between the MPU and the HD66712. DB_7 can be used as a busy flag. Open these pins during serial mode since these signals are not used.
DB_1 to DB_3	3	I/O	MPU	Three low order bidirectional tristate data bus pins. Used for data transfer between the MPU and the HD66712. Open these pins during 4-bit operation or serial mode since they are not used.
DB0/ SOD	1	I/O /O	MPU	The lowest bidirectional data bit (DB0) during 8-bit bus mode. Open these pins during 4-bit mode since they are not used. Outputs (transfers) serial data during serial mode. Open this pin if reading (transfer) is not performed.
COM_0 to COM_{33}	34	O	LCD	Common signals; those that are not used become non-selected waveforms. At 1/17 duty rate, COM_1 to COM_{16} are used for character display, COM_0 and COM_{17} for icon display, and COM_{18} to COM_{33} become non-selected waveforms. At 1/33 duty rate, COM_1 to COM_{32} are used for character display, and COM_0 and COM_{33} for icon display. Because two COM signals output the same level simultaneously, apply them according to the wiring pattern of the display device.
SEG_1 to SEG_{60}	60	O	LCD	Segment output signals

Table 1 Pin Functional Description (cont)

Signal	Number of pins	I/O	Device Interfaced with	Function
CL1	1	O	Extension driver	When EXT = high, outputs the extension driver latch pulse.
CL2	1	O	Extension driver	When EXT = high, outputs the extension driver shift clock.
D	1	O	Extension driver	When EXT = high, outputs extension driver data; data from the 61st dot on is output.
M	1	O	Extension driver	When EXT = high, outputs the extension driver AC signal.
EXT	1	I	—	When EXT = high, outputs the extension driver control signal. When EXT = low, the signal becomes tristate and can suppress consumption current.
V_1 to V_5	5	—	Power supply	Power supply for LCD drive $V_{CC} - V_5$ = 13 V (max)
V_{CC}/GND	2	—	Power supply	V_{CC}: +5 V or +3 V, GND: 0 V
OSC_1/OSC_2	2	—	Oscillation resistor clock	When crystal oscillation is performed, an external resistor must be connected. When the pin input is an external clock, it must be input to OSC_1.
Vci	1	I	—	Inputs voltage to the booster to generate the liquid crystal display drive voltage. Vci: 2.5 V to 4.5 V
V_5OUT_2	1	O	V_5 pin/ Booster capacitance	Voltage input to the Vci pin is boosted twice and output. When the voltage is boosted three times, the same capacitance as that of C1–C2 should be connected here.
V_5OUT_3	1	O	V_5 pin	Voltage input to the Vci pin is boosted three times and output.
C1/C2	2	—	Booster capacitance	External capacitance should be connected here when using the booster.
RESET*	1	I	—	Reset pin. Initialized to "low".
TEST	1	I	—	Test pin. Should be wired to ground.

Function Description

System Interface

The HD66712 has three types of system interfaces: synchronized serial, 4-bit bus, and 8-bit bus. The serial interface is selected by the IM-pin, and the 4/8-bit bus interface is selected by the DL bit in the instruction register.

The HD66712 has two 8-bit registers: an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for the display data RAM (DD RAM), the character generator RAM (CG RAM), and the segment RAM (SEG RAM). The MPU can only write to IR, and cannot be read from.

The DR temporarily stores data to be written into DD RAM, CG RAM, or SEG RAM. Data written into the DR from the MPU is automatically written into DD RAM, CG RAM, or SEG RAM by an internal operation. The DR is also used for data storage when reading data from DD RAM, CG RAM, or SEG RAM. When address information is written into the IR, data is read and then stored into the DR from DD RAM, CG RAM or SEG RAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DD RAM, CG RAM, or SEG RAM at the next address is sent to the DR for the next read from the MPU.

These two registers can be selected by the registor selector (RS) signal in the 4/8 bit bus interface, and by the RS bit in start byte data in synchronized serial interface (table 2).

Busy Flag (BF)

When the busy flag is 1, the HD66712 is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/W = 1 (table 2), the busy flag is output from DB_7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to DD RAM, CG RAM, or SEG RAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of DD RAM, CG RAM, and SEG RAM is also determined concurrently by the instruction.

After writing into (reading from) DD RAM, CG RAM, or SEG RAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB_0 to DB_6 when RS = 0 and R/$\overline{W}$ = 1 (table 2).

Table 2 Resistor Selection

RS	R/$\overline{W}$	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0 to DB_6)
1	0	DR write as an internal operation (DR to DD RAM, CG RAM, or SEGRAM)
1	1	DR read as an internal operation (DD RAM, CG RAM, or SEGRAM to DR)

Display Data RAM (DD RAM)

Display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 x 8 bits, or 80 characters. The area in display data RAM (DD RAM) that is not used for display can be used as general data RAM.

The DD RAM address (ADD) is set in the address counter (AC) as a hexadecimal number, as shown in figure 1.

The relationship between DD RAM addresses and positions on the liquid crystal display is described and shown on the following pages for a variety of cases.

	MSB						LSB
AC	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Example: DD RAM address 4E

1	0	0	1	1	1	0

Figure 1 DD RAM Address

• 1-line display (N = 0, and NW = 0)

— Case 1: When there are fewer than 80 display characters, the display begins at the beginning of DD RAM. For example, when 24 5-dot font-width characters are displayed using one HD66712, the display is generated as shown in figure 2.

When a display shift is performed, the DD RAM addresses shift as well as shown in the figure.

When 20 6-dot font-width characters are displayed using one HD66712, the display is generated as shown in figure 3. Note that COM9 to COM16 begins at address (0A)H in this case.20 characters are displayed.

When a display shift is performed, the DD RAM addresses shift as well as shown in the figure.

— Case 2: Figure 4 shows the case where the EXT pin is fixed high and the HD66712 and the 40-output extension driver are used to display 24 6-dot font-width characters. In this case, COM9 to COM16 begins at (0A)H.

When a display shift is performed, the DD RAM addresses shift as wellas shown in the figure.

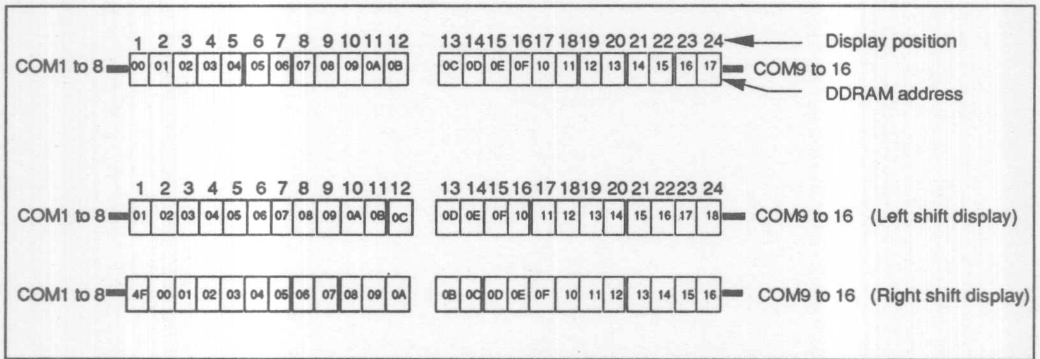


Figure 2 1-line by 24-Character Display (5-dot font width)

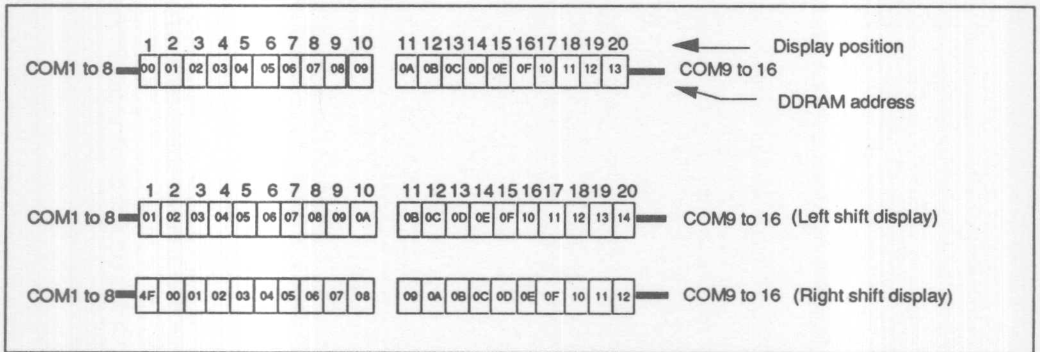


Figure 3 1-line by 20-Character Display (6-dot font width)

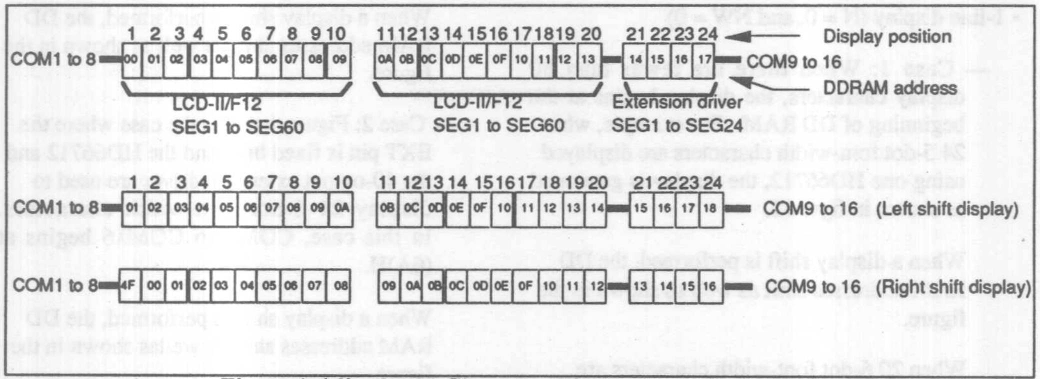


Figure 4 1-line by 24-Character Display (6-dot font width)

- 2-line display (N = 1, and NW = 0)

— Case 1: The first line is displayed from COM1 to COM16, and the second line is displayed from COM17 to COM32. Note that the last address of the first line and the first address of the second line are not consecutive. Figure 5 shows an example where a 5-dot font-width 24 x 2-line display is performed using one HD66712. Here, COM9 to COM16 begins at (0C)H, and COM25 to COM32 at (4C)H. When a display shift is performed, the DD RAM addresses shift as shown. Figure 6 shows an example where a 6-dot font-width 20 x 2-line display is performed using one HD66712. COM9 to COM16 begins at (0A)H, and COM25 to COM32 at (4A)H.

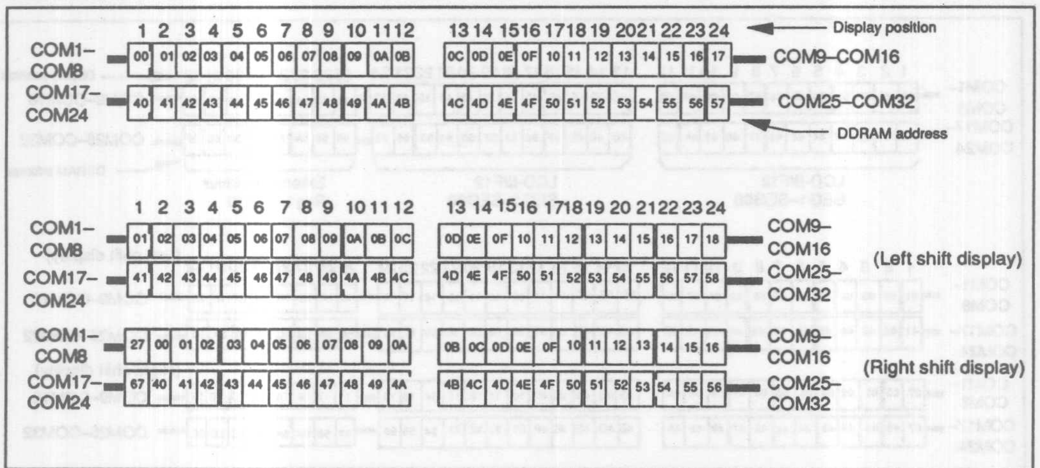


Figure 5 2-line by 24-Character Display (5-dot font width)

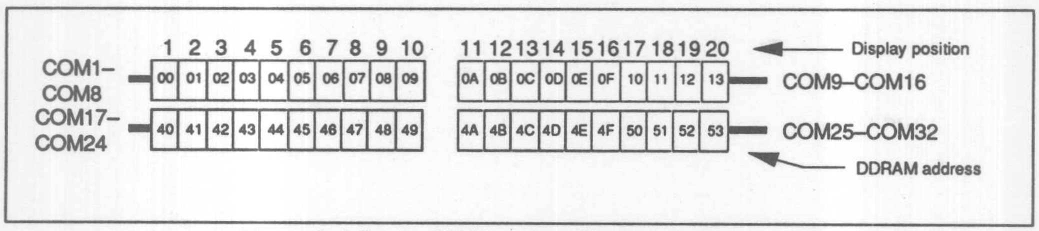


Figure 6 2-line by 20-Character Display (6-dot font width)

— Case 2: Figure 7 shows the case where the EXT pin is fixed high and the HD66712 and the 40-output extension driver are used to extend the number of display characters to 32 5-dot font-width characters.

In this case, COM9 to COM16 begins at (0C)H, and COM25 to COM32 at (4C)H.

When a display shift is performed, the DD RAM addresses shift as shown.

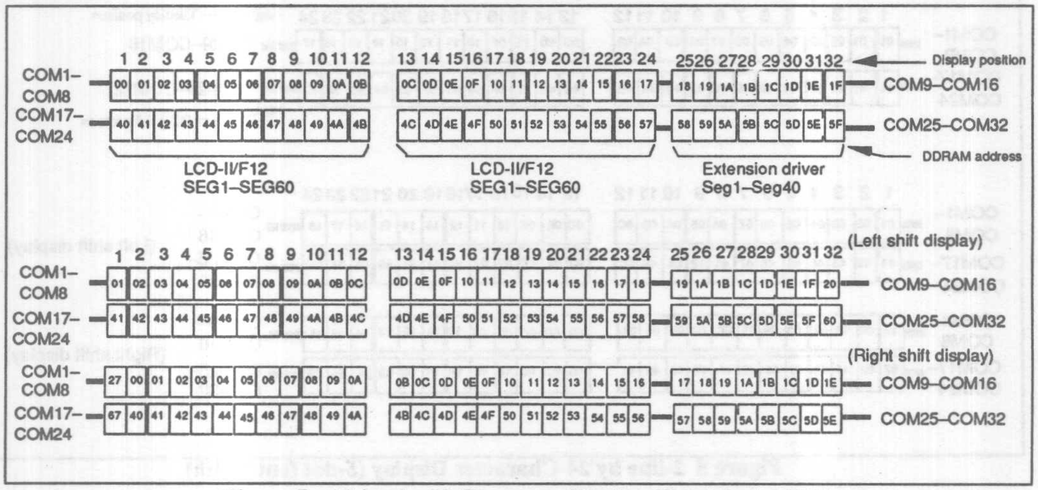


Figure 7 2-Line by 32 Character Display (5-dot font width)

• 4-line display (NW = 1)

— Case 1: The first line is displayed from COM1 to COM8, the second line is displayed from COM9 to COM16, the third line is displayed from COM17 to COM24, and the fourth line is displayed from COM25 to COM32.
Note that the DD RAM addresses of each line are not consecutive.
Figure 8 shows an example where a 12 x 4-line display is performed using one HD66712.

When a display shift is performed, the DD RAM addresses shift as shown.

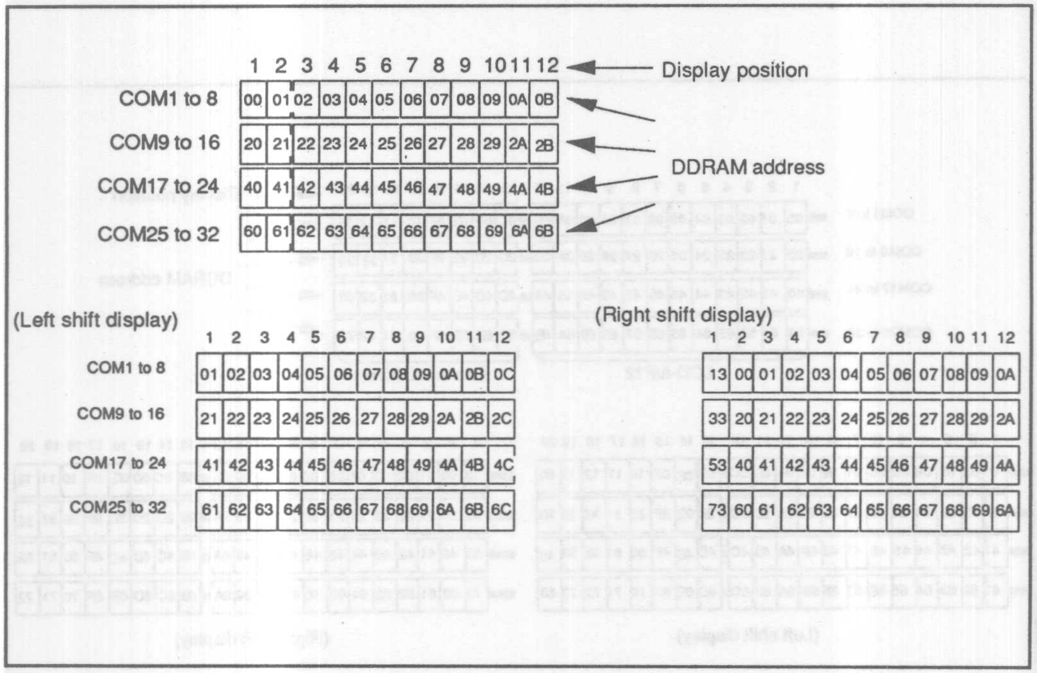


Figure 8 4-Line Display

— Case 2: Figure 9 shows the case where the EXT pin is fixed high and the HD66712 and the 40-output extension driver are used to extend the number of display characters.

When a display shift is performed, the DD RAM addresses shift as shown.

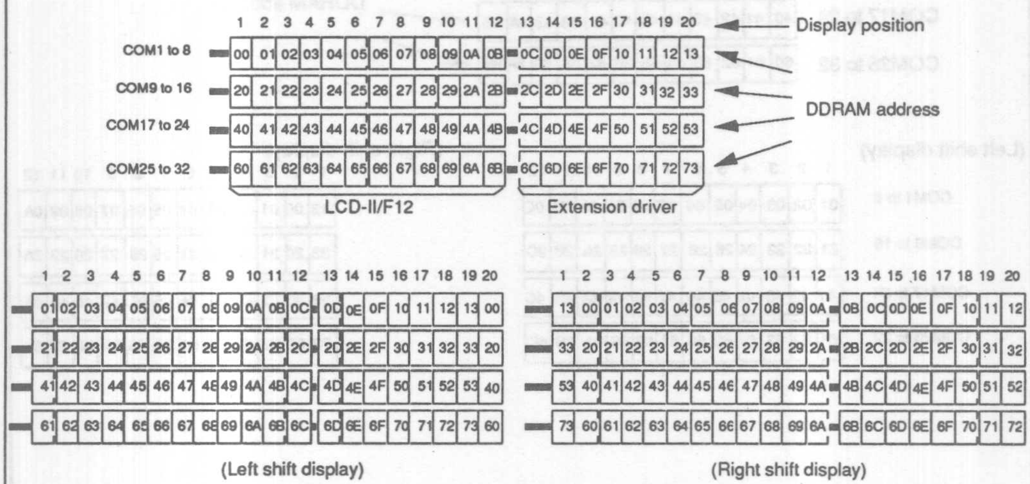


Figure 9 4-Line by 20-Character Display

Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 8 dot character patterns from 8-bit character codes (table 3). It can generate 240 5 × 8 dot character patterns. User-defined character patterns are also available using a mask-programmed ROM (see "Modifying Character Patterns").

Character Generator RAM (CG RAM)

The character generator RAM allows the user to redefine the character patterns. In the case of 5 × 8 dot character, up to eight character patterns may be redefined.

Write the character codes at the addresses shown as the left column of table 3 to show the character patterns stored in CG RAM.

See table 4 for the relationship between CG RAM addresses and data and display patterns.

Segment RAM (SEGRAM)

The segment RAM (SEGRAM) is used to enable control of segments such as an icon and a mark by the user program.
For a 1-line display, SEGRAM is read from the COM0 and the COM17 output, and for 2- or 4-line displays, it is read from the COM0 and the COM33 output, to perform 60-segment display (80-segment display when using the extension driver).
As shown in table 7, bits in SEGRAM corresponding to segments to be displayed are directly set by the MPU, regardless of the contents of DDRAM and CGRAM.

SEGRAM data is stored in eight bits. The lower six bits control the display of each segment, and the upper two bits control segment blinking.

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM, CGRAM, and SEGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DD RAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 34 common signal drivers and 60 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

Character pattern data is sent serially through a 60-bit shift register and latched when all needed data has arrived. The latched data then enables the driver to generate drive waveform outputs.

Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD66712 drives from the head display.

Cursor/Blink Control Circuit

The cursor/blink (or white-black inversion) control is used to produce a cursor or a flashing area on the display at a position corresponding to the location in stored in the address counter (AC).

For example (figure 11), when the address counter is (08)H, a cursor is displayed at a position corresponding to DDRAM address (08)H.

Scroll Control Circuit

The scroll control circuit is used to perform a smooth-scroll in the unit of dot. When the number of characters to be displayed is greater than that possible at one time on the liquid crystal module, this horizontal smooth scroll can be used to display all characters.

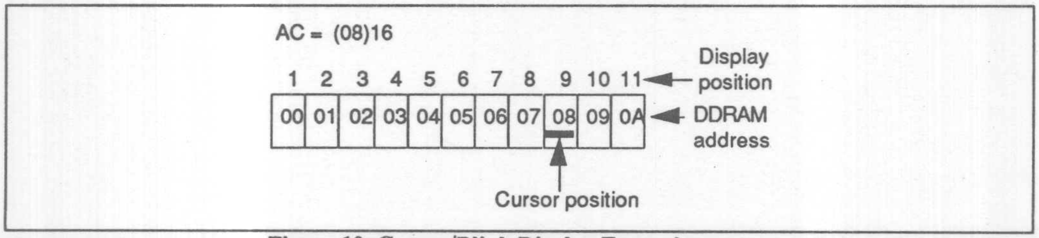


Figure 10 Cursor/Blink Display Example

Table 3 Relationship between Character Codes and Character Patterns (ROM code: A00)

Lower Bits \ Upper Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)			0	@	P	`	p				ー	タ	ミ	α	p
xxxx0001	CG RAM (2)		!	1	A	Q	a	q			。	ア	チ	ム	ä	q
xxxx0010	CG RAM (3)		"	2	B	R	b	r			「	イ	ツ	メ	β	θ
xxxx0011	CG RAM (4)		#	3	C	S	c	s			」	ウ	テ	モ	ε	∞
xxxx0100	CG RAM (5)		$	4	D	T	d	t			、	エ	ト	ヤ	μ	Ω
xxxx0101	CG RAM (6)		%	5	E	U	e	u			・	オ	ナ	ユ	σ	ü
xxxx0110	CG RAM (7)		&	6	F	V	f	v			ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	CG RAM (8)		'	7	G	W	g	w			ァ	キ	ヌ	ラ	g	π
xxxx1000	CG RAM (1)		(	8	H	X	h	x			ィ	ク	ネ	リ	√	x̄
xxxx1001	CG RAM (2)		)	9	I	Y	i	y			ゥ	ケ	ノ	ル	⁻¹	y
xxxx1010	CG RAM (3)		*	:	J	Z	j	z			ェ	コ	ハ	レ	j	千
xxxx1011	CG RAM (4)		+	;	K	[	k	{			ォ	サ	ヒ	ロ	×	万
xxxx1100	CG RAM (5)		,	<	L	¥	l	|			ャ	シ	フ	ワ	¢	円
xxxx1101	CG RAM (6)		-	=	M	]	m	}			ュ	ス	ヘ	ン	£	÷
xxxx1110	CG RAM (7)		.	>	N	^	n	→			ョ	セ	ホ	゛	ñ	
xxxx1111	CG RAM (8)		/	?	O	_	o	←			ッ	ソ	マ	゜	ö	█

Table 4 Relationship between Character Codes and Character Pattern (ROM code: A01)

Table 5 Relationship between Character Codes and Character Patterns (ROM code: A02)

Note: The character codes of the characters enclosed in the bold frame are the same as those of the first edition of the ISO8859 and the character code compatible.

Table 6 Example of Relationships between Character Code (DDRAM) and Character Pattern (CGRAM data)

a) When character pattern is 5 x 8 dots

Character code (DDRAM data)								CGRAM address						MSB CGRAM data LSB								
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	O7	O6	O5	O4	O3	O2	O1	O0	
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	*	1	0	0	0	1	Character pattern (1)
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				0	1	0	1	0	
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	0	1	0	0	
											1	1	1				0	0	0	0	0	
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	*	1	0	0	0	1	Character pattern (8)
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				0	1	0	1	0	
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	0	1	0	0	
											1	1	1				0	0	0	0	0	

b) When character pattern is 6 x 8 dots

Character code (DDRAM data)								CGRAM address						MSB CGRAM data LSB								
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	O7	O6	O5	O4	O3	O2	O1	O0	
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	0	1	0	0	0	1	Character pattern (1)
											0	0	1			0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
											0	1	1			0	0	1	0	1	0	
											1	0	0			0	0	0	1	0	0	
											1	0	1			0	0	0	1	0	0	
											1	1	0			0	0	0	1	0	0	
											1	1	1			0	0	0	0	0	0	
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	0	1	0	0	0	1	Character pattern (8)
											0	0	1			0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
											0	1	1			0	0	1	0	1	0	
											1	0	0			0	0	0	1	0	0	
											1	0	1			0	0	0	1	0	0	
											1	1	0			0	0	0	1	0	0	
											1	1	1			0	0	0	0	0	0	

Notes: 1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position (3 bits: 8 lines). The 8th line is the cursor position and its display is formed by a logical OR with the cursor.
3. The character data is stored with the rightmost character element in bit 0, as shown in the figure above. Characters with 5 dots in width (FW = 0) are stored in bits 0 to 4, and characters with 6 dots in width (FW = 1) are stored in bits 0 to 5.
4. When the upper four bits (bits 7 to 4) of the character code are 0, CGRAM is selected. Bit 3 of the character code is invalid (*). Therefore, for example, the character codes (00)H and (08)H correspond to the same CGRAM address.
5. A set bit in the CGRAM data corresponds to display selection, and 0 to non-selection.
6. When the BE bit of the function set register is 1, pattern blinking control of the lower six bits is controlled using the upper two bits (bits 7 and 6) in CGRAM.
When bit 7 is 1, of the lower six bits, only those which are set are blinked on the display.
When bit 6 is 1, a bit 4 pattern can be blinked as for a 5-dot font width, and a bit 5 pattern can be blinked as for a 6-dot font width.

* Indicates no effect.

Table 7 Relationship between SEGRAM addresses and display patterns

SEGRAM address				SEGRAM data															
				a) 5-dot font width								b) 6-dot font width							
A0	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	B1	B0	*	S1	S2	S3	S4	S5	B1	B0	S1	S2	S3	S4	S5	S6
0	0	0	1	B1	B0	*	S6	S7	S8	S9	S10	B1	B0	S7	S8	S9	S10	S11	S12
0	0	1	0	B1	B0	*	S11	S12	S13	S14	S15	B1	B0	S13	S14	S15	S16	S17	S18
0	0	1	1	B1	B0	*	S16	S17	S18	S19	S20	B1	B0	S19	S20	S21	S22	S23	S24
0	1	0	0	B1	B0	*	S21	S22	S23	S24	S25	B1	B0	S25	S26	S27	S28	S29	S30
0	1	0	1	B1	B0	*	S26	S27	S28	S29	S30	B1	B0	S31	S32	S33	S34	S35	S36
0	1	1	0	B1	B0	*	S31	S32	S33	S34	S35	B1	B0	S37	S38	S39	S40	S41	S42
0	1	1	1	B1	B0	*	S36	S37	S38	S39	S40	B1	B0	S43	S44	S45	S46	S47	S48
1	0	0	0	B1	B0	*	S41	S42	S43	S44	S45	B1	B0	S49	S50	S51	S52	S53	S54
1	0	0	1	B1	B0	*	S46	S47	S48	S49	S50	B1	B0	S55	S56	S57	S58	S59	S60
1	0	1	0	B1	B0	*	S51	S52	S53	S54	S55	B1	B0	S61	S62	S63	S64	S65	S66
1	0	1	1	B1	B0	*	S56	S57	S58	S59	S60	B1	B0	S67	S68	S69	S70	S71	S72
1	1	0	0	B1	B0	*	S61	S62	S63	S64	S65	B1	B0	S73	S74	S75	S76	S77	S78
1	1	0	1	B1	B0	*	S66	S67	S68	S69	S70	B1	B0	S79	S80	S81	S82	S83	S84
1	1	1	0	B1	B0	*	S71	S72	S73	S74	S75	B1	B0	S85	S86	S87	S88	S89	S90
1	1	1	1	B1	B0	*	S76	S77	S78	S79	S80	B1	B0	S91	S92	S93	S94	S95	S96
				Blinking control			Pattern on/off					Blinking control		Pattern on/off					

Notes: 1. Data set to SEGRAM is output when COM0 and COM17 are selected, as for a 1-line display, and output when COM0 and COM33 are selected, as for a 2-line or a 4-line display. COM0 and COM17 for a 1-line display and COM0 and COM33 for a 2-line or a 4-line display are the same signals.

2. S1 to S96 are pin numbers of the segment output driver. S1 is positioned to the left of the display. When the LCD-II/F12 is used by one chip, segments from S1 to S60 are displayed. An extension driver displays the segments after S61.
3. After S80 output at 5-dot font and S96 output at 6-dot font, S1 output is repeated again.
4. As for a 5-dot font width, lower five bits (D4 to D0) are display on.off information of each segment. For a 6-dot character width, the lower six bits (D5 to D0) are the display information for each segment.
5. When the BE bit of the function set register is 1, pattern blinking of the lower six bits is controlled using the upper two bits (bits 7 and 6) in SEGRAM.
   When bit 7 is 1, only a bit set to "1" of the lower six bits is blinked on the display.
   When bit 6 is 1, only a bit 4 pattern can be blinked as for a 5-dot font width, and only a bit 5 pattern can be blinked as for 6-dot font width.
6. Bit 5 (D5) is invalid for a 5-dot font width.
7. Set bits in the SEGRAM data correspond to display selection, and zeros to non-selection.

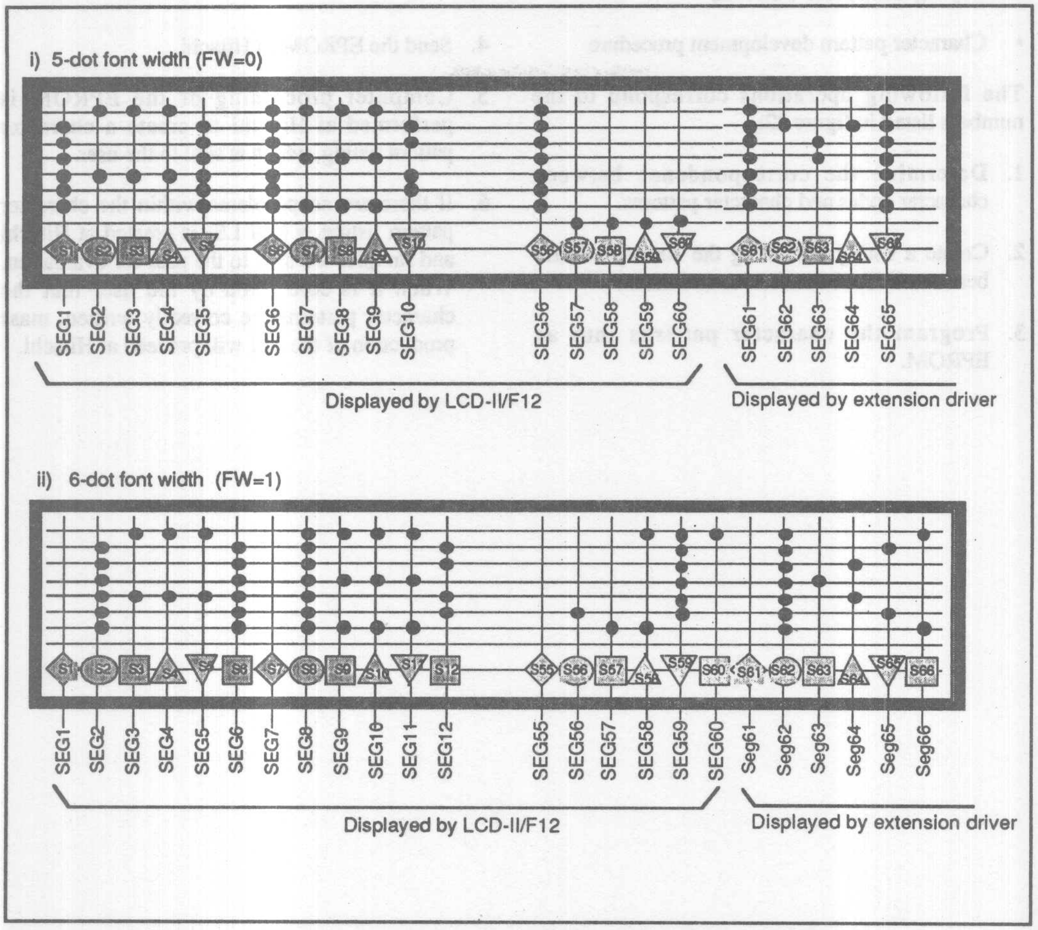


Figure 11 Correspondence between SEGRAM and segment display

Modifying Character Patterns

- Character pattern development procedure

The following operations correspond to the numbers listed in figure 12:

1. Determine the correspondence between character codes and character patterns.

2. Create a listing indicating the correspondence between EPROM addresses and data.

3. Program the character patterns into an EPROM.

4. Send the EPROM to Hitachi.

5. Computer processing of the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.

6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI will proceed at Hitachi.

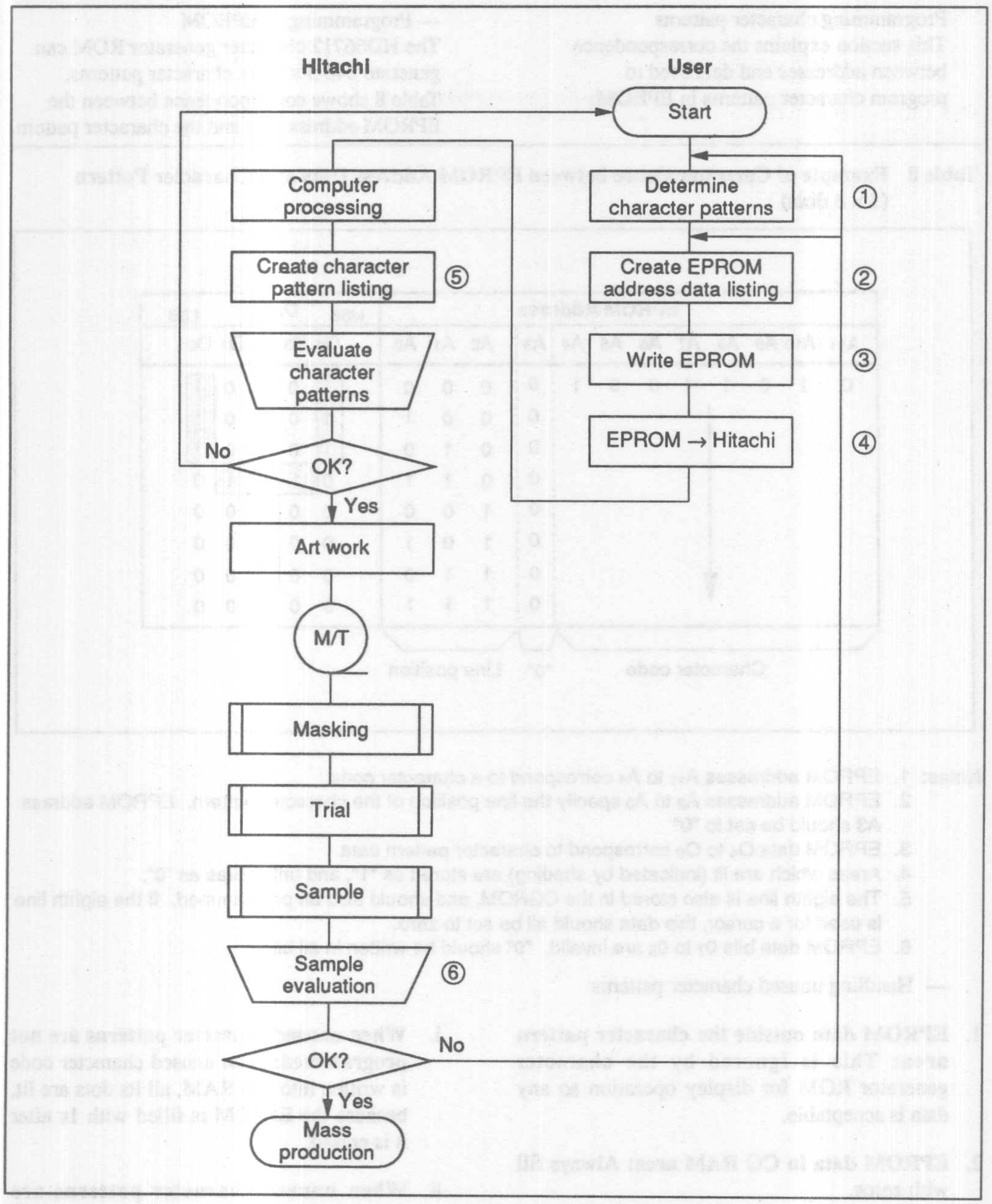


Figure 12 Character Pattern Development Procedure

Programming character patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM.

— Programming to EPROM

The HD66712 character generator ROM can generate 240 5 × 8 dot character patterns. Table 8 shows correspondence between the EPROM address data and the character pattern.

Table 8 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 8 dots)

EPROM Address												Data				
												MSB				LSB
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0
0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
								0	0	0	1	1	0	0	0	1
								0	0	1	0	1	0	0	0	1
								0	0	1	1	0	1	0	1	0
								0	1	0	0	0	0	1	0	0
								0	1	0	1	0	0	1	0	0
								0	1	1	0	0	0	1	0	0
								0	1	1	1	0	0	0	0	0
Character code								"0"	Line position							

Notes: 1. EPROM addresses A_{11} to A_4 correspond to a character code.

2. EPROM addresses A_2 to A_0 specify the line position of the character pattern. EPROM address A3 should be set to "0"
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. Areas which are lit (indicated by shading) are stored as "1", and unlit areas as "0".
5. The eighth line is also stored in the CGROM, and should also be programmed. If the eighth line is used for a cursor, this data should all be set to zero.
6. EPROM data bits O_7 to O_5 are invalid. "0" should be written in all bits.

— Handling unused character patterns

1. **EPROM data outside the character pattern area:** This is ignored by the character generator ROM for display operation so any data is acceptable.

2. **EPROM data in CG RAM area:** Always fill with zeros.

3. **Treatment of unused user patterns in the HD66712 EPROM:** According to the user application, these are handled in either of two ways:

i. **When unused character patterns are not programmed:** If an unused character code is written into DD RAM, all its dots are lit, because the EPROM is filled with 1s after it is erased.

ii. **When unused character patterns are programmed as 0s:** Nothing is displayed even if unused character codes are written into DD RAM. (This is equivalent to a space.)

Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD66712 when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 15 ms after V_{CC} rises to 4.5 V or 40 ms after the Vcc rises to 2.7 V.

1. Display clear:
   (20)H to all DDRAM
2. Set functions:
   DL = 1: 8-bit interface data
   N = 1: 2-line display
   RE = 0: Extension register write disable
   BE = 0: CGRAM/SEGRAM blink off
   LP = 0: Not in low power mode
3. Control display on/off:
   D = 0: Display off
   C = 0: Cursor off
   B = 0: Blinking off
4. Eet entry mode:
   I/D = 1: Increment by 1
   S = 0: No shift
5. Set extension function
   FW = 0: 5-dot character width
   B/W = 0: Normal cursor (eighth line)
   NW = 0: 1- or 2-line display (depending on N)
6. Enable scroll
   HSE = 0000: Scroll unable
7. Set scroll amount
   HDS = 000000: Not scroll

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD66712.

Initializing by Hardware Reset Input

The LCD-II/F12 also has a reset input pin: RESET*. If this pin is made low during operation, an internal reset and initialization is performed. This pin is ignored, however, during the internal reset period at power-on.

Interfacing to the MPU

The HD66712 can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB_4 to DB_7) are used for transfer. Bus lines DB_0 to DB_3 are disabled. The data transfer between the HD66712 and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB_4 to DB_7) are transferred before the four low order bits (for 8-bit operation, DB_0 to DB_3).

  The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

- For 8-bit interface data, all eight bus lines (DB_0 to DB_7) are used.

- When the IM pin is low, the HD66712 uses a serial interface. See "Transferring Serial Data".

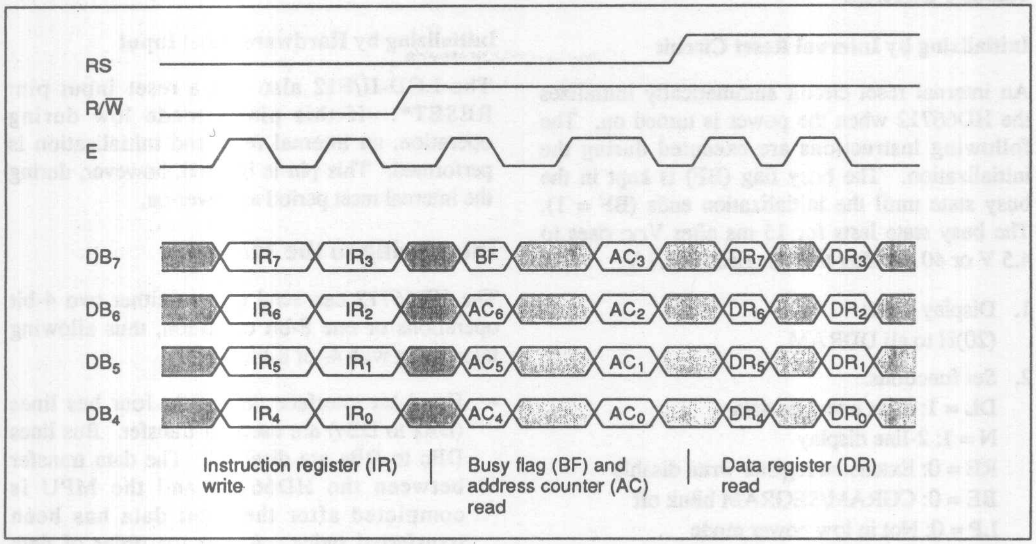


Figure 13 4-Bit Transfer Example

Transferring Serial Data

When the IM pin (interface mode) is low, the HD66712 enters serial interface mode. A three-line clock-synchronous transfer method is used. The HD66712 receives serial input data (SID) and transmits serial output data (SOD) by synchronizing with a transfer clock (SCLK) sent from the master side.

When the HD66712 interfaces with several chips, chip select pin (CS*) must be used. The transfer clock (SCLK) input is activated by making chip select (CS*) low. In addition, the transfer counter of the LCD-II/F12 can be reset and serial transfer synchronized by making chip select (CS*) high. Here, since the data which was being sent at reset is cleared, restart the transfer from the first bit of this data. In the case of a minimum 1 to 1 transfer system with the LCD-II/F12 used as a receiver only, an interface can be established by the transfer clock (SCLK) and serial input data (SID). In this case, chip select (CS*) should be fixed to low.

The transfer clock (SCLK) is independent from operational clock (CLK) of the LCD-II/F12. However, when several instructions are continuously transferred, the instruction execution time determined by the operational clock (CLK) (see continuous transfer) must be considered since the LCD-II/F12 does not have an internal transmit/receive buffer.

To begin with, transfer the start byte. By receiving five consecutive bits (synchronizing bit string) at the beginning of the start byte, the transfer counter of the LCD-II/F12 is reset and serial transfer is synchronized. The 2 bits following the synchronizing bit string (5 bits) specify transfer direction ($R/\overline{W}$ bit) and register select (RS bit). Be sure to transfer 0 in the 8th bit.

After receiving the start byte, instructions are received and the data/busy flag is transmitted. When the transfer direction and register select remain the same, data can be continuously transmitted or received.

The transfer protocol is described in detail below.

— Receiving (write)

After receiving the start synchronization bits, the $R/\overline{W}$ bit (= 0), and the RS bit with the start byte, an 8-bit instruction is received in 2 bytes: the lower 4 bits of the instruction are placed in the LSB of the first byte, and the higher 4 bits of the instruction are placed in the LSB of the second byte. Be sure to transfer 0 in the following 4 bits of each byte. When instructions are continuously received with $R/\overline{W}$ bit and RS bit unchanged, continuous transfer is possible (see "Continuous Transfer" below).

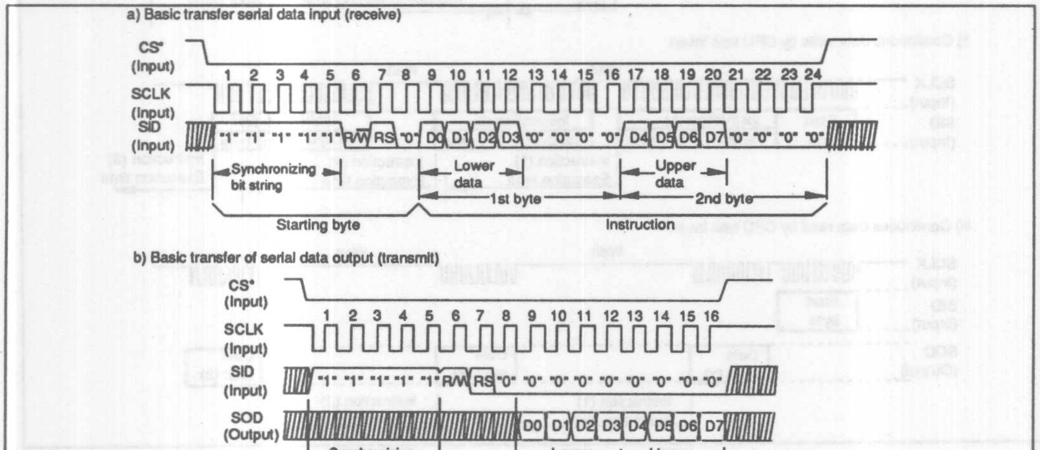


Figure 14 Basic Procedure for Transferring Serial Data

— Transmitting (read)

After receiving the start synchronization bits, the R/$\overline{W}$ bit (= 1), and the RS bit with the start byte, 8-bit read data is transmitted in the same way as receiving. When read data is continuously transmitted with R/$\overline{W}$ bit and RS bit unchanged, continuous transfer is possible (see "Continuous Transfer" below).
Even at the time of the transmission (the data output), since the HD66712 monitors the start synchronization bit string ("11111") by the SID input, the HD66712 receives the R/W bit and RS bit after detecting the start synchronization. Therefore, in the case of a continuous transfer, fix the SID input "0".

— Continuous transfer

When instructions are continuously received with the R/$\overline{W}$ bit and RS bit unchanged, continuous receive is possible without inserting a start byte between instructions.
After receiving the last bit (the 8th bit in the 2nd byte) of an instruction, the system begins to execute it.

To execute the next instruction, the instruction execution time of the LCD-II/F12 must be considered. If the last bit (the 8th bit in the 2nd byte) of the next instruction is received during execution of the previous instruction, the instruction will be ignored.
In addition, if the next unit of data is read before read execution of previous data is completed for busy flag/address counter/RAM data, normal data is not sent. To transfer data normally, the busy flag must be checked. However, it is possible to transfer without reading the busy flag if wiring for transmission (SOD pin) needs to be reduced or if the burden of polling on the CPU needs to be removed. In this case, insert a transfer wait so that the current instruction first completes execution during instruction transfer.

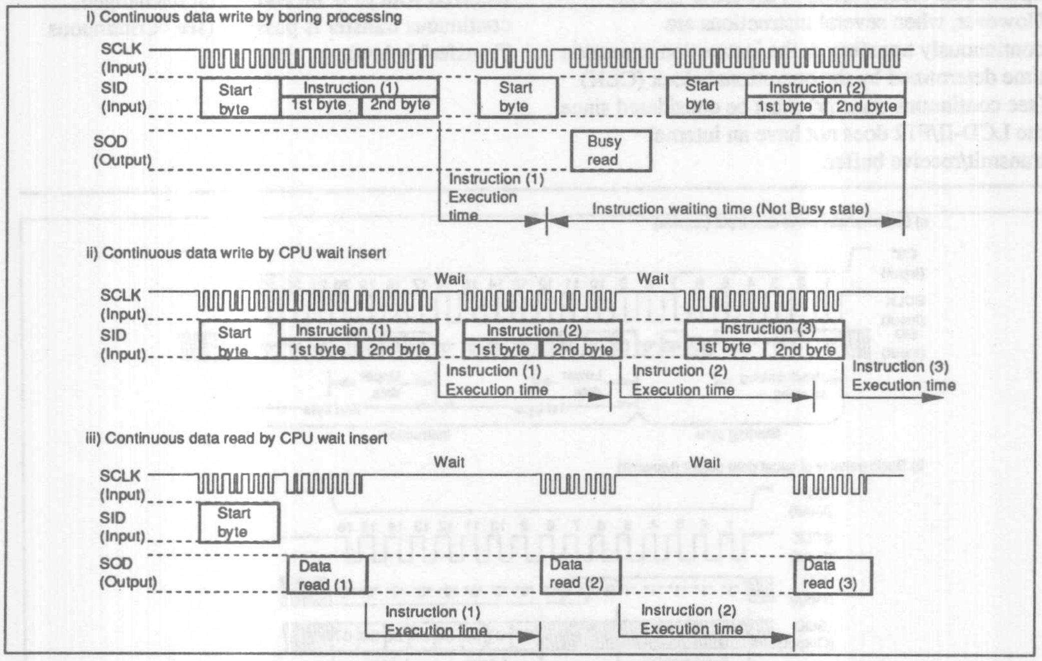


Figure 15 Procedure for Continuous Data Transfer

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66712 can be controlled by the MPU. Before starting internal operation of the HD66712, control information is temporarily stored in these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD66712 is determined by signals sent from the MPU. These signals, which include register selection (RS), read/write ($R/\overline{W}$), and the data bus (DB_0 to DB_7), make up the HD66712 instructions (table 11). There are four categories of instructions that:

- Designate HD66712 functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66712 RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (table 16) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the HD66712 is not in the busy state (BF = 1) before sending an instruction from the MPU to the HD66712. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to table 11 for the list of each instruction execution time.

Instruction Description

Clear Display

Clear display writes space code (20)H (character pattern for character code (20)H must be a blank pattern) into all DD RAM addresses. It then sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change.

Return Home

Return home sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DD RAM contents do not change.

The cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). In addition, flicker may occur in a moment at the time of this instruction issue.

Entry Mode Set

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from DD RAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM and SEG RAM.

S: Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1 during DD RAM write. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DD RAM. Also, writing into or reading out from CG RAM and SEG RAM does not shift the display. In a low power mode (LP = 1), do not set S = 1 because the whole display does not normally shift.

Display On/Off Control

When extension register enable bit (RE) is 0, bits D, C, and B are accessed.

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in DD RAM, but can be displayed instantly by setting D to 1.

C: The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5×8 dot character font.

B: The character indicated by the cursor blinks when B is 1 (figure 16). The blinking is displayed as switching between all blank dots and displayed characters at a speed of 370-ms intervals when f_{cp} or f_{OSC} is 270 kHz. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to f_{OSC} or the reciprocal of f_{cp}. For example, when f_{cp} is 300 kHz, $370 \times 270/300 = 333$ ms.)

Extended Function Set

When the extended register enable bit (RE) is 1, FW, B/W, and NW bit shown below are accessed. Once these registers are accessed, the set values are held even if the RE bit is set to zero.

FW: When FW is 1, each displayed character is controlled with a 6-dot width. The user font in CG RAM is displayed with a 6-bit character width from bits 5 to 0. As for fonts stored in CG ROM, no display area is assigned to the leftmost bit, and the font is displayed with a 5-bit character width. If the FW bit is changed, data in DD RAM and CG RAM SEG RAM is destroyed. Therefore, set FW before data is written to RAM. When font width is set to 6 dots, the frame frequency decreases to 5/6 compared to 5-dot time. See "Oscillator Circuit" for details.

B/W: When B/W is 1, the character at the cursor position is cyclically displayed with black-white invertion. At this time, bits C and B in display on/off control register are "Don't care". When f_{CP} or fosc is 270 kHz, display is changed by switching every 370 ms.

NW: When NW is 1, 4-line display is performed. At this time, bit N in the function set register is "Don't care".

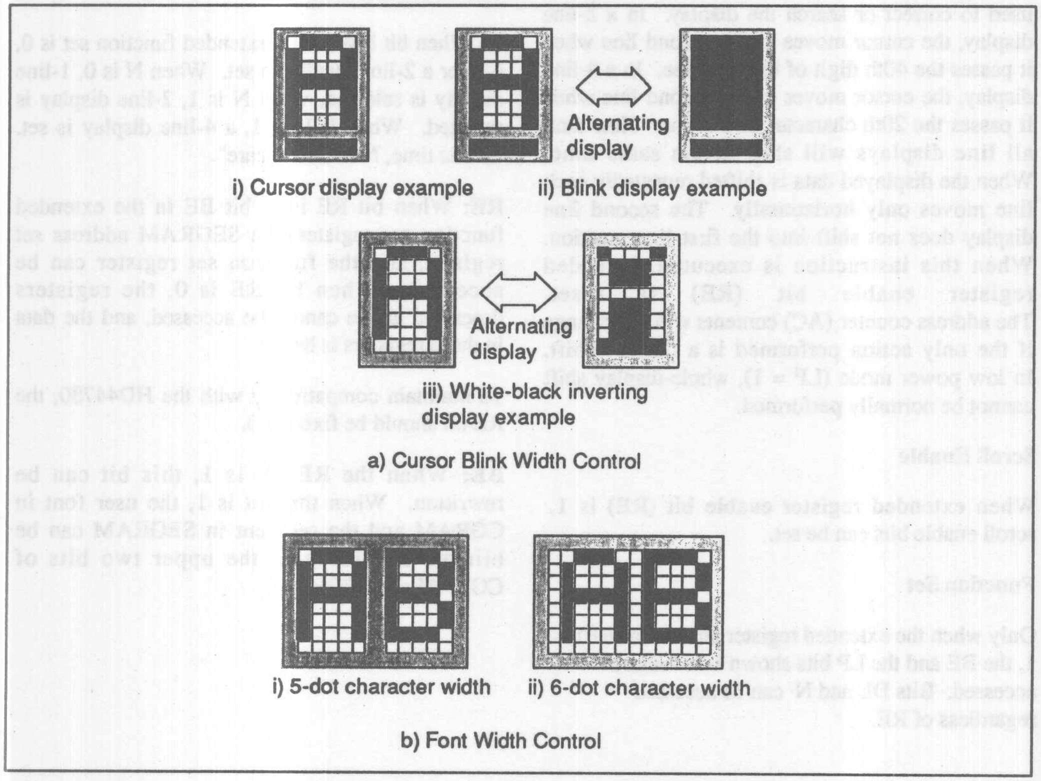


Figure 16 Example of Display Control

Cursor or Display Shift

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (table 9). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. In a 4-line display, the cursor moves to the second line when it passes the 20th character of the line. Note that, all line displays will shift at the same time. When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position. When this instruction is executed, extended register enable bit (RE) is reset. The address counter (AC) contents will not change if the only action performed is a display shift. In low power mode (LP = 1), whole-display shift cannot be normally performed.

Scroll Enable

When extended register enable bit (RE) is 1, scroll enable bits can be set.

Function Set

Only when the extended register enable bit (RE) is 1, the BE and the LP bits shown below can be accessed. Bits DL and N can be accessed regardless of RE.

DL: Sets the interface data length. Data is sent or received in 8-bit lengths (DB_7 to DB_0) when DL is 1, and in 4-bit lengths (DB_7 to DB_4) when DL is 0. When 4-bit length is selected, data must be sent or received twice.

N: When bit NW in the extended function set is 0, a 1- or a 2-line display is set. When N is 0, 1-line display is selected; when N is 1, 2-line display is selected. When NW is 1, a 4-line display is set. At this time, N is "Don't care".

RE: When bit RE is 1, bit BE in the extended function set register, the SEGRAM address set register, and the function set register can be accessed. When bit RE is 0, the registers described above cannot be accessed, and the data in these registers is held.

To maintain compatibility with the HD44780, the RE bit should be fixed to 0.

BE: When the RE bit is 1, this bit can be rewritten. When this bit is 1, the user font in CGRAM and the segment in SEGRAM can be blinked according to the upper two bits of CGRAM and SEGRAM.

Table 9 Shift Function

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

LP: When bit RE is 1, this bit can be rewritten. When LP is set to 1 and the EXT pin is low (without an extended driver), the HD66712 operates in low power mode. In 1-line display mode, the HD66712 operates on a 4-division clock, and in a 2-line or a 4-line display mode, the HD66712 operates on a 2-division clock. According to these operations, instruction execution takes four times or twice as long. Note that in low power mode, display shift cannot be performed. The frame frequency is reduced to 5/6 that of normal operation. See "Oscillator Circuit" for details.

Note: Perform the DL, N, NW, and FW fucntions at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, if bits N, NW, or FW are changed after other instructions are executed, RAM contents may be broken.

Set CG RAM Address

A CG RAM address can be set while the RE bit is cleared to 0.

Set CG RAM address into the address counter displayed by binary AAAAAA. After this address set, data is written to or read from the MPU for CG RAM.

Set SEGRAM Address

Only when the extended register enable (RE) bit is 1, HS2 to HS0 and the SEGRAM address can be set.

The SEGRAM address in the binary form AAAA is set to the address counter. After this address set, SEGRAM can be written to or read from by the MPU.

Set DD RAM Address

A DD RAM address can be set while the RE bit is cleared to 0. Set DD RAM address sets the DD RAM address binary AAAAAAA into the address counter.

After this address set, data is written to or read from the MPU for DD RAM.

However, when N and NW is 0 (1-line display), AAAAAAA can be (00)H to (4F)H. When N is 1 and NW is 0 (2-line display), AAAAAAA is (00) H to (27)H for the first line, and (40)H to (67)H for the second line. When NW is 1 (4-line display), AAAAAAA is (00)H to (13)H for the first line, (20)H to (33)H for the second line, (40)H to (53)H for the third line, and (60)H to (73)H for the fourth line.

Set Scroll Quantity

When extended registor enable bit (RE) is 1, HDS5 to HDS0 can be set.

HDS5 to HDS0 specifies horizontal scroll quantity to the left of the display in dot units. The HD66712 uses the unused DDRAM area to execute a desired horizontal smooth scroll from 1 to 48 dots.

Note: When performing a horizontal scroll as described above by connecting an extended driver, the maximum number of characters per line decreases by the quantity set by the above horizontal scroll. For example, when the maximum 24-dot scroll quantity (4 characters) is used with 6-dot font width and 4-line display, the maximum numbers of characters is 20 – 4 = 16. Notice that in low power mode (LP = 1), display shift and scroll cannot be performed.

Read Busy Flag and Address

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by both CG, DD, and SEG RAM addresses, and its value is determined by the previous instruction. The address contents are the same as for CG RAM, DD RAM, and SEG RAM address set instructions.

Write Data to CG, DD, or SEG RAM

This instruction writes 8-bit binary data DDDDDDDD to CG, DD or SEG RAM. CG, DD or SEG RAM is selected by the previous specification of the address set instruction (CG RAM address set / DD RAM address set / SEG RAM address set). After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift direction.

Read Data from CG, DD, or SEG RAM

This instruction reads 8-bit binary data DDDDDDDD from CG, DD, or SEG RAM. CG, DD or SEG RAM is selected by the previous specification of the address set instruction. If no address is specified, the first data read will be invalid. When executing serial read instructions, the next address is normally read from the next address. An address set instruction need not be executed just before this read instruction when shifting the cursor by a cursor shift instruction (when reading from DD RAM). A cursor shift instruction is the same as a set DD RAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, a display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented after write instructions to CG, DD or SEG RAM. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to read data correctly, execute either an address set instruction or a cursor shift instruction (only with DD RAM), or alternatively, execute a preliminary read instruction to ensure the address is correctly set up before accessing the data.

Table 10 HS5 to HS0 Settings

HDS5	HDS4	HDS3	HDS2	HDS1	HDS0	Description
0	0	0	0	0	0	No shift
0	0	0	0	0	1	Shift the display position to the left by one dot.
0	0	0	0	1	0	Shift the display position to the left by two dots.
0	0	0	0	1	1	Shift the display position to the left by three dots.
				⋮		
1	0	1	1	1	1	Shift the display position to the left by forty-seven dots.
1	1	•	•	•	•	Shift the display position to the left by forty-eight dots.

Table 11 Instructions

Instruction	RE bit	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (max) (when f_{cp} or fosc is 270 kHz)
		Code											
Clear display	0/1	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.52 ms
Return home	0/1	0	0	0	0	0	0	0	0	1	—	Sets DD RAM address 0 IN address counter. Also returns display from being shifted to original position. DDRAM contents remain unchanged.	1.52 ms
Entry mode set	0/1	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations areperformed during data write and read.	37 µs
Display on/off control	0	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	37 µs
Extension function set	1	0	0	0	0	0	0	1	FW	B/W	NW	Sets a font width, a black-white inverting cursor (B/W), and a 4-line display (NW).	37 µs
Cursor or display shift	0	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DD RAM contents.	37 µs
Scroll enable	1	0	0	0	0	0	1	HSE	HSE	HSE	HSE	Specifies which display lines to undergo horizontal smooth scroll.	37 µs
Function set	0	0	0	0	0	1	DL	N	RE	—	—	Sets interface data length (DL), number of display lines (L), and extension register write enable (RE)).	37 µs
	1	0	0	0	0	1	DL	N	RE	BE	LP	Sets CGRAM/SEGRAM blinking enable (BE), and power-down mode (LP). LP is available when the EXT pin is low.	37 µs
Set CGRAM address	0	0	0	0	1	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	Sets CG RAM address. CG RAM data is sent and received after this setting.	37 µs
Set SEGRAM address set	1	0	0	0	1	*	*	A_{SEG}	A_{SEG}	A_{SEG}	A_{SEG}	Sets SEGRAM address. DDRAM data is sent and received after this setting. Also sets a horizontal dot scroll quantity (HDS).	37 µs
Set DDRAM address	0	0	0	1	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	Sets DD RAM address. DD RAM data is sent and received after this setting.	37 µs
Set scroll quantity	1	0	0	1	*	HDS	HDS	HDS	HDS	HDS	HDS	Sets horizontal dot scroll quantity.	37 µs

Table 11 Instructions (cont)

Instruction	RE bit	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (max) (when f_{cp} or f_{osc} is 270 kHz)
Read busy flag & address	0/1	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs
Write data to RAM	0/1	1	0	Write data								Writes data into DD RAM, CG RAM, or SEGRAM.	37 µs t_{ADD} = 5.5 µs*
Read data from RAM	0/1	1	1	Read data								Reads data from DD RAM, CG RAM, or SEGRAM.	37 µs t_{ADD} = 5.5 µs*

I/D = 1: Increment
I/D = 0: Decrement
S = 1: Accompanies display shift
D = 1: Display on
C = 1: Cursor on
B = 1: Blink on
FW = 1: 6-dot font width
B/W = 1: Black-white inverting cursor on
NW = 1: Four lines
NW = 0: One or two lines
S/C = 1: Display shift
S/C = 0: Cursor move
R/L = 1: Shift to the right
R/L = 0: Shift to the left
DL = 1: 8 bits, DL = 0: 4 bits
N = 1: 2 lines, N = 0: 1 line
RE = 1: Extension register access enable
BE = 1: CGRAM/SEGRAM blinking enable
LP = 1: Low-power mode
BF = 1: Internally operating
BF = 0: Instructions acceptable

DD RAM: Display data RAM
A_{DD}: DD RAM address (corresponds to cursor address)
CG RAM: Character generator RAM
A_{CG}: CG RAM address:
SEGRAM: Segment RAM
A_{SEG}: Segment RAM address
HSE: Specifies horizontal scroll lines
HDS: Horizontal dot scroll quantity
AC: Address counter used for both DD, CG, and SEG RAM addresses.

Note: 1. — indicates no effect.
*After execution of the CG RAM/DD RAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In figure 18, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

2. Extension time changes as frequency changes. For example, when f is 300 kHz, the execution time is: 37 µs x 270/300 = 33 µs.

3. Execution time in a low-power mode (LP = 1 & EXT = low) becomes four times for a 1-line mode, and twice for a 2- or 4-line mode.

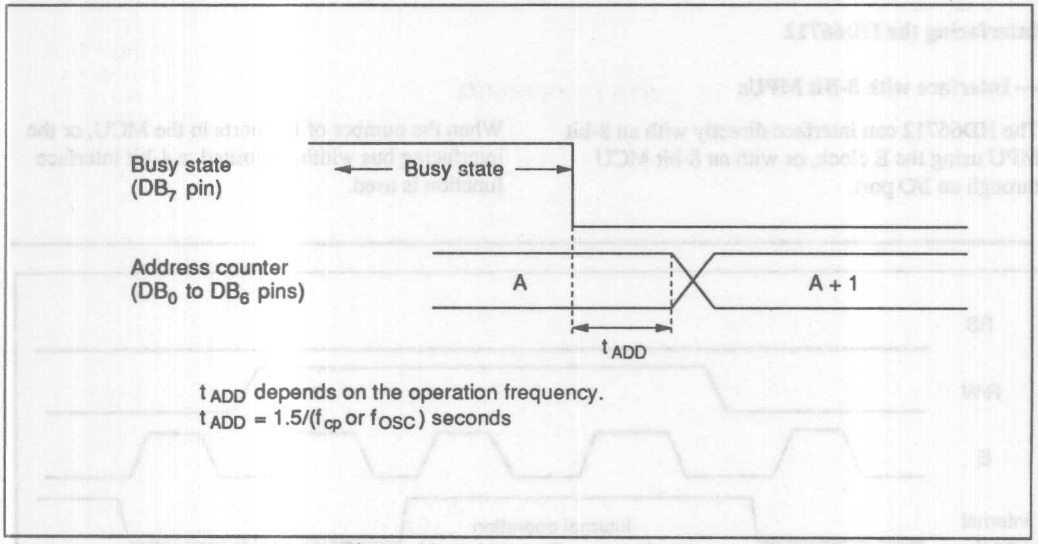


Figure 18 Address Counter Update

Interfacing the HD66712

— Interface with 8-Bit MPUs

The HD66712 can interface directly with an 8-bit MPU using the E clock, or with an 8-bit MCU through an I/O port.

When the number of I/O ports in the MCU, or the interfacing bus width, if limited, a 4-bit interface function is used.

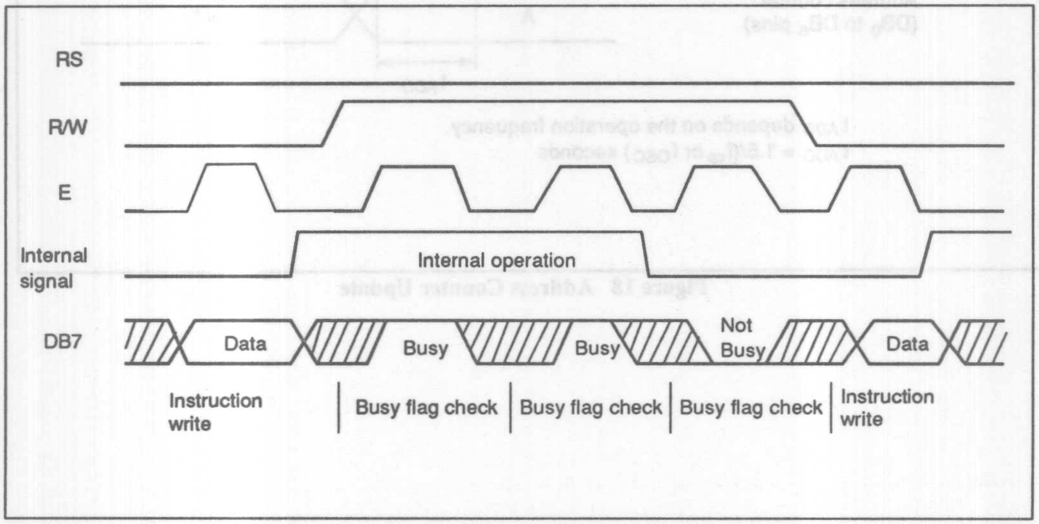


Figure 19 Example of 8-Bit Data Transfer Timing Sequence

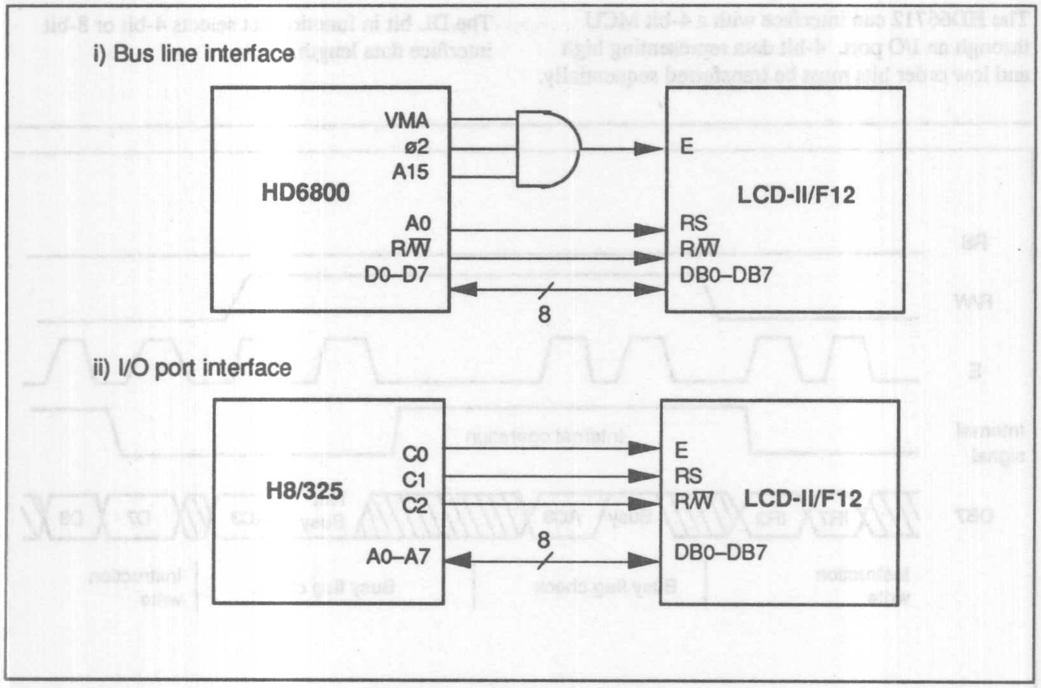


Figure 20 8-Bit MPU Interface

— Interface with 4-Bit MPUs

The HD66712 can interface with a 4-bit MCU through an I/O port. 4-bit data representing high and low order bits must be transferred sequentially.

The DL bit in function-set selects 4-bit or 8-bit interface data length.

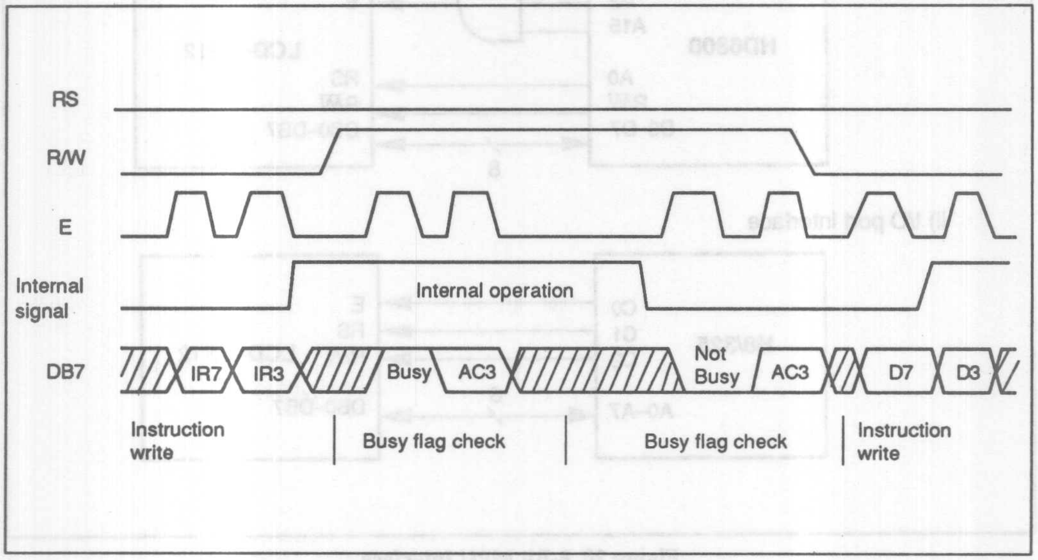


Figure 21 Example of 4-Bit Data Transfer Timing Sequence

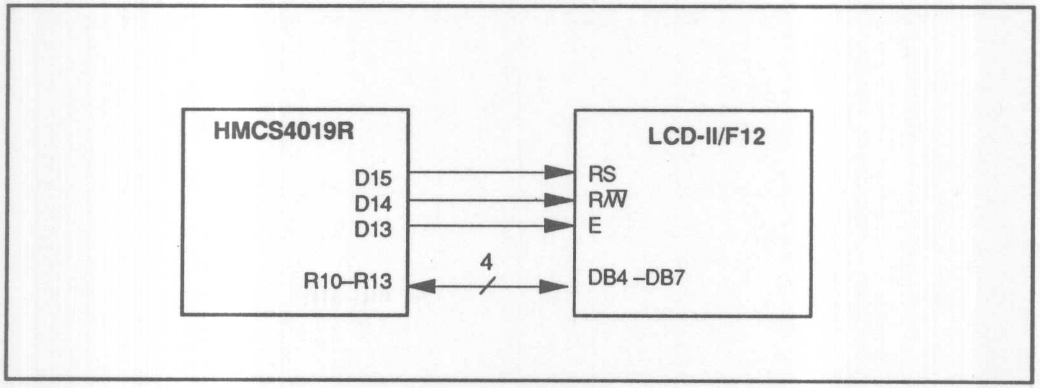
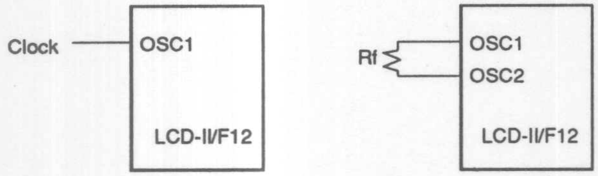


Figure 22 4-bit MPU Interface

Oscillator Circuit

1) When an external clock is used

2) When an internal oscillator is used

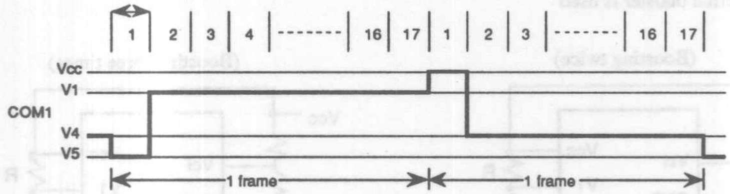


The oscillator frequency can be adjusted by oscillator resistance (Rf). If Rf is increased or power supply voltage is decreased, the oscillator frequency decreases. The recommended oscillator resistor is as follows.

- Rf = 91 kΩ ± 2% (Vcc = 5 V)
- Rf = 75 kΩ ± 2% (Vcc = 3 V)

Figure 23 Oscillator Circuit

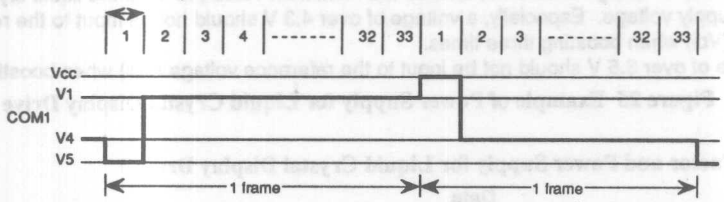
(1) 1 /17 duty cycle



Item	Normal Display Mode (LP = 0) 5-Dot Font Width	Normal Display Mode (LP = 0) 6-Dot Font Width	Low Power Mode (LP = 1) 5-Dot Font Width	Low Power Mode (LP = 1) 6-Dot Font Width
Line selection period	200 clocks	240 clocks	60 clocks	72 clocks
Frame frequency	79.4 Hz	66.2 Hz	66.2 Hz	55.1 Hz

Note: At the calculation example above for displayed frame frequency, all oscillator frequencies are 270 kHz (1 clock = 3.7 µs).

(2) 1 /33 duty cycle



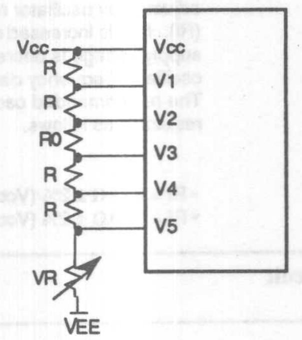
Item	Normal Display Mode (LP = 0) 5-Dot Font Width	Normal Display Mode (LP = 0) 6-Dot Font Width	Low Power Mode (LP = 1) 5-Dot Font Width	Low Power Mode (LP = 1) 6-Dot Font Width
Line selection period	100 clocks	120 clocks	60 clocks	72 clocks
Frame frequency	81.8 Hz	68.2 Hz	68.2 Hz	56.8 Hz

Note: At the calculation example above for displayed frame frequency, all oscillator frequencies are 270 kHz (1 clock = 3.7 µs).

Figure 24 Frame Frequency

Power Supply for Liquid Crystal Display Drive

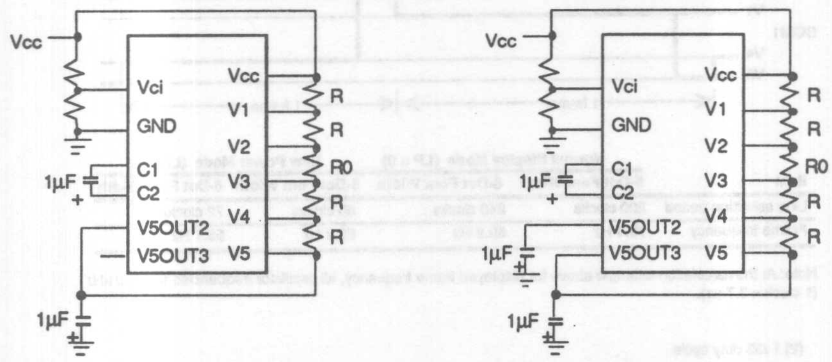
1) When an external power supply is used



2) When an internal booster is used

(Boosting twice)

(Boosting three times)



Notes 1. Boosted output voltage should not exceed the maximum value (13 V) of the liquid crystal power supply voltage. Especially, a voltage of over 4.3 V should not be input to the reference voltage (Vci) when boosting three times.

2. A voltage of over 5.5 V should not be input to the reference voltage (Vci) when boosting twice.

Figure 25 Example of Power Supply for Liquid Crystal Display Drive

Table 12 Duty Factor and Power Supply for Liquid Crystal Display Drive

Item		Data	
Number of Lines		1	2/4
Duty factor		1/17	1/33
Bias		1/5	1/6.7
Divided resistance	R	R	R
	R0	R	2.7R

Note: R changes depending on the size of liquid crystal penel. Normally, R must be 2 kΩ to 10 kΩ.

Extension Driver LSI Interface

By bringing the EXT pin high, extended driver interface signals (CL1, CL2, D, and M) are output.

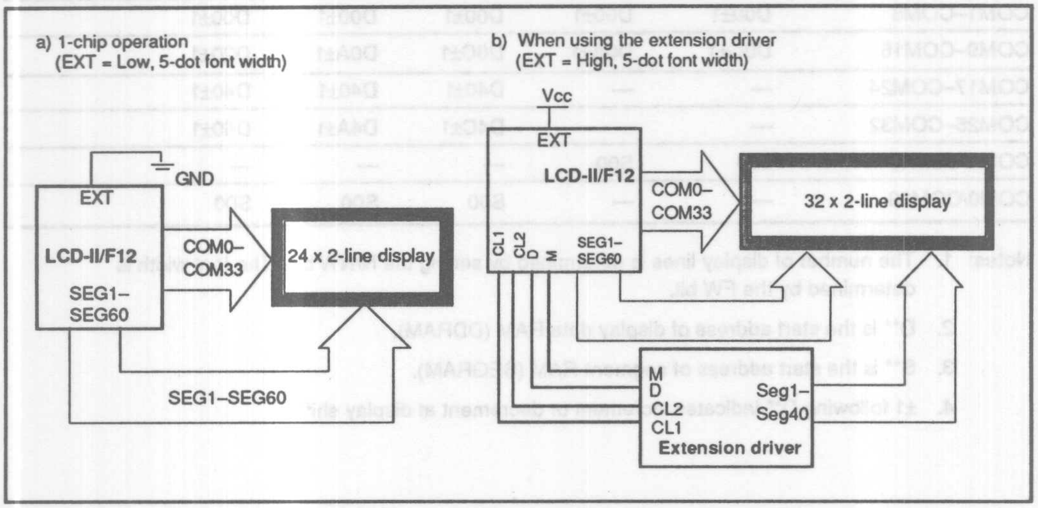


Figure 26 HD66712 and the Extension Driver Connection

Table 13 Relationships between the Number of Display Lines and 40-Output Extension Driver

	Controller					
	LCD-II/F12		LCD-II/F8		HD44780	HD66702
Display Lines	5-Dot Width	6-Dot Width	5-Dot Width	6-Dot Width	5-Dot Width	5-Dot Width
16 x 2 lines	Not required	Not required	Not required	1	1	Not required
20 x 2 lines	Not required	Not required	1	1	2	Not required
24 x 2 lines	Not required	1	1	2	2	1
40 x 2 lines	Disabled	Disabled	Disabled	Disabled	4	3
12 x 4 lines	Not required	1	1	1	Disabled	Disabled
16 x 4 lines	1	1	1	2	Disabled	Disabled
20 x 4 lines	1	2	2	3	Disabled	Disabled

Note: The number of display lines can be extended to 32 x 2 lines or 20 x 4 lines in the LCD-II/F12.
The number of display lines can be extended to 30 x 2 lines or 20 x 4 lines in the LCD-II/F8.

Table 14 Display Start Address in Each Mode

	Number of Lines				
	1-Line Mode		2-Line Mode		4-Line Mode
Output	5 dot	6 dot	5 dot	6 dot	5 dot/6 dot
COM1–COM8	D00±1	D00±1	D00±1	D00±1	D00±1
COM9–COM16	D0C±1	D0A±1	D0C±1	D0A±1	D20±1
COM17–COM24	—	—	D40±1	D40±1	D40±1
COM25–COM32	—	—	D4C±1	D4A±1	D60±1
COM0/COM17	S00	S00	—	—	—
COM0/COM33	—	—	S00	S00	S00

Notes: 1. The number of display lines is determined by setting the N/NW bit. The font width is determined by the FW bit.

2. D** is the start address of display data RAM (DDRAM).

3. S** is the start address of segment RAM (SEGRAM).

4. ±1 following D** indicates increment or decrement at display shift.

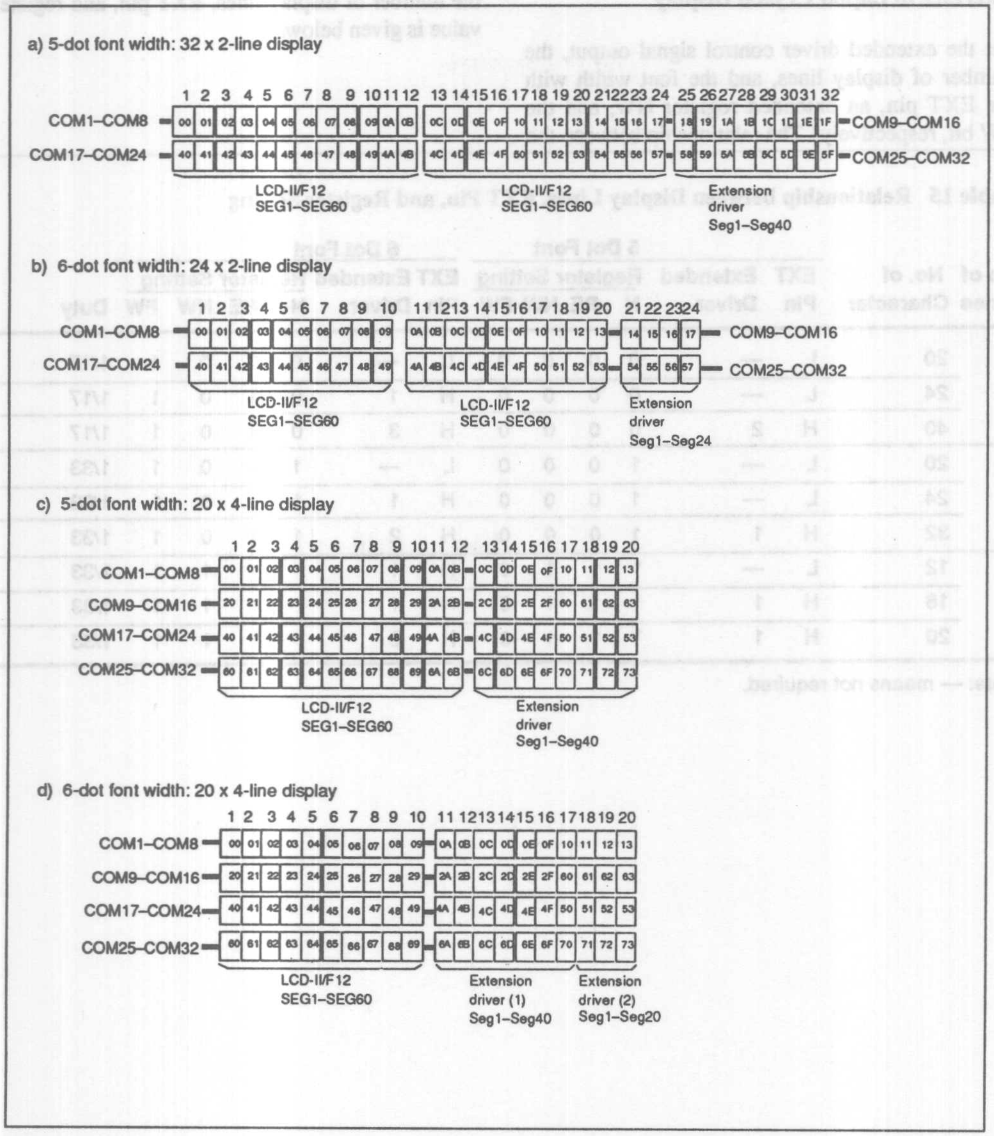


Figure 27 Correspondence between the Display Position at Extension Display and the DDRAM Address

Interface to Liquid Crystal Display

Set the extended driver control signal output, the number of display lines, and the font width with the EXT pin, an extended register NW, and the FW bit, respectively. The relationship between the the number of display lines, EXT pin, and register value is given below.

Table 15 Relationship between Display Lines, EXT Pin, and Register Setting

		5 Dot Font						6 Dot Font						
				Registor Setting						Registor Setting				
No of Lines	No. of Character	EXT Pin	Extended Driver	N	RE	NW	FW	EXT Pin	Extended Driver	N	RE	NW	FW	Duty
1	20	L	—	0	0	0	0	L	—	0	1	0	1	1/17
	24	L	—	0	0	0	0	H	1	0	1	0	1	1/17
	40	H	2	0	0	0	0	H	3	0	1	0	1	1/17
2	20	L	—	1	0	0	0	L	—	1	1	0	1	1/33
	24	L	—	1	0	0	0	H	1	1	1	0	1	1/33
	32	H	1	1	0	0	0	H	2	1	1	0	1	1/33
4	12	L	—	*	1	1	0	H	1	*	1	1	1	1/33
	16	H	1	*	1	1	0	H	1	*	1	1	1	1/33
	20	H	1	*	1	1	0	H	2	*	1	1	1	1/33

Note: — means not required.

• Example of 5-dot font width connection

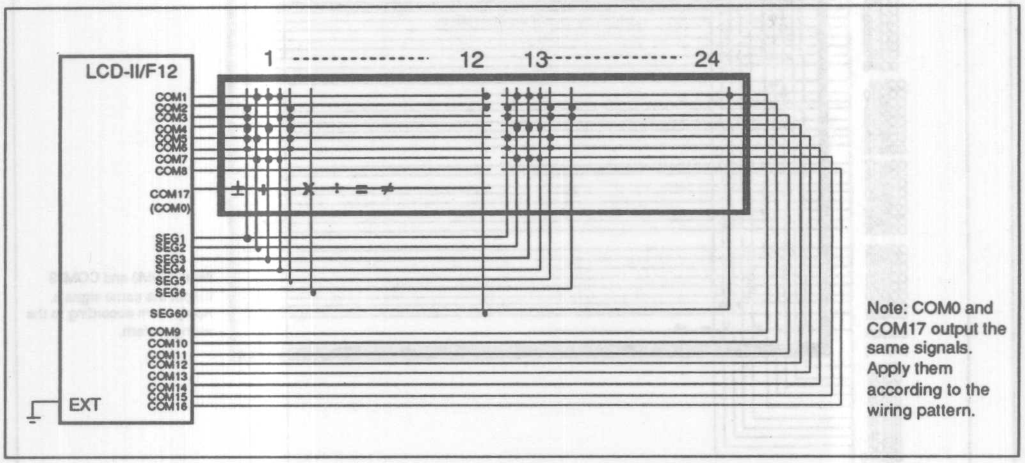


Figure 28 24 x 1-Line + 60-Segment Display (5-dot font, 1/17 Duty)

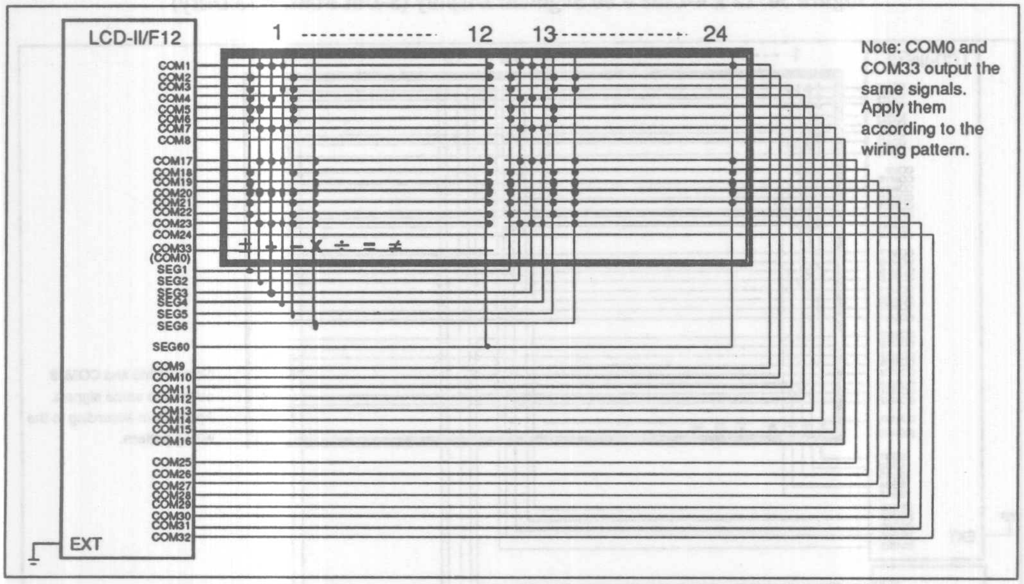


Figure 29 24 x 1-Line + 60-Segment Display (5-dot font, 1/33 Duty)

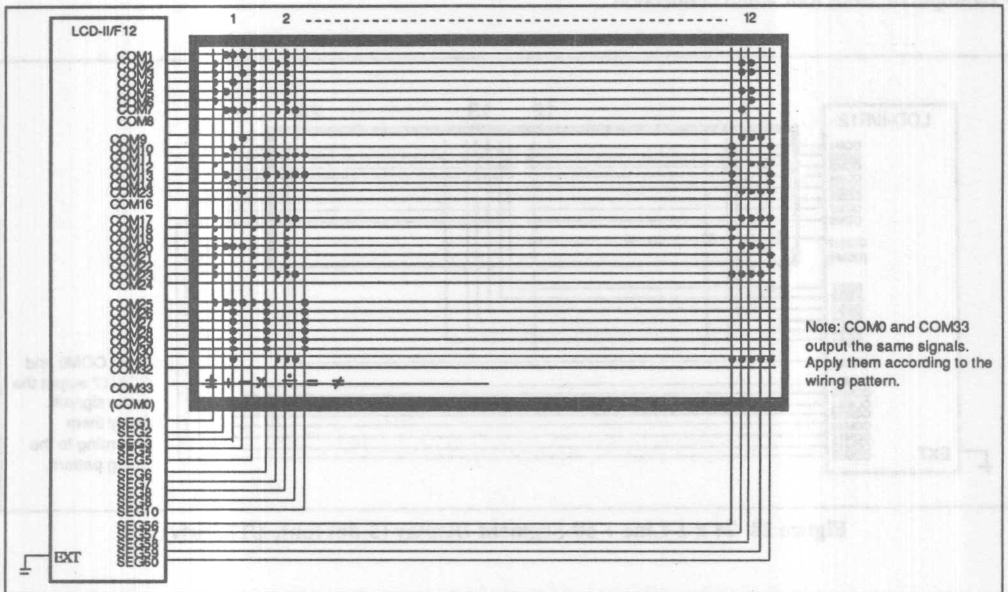


Figure 30 12 x 4-Line + 60 Segment Display (5-Dot Font, 1/33 Duty)

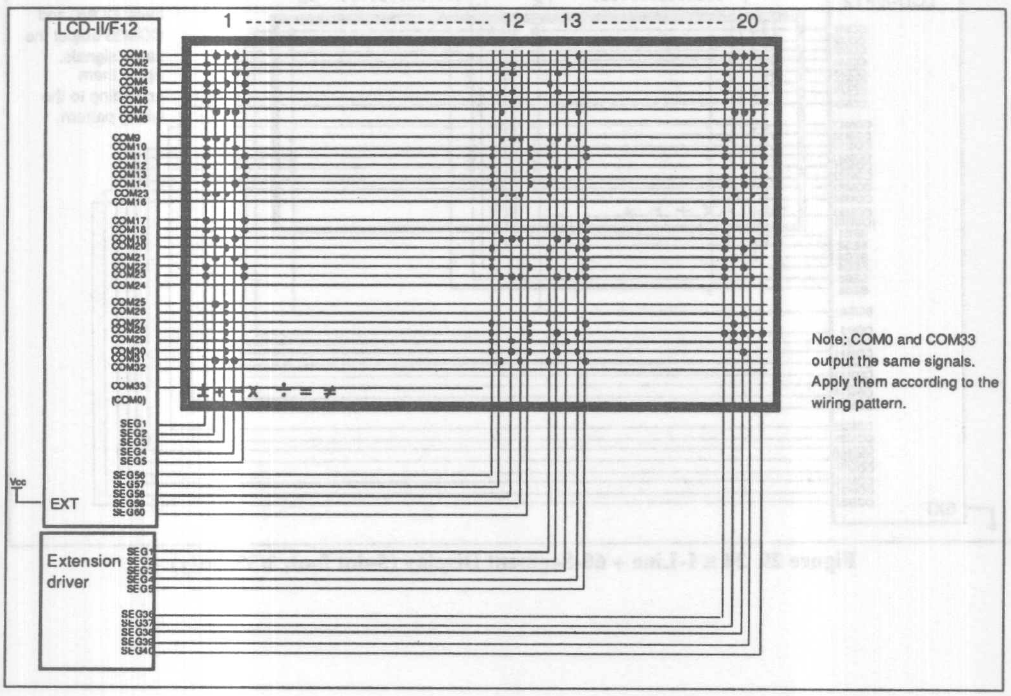


Figure 31 20 x 4-Line + 80 Segment Display (5-Dot Font, 1/33 Duty)

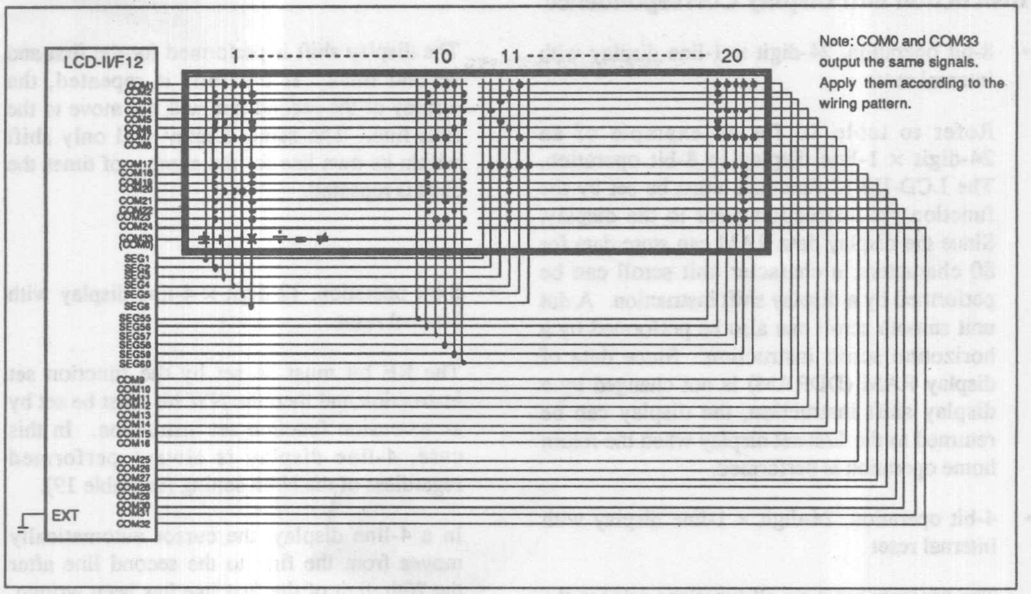


Figure 32 20 x 2-Line + 60 Segment Display (6-Dot Font, 1/33 Duty)

Instruction and Display Correspondence

- 8-bit operation, 24-digit × 1-line display with internal reset

  Refer to table 16 for an example of an 24-digit × 1-line display in 8-bit operation. The LCD-II/F12 functions must be set by the function set instruction prior to the display. Since the display data RAM can store data for 80 characters, a character unit scroll can be performed by a display shift instruction. A dot unit smooth scroll can also be performed by a horizontal scroll instruction. Since data of display RAM (DDRAM) is not changed by a display shift instruction, the display can be returned to the first set display when the return home operation is performed.

- 4-bit operation, 24-digit × 1-line display with internal reset

  The program must set all functions prior to the 4-bit operation (see table 17). When the power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since DB_0 to DB_3 are not connected, a rewrite is then required. However, since one operation is completed in two accesses for 4-bit operation, a rewrite is needed to set the functions. Thus, DB_4 to DB_7 of the function set instruction is written twice.

- 8-bit operation, 24-digit × 2-line display with internal reset

  For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 16 characters in the first line, the DD RAM address must be again set after the 16th character is completed. (See table 18.)

  The display shift is performed for the first and second lines. If the shift is repeated, the display of the second line will not move to the first line. The same display will only shift within its own line for the number of times the shift is repeated.

- 8-bit operation, 12-digit × 4-line display with internal reset

  The RE bit must be set by the function set instruction and then the NW bit must be set by an extension function set instruction. In this case, 4-line display is always performed regardless of the N bit setting (see table 19).

  In a 4-line display, the cursor automatically moves from the first to the second line after the 20th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must be set again after the 8th character is completed. Display shifts are performed on all lines simultaneously.

Note: When using the internal reset, the electrical characteristics in the Power Supply Conditions Using Internal Reset Circuit table must be satisfied. If not, the LCD-II/F12 must be initialized by instructions. See the section, Initializing by Instruction.

Table 16 8-Bit Operation, 24-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS R/$\overline{W}$ D7 D6 D5 D4 D3 D2 D1 D0	Display	Operation
1	Power supply on (the HD66712 is initialized by the internal reset circuit)		Initialized. No display.
2	Function set RS R/$\overline{W}$ D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 0 0 0 0 1 1 0 0 * *		Sets to 8-bit operation and selects 1-line display. Bit 2 must always be cleared.
3	Display on/off control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
5	Write data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Writes H. DD RAM has already been selected by initialization when the power was turned on.
6	Write data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HI_	Writes I.
7	⋮	⋮	
8	Write data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes I.
9	Entry mode set 0 0 0 0 0 0 0 1 1 1	HITACHI_	Sets mode to shift display at the time of write.
10	Write data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI _	Writes a space.

Table 16 8-Bit Operation, 24-Digit × 1-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
11	Write data to CG RAM/DD RAM											Writes M.
	1	0	0	1	0	0	1	1	0	1	TACHI M_	
12					⋮						⋮	
13	Write data to CG RAM/DD RAM											Writes O.
	1	0	0	1	0	0	1	1	1	1	MICROKO_	
14	Cursor or display shift											Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*	MICROKO	
15	Cursor or display shift											Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*	MICROKO	
16	Write data to CG RAM/DD RAM											Writes C over K. The display moves to the left.
	1	0	0	1	0	0	0	0	1	1	ICROCO	
17	Cursor or display shift											Shifts the display and cursor position to the right.
	0	0	0	0	0	1	1	1	*	*	MICROCO	
18	Cursor or display shift											Shifts the display and cursor position to the right.
	0	0	0	0	0	1	0	1	*	*	MICROCO_	
19	Write data to CG RAM/DD RAM											Writes M.
	1	0	0	1	0	0	1	1	0	1	ICROCOM_	
20					⋮						⋮	
21	Return home											Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0	HITACHI	

Table 17 4-Bit Operation, 24-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS	R/W̄	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
1	Power supply on (the HD66712 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 4-bit operation. Clear bit 2. In this case, operation is handled as 8 bits by initialization.
	RS	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
	0	0	0	0	1	0	—	—	—	—		
	—	—	—	—	—	—	—	—	—	—		
3	Function set											Sets 4-bit operation and selects 1-line display. Clear bit 2. 4-bit operation starts from this step.
	0	0	0	0	1	0	—	—	—	—		
	0	0	0	0	*	*	—	—	—	—		
4	Display on/off control										_	Turns on display and cursor. Entire display is in space mode because of initialization.
	0	0	0	0	0	0	—	—	—	—		
	0	0	1	1	1	0	—	—	—	—		
5	Entry mode set										_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
	0	0	0	0	0	0	—	—	—	—		
	0	0	0	1	1	0	—	—	—	—		
6	Write data to CG RAM/DD RAM										H_	Writes H. DDRAM has already been selected by initialization.
	1	0	0	1	0	0	—	—	—	—		
	1	0	1	0	0	0	—	—	—	—		
7	. . .											Based on 8-bit operation after this instruction.

Note: The control is the same as for 8-bit operation beyond step #6.

Table 18 8-Bit Operation, 24-Digit × 2-Line Display Example with Internal Reset

Step No.	RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
1	Power supply on (the HD66712 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 8-bit operation and selects 2-line display. Clear bit 2.
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
	0	0	0	0	1	1	1	0	*	*		
3	Display on/off control										_	Turns on display and cursor. All display is in space mode because of initialization.
	0	0	0	0	0	0	1	1	1	0		
4	Entry mode set										_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
	0	0	0	0	0	0	0	1	1	0		
5	Write data to CG RAM/DD RAM										H_	Writes "H". DD RAM has already been selected by initialization at power-on.
	1	0	0	1	0	0	1	0	0	0		
6					⋮						⋮	
7	Write data to CG RAM/DD RAM										HITACHI_	Writes I.
	1	0	0	1	0	0	1	0	0	1		
8	Set DD RAM address										HITACHI _	Sets DD RAM address so that the cursor is positioned at the head of the second line.
	0	0	1	1	0	0	0	0	0	0		

Table 18 8-Bit Operation, 24-Digit × 2-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/W̄	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
9	Write data to CG RAM/DD RAM										HITACHI M_	Writes a space.
	1	0	0	1	0	0	1	1	0	1		
10	⋮										⋮	
11	Write data to CG RAM/DD RAM										HITACHI MICROCO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
12	Entry mode set										HITACHI MICROCO_	Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1		
13	Write data to CG RAM/DD RAM										ITACHI ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
14	⋮										⋮	
17	Return home										HITACHI MICROCOM	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 19 8-Bit Operation, 12-Digit × 4-Line Display Example with Internal Reset

Step No.	Instruction	RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
1	Power supply on (the HD66712 is initialized by the internal reset circuit)												Initialized. No display.
2	Function set	0	0	0	0	1	1	0	1	*	*		Sets 8-bit operation and enables write to the extension register.
3	4-line mode set	0	0	0	0	0	0	1	0	0	1		Sets 4-line operation.
4	Function set Inhibit write to extension register	0	0	0	0	1	1	0	0	*	*		Inhibits write to extension register. Invalidates selection of 1-line/2-line by bit 3.
5	Display on/off control	0	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. Entire display is cleared because of initialization.
6	Entry mode set	0	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right when writing to RAM. Display is not shifted.
7	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	0	H_	Writes H. DDRAM has already been selected by initialization.
8	. . .												
9	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.

Table 19 8-Bit Operation, 12-Digit × 4-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
10	Set DD RAM address											
	0	0	1	0	1	0	0	0	0	0	HITACHI _	Sets DD RAM address to (20)H so that the cursor is positioned at the beginning of the second line.
11	Write data to CG RAM											
	1	0	0	0	1	1	0	0	0	0	HITACHI 0_	Writes 0.

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

- Initializing when a length of interface is 8-bit system

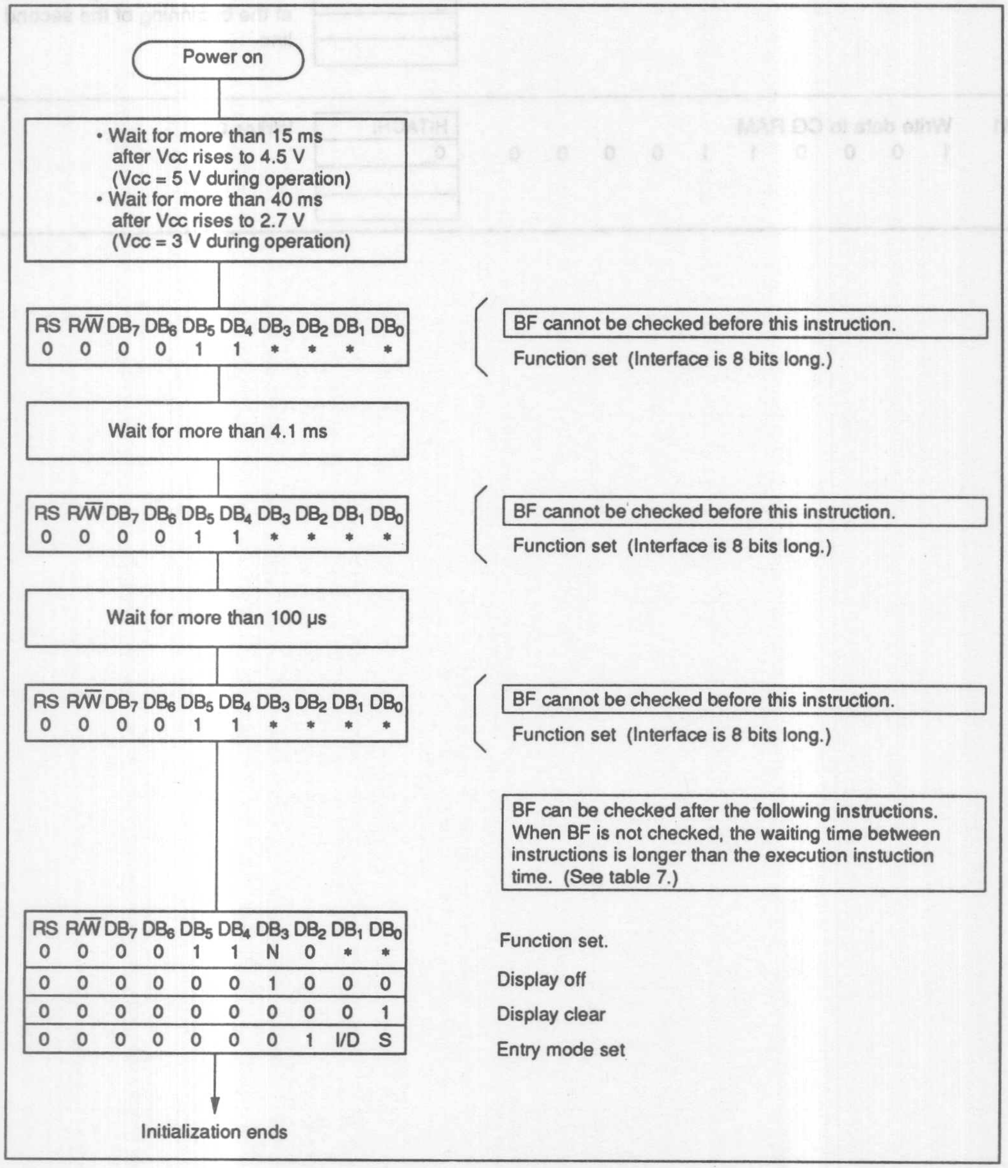


Figure 33 Initializing Flow of 8-Bit Interface

• **Initializing when a length of interface is 4-bit system.**

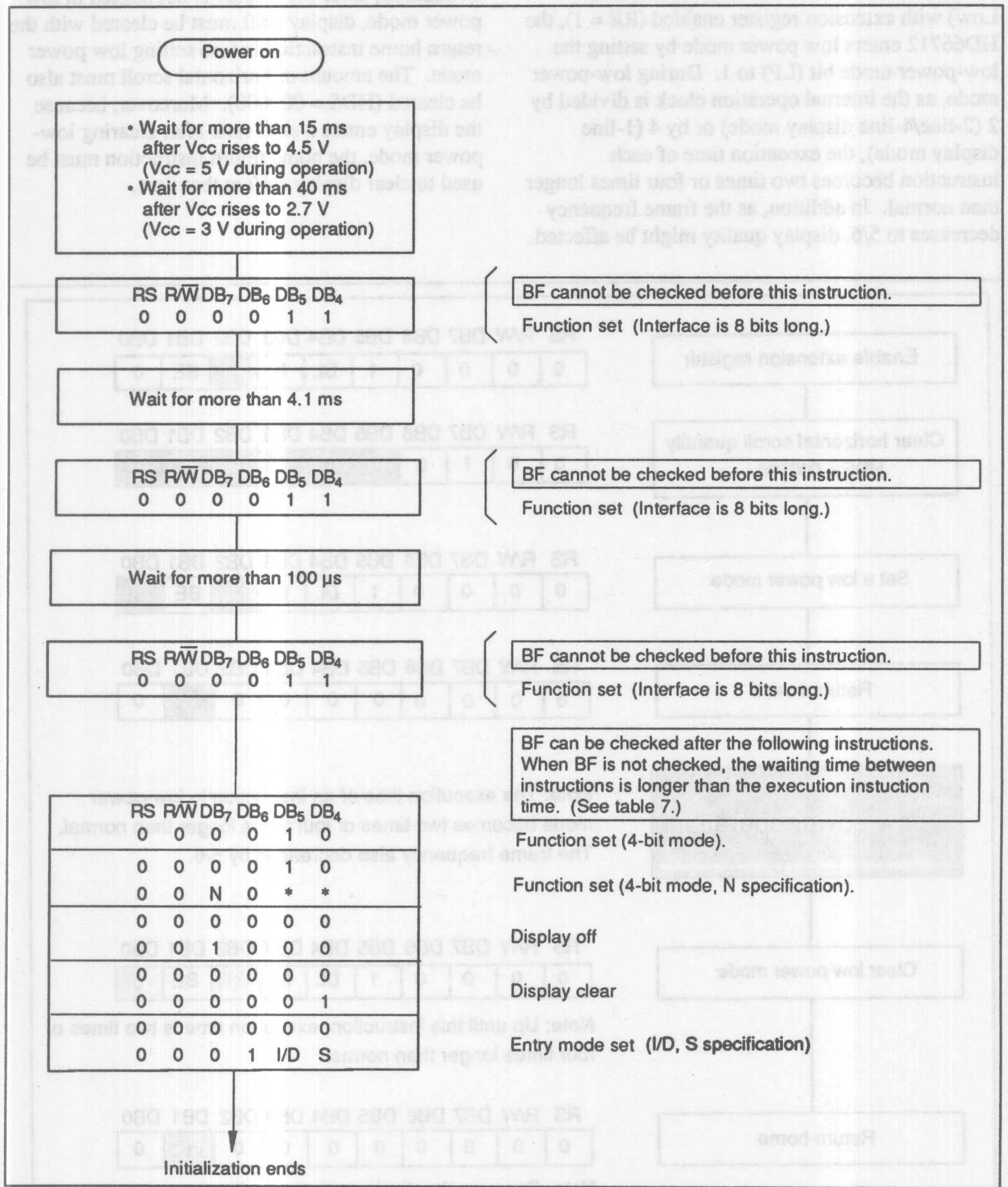


Figure 34 Initializing Flow of 4-Bit Interface

Low Power Mode

When the extension driver is not used (EXT = Low) with extension register enabled (RE = 1), the HD66712 enters low power mode by setting the low-power mode bit (LP) to 1. During low-power mode, as the internal operation clock is divided by 2 (2-line/4-line display mode) or by 4 (1-line display mode), the execution time of each instruction becomes two times or four times longer than normal. In addition, as the frame frequency decreases to 5/6, display quality might be affected.

In addition, since the display is not shifted in low power mode, display shift must be cleared with the return home instruction before setting low power mode. The amount of horizontal scroll must also be cleared (HDS = 000000). Moreover, because the display enters a shift state after clearing low-power mode, the home return instruction must be used to clear display shift at that time.

Enable extension register

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	1	BE	0

Clear horizontal scroll quantity HDS = 000000

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	0

Set a low power mode

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	1	BE	1

Return home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	0

Low power operation

Note: The execution time of an instruction in low-power mode becomes two times or four times longer than normal. The frame frequency also decreases by 5/6.

Clear low power mode

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	1	BE	0

Note: Up until this instruction, execution time is two times or four times longer than normal.

Return home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	0

Note: Because the display enters a shift state, be sure to execute this instruction.

Figure 38 Usage of Low Power Mode

Absolute Maximum Ratings*

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	1
Power supply voltage (2)	V_{CC}–V_5	V	–0.3 to +15.0	1, 2
Input voltage	V_t	V	–0.3 to V_{CC} +0.3	1
Operating temperature	T_{opr}	°C	–20 to +75	3
Storage temperature	T_{stg}	°C	–55 to +125	4

Note: If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C*3)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC_1)	V_{IH1}	0.7V_{CC}	—	V_{CC}	V		6
Input low voltage (1) (except OSC_1)	V_{IL1}	–0.3	—	0.2V_{CC}	V	V_{CC} = 2.7 to 3.0 V	6
		–0.3	—	0.6	V	V_{CC} = 3.0 to 4.5 V	
Input high voltage (2) (OSC_1)	V_{IH2}	0.7V_{CC}	—	V_{CC}	V		15
Input low voltage (2) (OSC_1)	V_{IL2}	—	—	0.2V_{CC}	V		15
Output high voltage (1) (D_0–D_7)	V_{OH1}	0.75V_{CC}	—	—	V	$-I_{OH}$ = 0.1 mA	7
Output low voltage (1) (D_0–D_7)	V_{OL1}	—	—	0.2V_{CC}	V	I_{OL} = 0.1 mA	7
Output high voltage (2) (except D_0–D_7)	V_{OH2}	0.8V_{CC}	—	—	V	$-I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except D_0–D_7)	V_{OL2}	—	—	0.2V_{CC}	V	I_{OL} = 0.04 mA	8
Driver ON resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA (COM)	13
Driver ON resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA (SEG)	13
I/O leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (RESET* pin)	–Ip	10	50	120	µA	V_{CC} = 3 V	
Power supply current	Icc	—	T.B.D.	T.B.D.	mA	R_f oscillation, external clock V_{CC} = 3V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD1}	3.0	—	13.0	V	V_{CC}–V_5, 1/5 bias	16
	V_{LCD2}	3.0	—	13.0	V	V_{CC}–V_5, 1/4 bias	16

Note: * Refer to Electrical Characteristics Notes following these tables.

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Output voltage (V5OUT2 pin)	V_{UP2}	—	TBD	—	V	V_{ci} = 4.5 V, I_O = 0.5 mA, T_a = 25°C	18
Output voltage (V5OUT3 pin)	V_{UP3}	—	TBD	—	V	V_{ci} = 3 V, I_O = 0.3 mA, T_a = 25°C	18
Input voltage	V_{CI}	2.5	—	4.5	V		18

AC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C*3)

Clock Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C*3)

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	125	270	410	kHz		11
	External clock duty	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{fcp}	—	—	0.2	µs		
R_f oscillation	Clock oscillation frequency	f_{OSC}	190	270	350	kHz	R_f = 75 kΩ, V_{CC} = 3 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

System Interface Timing Characteristics (1) (V_{CC} = 2.7 V to 4.5 V, T_a = –20 to +75° C*3)

Bus Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 39
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/W to E)	t_{AS}	T.B.D	—	—		
Address hold time	t_{AH}	20	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Bus Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 40
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/W to E)	t_{AS}	T.B.D	—	—		
Address hold time	t_{AH}	20	—	—		
Data delay time	t_{DDR}	—	—	360		
Data hold time	t_{DHR}	5	—	—		

Serial Interface Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	1	—	20	µs	Figure 41
Serial clock (high level width)	t_{SCH}	400	—	—	ns	
Serial clock (low level width)	t_{SCL}	400	—	—		
Serial clock rise/fall time	t_{SCr}, t_{SCf}	—	—	50		
Chip select set-up time	t_{CSU}	T.B.D	—	—		
Chip select hold time	t_{CH}	T.B.D	—	—		
Serial input data set-up time	t_{SISU}	200	—	—		
Serial input data hold time	t_{SIH}	200	—	—		
Serial output data delay time	t_{SOD}	—	—	360		
Serial output data hold time	t_{SOH}	5	—	—		

System Interface Timing Characteristics (2) (V_{CC} = 4.5 V to 5.5 V, T_a = –20 to +75° C[*3])

Bus Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 39
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/W to E)	t_{AS}	T.B.D	—	—		
Address hold time	t_{AH}	10	—	—		
Data set-up time	t_{DSW}	60	—	—		
Data hold time	t_H	10	—	—		

Bus Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 40
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/W to E)	t_{AS}	T.B.D	—	—		
Address hold time	t_{AH}	10	—	—		
Data delay time	t_{DDR}	—	—	160		
Data hold time	t_{DHR}	5	—	—		

Serial Interface Sequence

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	0.5	—	20	µs	Figure 41
Serial clock (high level width)	t_{SCH}	200	—	—	ns	
Serial clock (low level width)	t_{SCL}	200	—	—		
Serial clock rise/fall time	t_{SCr}, t_{SCf}	—	—	50		
Chip select set-up time	t_{CSU}	T.B.D	—			
Chip select hold time	t_{CH}	T.B.D	—	—		
Serial input data set-up time	t_{SISU}	100	—	—		
Serial input data hold time	t_{SIH}	100				
Serial output data delay time	t_{SOD}	—	—	160		
Serial output data hold time	t_{SOH}	5	—	—		

Segment Extension Signal Timing (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 42
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}		—	100		

Reset Timing (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	10	—	—	ms	Figure 43

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 44
Power supply off time	t_{OFF}	1	—	—		

Electrical Characteristics Notes

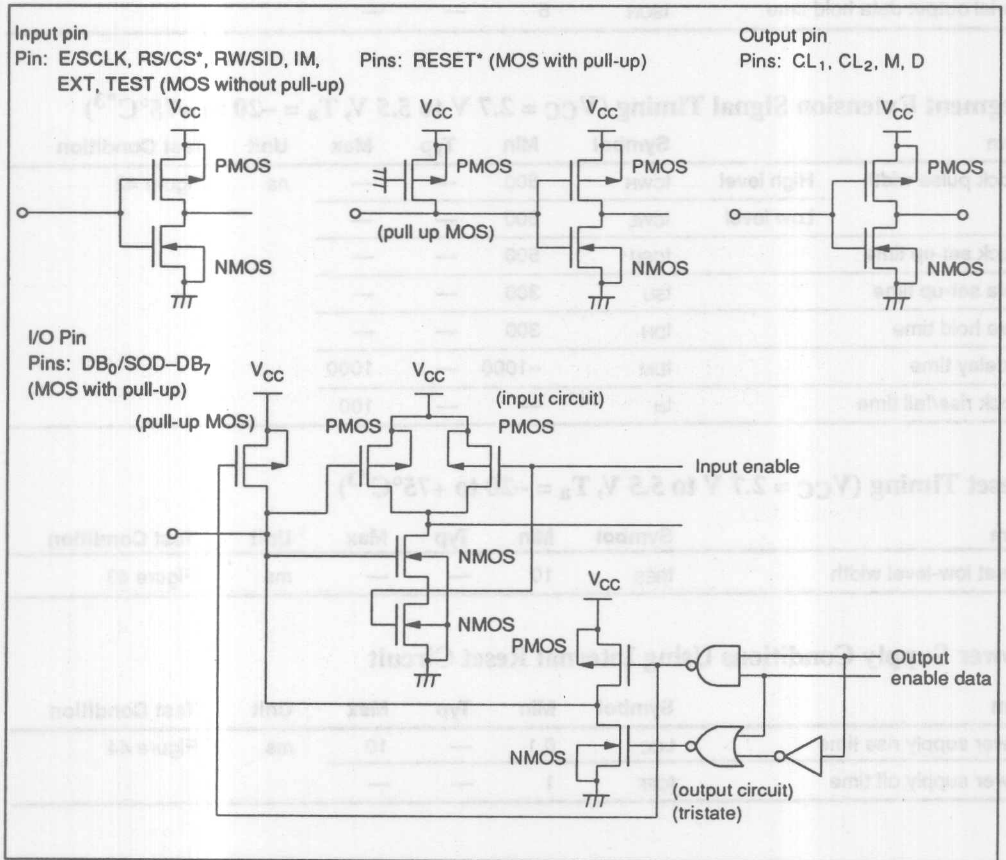
1. All voltage values are referred to GND = 0 V. If the LSI is used above the absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic is strongly recommended to ensure normal operation. If these electrical characteristic are also exceeded, the LSI may malfunction or exhibit poor reliability.

2. $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ must be maintained.

3. For die products, specified up to 75°C.

4. For die products, specified by the die shipment specification.

5. The following four circuits are I/O pin configurations except for liquid crystal display output.



6. Applies to input pins and I/O pins, excluding the OSC_1 pin.

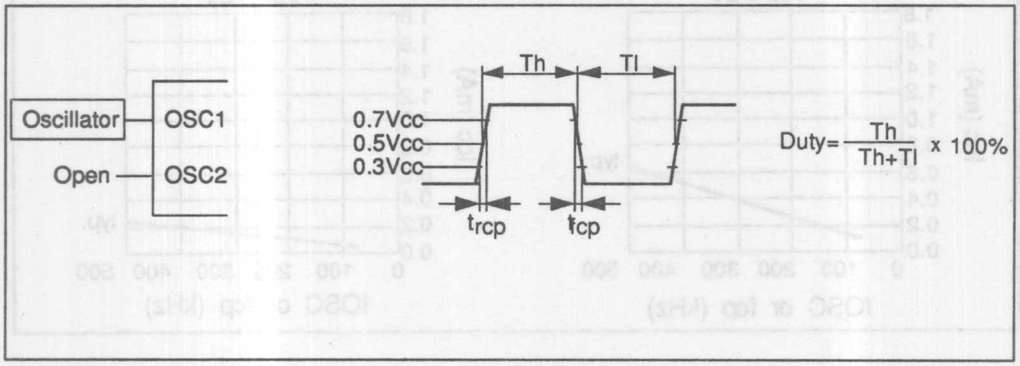
7. Applies to I/O pins.

8. Applies to output pins.

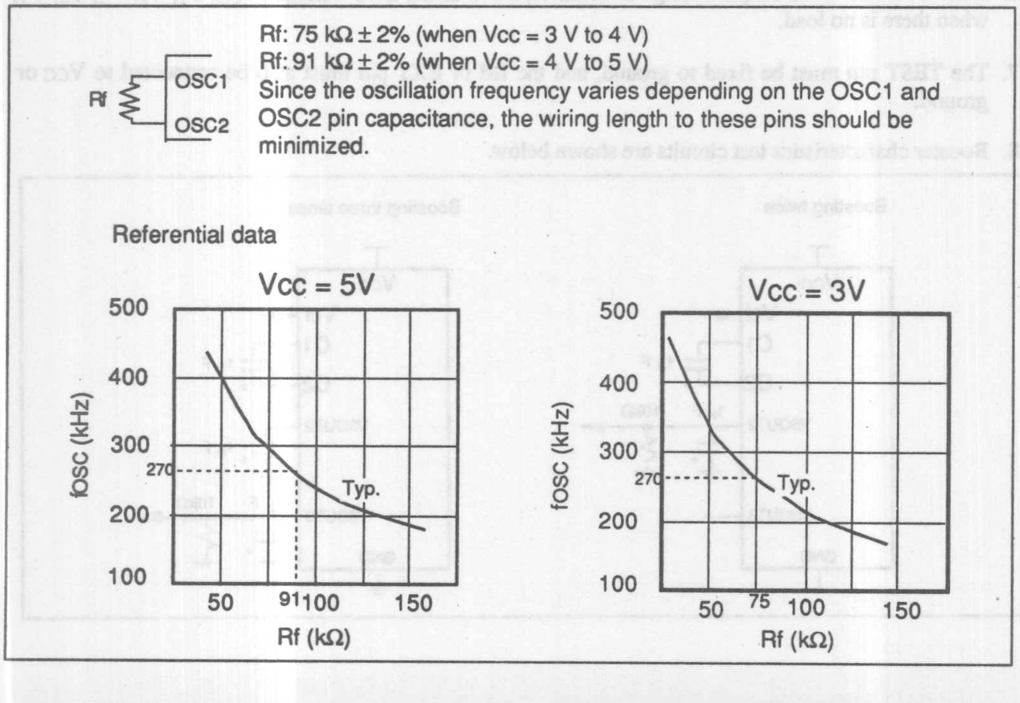
9. Current flowing through pull-up MOSs, excluding output drive MOSs.

10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.

11. Applies only to external clock operation.



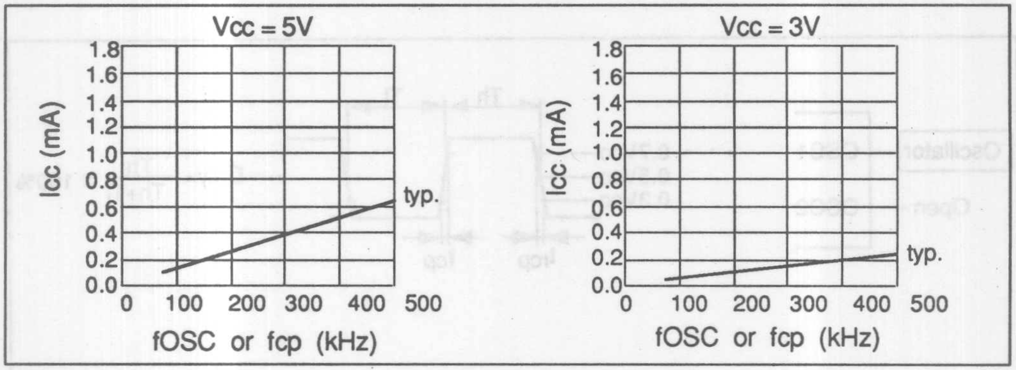
12. Applies only to the internal oscillator operation using oscillation resistor R_f.



13. R_{COM} is the resistance between the power supply pins (V_{CC}, V_1, V_4, V_5) and each common signal pin (COM_0 to COM_{33}).

    R_{SEG} is the resistance between the power supply pins (V_{CC}, V_2, V_3, V_5) and each segment signal pin (SEG_1 to SEG_{60}).

14. The following graphs show the relationship between operation frequency and current consumption.

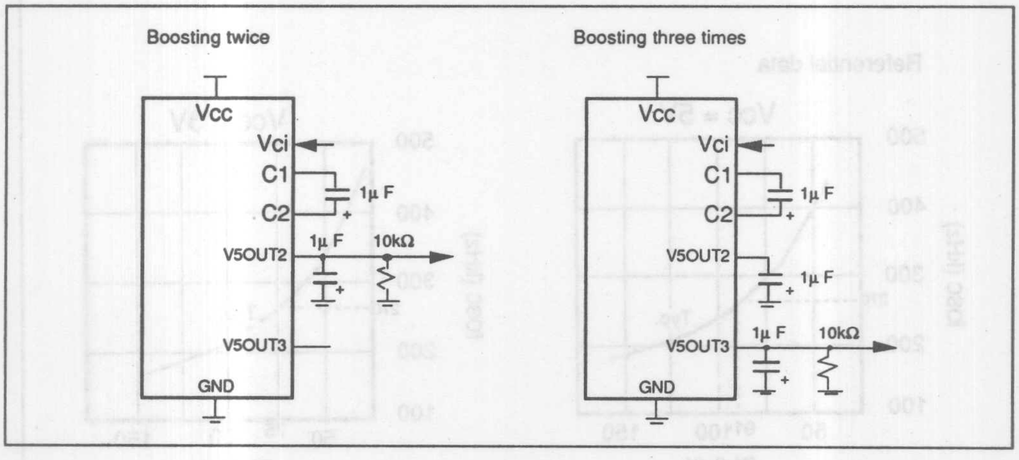


15. Applies to the OSC_1 pin.

16. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (V_{CC}, V_1, V_2, V_3, V_4, V_5) when there is no load.

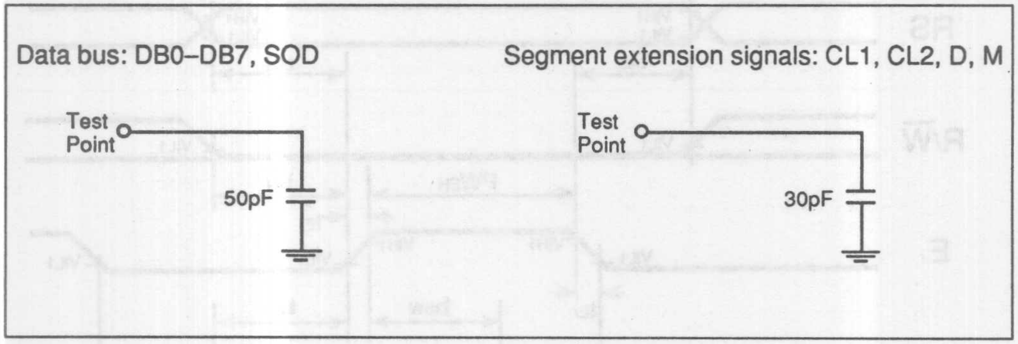
17. The TEST pin must be fixed to ground, and the IM or EXT pin must also be connected to V_{CC} or ground.

18. Booster characteristics test circuits are shown below.



Load Circuits

AC Characteristics Test Load Circuits



Timing Characteristics

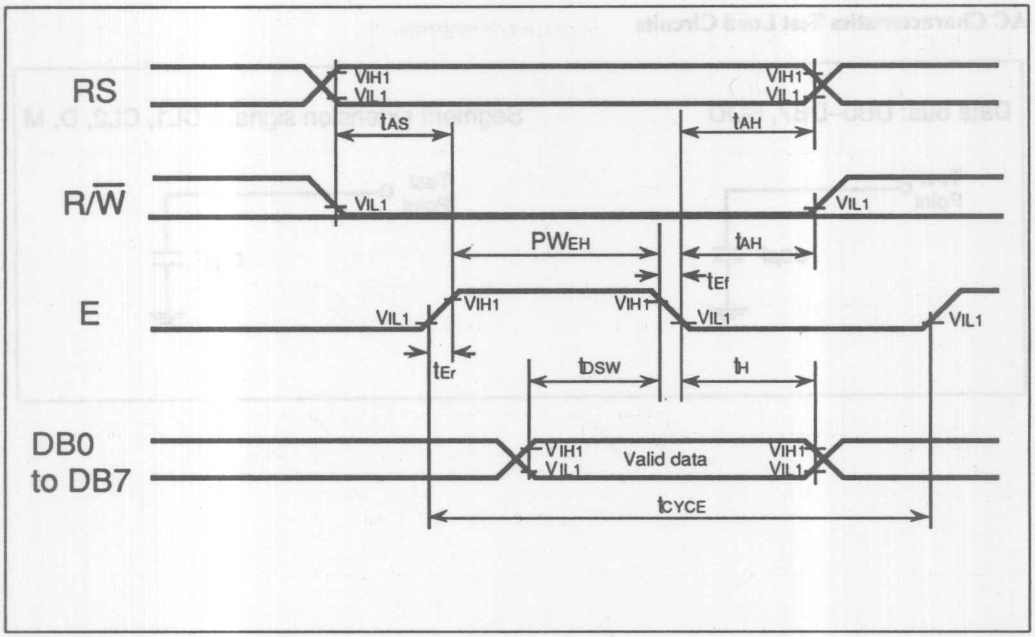


Figure 39 Bus Write Operation

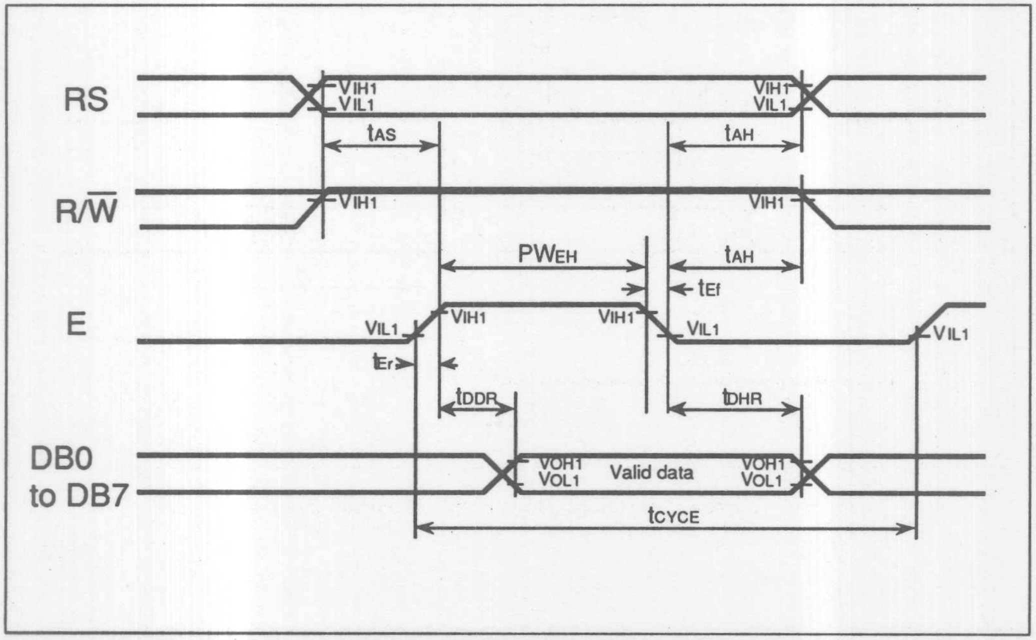


Figure 40 Bus Read Operation

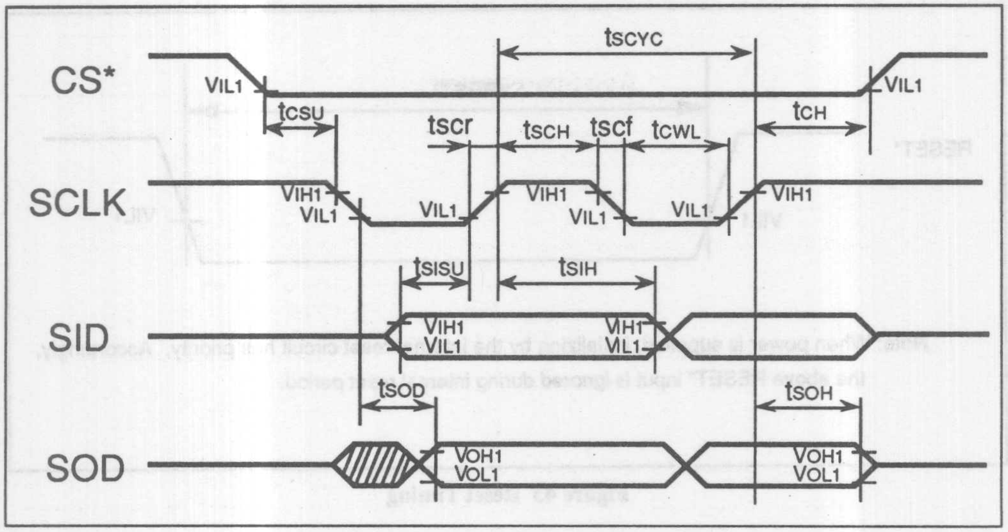


Figure 41 Serial Interface Timing

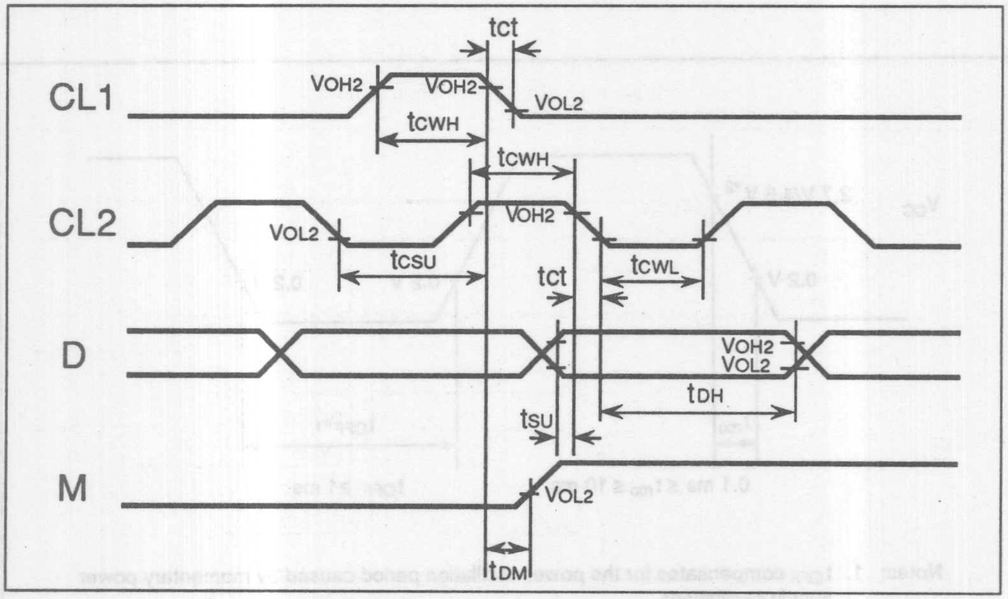
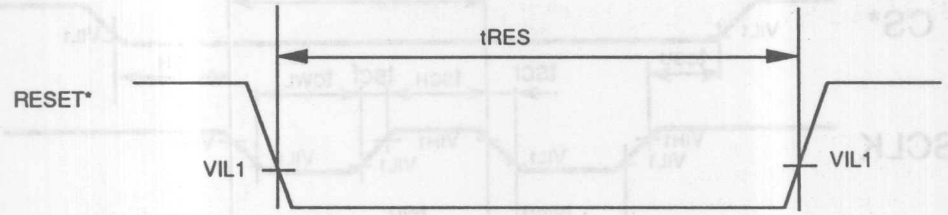
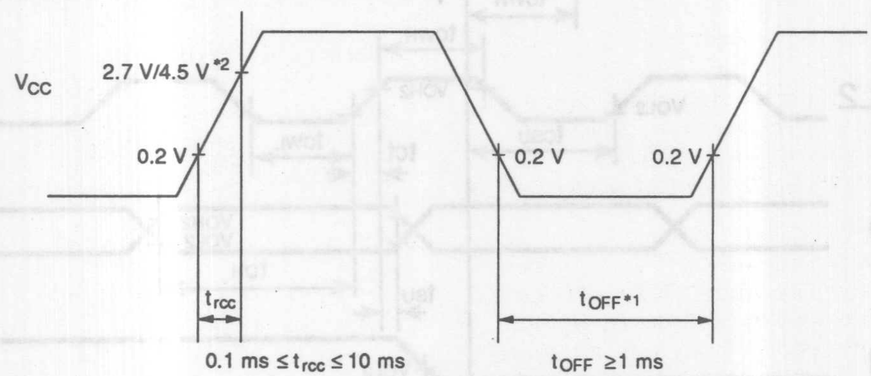


Figure 42 Interface Timing with Extension Driver



Note: When power is supplied, initializing by the internal reset circuit has priority. Accordingly, the above RESET* input is ignored during internal reset period.

Figure 43 Reset Timing



Notes: 1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for 5-volt operation, and at 2.7 V for 3-volt operation.
3. If the above electrical conditions are not satisfied, the internal reset circuit will not operate normally. In this case, initialize by instruction. (Refer to Initializing by Instruction.)

Figure 44 Power Supply Sequemce

HD44102

(Dot Matrix Liquid Crystal Graphic Display Column Driver)

Description

The HD44102CH is a column (segment) driver for dot matrix liquid crystal graphic display systems, storing the display data transferred from a 4-bit or 8-bit microcomputer in the internal display RAM and generating dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to on/off state of each dot of a liquid crystal display to provide more flexible than character display.

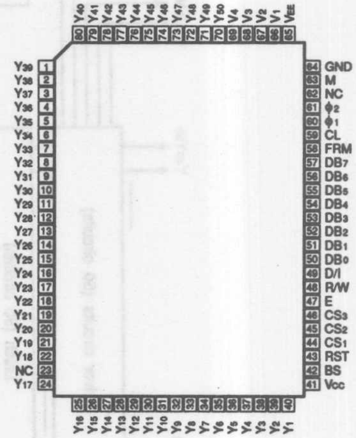
The HD44102CH is produced by the CMOS process. Therefore, the combination of HD44102CH with a CMOS microcontroller can complete portable battery-driven unit ntilizing the liquid crystal display's low power dissipation.

The combination of HD44102CH with the row (common) driver HD44103CH facilitates dot matrix liquid crystal graphic display system configuration.

Features

- Dot matrix liquid crystal graphic display column driver incorporating display RAM
- Interfaces with 4-bit or 8-bit MPU
- RAM data directly displayed by internal display RAM
  - RAM bit data 1: On
  - RAM bit data 0: Off
- Display RAM capacity: $50 \times 8 \times 4$ (1600 bits)
- Internal liquid crystal display driver circuit (segment output): 50 segment signal drivers
- Duty factor (can be controlled by external input waveform)
  - Selectable duty factors: 1/8, 1/12, 1/16, 1/24, 1/32
- Wide range of instruction functions
  - Display Data Read/Write, Display On/Off, Set Address, Set Display
  - Start Page, Set Up/Down, Read Status
- Low power dissipation
- Power supplies: V_{CC} 5 V ± 10%, V_{EE} 0 to –5 V
- CMOS process

Pin Arrangement

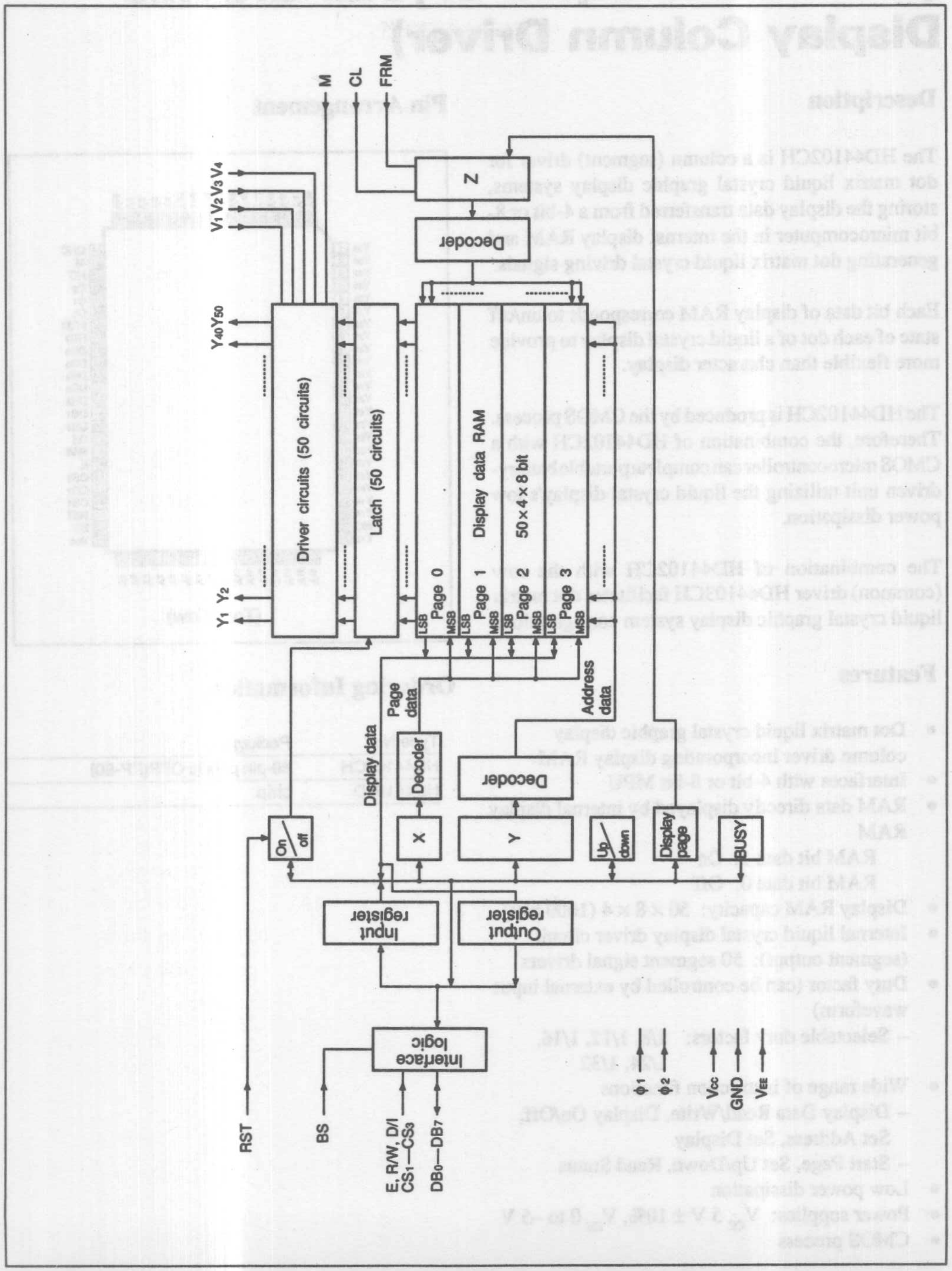


(Top-View)

Ordering Information

Type No.	Package
HD44102CH	80-pin plastic OFP(FP-80)
HD44102D	chip

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V	1
Supply voltage (2)	V_{EE}	V_{CC} –13.5 to V_{CC} + 0.3	V	
Input voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (2)	V_{T2}	V_{EE} –0.3 to V_{CC} + 0.3	V	3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. Referenced to GND = 0.
2. Applied to input terminals (except V1, V2, V3, and V4), and I/O common terminals.
3. Applied to terminals V1, V2, V3, and V4.

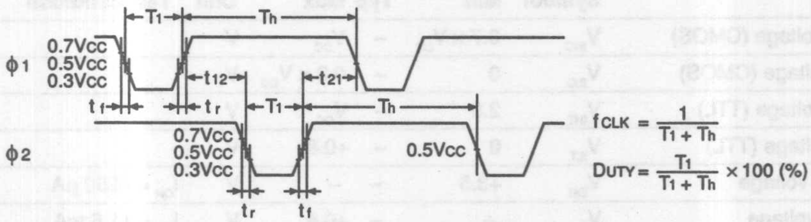
Electrical Characteristics

(V_{CC} = +5 V ±10%, GND = 0 V, V_{EE} = 0 to –5.5 V, Ta = –20 to 75 °C) (Note 4)

Item	Symbol	Min	Typ	Max	Unit	Test condition	Notes
Input high voltage (CMOS)	V_{IHC}	0.7 × V_{CC}	–	V_{CC}	V		5
Input low voltage (CMOS)	V_{ILC}	0	–	0.3 × V_{CC}	V		5
Input high voltage (TTL)	V_{IHT}	2.0	–	V_{CC}	V		6
Input low voltage (TTL)	V_{ILT}	0	–	+0.8	V		6
Output high voltage	V_{OH}	+3.5	–	–	V	I_{OH} = –250 µA	7
Output low voltage	V_{OL}	–	–	+0.4	V	I_{OL} = +1.6 mA	7
Vi-Xj ON resistance	R_{ON}	–	–	7.5	kΩ	V_{EE} = –5 V ± 10%, Load current 100 µA	
Input leakage current (1)	I_{IL1}	–1	–	1	µA	V_{IN} = V_{CC} to GND	8
Input leakage current (2)	I_{IL2}	–2	–	2	µA	V_{IN} = V_{CC} to V_{EE}	9
Operating frequency	f_{CLK}	25	–	280	kHz	ϕ1, ϕ2 frequency	10
Dissipation current (1)	I_{CC1}	–	–	100	µA	f_{clk} = 200 kHz frame = 65 Hz during display	11
Dissipation current (2)	I_{CC2}	–	–	500	µA	Access cycle 1 MHz at access	12

Notes: 4. Specified within this range unless otherwise noted.
5. Applied to M, FRM, CL, BS, RST,ϕ1, ϕ2.
6. Applied to CS1 to CS3, E, D/I, R/W and DBO to DB7.
7. Applied to DB0 to DB7.
8. Applied to input terminals, M, FRM,CL, BS, RST, ϕ1, ϕ2, CS1 to CS3, E, D/I and R/W, and I/O common terminals DB0 to DB7 at high impedance.
9. Applied to V1, V2, V3, and V4.
10. ϕ1 and ϕ2 AC characteristics.

	Symbol	Min	Typ	Max	Unit
Duty factor	Duty	20	25	30	%
Fall time	t_f	–	–	100	ns
Rise time	t_r	–	–	100	ns
Phase difference time	t_{12}	0.8	–	–	µs
Phase difference time	t_{21}	0.8	–	–	µs
$T_1 + T_h$		–	–	40	µs



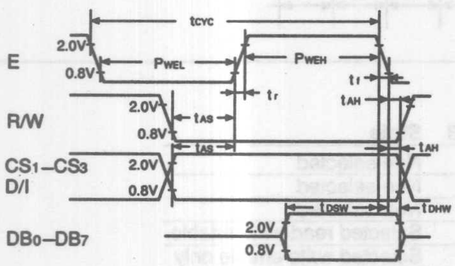
11. Measured by V_{CC} terminal at no output load, at 1/32 dury factor, and frame frequency of 65 Hz, in checker pattern display. Access from the CPU is stopped.
12. Measured by V_{CC} terminal at no output load, 1/32 duty factor and frame frequency of 65 Hz.

Interface AC Characteristics

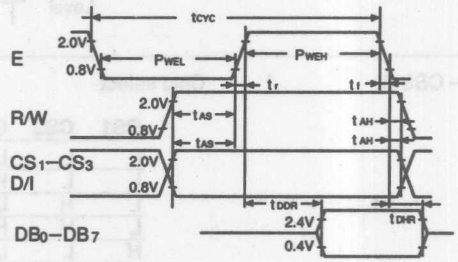
Item	Symbol	Min	Typ	Max	Unit	Notes
E cycle time	t_{CYC}	1000	–	–	ns	13, 14
E high level width	P_{WEH}	450	–	–	ns	13, 14
E low level width	P_{WEL}	450	–	–	ns	13, 14
E rise time	t_r	–	–	25	ns	13, 14
E fall time	t_f	–	–	25	ns	13, 14
Address setup time	t_{AS}	140	–	–	ns	13, 14
Address hold time	t_{AH}	10	–	–	ns	13, 14
Data setup time	t_{DSW}	200	–	–	ns	13
Data delay time	t_{DDR}	–	–	320	ns	14, 15
Data hold time at write	t_{DHW}	10	–	–	ns	13
Data hold time at read	t_{DHR}	20	–	–	ns	14

Notes:

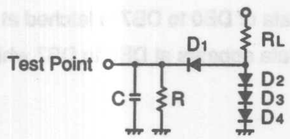
13. At CPU write



14. At CPU read



15. DB0 to DB7 load circuits



R_L = 2.4 kΩ

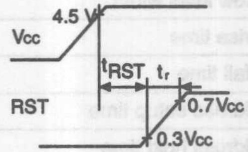
R = 11 kΩ

C = 130 pF (including jig capacitance)

Diodes D_1 to D_4 are all 1S2074 Ⓗ

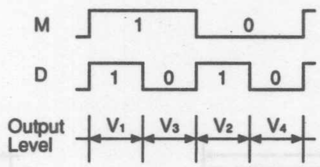
Notes: 16. Display off at initial power up.
The HD44102CH can be placed in the display off state by setting terminal RST to low at initial power up.
No instruction other than the Read Status can be accepted while the RST is at the low level.

	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	–	–	μs
Rise time	t_r	–	–	200	ns



Pin Description

Pin Name	Pin Number	I/O	Function
Y1 – Y50	50	O	Liquid crystal display drive output. Relationship among output level, M and display data (D):



Pin Name	Pin Number	I/O	Function
CS1 – CS3	3	I	Chip select

CS1	CS2	CS3	State
L	L	L	Non-selected
L	L	H	Non-selected
L	H	L	Non-selected
L	H	H	Selected read/write enable
H	L	L	Selected write enable only
H	L	H	Selected write enable only
H	H	L	Selected write enable only
H	H	H	Selected read/write enable

Pin Name	Pin Number	I/O	Function
E	1	I	Enable

At write (R/W = Low): Data of DB0 to DB7 is latched at the fall of E.

At read (R/W = High): Data appears at DB0 to DB7 while E is at high level.

Pin Name	Pin Number	I/O	Function
R/W	1	I	Read/Write R/W = High: Data appears at DB0 to DB7 and can be read by the CPU when E = high and CS2, CS3 = high. R/W = Low: DB0 to DB7 can accept input when CS2, CS3 = high or CS1 = high.
D/I	1	I	Data/Instruction D/I = High: Indicates that the data of DB0 to DB7 is display data. D/I = Low: Indicates that the data of DB0 to DB7 is display control data.
DB0–DB7	8	I/O	Data bus, three-state I/O common terminal
M	1	I	Signal to convert liquid crystal display drive output to AC.
CL	1	I	Display synchronous signal At the rise of CL signal, the liquid crystal display drive signal corresponding to display data appears.
FRM	1	I	Display synchronous signal (frame signal) This signal presets the 5-bit display line counter and synchronizes a common signal with the frame timing when the FRM signal becomes high.
$\phi 1$, $\phi 2$	2	I	2-phase clock signal for internal operation The $\phi 1$ and $\phi 2$ clocks are used to perform the operations (input/output of display data and execution of instructions) other than display.
RST	1	I	Reset signal The display disappears and Y address counter is set in the up counter state by setting the RST signal to low level. After releasing reset, the display off state and up mode is held until the state is changed by the instruction.
BS	1	I	Bus select signal BS = Low: DB0 to DB7 operate for 8–bit length. BS = High: DB4 to DB7 are valid for 4–bit length only. 8–bit data is accessed twice in the high and low order.
V1, V2, V3, V4	4		Power supply for liquid crystal display drive V1 and V2: Selection voltage V3 and V4: Non-selection voltage

DB0–DB7 states:

E	R/W	CS1	CS2	CS3	State of DB0 to DB7
H	H	*	H	H	Output state
*	L	H	*	*	Input state,
*	L	*	H	H	High impedance
Others					High impedance

Pin Name	Pin Number	I/O	Function
V_{CC}	3		Power supply
GND			V_{CC}–GND: Power supply for internal logic
V_{EE}			V_{CC}–V_{EE}: Power supply for liquid crystal display drive circuit logic

Function of Each Block

Interface Logic

The HD44102CH can use the data bus in 4-bit or 8-bit word length to enable interface to a 4-bit or 8-bit CPU.

1. 4 bit mode (BS = High)
   8-bit data is transferred twice for every 4 bits through the data bus when the BS signal is high.

The data bus uses the high order 4 bits (DB4 to DB7). First, the high order 4 bits (DB4 to DB7 in 8-bit data length) are transferred and then the low order 4 bits (DB0 to DB3 in 8-bit data length).

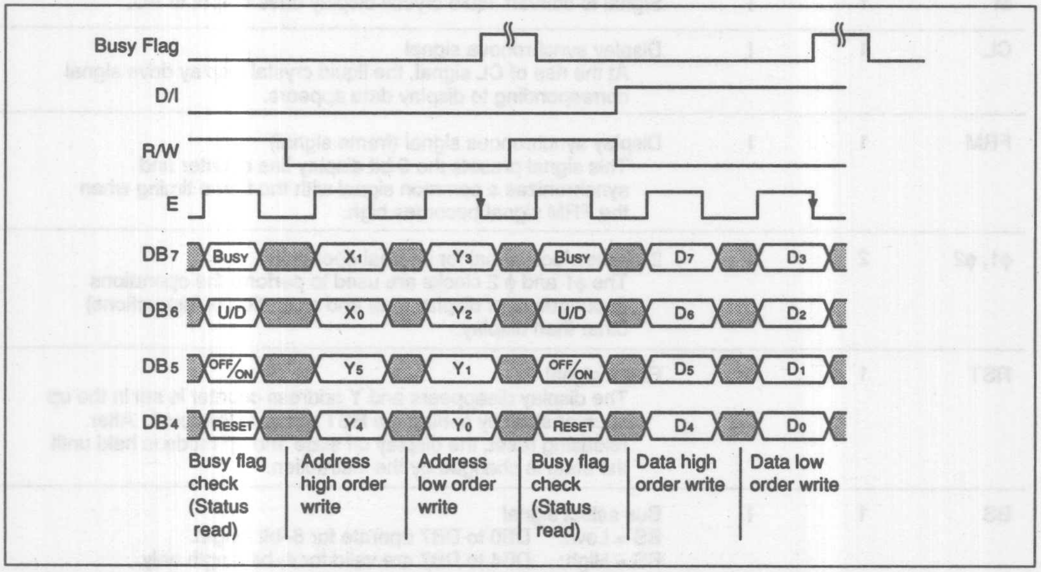


Figure 1 4-Bit Mode Timing

Note: Execute instructions other than status read in 4-bit length each. The busy flag is set at the fall of the second E signal. The status read is executed once. After the execution of the status read, the first 4 bits are considered the high order 4 bits. Therefore, if the busy flag is checked after the transfer of the high order 4 bits, retransfer data from the higher order bits. No busy check is required in the transfer between the high and low order bits.

2. 8-bit mode (BS = Low)

If the BS signal is low, the 8 data bus lines (DB0 to DB7) are used for data transfer.

DB7: MSB (Most significant bit)

DB0: LSB (Least significant bit)

For AC timing, refer to note 12 to note 15 of "Electrical Characteristics".

Input Register

8-bit data is written into this register by the CPU. The instruction and display data are distinguished by the 8-bit data and D/I signal and then a given operation is performed. Data is received at the fall of the E signal when the CS is in the select state and R/W is in write state.

Output Register

The output register holds the data read from the display data RAM. After display data is read, the display data at the address now indicated is set in this output register. After that, the address is increased or decreased by 1. Therefore, when an address is set, the correct data doesn't appear at the read of the first display data. The data at a specified address appears at the second read of data (figure 2).

X, Y Address Counter

The X, Y address counter holds an address for reading/writing display data RAM. An address is set in it by the instruction. The Y address register is composed of a 50-bit up/down counter. The address is increased or decreased by 1 by the read/write operation of display data. The up/down mode can be determined by the instruction or RST signal. The Y address register counts by looping the values of 0 to 49. The X address register has no count function.

Display On/Off Flip/Flop

This flip/flop is set to on/off state by the instruction or RST signal. In the off state, the latch of display data RAM output is held reset and the display data output is set to 0. Therefore, display disappears. In the on state, the display data appears according to the data in the RAM and is displayed. The display data in the RAM is independent of the display on/off.

Up/Down Flip/Flop

This flip/flop determines the count mode of the Y address counter. In the up mode, the Y address register is increased by 1. 0 follows 49. In the down mode, the register is decreased by 1. 0 is followed by 49.

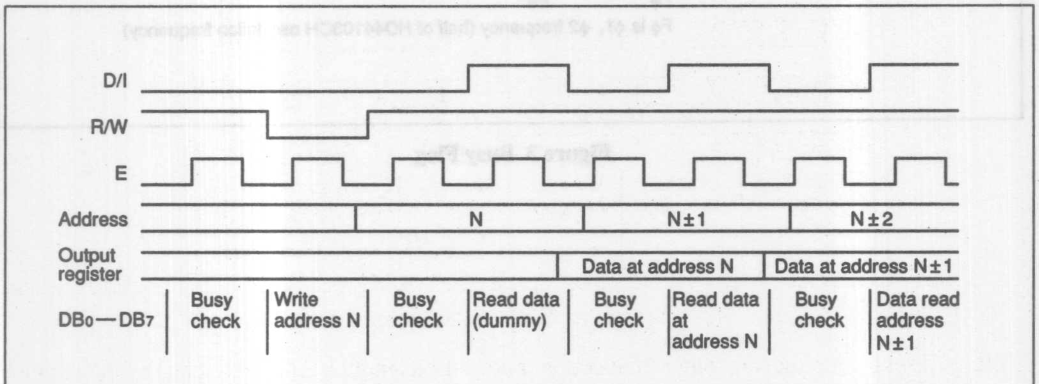


Figure 2 Data Output

Display Page Register

The display page register holds the 2-bit data that indicates a display start page. This value is preset to the high order 2 bits of the Z address counter by the FRM signal. This value indicates the value of the display RAM page displayed at the top of the screen.

Busy Flag

After an instruction other than status read is accepted, the busy flag is set during its effective period, and reset when the instruction is not effective (figure 3). The value can be read out on DB7 by the status read instruction.

The HD44102CH cannot accept any other instructions than the status read in the busy state. Make sure the busy flag is reset before issuing an instruction.

Z Address Counter

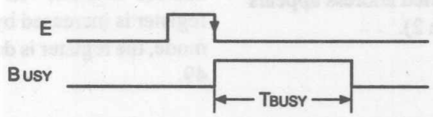
The Z address counter is a 5-bit counter that counts up at the fall of CL signal and generates an address for outputting the display data synchronized with the common signal. 0 is preset to the low order 3 bits and a display start page to the high order 2 bits by the FRM signal.

Latch

The display data from the display data RAM is latched at the rise of CL signal.

Liquid Crystal Driver Circuit

Each of 50 driver circuits is a multiplex circuit composed of 4 CMOS switches. The combination of display data from latchs and the M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.



$$\frac{1}{F\phi} \leqq T_{BUSY} \leqq \frac{3}{F\phi}$$

$F\phi$ is $\phi 1$, $\phi 2$ frequency (half of HD44103CH oscillation frequency)

Figure 3 Busy Flag

Display RAM

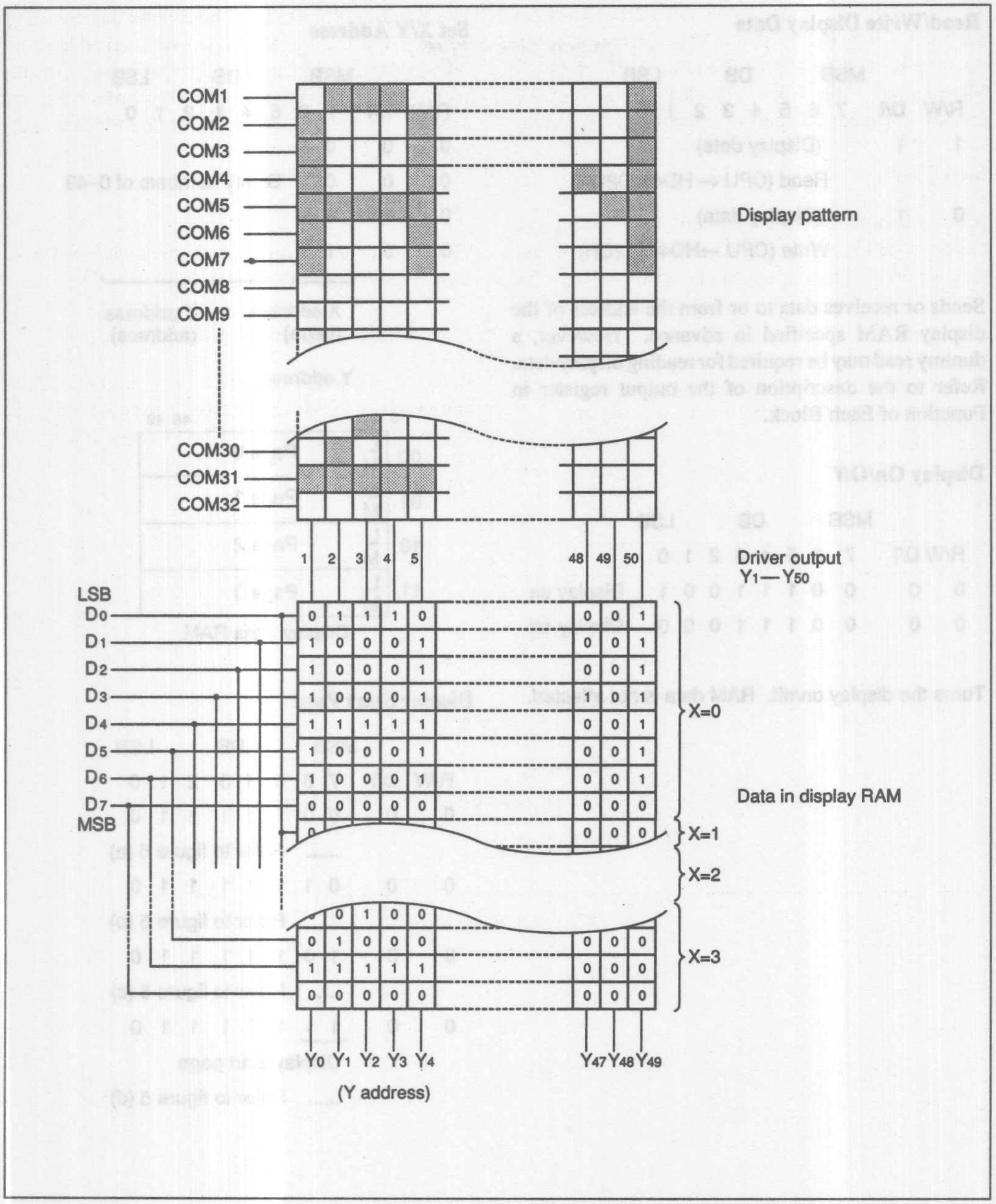


Figure 4 Relationship between Data in RAM and Display (Display start page 0, 1/32 duty)

Display Control Instructions

Read/Write Display Data

R/W	D/I	7 (MSB)	6	5	4 (DB)	3	2	1	0 (LSB)	
1	1	(Display data)								Read (CPU ← HD44102CH)
0	1	(Display data)								Write (CPU →HD44102CH)

Sends or receives data to or from the address of the display RAM specified in advance. However, a dummy read may be required for reading display data. Refer to the description of the output register in Function of Each Block.

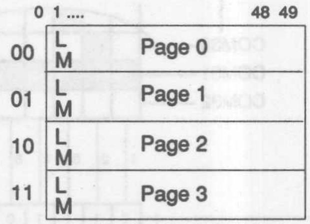
Display On/Off

R/W	D/I	7 (MSB)	6	5	4 (DB)	3	2	1	0 (LSB)	
0	0	0	0	1	1	1	0	0	1	Display on
0	0	0	0	1	1	1	0	0	0	Display off

Turns the display on/off. RAM data is not affected.

Set X/Y Address

R/W	D/I	7 (MSB)	6	5	4 (DB)	3	2	1	0 (LSB)
0	0	0	0	Binary numbers of 0–49					
0	0	0	1						
0	0	1	0						
0	0	1	1						
		X address (page)		Y address (address)					



Display Data RAM

Display Start Page

R/W	D/I	7 (MSB)	6	5	4 (DB)	3	2	1	0 (LSB)	
0	0	0	0	1	1	1	1	1	0	...... Refer to figure 5 (a)
0	0	0	1	1	1	1	1	1	0	...... Refer to figure 5 (b)
0	0	1	0	1	1	1	1	1	0	...... Refer to figure 5 (c)
0	0	1	1	1	1	1	1	1	0	...... Refer to figure 5 (d)
		Display start page								

Specifies the RAM page displayed at the top of the screen. Display is as shown in figure 4. When the display duty factor is more than 1/32 (For example, 1/24, 1/16), display begins at a page specified by the display start page only by the number of lines.

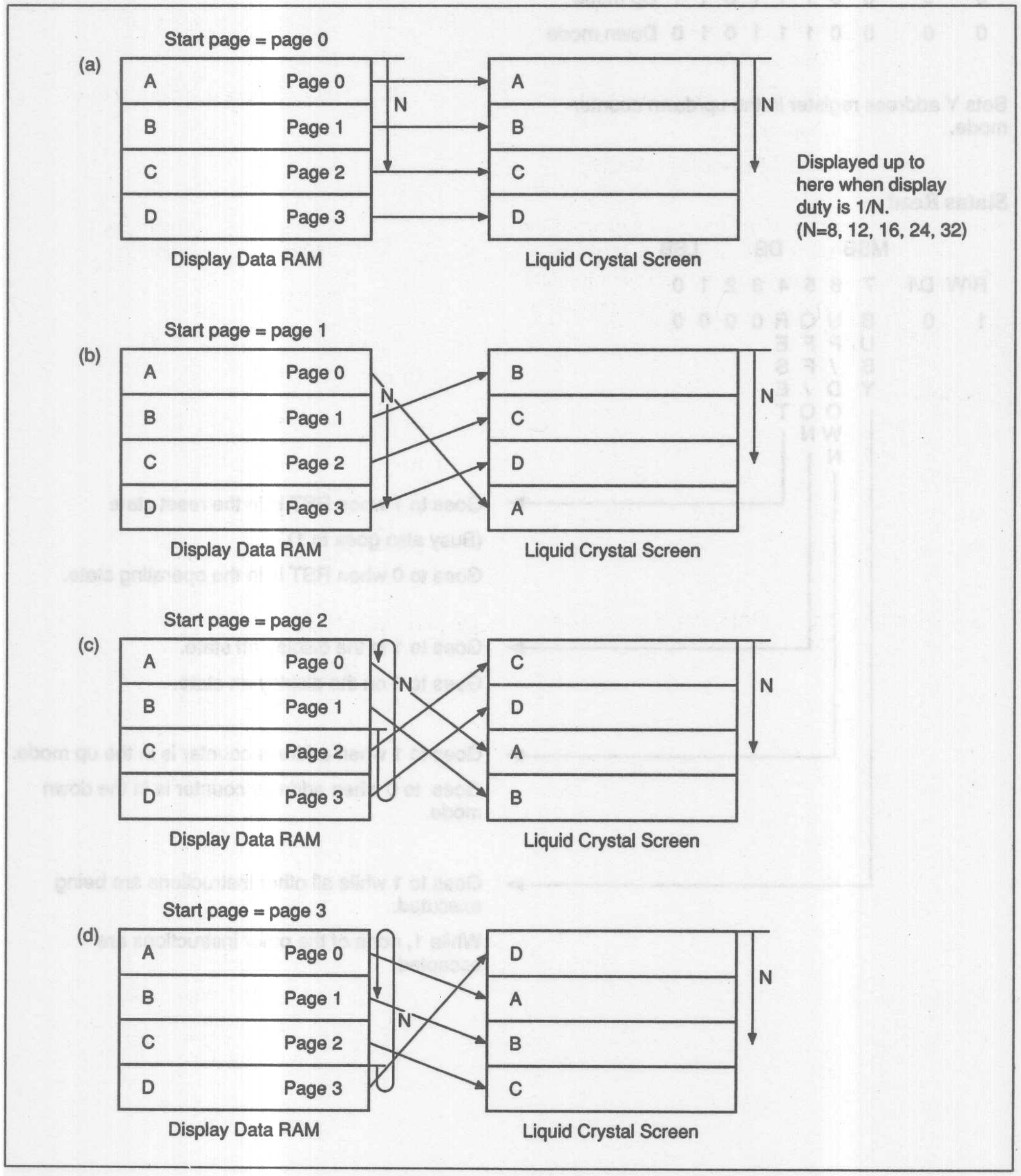


Figure 5 Display Start Page

Up/Down Set

R/W	D/I	MSB 7	6	5	DB 4	3	2	1	LSB 0	
0	0	0	0	1	1	1	0	1	1	Up mode
0	0	0	0	1	1	1	0	1	0	Down mode

Sets Y address register in the up/down counter mode.

Status Read

R/W	D/I	MSB 7	6	5	DB 4	3	2	1	LSB 0
1	0	BUSY	UP/DOWN	OFF/ON	RESET	0	0	0	0

Goes to 1 when RST is in the reset state (Busy also goes to 1).
Goes to 0 when RST is in the operating state.

Goes to 1 in the display off state.
Goes to 0 on the display on state.

Goes to 1 when address counter is in the up mode.
Goes to 0 when address counter is in the down mode.

Goes to 1 while all other instructions are being executed.
While 1, none of the other instructions are accepted.

Connection Between LCD Drivers (Example of 1/32 Duty Factor)

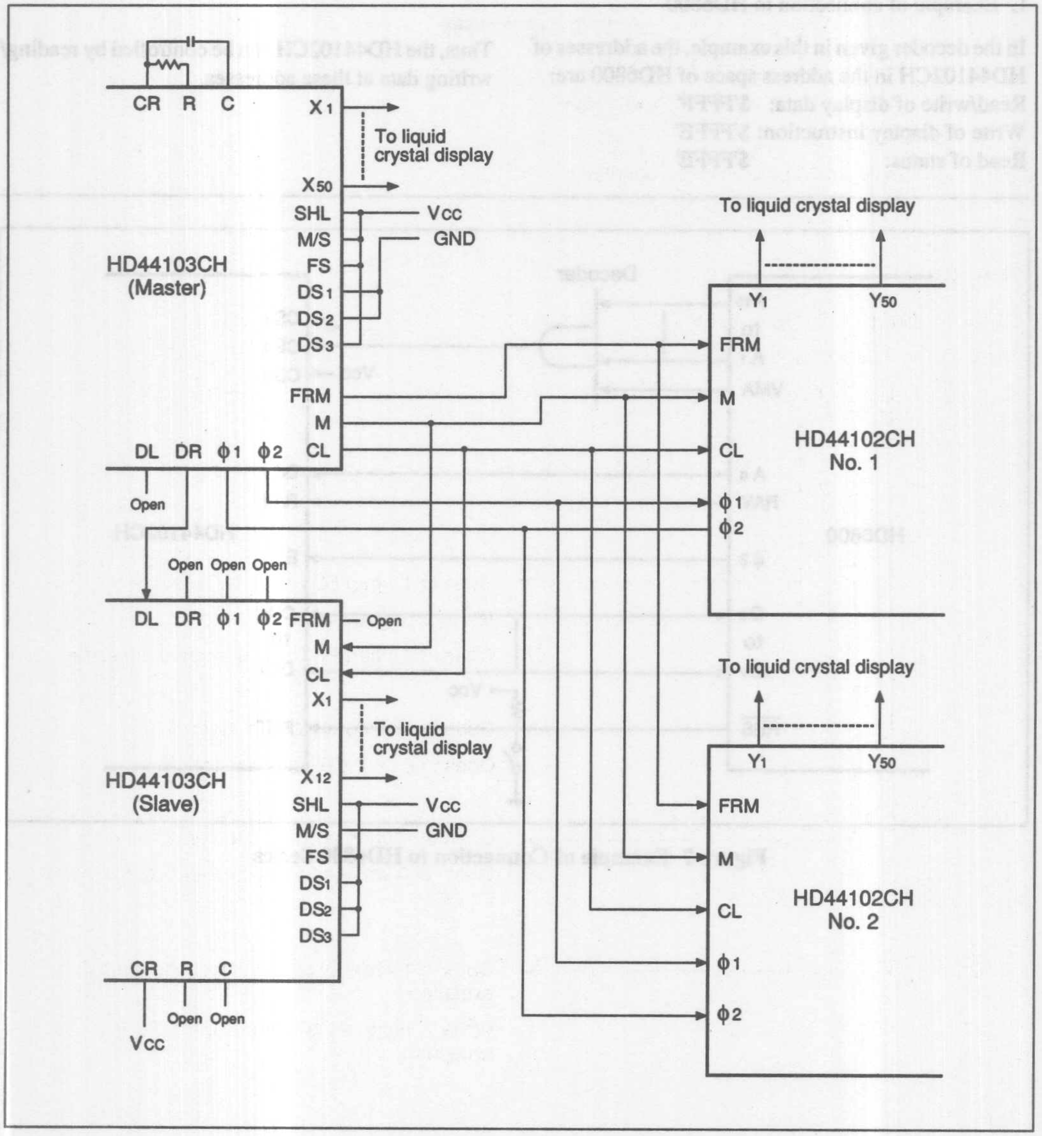


Figure 6 1/32 Duty Factor Connection Example

Interface to CPU

1. Example of connection to HD6800

In the decoder given in this example, the addresses of HD44102CH in the address space of HD6800 are:
Read/write of display data: $'FFFF'
Write of display instruction: $'FFFE'
Read of status: $'FFFE'

Thus, the HD44102CH can be controlled by reading/writing data at these addresses.

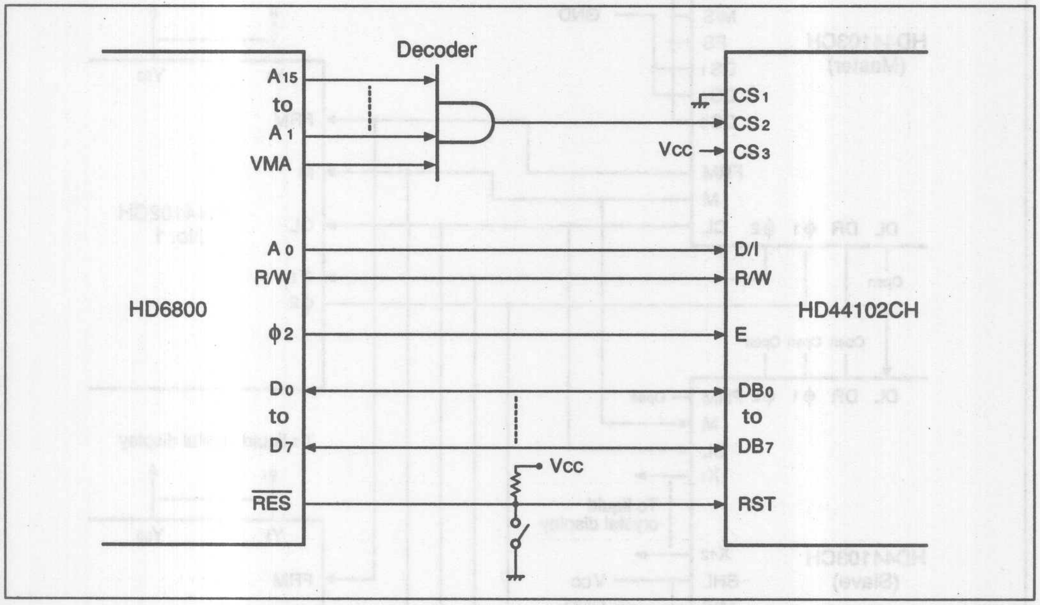


Figure 7 Example of Connection to HD6800 Series

2. Example of connection to HD6801

- The HD6801 is set to mode 5. P10–P14 are used as output ports, and P30–P37 are used as the data bus.
- The 74LS154 is a 4–to–16 decoder that decodes 4 bits of P10–P13 to select the chips.
- Therefore, the HD44102CH can be controlled by selecting the chips through P10–P13 and specifying the D/I signal through P14 in advance, and later conducting memory read or write for external memory space $0100 to $01FF of HD6801. The IOS signal is output to SC1, and the R/W signal is output to SC2.
- For further details on HD6800 and HD6801, refer to their manuals.

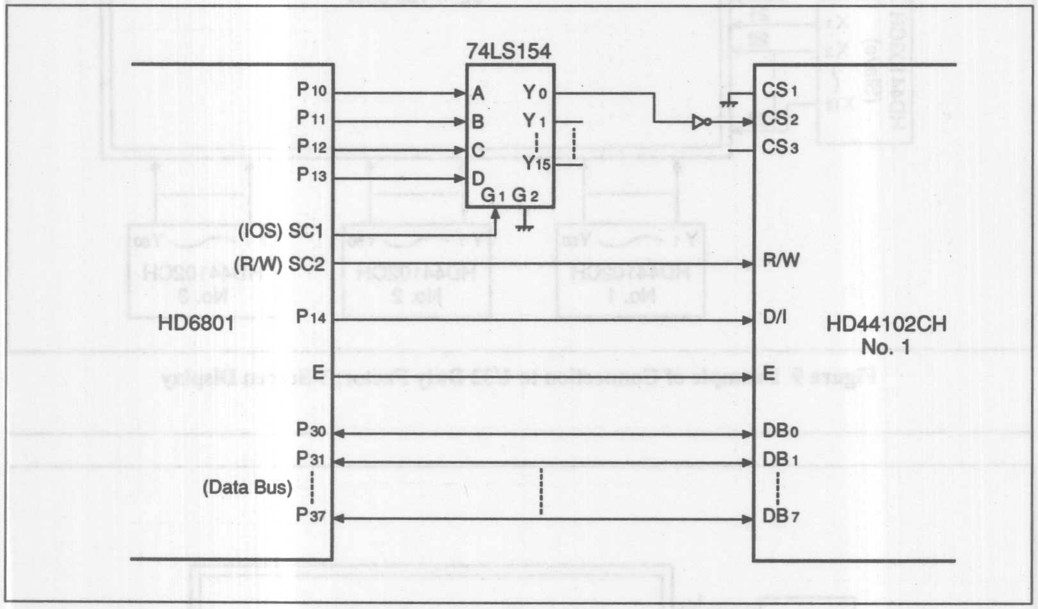


Figure 8 Example of Connection to HD6801

Connection to Liquid Crystal Display

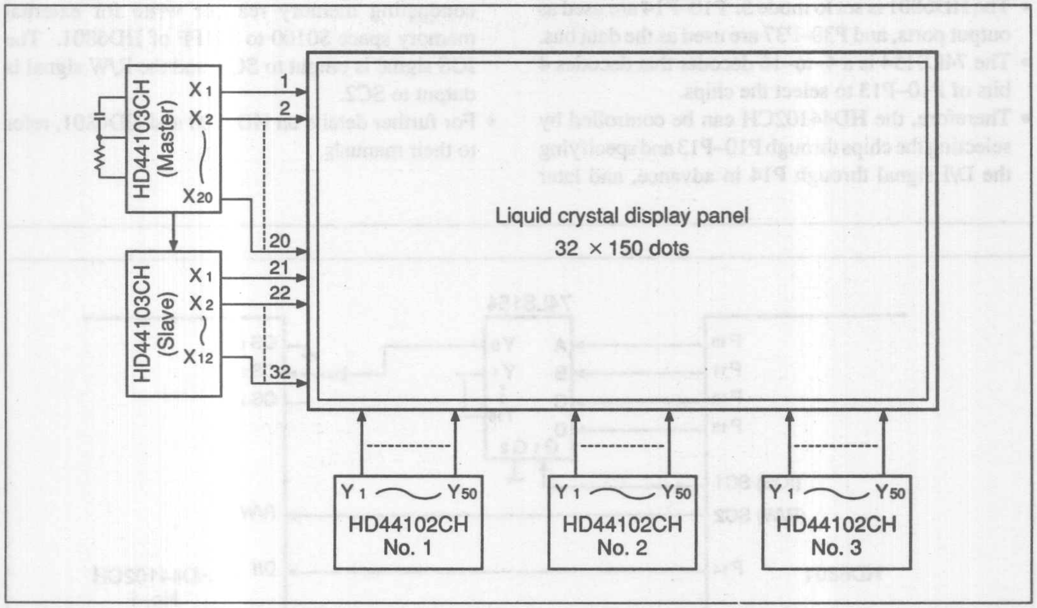


Figure 9 Example of Connection to 1/32 Duty Factor, 1-Screen Display

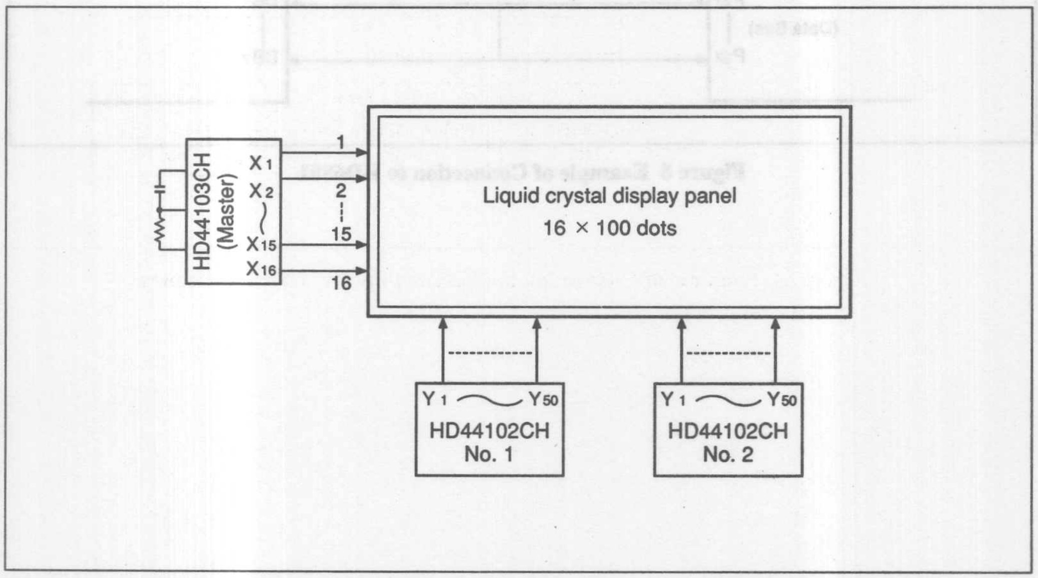


Figure 10 Example of Connection to 1/16 Duty Factor, 1–Screen Display

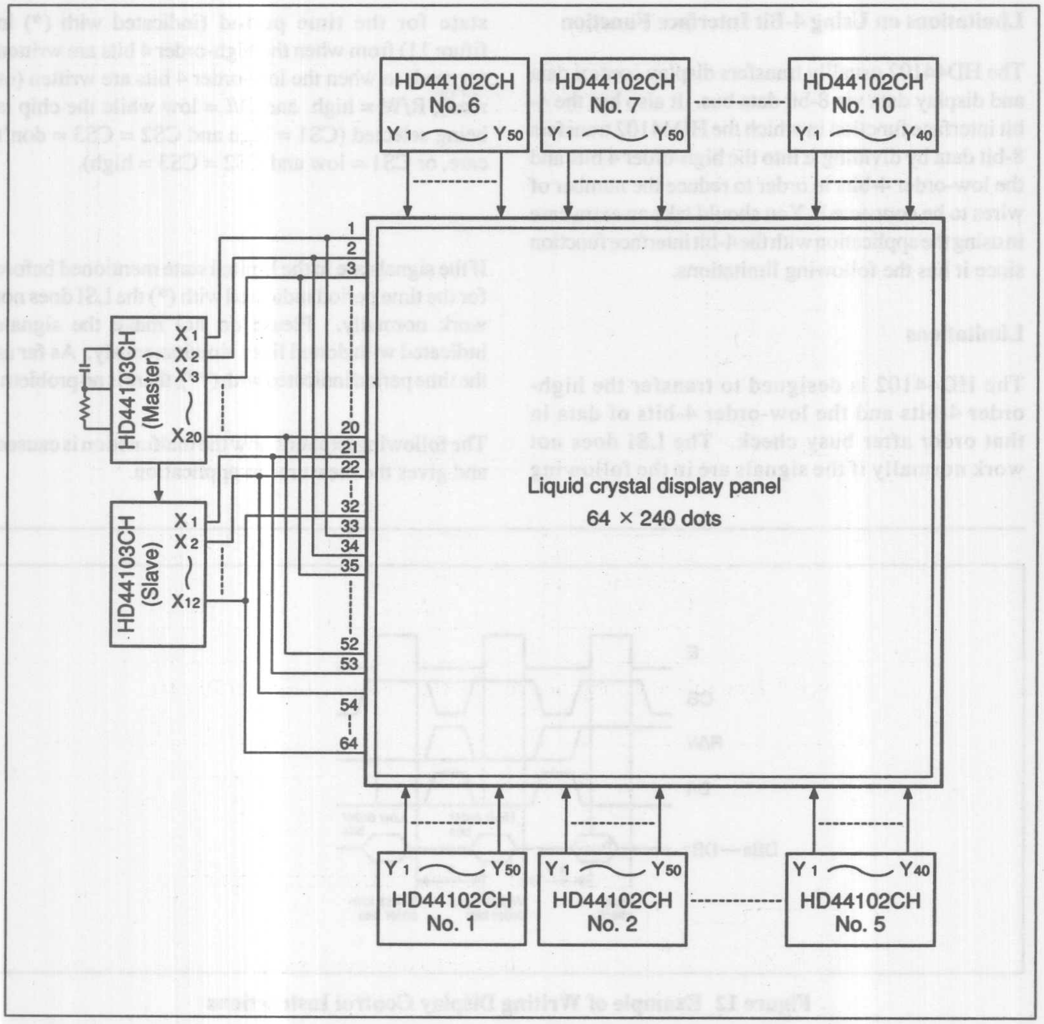


Figure 11 Example of Connection to 1/32 Duty Factor, 2-Screen Display

Limitations on Using 4-Bit Interface Function

The HD44102 usuallly transfers display control data and display data via 8-bit data bus. It also has the 4-bit interface function in which the HD44102 transfers 8-bit data by dividing it into the high-order 4 bits and the low-order 4-bits in order to reduce the number of wires to be connected. You should take an extra care in using the application with the 4-bit interface function since it has the following limitations.

Limitations

The HD44102 is designed to transfer the high-order 4-bits and the low-order 4-bits of data in that order after busy check. The LSI does not work normally if the signals are in the following state for the time period (indicated with (*) in fifure 11) from when the high-order 4 bits are written (or read) to when the low-order 4 bits are written (or read); R/W = high and D/I = low while the chip is being selected (CS1 = high and CS2 = CS3 = don't care, or CS1 = low and CS2 = CS3 = high).

If the signals are in the limited state mentioned before for the time period indicated with (*) the LSI does not work normally. Please do not make the signals indicated with dotted lines simultaneously. As far as the time period indicated with (**), there is no problem.

The following explains how the malfunction is caused and gives the measures in application.

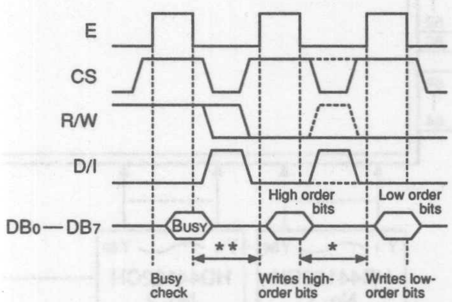


Figure 12 Example of Writing Display Control Instructions

Cause

Busy check checks if the LSI is ready to accept the next instruction or display data by reading the status register to the HD44102. And at the same time, it resets the internal counter counting the order of high-order data and low-order data. This function makes the LSI ready to accept only the high-order data after busy check. Strictly speaking, if R/W = high and D/I = low while the chip is being selected, the internal counter is reset and the LSI gets ready to accept high-order bits. Therefore, the LSI takes low-order data for high-order data if the state mentioned above exist in the interval between transferring high-order data and transferring low-order data.

Measures in Application

1. HD44102 Controlled Via Port

When you control the HD44102 with the port of a single-chip microcomputer, you should take care of the software and observe the limitations strictly.

2. HD44102 Controlled Via Bus

a. Malfunction Caused by Hazard

Hazard of input signals may also cause the phenomenon mentioned before. The phase shift at transition of the input signals may cause the malfunction and so the AC characteristics must be carefully studied.

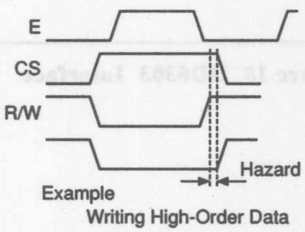


Figure 13 Input Hazard

b. Using 2-Byte Instruction

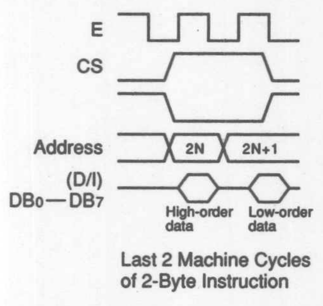


Figure 14 2-Byte Instruction

In an application with the HD6303, you can prevent malfunction by using 2-byte instructions such as STD and STX. This is because the high-order and low-order data are accessed in that order without a break in the last machine cycle of the instruction and R/W and D/I do not change in the meantime. However, you cannot use the least significant bit of the address signals as the D/I signal since the address for the second byte has an added 1. Design the CS decoder so that the addresses for the HD44102 should be 2N and 2N + 1, and that those addresses should be accessed when using 2-byte instructions. For example, in figure 14 the address signal A_1 is used as D/I signal and A_2–A_{15} are used for the CS decoder. Addresses 4N and 4N + 1 are for instruction access and addresses 4N + 2 and 4N + 3 are for display data access.

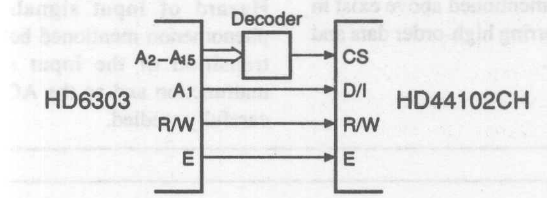


Figure 15 HD6303 Interface

HD44103

(Dot Matrix Liquid Crystal Graphic Display Common Driver)

Description

The HD44103CH is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals required for display with its internal oscillator and supplies them to the column driver (HD44102CH) to control display, also automatically scanning the common signals of the liquid crystal according to the display duty. It can select 5 types of display duty ratio: 1/8, 1/12, 1/16, 1/24, and 1/32. 20 driver output lines are provided, and the impedance is low (500 Ω max.) to enable a large screen to be driven.

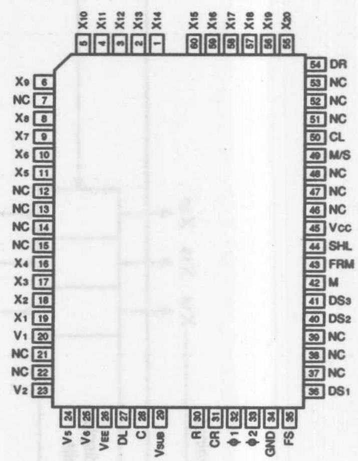
Features

- Dot matrix liquid crystal graphic display common driver incorporating the timing generation circuit
- Internal oscillator (Oscillation frequency can be selected by attaching an oscillation resistor and an oscillation capacity)
- Generates display timing signals
- 20-bit bidirectional shift register for generating common signals
- 20 liquid crystal driver circuits with low output impedance
- Selectable display duty ratio: 1/8, 1/12, 1/16, 1/24, 1/32
- Low power dissipation
- Power supplies: V_{CC}: 5 V ±10%, V_{EE}: 0 to −5.5 V
- CMOS process

Ordering Information

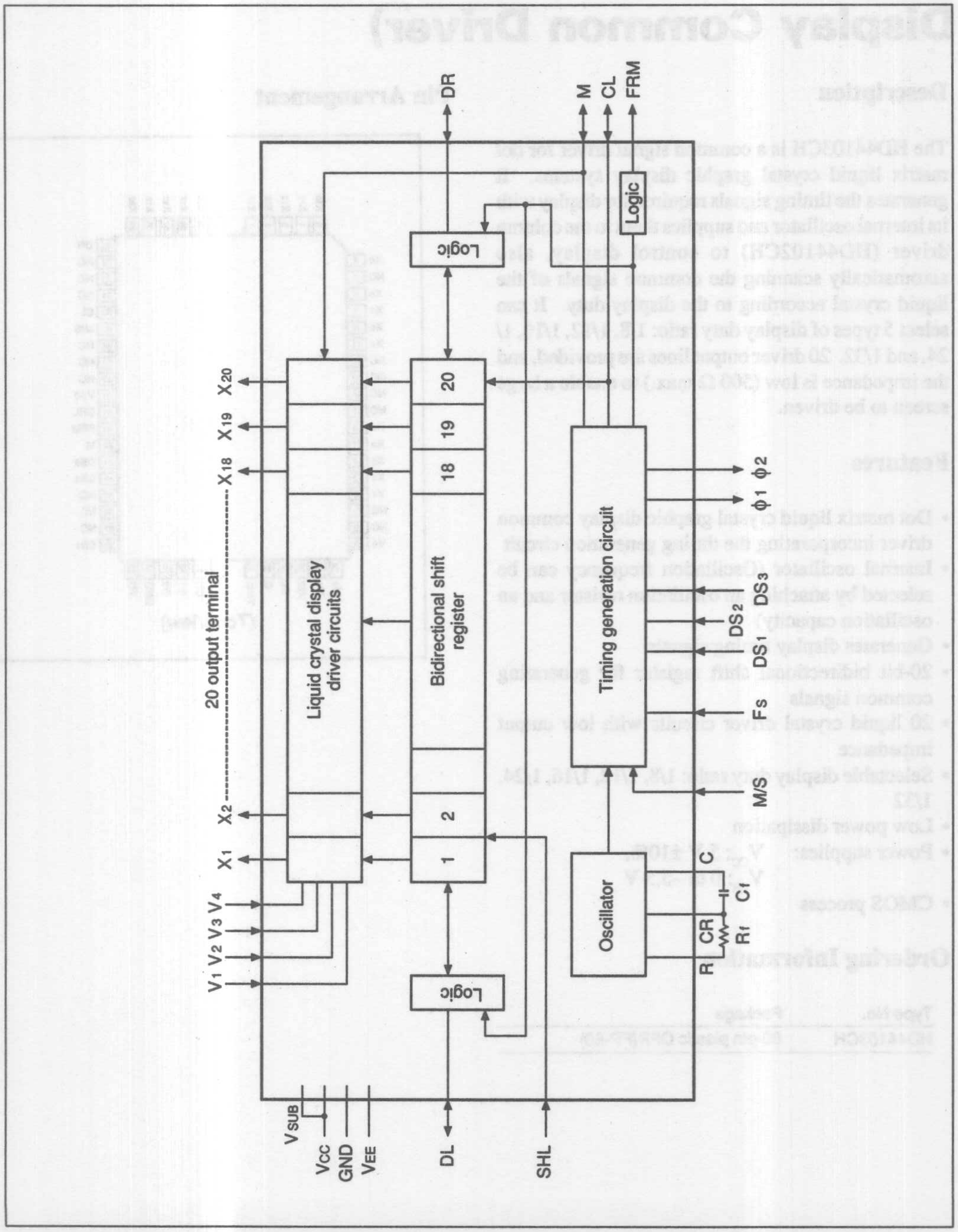
Type No.	Package
HD44103CH	60-pin plastic QFP(FP-60)

Pin Arrangement



(Top View)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rated Value	Unit	Note
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V	1
Supply voltage (2)	V_{EE}	V_{CC} –13.5 to V_{CC} + 0.3	V	4
Terminal voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Terminal voltage (2)	V_{T2}	V_{EE} –0.3 to V_{CC} + 0.3	V	3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. Referenced to GND = 0.
2. Applied to input terminals (except V1, V2, V5, and V6) and I/O common terminals.
3. Applied to terminals V1, V2, V5, and V6.
4. Connect a protection resistor of 220 Ω ± 5% to V_{EE} power supply in series.

Electrical Characteristics

(V_{CC} = +5 V ±10%, GND = 0 V, V_{EE} = 0 to –5.5 V, Ta = –20 to +75 °C) (Note 5)

Item	Symbol	Min	Typ	Max	Unit	Test condition	Note
Input high voltage	V_{IH}	0.7 × V_{CC}		V_{CC}	V		6
Input low voltage	V_{IL}	0	–	0.3 × V_{CC}	V		6
Output high voltage	V_{OH}	V_{CC} – 0.4	–	–	V	I_{OH} = –400 µA	7
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = +400 µA	7
Vi-Xj on resistance	R_{ON}	–	–	500	Ω	V_{EE} = –5 ± 10%, Load current ±150 µA	
Input leakage current (1)	I_{IL1}	–1	–	1	µA	V_{IN} = V_{CC} to GND	8
Input leakage current (2)	I_{IL2}	–2	–	2	µA	V_{IN} = V_{CC} to V_{EE}	9
Shift frequency	f_{SFT}	–	–	50	kHz	In slave mode	10
Oscillation frequency	f_{OSC}	300	430	560	kHz	R_f = 68 kΩ ± 2% C_f = 10 pF ± 5%	11
External clock operating frequency	f_{cp}	50	–	560	kHz		
External clock duty	Duty	45	50	55	%		12
External clock rise time	t_{rcp}	–	–	50	ns		12
External clock fall time	t_{fcp}	–	–	50	ns		12
Dissipation power (master)	P_{w1}	–	–	4.4	mW	CR oscillation = 430 kHz	13
Dissipation power (slave)	P_{w2}	–	–	1.1	mW	Frame frequency = 70 Hz	14

Notes: 5. Specified within this range unless otherwise noted.

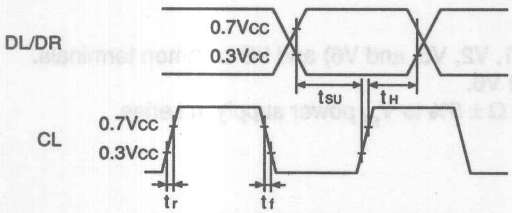
6. Applied to CR, FS, DS1 to DS3, M, SHL, M/S, CL, DR, and DL.

7. Applied to DL, DR, M, FRM, CL, ϕ1 and ϕ2.

8. Applied to input terminals CR, FS, DS1 to DS3, SHL and M/S, and I/O common terminals DL, DR, M, and CL at high impedance.

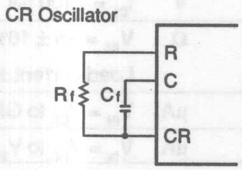
9. Applied to V1, V2, V5, and V6.

10. Shift operation timing

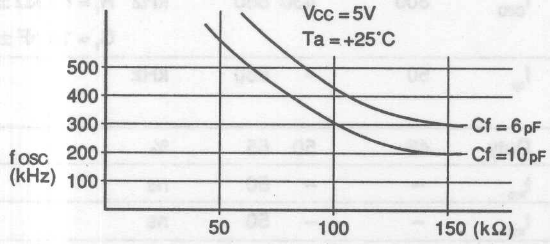


	Min	Typ	Max	Unit
t_{su}	5	–	–	µs
t_H	5	–	–	µs
t_r	–	–	100	ns
t_f	–	–	100	ns

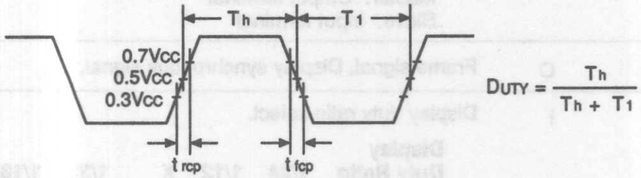
11. Relationship between oscillation frequency and R_f/C_f

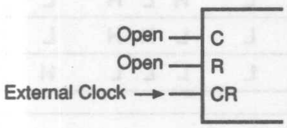


The values of R_f and C_f are typical values. The oscillation frequency varies with the mounting condition. Adjust oscillation frequency to the required value.



12.



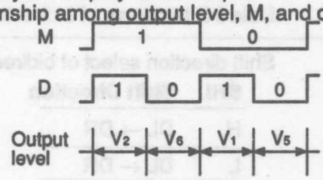


13. Measured by V_{CC} terminal at output non-load of R_f = 68 kΩ ± 2% and C_f = 10pF ± 5%, 1/32 duty factor in the master mode. Input terminals must be fixed at V_{CC} or GND while measuring.

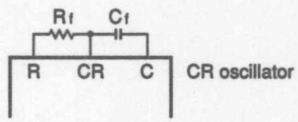
14. Measured by V_{CC} terminal at output non-load, 1/32 duty factor, frame frequency of 70 Hz in the slave mode. Input terminals must be fixed at V_{CC} or GND while measuring.

Pin Description

Pin Name	Pin Number	I/O	Function
X1–X20	20	O	Liquid crystal display driver output. Relationship among output level, M, and data (D) in shift register:



Pin Name	Pin Number	I/O	Function
CR, R, C	3		Oscillator



Pin Name	Pin Number	I/O	Function
M	1	I/O	Signal for converting liquid crystal display driver signal into AC. Master: Output terminal Slave: Input terminal

<table>
<tr><th>Pin Name</th><th>Pin Number</th><th>I/O</th><th>Function</th></tr>
<tr><td>CL</td><td>1</td><td>I/O</td><td>Shift register shift clock.
Master: Output terminal
Slave: Input terminal</td></tr>
<tr><td>FRM</td><td>1</td><td>O</td><td>Frame signal, Display synchronous signal.</td></tr>
<tr><td>DS1–DS3</td><td>3</td><td>I</td><td>Display duty ratio select.
<table>
<tr><th>Display Duty Ratio</th><th>1/24</th><th>1/12</th><th></th><th>X</th><th>1/32</th><th>1/16</th><th></th><th>1/8</th></tr>
<tr><td>DS1</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>DS2</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>DS3</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td></tr>
</table></td></tr>
<tr><td>FS</td><td>1</td><td>I</td><td>Frequency select.
The relationship between the frame frequency f_{FRM} and the oscillation frequency f_{OSC} is as follows:
FS = High: $f_{OSC} = 6144 \times f_{FPM}$ (1)
FS = Low: $f_{OSC} = 3072 \times f_{FRM}$ (2)
Example (1) When FS = high, adjust Rf and Cf so that the oscillation frequency is approx. 430 kHz if the frame frequency is 70 Hz.
Example (2) When FS = low, adjust Rf and Cf so that the oscillation is approx. 215 kHz, in order to obtain the same display waveforms as example 1. When compared with example 1, the power dissipation is reduced because of operation at lower frequency. However, the operating clocks $\phi 1$ and $\phi 2$ supplied to the column driver have lower frequencies. Therefore, the access time of the column driver HD44102CH becomes longer.</td></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Data I/O terminals of bidirectional shift register.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>Shift direction select of bidirectional shift register.
<table>
<tr><th>SHL</th><th>Shift Direction</th></tr>
<tr><td>H</td><td>DL → DR</td></tr>
<tr><td>L</td><td>DL ← DR</td></tr>
</table></td></tr>
</table>

Pin Name	Pin Number	I/O	Function
M/S	1	I	Master/slave select. M/S = High: Master mode The oscillator and timing generation circuit supply display timing signals to the display system. Each of I/O common terminals, DL, DR, M, and CL is placed in the output state. M/S = Low: Slave mode The timing generation circuit stops operating. The oscillator is not required. Connect terminal CR to V_{CC}. Open terminals C and R. One (determined by SHL) of DL and DR, and terminals M and Cl are placed in the input state. Connect M, CL and one of DL and DR of the master to the respective terminals. Connect FD, DS1, DS2, and DS3 to V_{CC}. When display duty ratio is 1/8, 1/12, or 1/16, one HD44103CH is required. Use it in the master mode. When display duty ratio is 1/24 or 1/32, two HD44103CHs are required. Use the one in the master mode to drive common signals 1 to 20, and the other in the slave mode to drive common signals 21 to 24 (32).
ϕ1, ϕ2	2	O	Operating clock output terminals for HD44102CH. The frequencies of ϕ1 and ϕ2 become half of oscillation frequency.
V1, V2, V5, V6	4		Liquid crystal display driver level power supply. V1 and V2: Selected level V5 and V6: Non-selected level
V_{CC} GND V_{EE}	3		Power supply. V_{CC}–GND: Power supply for internal logic V_{CC}–V_{EE}: Power supply for driver circuit logic

Block Functions

Oscillator

The oscillator is a CR oscillator attached to an oscillation resistor Rf ans osckllation capacity Cf. The oscillation frequency varies with the values of Rf and Cf and the mounting conditions. Refer to Electrical Characteristics (Note 10) to make proper adjustment.

Timing Genaration Circuit

The timing generation circuit divides the signals from the oscillator and generates display timing signals (M, CL, and FRM) and operating clock (ϕ1 and ϕ2) for HD44102CH according to the display duty ratio set by DS1 to DS3. In the slave mode, this block stops operating. It is meaningless to set FS, DS1 to DS3. However, connect them to V_{cc} to prevent floating current.

Bidirectional Shift Register

20-bit bidirectional shift register. The shift direction is determined by SHL. The data input from DL or DR performs a shift operation at the rise of shift clock CL.

Liquid Crystal Display Driver Circuit

Each of 20 driver circuits is a multiplex circuit composed of four CMOS switches. The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5, and V6 to be transferred to the output terminals.

Applications

Refer to the applications of the HD44102CH.

HD44105

(Dot Matrix Liquid Crystal Graphic Display Common Driver)

Description

The HD44105H is a common signal driver for LCD dot matrix graphic display systems. It generates the timing signals required for display with its internal oscillator and supplies them to the column driver (HD44102H) to control display, also automatically scanning the common signals of the liquid crystal according to the display duty cycle.

It can select 7 types of display duty cycle 1/8, 1/12, 1/16, 1/24,1/32, 1/48, and 1/64. It provides 32 driver output lines and the impedance is low (1 kΩ max) enough to drive a large screen.

Features

- Dot matrix graphic display common driver including the timing generation circuit
- Internal oscillator (Oscillation frequency is selectable by attaching an oscillation resistor and an oscillation capacitor)
- Generates display timing signals
- 32-bit bidirectional shift register for generating common signals
- 32 liquid crystal driver circuits with low impedance
- Selectable display duty ratio: 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64
- Low power dissipation
- Power supplies: V_{CC} = +5 V ± 10%, V_{EE} = 0 to −5.5 V
- CMOS process

Ordering Information

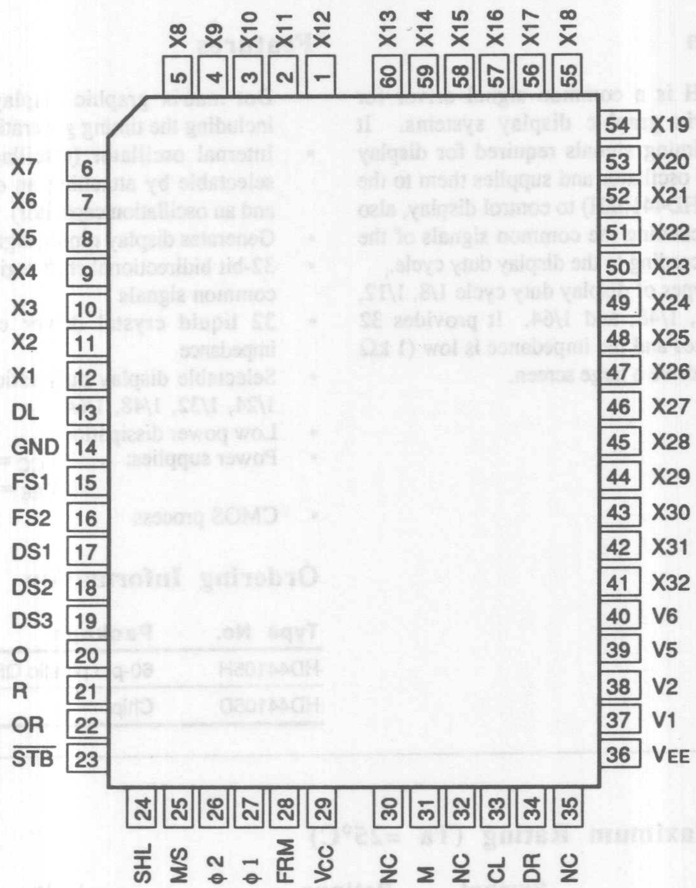
Type No.	Package
HD44105H	60-pin plastic QFP(FP-60)
HD44105D	Chip

Absolute Maximum Rating (Ta =25°C)

Item	Symbol	Ratings	Unit	Note
Supply voltage (1)	V_{CC}	−0.3 to +7.0	V	1
Supply voltage (2)	V_{EE}	V_{CC} −13.5 to V_{CC} +0.3	V	
Terminal voltage (1)	V_{T1}	−0.3 to V_{CC} +0.3	V	1, 2
Terminal voltage (2)	V_{T2}	V_{EE} −0.3 to V_{CC} +0.3	V	3
Operating temperature	Topr	−20 to +75	°C	
Storage temperature	Tstg	−55 to +125	°C	

Notes: 1. Referred to GND = 0 V.
2. Applied to input terminals (except for V1, V2, V5, and V6) and I/O common terminals.
3. Applied to terminals V1, V2, V5, and V6. Connect a protection resistor of 47 Ω ± 10% to each terminal in series.

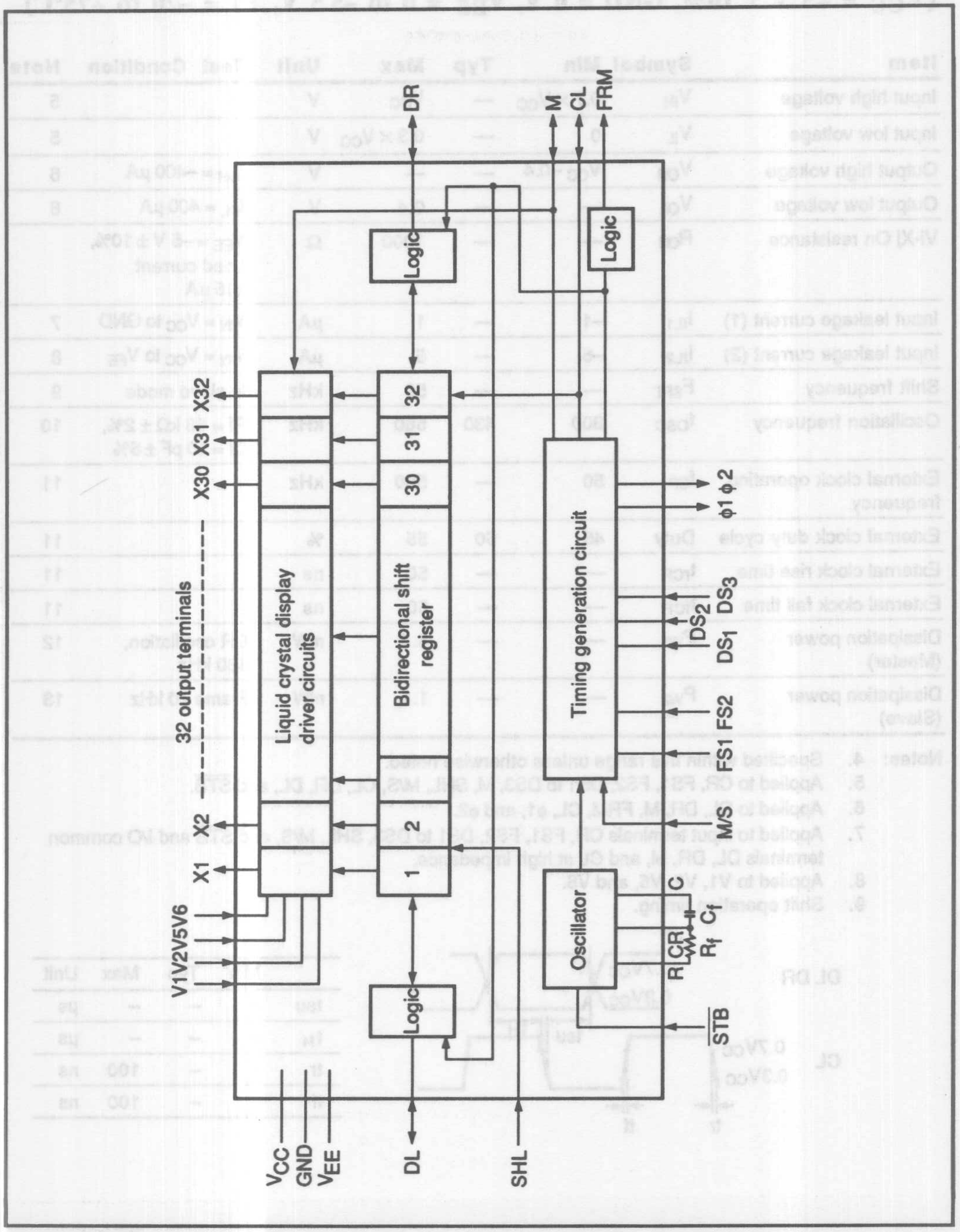
Pin Arrangement



(Top View)

Note: NCs show unused terminals. Don't connect any lines to them in using this LSI.

Block Diagram



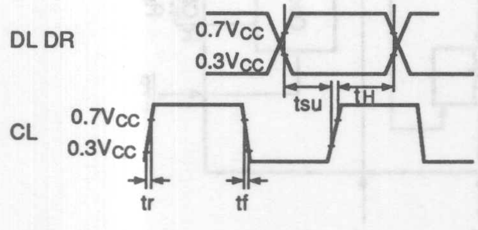
Electrical Characteristics

(Note 4)

(V_{CC} = +5 V ± 10%, GND = 0 V, V_{EE} = 0 to –5.5 V, Ta = –20 to +75°C)

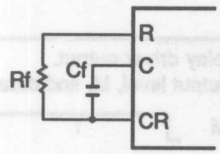
Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	$0.7 \times V_{CC}$	—	V_{CC}	V		5
Input low voltage	V_{IL}	0	—	$0.3 \times V_{CC}$	V		5
Output high voltage	V_{OH}	V_{CC} –0.4	—	—	V	I_{OH} = –400 µA	6
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 400 µA	6
Vi-Xj On resistance	R_{ON}	—	—	1000	Ω	V_{EE} = –5 V ± 10%, Load current ±15 µA	
Input leakage current (1)	I_{IL1}	–1	—	1	µA	V_{IN} = V_{CC} to GND	7
Input leakage current (2)	I_{IL2}	–5	—	5	µA	V_{IN} = V_{CC} to V_{EE}	8
Shift frequency	F_{SFT}	—	—	50	kHz	In slave mode	9
Oscillation frequency	f_{OSC}	300	430	560	kHz	Rf = 68 kΩ ± 2%, Cf = 10 pF ± 5%	10
External clock operating frequency	f_{CP}	50	—	560	kHz		11
External clock duty cycle	Duty	45	50	55	%		11
External clock rise time	t_{rCP}	—	—	50	ns		11
External clock fall time	t_{fCP}	—	—	50	ns		11
Dissipation power (Master)	P_{W1}	—	—	4.4	mW	CR oscillation, 430 kHz	12
Dissipation power (Slave)	P_{W2}	—	—	1.1	mW	Frame 70 kHz	13

Notes:
4. Specified within this range unless otherwise noted.
5. Applied to CR, FS1, FS2, DS1 to DS3, M, SHL, M/S, CL, DR, DL, and $\overline{STB}$.
6. Applied to DL, DR, M, FRM, CL, φ1, and φ2.
7. Applied to input terminals CR, FS1, FS2, DS1 to DS3, SHL, M/S, and $\overline{STB}$ and I/O common terminals DL, DR, M, and CL at high impedance.
8. Applied to V1, V2, V5, and V6.
9. Shift operation timing.

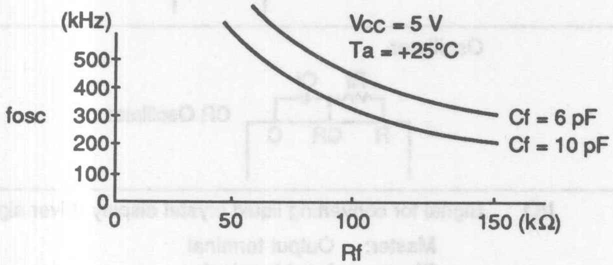


	Min	Typ	Max	Unit
tsu	5	–	–	µs
t_H	5	–	–	µs
tr	–	–	100	ns
tf	–	–	100	ns

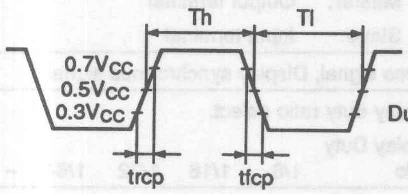
Notes: 10. Relation between oscillation frequency and Rf, Cf.



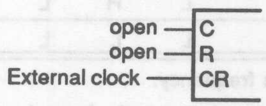
The values of Rf and Cf are typical values. The oscillation frequency varies with the mounting condition. Adjust oscillation frequency to a required value.



11.



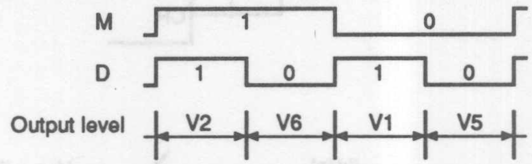
$$\text{Duty} = \frac{Tb}{Th - Tl}$$



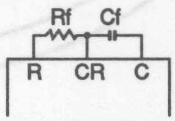
12. Measured by V_{CC} terminal at output non-load of Rf = 68 kΩ ± 2% and Cf = 10 pF ± 5%, and 1/32 duty cycle in the master mode.
Input terminals are connected to V_{CC} or GND.
13. Measured by V_{CC} terminal at output non-load, 1/32 duty cycle, and frame frequency of 70 Hz in the slave mode.
Input terminals are connected to V_{CC} or GND.

Pin Description

Pin Name	Pin Number	I/O	Function
X1–X32	32	O	Liquid crystal display driver output. Relation among output level, M, and data (D) in shift register.



Pin Name	Pin Number	I/O	Function
CR, R, C	3		Oscillator.



CR Oscillator

Pin Name	Pin Number	I/O	Function
M	1	I/O	Signal for converting liquid crystal display driver signal into AC. Master: Output terminal Slave: Input terminal
CL	1	I/O	Shift register shift clock. Master: Output terminal Slave: Input terminal
FRM	1	O	Frame signal, Display synchronous signal.
DS1–DS3	3	I	Display duty ratio select.

Display Duty Ratio	1/8	1/16	1/32	1/64	–	1/12	1/24	1/48
DS1	L	L	H	H	L	L	H	H
DS2	L	H	L	H	L	H	L	H
DS3	L	L	L	L	H	H	H	H

Pin Name	Pin Number	I/O	Function
FS1–FS2	2	1	Selects frequency.

The relation between the frame frequency f_{FRM} and the oscillation frequency f_{OSC} is as follows:

FS1	FS2	f_{OSC}(kHz)	f_{FRM}(Hz)	f_M(Hz)	f_{CP}(kHz)
L	L	107.5	70	35	53.8
H	L	107.5	70	35	53.8
L	H	215.0	70	35	107.5
H	H	430.0	70	35	215.0

f_{OSC}: Oscillation frequency
f_{FRM}: Frame frequency
f_M: M signal frequency
f_{CP}: Frequencies of $\phi 1$ and $\phi 2$

Pin Description (cont)

Pin Name	Pin Number	I/O	Function
$\overline{STB}$	1	I	Input terminal for testing. Connect this terminal to V_{CC}.
DL, DR	2	I/O	Data I/O terminals of bidirectional shift register.
SHL	1	I	Selects shift direction of bidirectional shift register. SHL — Shift Direction H — DL → DR L — DL ← DR
M/S	1	I	Selects Master/Slave. M/S = High: Master mode The oscillator and timing generation circuit operate to supply display timing signals to the display system. Each of I/O common terminals, DL, DR, M, and CL is in the output state. M/S = Low: Slave mode The timing generation circuit stop operating. The oscillator is not required. Connect terminal CR to V_{CC}. Open terminals C and R. One (determined by SHL) of DL and DR, and terminals M and CL are in the input state. Connect M, CL and one of DL and DR of the master to the respective terminals. Connect FS1, FS2, DS1, DS2, DS3, $\overline{STB}$ to V_{CC}. When display duty ratio is 1/8, 1/12, 1/16, 1/24, 1/32, one HD44105H is required. Use it in the master mode. When display duty ratio is 1/48, 1/64, two HD44105Hs are required. Use one in the master mode to drive common signals 1 to 32, and another in the slave mode to drive common signals 33 to 48(64).
$\phi 1$, $\phi 2$	2	O	Operating clock output terminals for HD44102CH. The frequencies of $\phi 1$ and $\phi 2$ are half of oscillation frequency.
V1, V2, V5, V6	4		Liquid crystal display driver level power supply. V1 and V2: Selected level V5 and V6: Non-selected level
V_{CC}, GND V_{EE}	3		Power supply. V_{CC} – GND: Power supply for internal logic V_{CC} – V_{EE}: Power supply for driver circuit logic

Block Functions

Oscillator

A CR oscillator attached to an oscillation resistor Rf and an oscillation capacitor Cf. The oscillation frequency v aries with the values of Rf and Cf and the mounting conditions. Refer to electrical characteristics (note 10) to make proper adjustment.

Timing Generation Circuit

This circuit divides the signals from the oscillator and generates display timing signals (M, CL, and FRM) and operating clock ($\phi 1$ and $\phi 2$) for HD44102CH according to the display duty ratio set by DS1 to DS3. In the slave mode, this block stops operating. It is meaningless to set FS1, FS2 and DS1 to DS3. However, connect them to V_{CC} to prevent floating current.

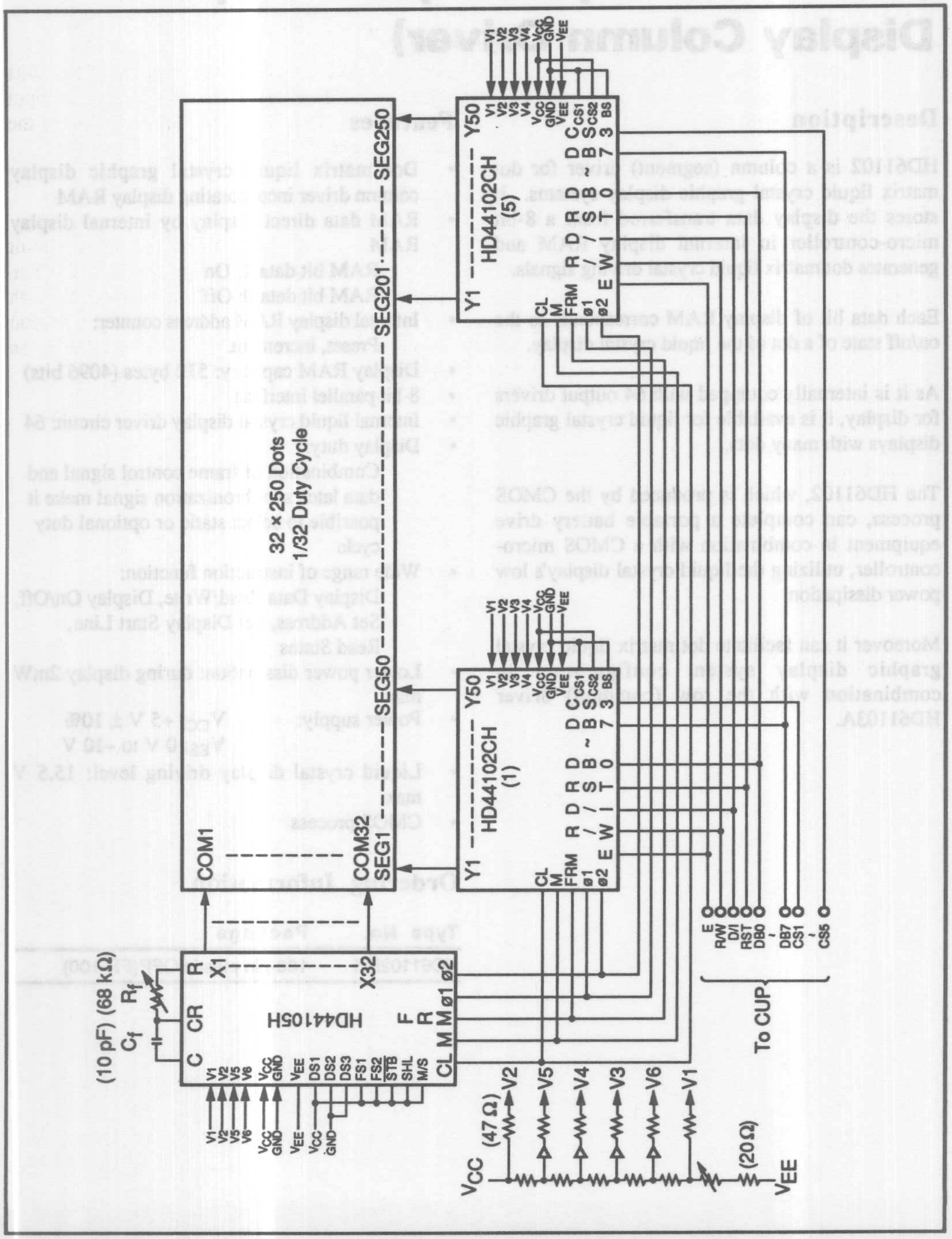
Bidirectional Shift Register

A 32-bit bidirectional shift register. The shift direction is determined by the SHL. The data input from DL or DR performs a shift operation at the rise of shift clock CL.

Liquid Crystal Display Driver Circuit

Each of 32 driver circuits is a multiplex circuit composed of four CMOS switches. The combination of the data from the shift register with the M signal allows one of the four liquid crystal display driver levels V1, V2, V5, and V6 to be transferred to the output terminals.

Connection between HD44105H and HD44102CH



HD61102
(Dot Matrix Liquid Crystal Graphic Display Column Driver)

Description

HD61102 is a column (segment) driver for dot matrix liquid crystal graphic display systems. It stores the display data transferred from a 8-bit micro-controller in internal display RAM and generates dot matrix liquid crystal driving signals.

Each data bit of display RAM corresponds to the on/off state of a dot of the liquid crystal display.

As it is internally equipped with 64 output drivers for display, it is available for liquid crystal graphic displays with many dots.

The HD61102, which is produced by the CMOS process, can complete a portable battery drive equipment in combination with a CMOS micro-controller, utilizing the liquid crystal display's low power dissipation.

Moreover it can facilitate dot matrix liquid crystal graphic display system configuration in combination with the row (common) driver HD61103A.

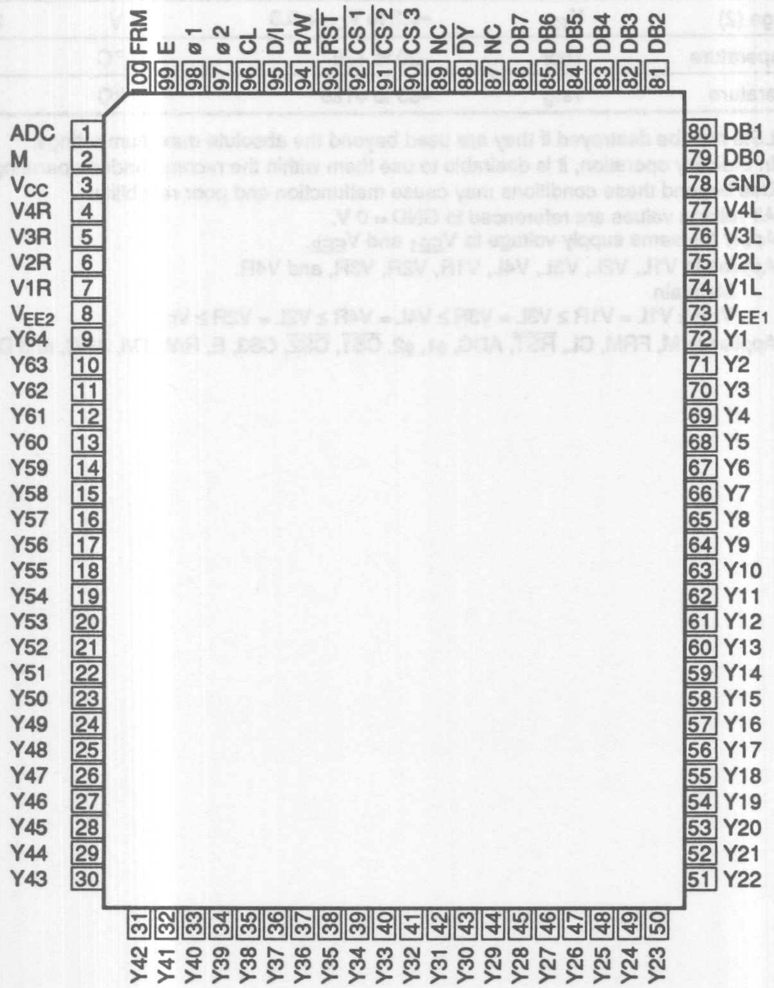
Features

- Dot matrix liquid crystal graphic display column driver incorporating display RAM
- RAM data direct display by internal display RAM
  - RAM bit data 1: On
  - RAM bit data 0: Off
- Internal display RAM address counter:
  - Preset, increment
- Display RAM capacity: 512 bytes (4096 bits)
- 8-bit parallel interface
- Internal liquid crystal display driver circuit: 64
- Display duty:
  - Combination of frame control signal and data latch synchronization signal make it possible to select static or optional duty cycle
- Wide range of instruction function:
  - Display Data Read/Write, Display On/Off, Set Address, Set Display Start Line, Read Status
- Lower power dissipation: during display 2mW max
- Power supply: V_{CC}: +5 V ± 10%, V_{EE}: 0 V to −10 V
- Liquid crystal display driving level: 15.5 V max
- CMOS process

Ordering Information

Type No.	Package
HD61102RH	100-pin plastic QFP(FP-100)

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	– 0.3 to +7.0	V	2
	V_{EE}	V_{CC} – 16.5 to V_{CC} + 0.3	V	3
Terminal voltage (1)	V_{T1}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Terminal voltage (2)	V_{T2}	–0.3 to V_{CC} + 0.3	V	2, 5
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +125	°C	

Notes:
1. LSIs may be destroyed if they are used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the recommended operating conditions. Use beyond these conditions may cause malfunction and poor reliability.
2. All voltage values are referenced to GND = 0 V.
3. Apply the same supply voltage to V_{EE1} and V_{EE2}.
4. Applies to V1L, V2L, V3L, V4L, V1R, V2R, V3R, and V4R.
   Maintain
   V_{CC} ≥ V1L = V1R ≥ V3L = V3R ≥ V4L = V4R ≥ V2L = V2R ≥ V_{EE}
5. Applies to M, FRM, CL, $\overline{RST}$, ADC, φ1, φ2, $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, ADC, and DB0–DB7.

Electrical Characteristics
(GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to –10V, Ta = –20 to +75°C)

Item	Symbol	Limit Min	Limit Typ	Limit Max	Unit	Test Condition	Note
Input high voltage	V_{IHC}	0.7 × V_{CC}	—	V_{CC}	V		1
	V_{IHT}	2.0	—	V_{CC}	V		2
Input low voltage	V_{ILC}	0	—	0.3 × V_{CC}	V		1
	V_{ILT}	0	—	0.8	V		2
Output high voltage	V_{OH}	2.4	—	—	V	IOH = –205 µA	3
Output low voltage	V_{OL}	—	—	0.4	V	IOL = 1.6 mA	3
Input leakage current	I_{IL}	–1.0	—	+1.0	µA	Vin = GND–V_{CC}	4
High impedance off input current	I_{TSL}	–5.0	—	+5.0	µA	Vin = GND–V_{CC}	5
Liquid crystal supply leakage current	I_{LSL}	–2.0	—	+2.0	µA	Vin = V_{EE} –V_{CC}	6
Driver on resistance	R_{ON}	—	—	7.5	KΩ	V_{CC} – V_{EE} = 15 V, ±I_{LOAD} = 0.1 mA	7
Dissipation current	$I_{CC(1)}$	—	—	100	µA	During display	8
	$I_{CC(2)}$	—	—	500	µA	During access, Access cycle = 1 MHz	8

Notes:
1. Applies to M, FRM, CL, $\overline{RST}$, ADC, φ1, and φ2.
2. Applies to $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, and DB0–DB7.
3. Applies to DB0–DB7.
4. Applies to terminals except for DB0–DB7.
5. Applies to DB0–DB7 at high impedance.
6. Applies to V1L–V4L and V1R–V4R.
7. Applies to Y1–Y64.
8. Specified when liquid crystal display is in 1/64 duty.
   Operation frequency: f_{CLK} = 250 kHz (φ1 and φ2 frequency)
   Frame frequency: f_M = 70 Hz (FRM frequency)
   Specified in the state of
   Output terminal: Not loaded
   Input level: V_{IH} = V_{CC} (V)
   V_{IL} = GND (V)
   Measured at V_{CC} terminal

Interface AC Characteristics

MPU Interface
(GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to –10 V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Note
E cycle time	t_{CYC}	1000	—	—	ns	1, 2
E high level width	P_{WEH}	450	—	—	ns	1, 2
E low level width	P_{WEL}	450	—	—	ns	1, 2
E rise time	tr	—	—	25	ns	1, 2
E fall time	tf	—	—	25	ns	1, 2
Address setup time	t_{AS}	140	—	—	ns	1, 2
Address hold time	t_{AH}	10	—	—	ns	1, 2
Data setup time	t_{DSW}	200	—	—	ns	1
Data delay time	t_{DDR}	—	—	320	ns	2, 3
Data hold time (Write)	t_{DHW}	10	—	—	ns	1
Data hold time (Read)	t_{DHR}	20	—	—	ns	2

Notes: 1.

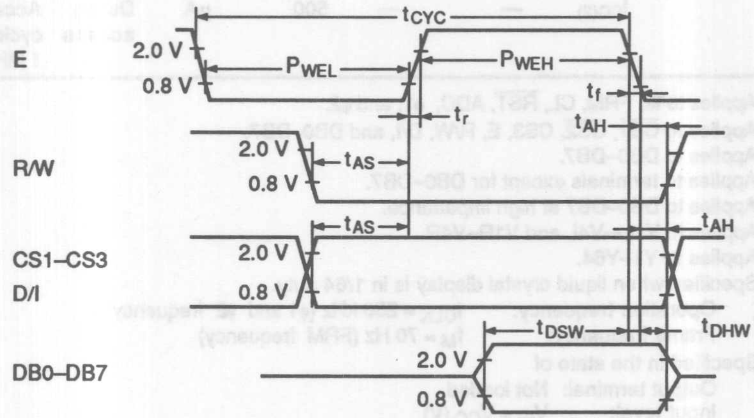


Figure 1 CPU Write Timing

2.

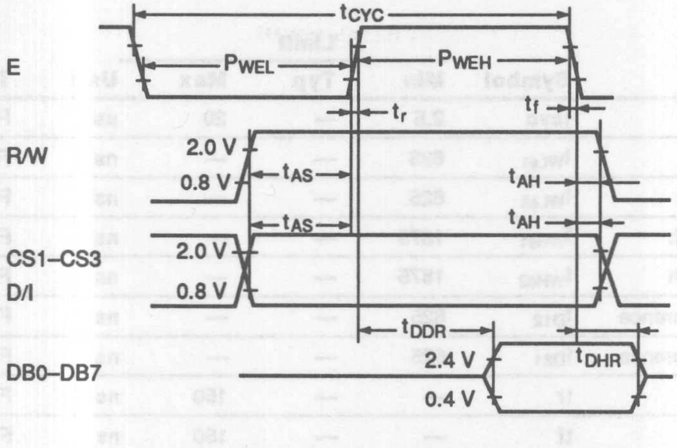
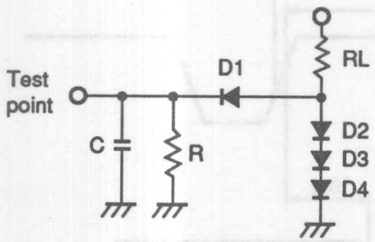


Figure 2 CPU Read Timing

3. DB0–DB7: load circuit



RL = 2.4 kΩ
R = 11 kΩ
C = 130 pF (including jig capacitance)
Diodes D1 to D4 are all IS2074 Ⓗ.

Clock Timing
(GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to −10V, Ta = −20 to +75°C)

Item	Symbol	Limit Min	Limit Typ	Limit Max	Unit	Test Condition
φ1, φ2 cycle time	tcyc	2.5	—	20	μs	Fig. 3
φ1 low level width	$t_{WL\phi1}$	625	—	—	ns	Fig. 3
φ2 low level width	$t_{WL\phi2}$	625	—	—	ns	Fig. 3
φ1 high level width	$t_{WH\phi1}$	1875	—	—	ns	Fig. 3
φ2 high level width	$t_{WH\phi2}$	1875	—	—	ns	Fig. 3
φ1−φ2 phase difference	t_{D12}	625	—	—	ns	Fig. 3
φ2−φ1 phase difference	t_{D21}	625	—	—	ns	Fig. 3
φ1, φ2 rise time	tr	—	—	150	ns	Fig. 3
φ1, φ2 fall time	tf	—	—	150	ns	Fig. 3

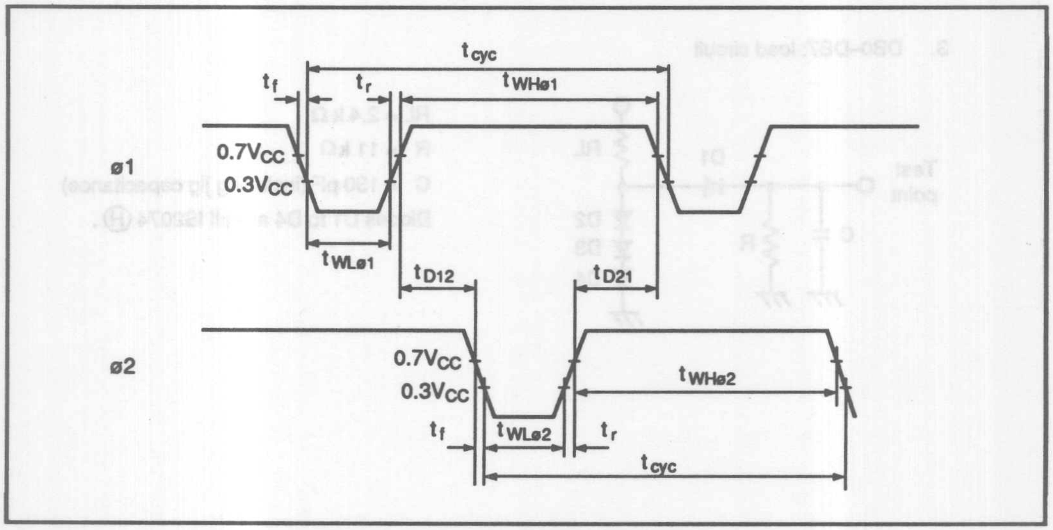


Figure 3 External Clock Waveform

Display Control Timing
(GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to −10V, Ta = −20 to +75°C)

Item	Symbol	Limit Min	Limit Typ	Limit Max	Unit	Test Condition
FRM delay time	t_{DFRM}	−2	—	+2	µs	Fig. 4
M delay time	t_{DM}	−2	—	+2	µs	Fig. 4
CL low level width	t_{WLCL}	35	—	—	µs	Fig. 4
CL high level width	t_{WHCL}	35	—	—	µs	Fig. 4

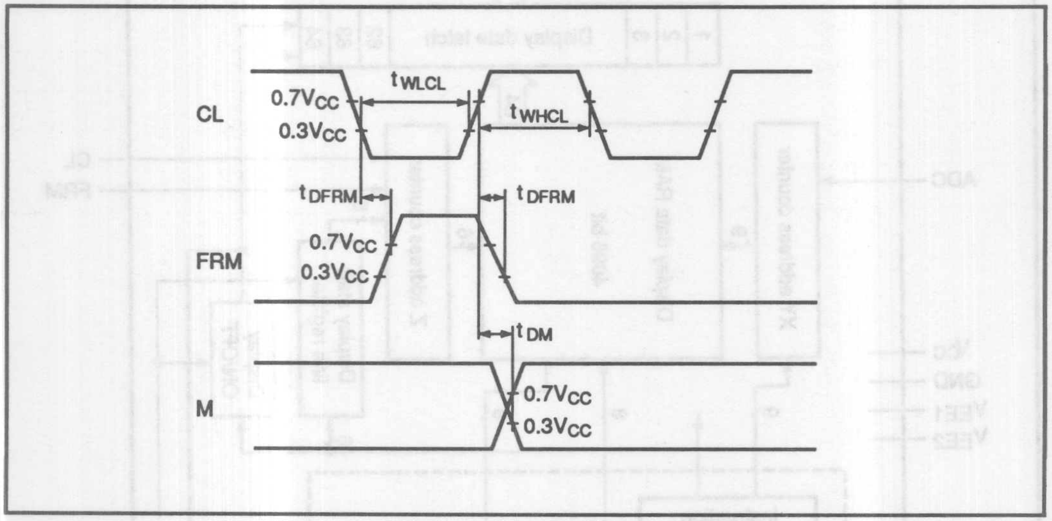
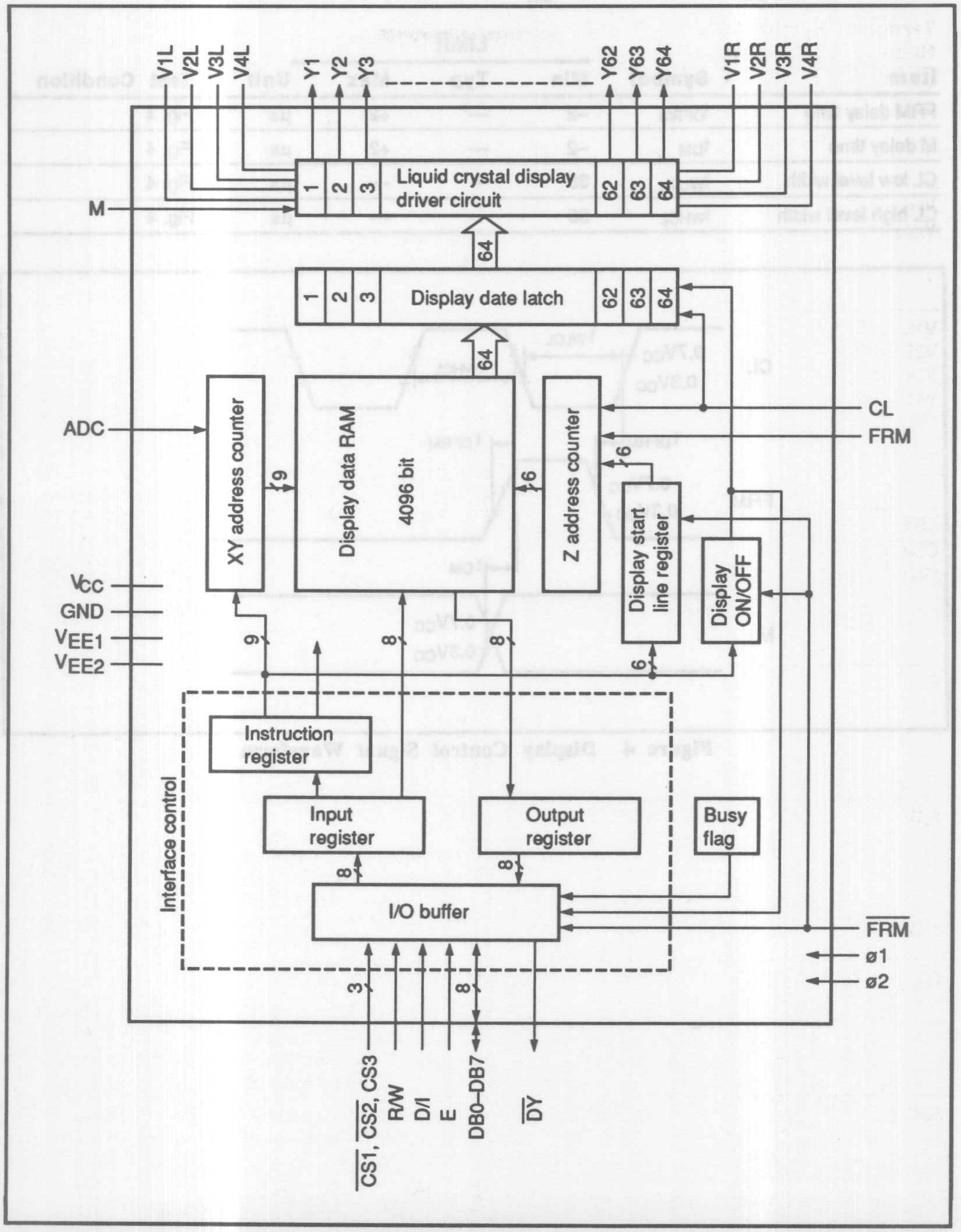


Figure 4 Display Control Signal Waveform

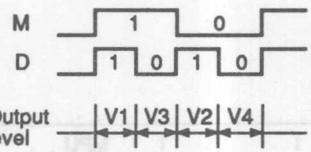
Block Diagram



Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND	2		Power supply	Power supply for internal logic. Recommended voltage is GND = 0 V $V_{CC} = +5\ V \pm 10\%$
V_{EE1} V_{EE2}	2		Power supply	Power supply for liquid crystal display drive circuit. Recommended power supply voltage is V_{CC} −15 to GND. Connect the same power supply to V_{EE1} and V_{EE2}. V_{EE1} and V_{EE2} are not connected to each other in the LSI.
V1L, V1R V2L, V2R V3L, V3R V4L, V4R	8		Power supply	Power supply for liquid crystal display drive. Apply the voltage specified for the liquid crystals within the limit of V_{EE} through V_{CC}. VIL (V1R), V2L (V2R): Selection level V3L (V3R), V4L (V4R): Non-selection level Power supplies connected with V1L and V1R (V2L & V2R, V3L & V3R, V4L & V4R) should have the same voltages.
$\overline{CS1}$ $\overline{CS2}$ CS3	3	I	MPU	Chip selection. Data can be input or output when the terminals are in the following conditions: Terminal name: $\overline{CS1}$, $\overline{CS2}$, CS3 Condition: L, L, H
E	1	I	MPU	Enable At write(R/W = low): Data of DB0 to DB7 is latched at the fall of E. At read(R/W = high): Data appears at DB0 to DB7 while E is high.
R/W	1	I	MPU	Read/write. R/W = High: Data appears at DB0 to DB7 and can be read by the CPU when E = high, $\overline{CS1}$, $\overline{CS2}$ = low and CS3 = high. R/W = Low: DB0 to DB7 accepted at fall of E when $\overline{CS1}$, $\overline{CS2}$ = low and CS3 = high.
D/I	1	I	MPU	Data/Instruction. D/I = High: Indicates that the data of DB0 to DB7 is display data. D/I = Low: Indicates that the data of DB0 to DB7 is display control data.
ADC	1	I	V_{CC}/GND	Address control signal determine the relation between Y address of display RAM and terminals from which the data is output. ADC = High: Y1–\$0, Y64–\$63 ADC = Low: Y64–\$0, Y1–\$63

Terminal Functions (cont)

Terminal Name	Number of Terminals	I/O	Connected to	Functions
DB0–DB7	8	I/O	MPU	Data bus, three-state I/O common terminal.
M	1	I	HD61103A	Switch signal to convert liquid crystal drive waveform into AC.
FRM	1	I	HD61103A	Display synchronous signal (frame signal). Presets the 6-bit display line counter and synchronizes a common signal with the frame timing when the FRM signal becomes high.
CL	1	I	HD61103A	Synchronous signal to latch display data. The rising edge of the CL signal increments the display output address counter and latches the display data.
$\phi 1$, $\phi 2$	1	I	HD61103A	2-phase clock signal for internal operation. The $\phi 1$ and $\phi 2$ clocks are used to perform operations (I/O of display data and execution of instructions) other than display.
Y1-Y64	64	O	Liquid crystal display	Liquid crystal display column (segment) drive output. These pins output light on level when 1 is in the display RAM, and light off level when 0 is in it. Relation among output level, M, and display data (D) is as follows: 
$\overline{RST}$	1	I	CPU or external CR	The following registers can be initialized by setting the $\overline{RST}$ signal to low level: 1. On/off register set to 0 (display off) 2. Display start line register set to line 0 (displays from line 0) After releasing reset, this condition can be changed only by instruction.
$\overline{DY}$	1	O	Open	Output terminal for test. Normally, don't connect any lines to this terminal.
NC	2		Open	Unused terminals. Don't connect any lines to these terminals.

Note: 1 corresponds to high level in positive logic.

Function of Each Block

Interface Control

1. I/O buffer

Data is transferred through 8 data buses (DB0-DB7).

DB7: MSB (most significant bit)

DB0: LSB (least significant bit)

Data can neither be input nor output unless $\overline{CS1}$ to CS3 are in the active mode. Therefore, when $\overline{CS1}$ to CS3 are not in active mode it is useless to switch the signals of input terminals except $\overline{RST}$ and ADC, that is namely, the internal state is maintained and no instruction excutes. Besides, pay attention to $\overline{RST}$ and ADC which operate irrespectively by $\overline{CS1}$ to CS3.

2. Register

Both input register and output register are provided to interface to MPU whose the speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals.

a. Input Register

The input register is used to store data temporarily before writing it into display data RAM. The data from MPU is written into input register, then into display data RAM automatically by internal operation.

When $\overline{CS1}$ to CS3 are in the active mode and D/I and R/W select the input register as shown in table 1, data is latched at the fall of E signal.

b. Output Register

The output register is used to store data temporarily that is read from display data RAM. To read out the data from the output register, $\overline{CS1}$ to CS3 should be in the active mode and both D/I and R/W should be 1. The read display data instruction outputs data stored in the output register while E is high. Then, at the fall of E, the display data at the indicated address is latched into the output register and the address is increased by 1. The contents in the output register is rewritten with READ instruction, while is held with address set instruction, etc.

Therefore, the data of the specified address cannot be output with the read display data instruction right after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Figure 5 shows the CPU read timing.

Table 1 Register Selection

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register).
1	0	Writes data into input register as internal operation (input register → display data RAM).
0	1	Busy check. Read of status data.
0	0	Instruction.

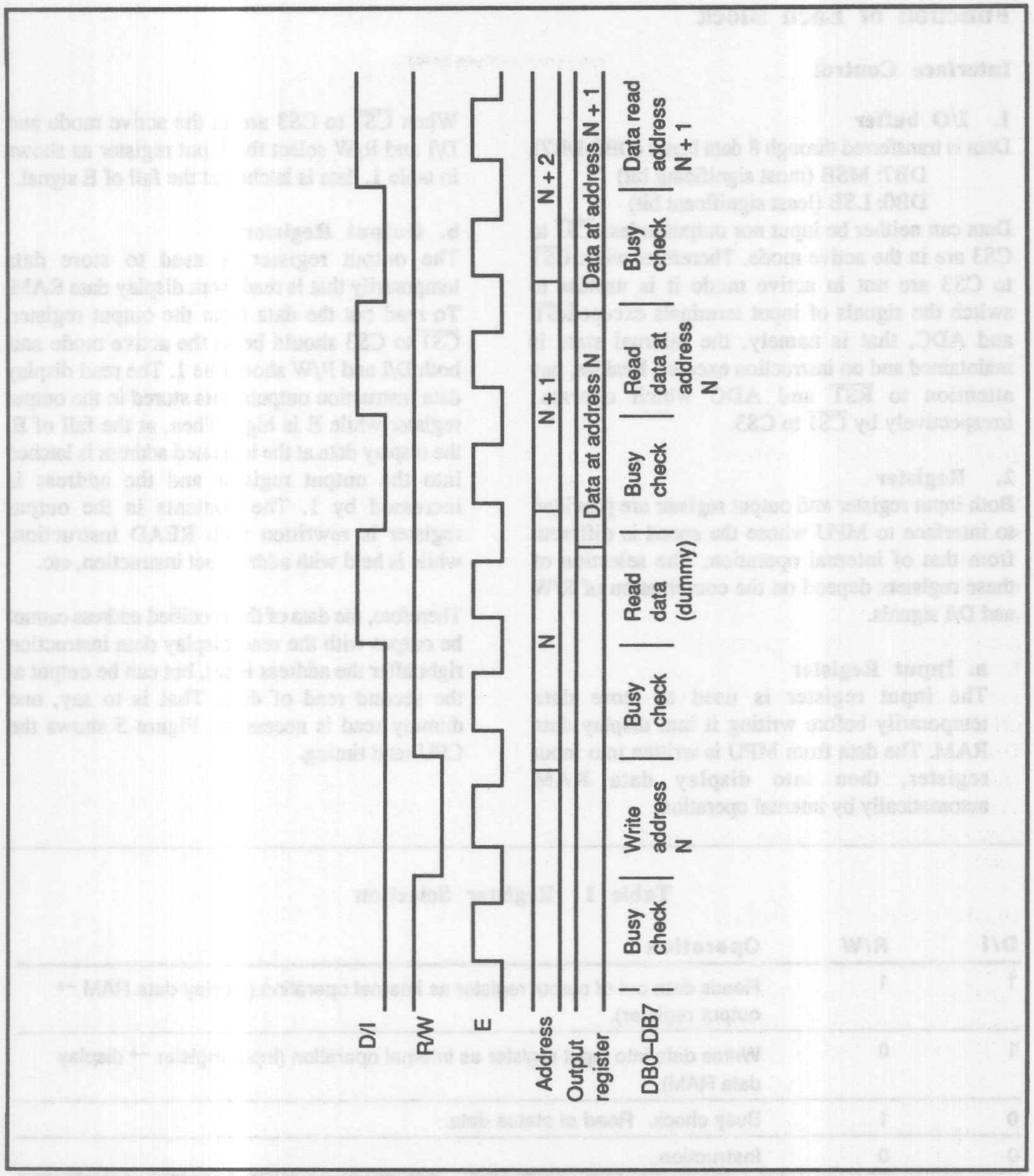


Figure 5 CPU Read Timing

Busy Flag

Busy flag = 1 indicates that HD61102 is operating and no instructions except status read can be accepted (figure 6). The value of the busy flag is read out on DB7 by the Status Read instruction. Make sure that the busy flag is reset (0) before issuing an instruction.

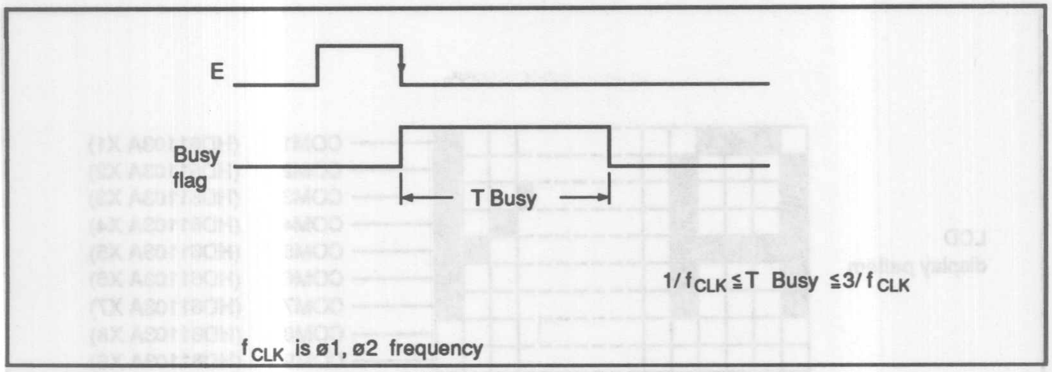


Figure 6 Busy Flag

Display On/Off Flip/Flop

The display On/off flip/flop selects one of two states, on state and off state of segments Y1 to Y64. In on state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in off state independent of the data in RAM. It is controlled by the display on/off instruction. $\overline{RST}$ signal = 0 sets the segments in off state. The status of the flip/flop is output to DB5 by the status read instruction. The display on/off instruction does not influence data in RAM. To control display data latch by this flip/flop, Cl signal (display synchronous signal) should be input correctly.

Display Start Line Register

The register specifies a line in RAM that corresponds to the top line of the LCD panel, when displaying contents in display data RAM on the LCD panel. It is used for scrolling the screen.

6-bit display start line information is written into this register by the display start line set instruction, with high level of FRM signal signalling the start of the display, the information in this register is transferred to the Z address counter, which controls the display address, and the Z address counter is preset.

X, Y Address Counter

A 9-bit counter that designates addresses of internal display data RAM. X address counter (upper 3 bits) and Y address counter (lower 6 bits) should be set by the respective instructions.

1. X address counter
Ordinary register with no count functions. An address is set by instruction.

2. Y address counter
An address is set by instruction and it is increased by 1 automatically by display data R/W operations. The Y address counter loops the values of 0 to 63 to count.

Display Data RAM

Dot data for display is stored in this RAM. 1-bit data of this RAM corresponds to light on (data = 1) and light off (data = 0) of 1 dot in the display panel. The correspondence between Y addresses of RAM and segment PINs can be reversed by ADC signal.

As the ADC signal controls the Y address counter, a reverse of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore, always connect ADC pin to V_{CC} or GND when using.

Figure 7 shows the relations between Y address of RAM and segment pins in the cases of ADC = 1 and ADC = 0 (display start line = 0, 1/64 duty cycle).

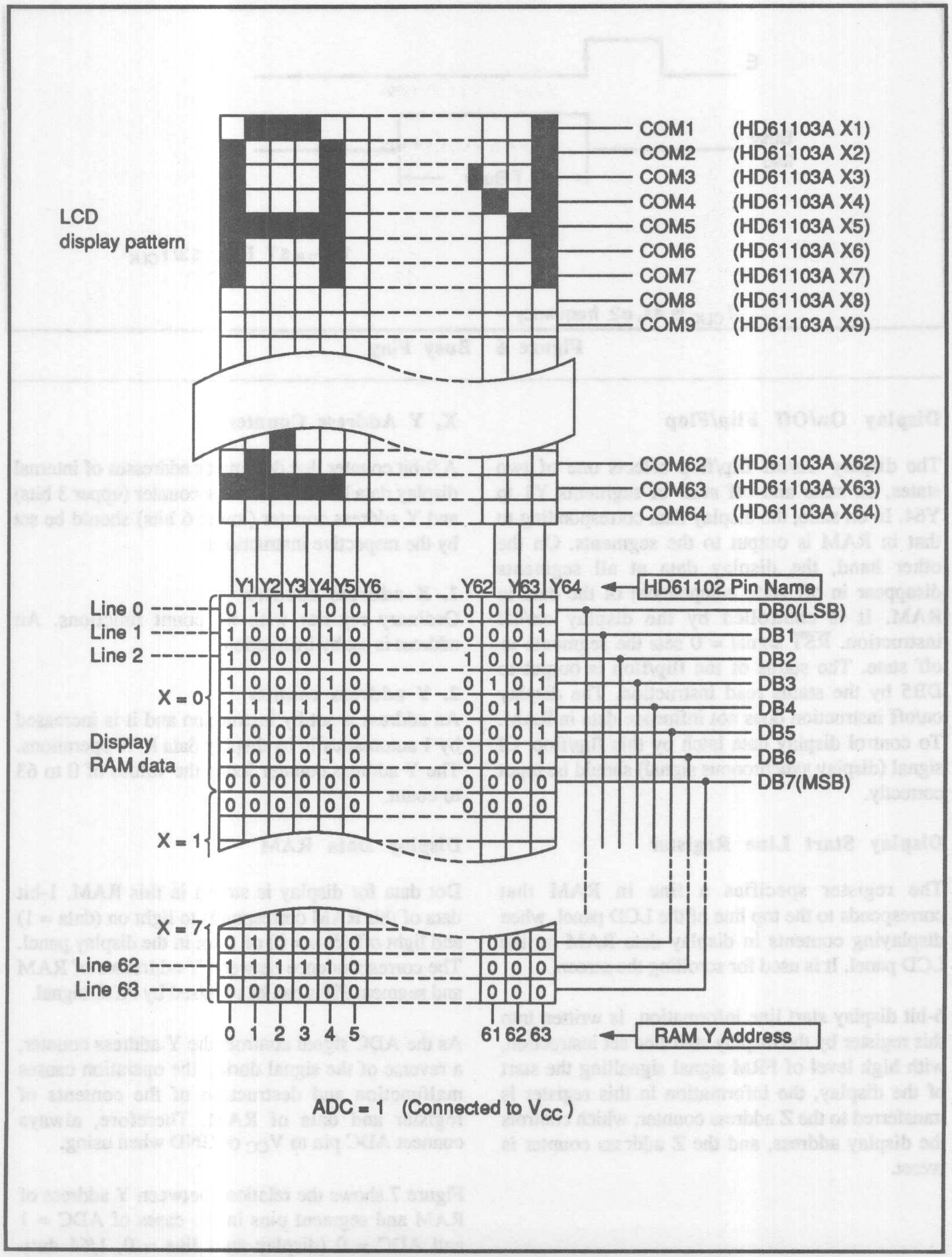


Figure 7 Relation between RAM Data and Display

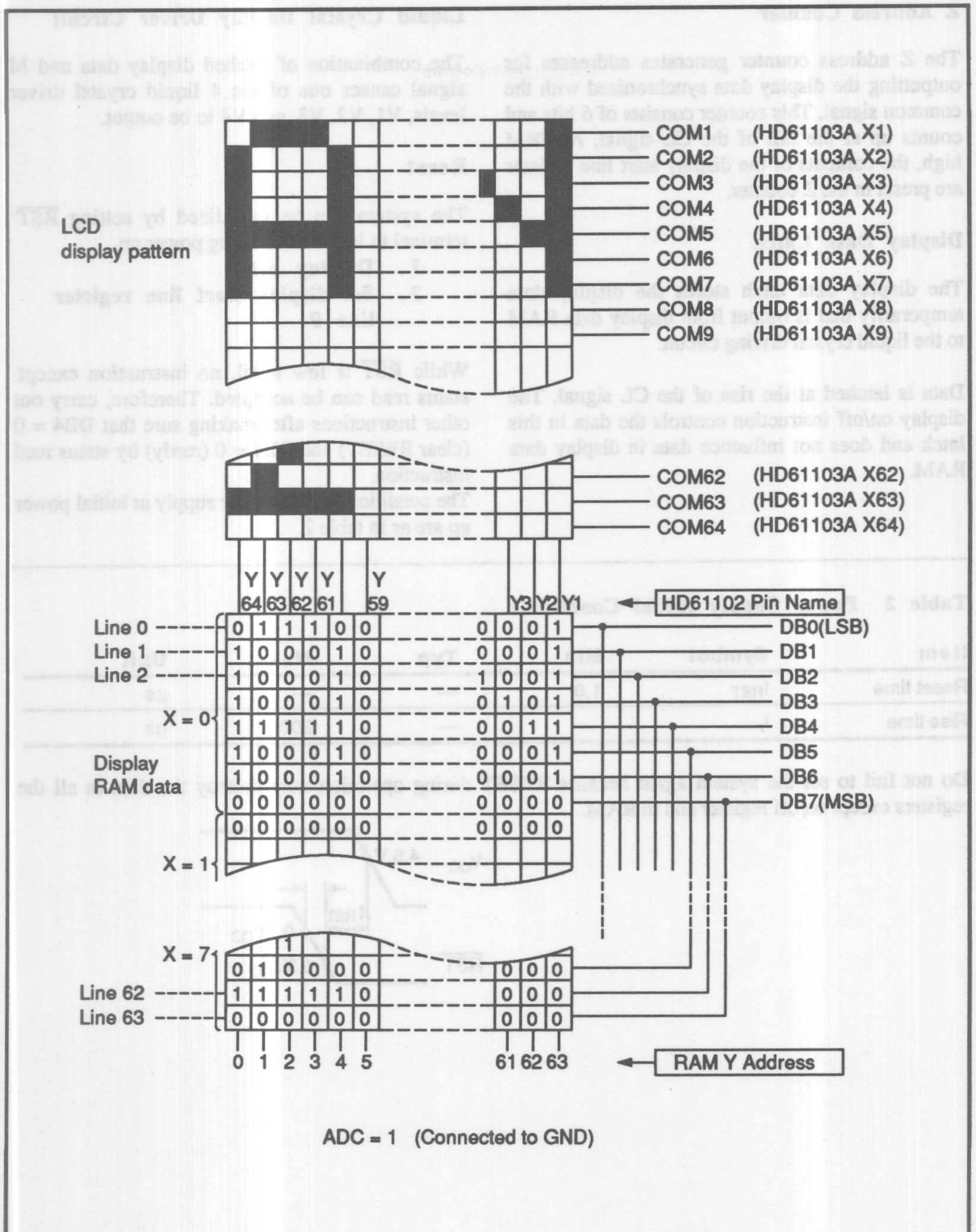


Figure 7 Relation between RAM Data and Display (cont)

Z Address Counter

The Z address counter generates addresses for outputting the display data synchronized with the common signal. This counter consists of 6 bits and counts up at the fall of the CL signal. At FRM high, the contents of the display start line register are preset in the Z counter.

Display Data Latch

The display data latch stores the display data temporarily that is output from display data RAM to the liquid crystal driving circuit.

Data is latched at the rise of the CL signal. The display on/off instruction controls the data in this latch and does not influence data in display data RAM.

Liquid Crystal Display Driver Circuit

The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3, and V4 to be output.

Reset

The system can be initialized by setting $\overline{RST}$ terminal to low when turning power on.

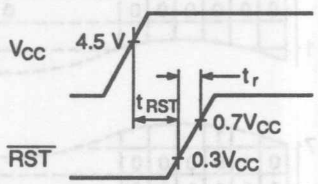
1. **Display off**
2. **Set display start line register line 0**

While $\overline{RST}$ is low level, no instruction except status read can be accepted. Therefore, carry out other instructions after making sure that DB4 = 0 (clear RESET) and DB7 = 0 (ready) by status read instruction.
The conditions of the power supply at initial power up are as in table 2.

Table 2 Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	—	—	µs
Rise time	t_r	—	—	200	ns

Do not fail to set the system again because RESET during operation may destroy the data in all the registers except on/off register and in RAM.



Display Control Instructions

Outline

Table 3 shows the instructions. Read/write (R/W) signal, data/instruction (D/I) signal and data bus signals (DB0 to DB7) are also called instructions because the internal operation depends on the signals from MPU.

These explanations are detailed in the following pages. Generally, there are the following three kinds of instructions.

1. Instruction to set addresses in the internal RAM
2. Instruction to transfer data from/to the internal RAM
3. Other instructions

In general use, the second type of instruction are used most frequently. Since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be shortened. During the execution of an instruction, the system cannot accept instructions other than the status read instruction. Send instructions from MPU after making sure that the busy flag is 0, which is the proof that an instruction is not being excuted.

Table 3 Instructions

<table>
<tr><th rowspan="2">Instructions</th><th colspan="10">Code</th><th rowspan="2" colspan="2">Functions</th></tr>
<tr><th>R/W</th><th>D/I</th><th>DB7</th><th>DB6</th><th>DB5</th><th>DB4</th><th>DB3</th><th>DB2</th><th>DB1</th><th>DB0</th></tr>
<tr><td>Display on/off</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1/0</td><td colspan="2">Controls display on/off. RAM data and internal status are not affected. 1: on, 0: off.</td></tr>
<tr><td>Display start line</td><td>0</td><td>0</td><td>1</td><td>1</td><td colspan="6">Display start line (0–63)</td><td colspan="2">Specifies the RAM line displayed at the top of the screen.</td></tr>
<tr><td>Set page (X address)</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td colspan="3">Page (0–7)</td><td colspan="2">Sets the page (X address) of RAM in the page (X address) register.</td></tr>
<tr><td>Set Y address</td><td>0</td><td>0</td><td>0</td><td>1</td><td colspan="6">Y address (0–63)</td><td colspan="2">Sets the Y address in the Y address counter.</td></tr>
<tr><td>Status read</td><td>1</td><td>0</td><td>Busy</td><td>0</td><td>ON/ OFF</td><td>RE- SET</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">Reads the status.
RESET 1: Reset
0: Normal
ON/OFF 1: Display off
0: Display on
Busy 1: Executing internal operation
0: Ready</td></tr>
<tr><td>Write display data</td><td>0</td><td>1</td><td colspan="8">Write data</td><td>Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM.</td><td rowspan="2">Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.</td></tr>
<tr><td>Read display data</td><td>1</td><td>1</td><td colspan="8">Read data</td><td>Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.</td></tr>
</table>

Note: 1. Busy time varies with the frequency (f_{CLK}) of $\phi1$, and $\phi2$.
($1/f_{CLK} \leq T_{BUSY} \leq 3/f_{CLK}$)

Detailed Explanation

1. Display on/off

	R/W	D/I	DB7							DB0
Code	0	0	0	0	1	1	1	1	1	D

← high-order bit   low-order bit →

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen when D = 0, it remains in the display data RAM. Therefore, you can make it appear by changing D = 0 into D = 1.

2. Display start line

	R/W	D/I	DB7							DB0
Code	0	0	1	1	A	A	A	A	A	A

← high-order bit   low-order bit →

Z address AAAAAA (binary) of the display data RAM is set in the display start line register and displayed at the top of the screen.

Figure 7 shows examples of display (1/64 duty cycle) when the start line = 0–3. When the display duty cycle is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

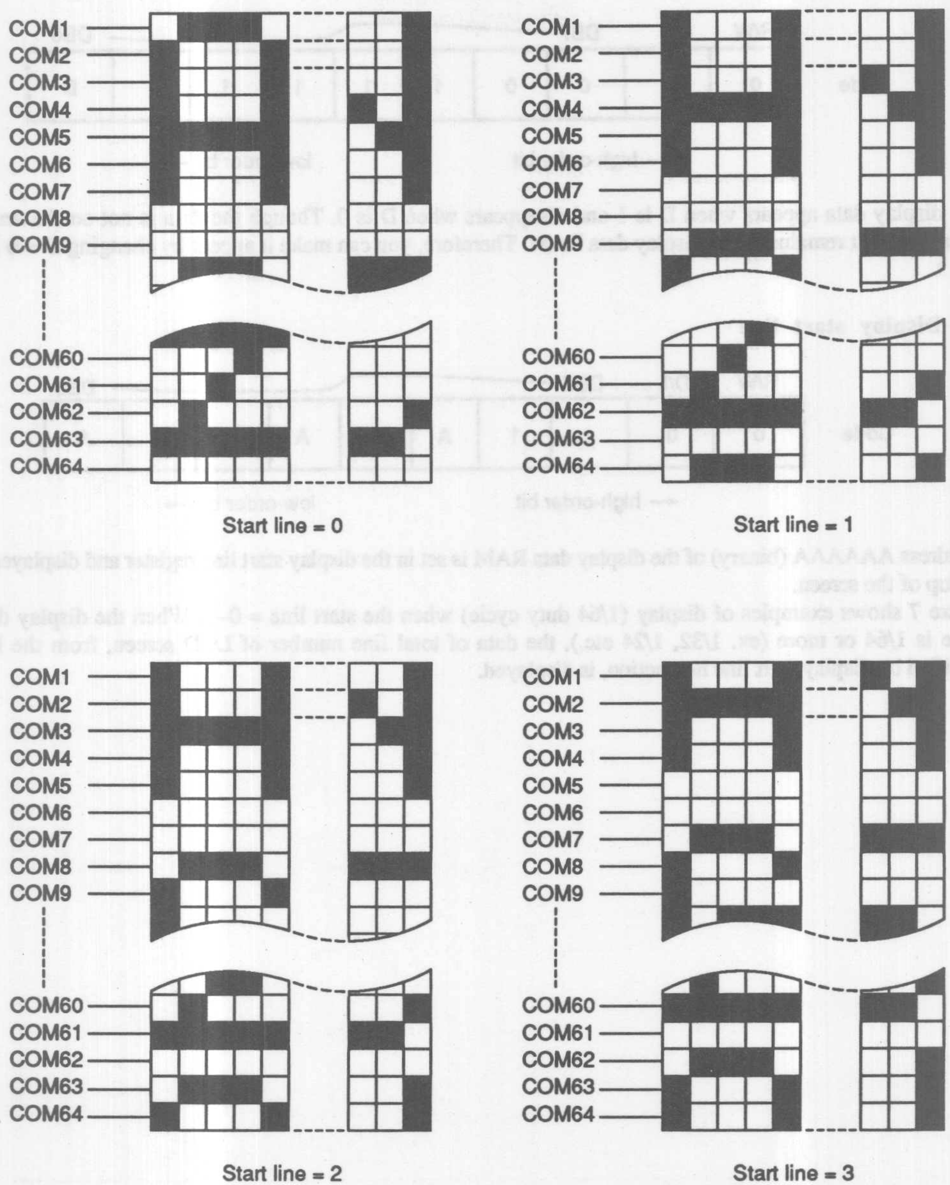


Figure 7 Relation Between Start Line and Display

3. Set page (X address)

	R/W	D/I	DB7							DB0
Code	0	0	1	0	1	1	1	A	A	A

← high-order bit   low-order bit →

X address AAA (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set. See figure 8.

4. Set Y address

	R/W	D/I	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← high-order bit   low-order bit →

Y address AAAAAA (binary) of the display data RAM is set in the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

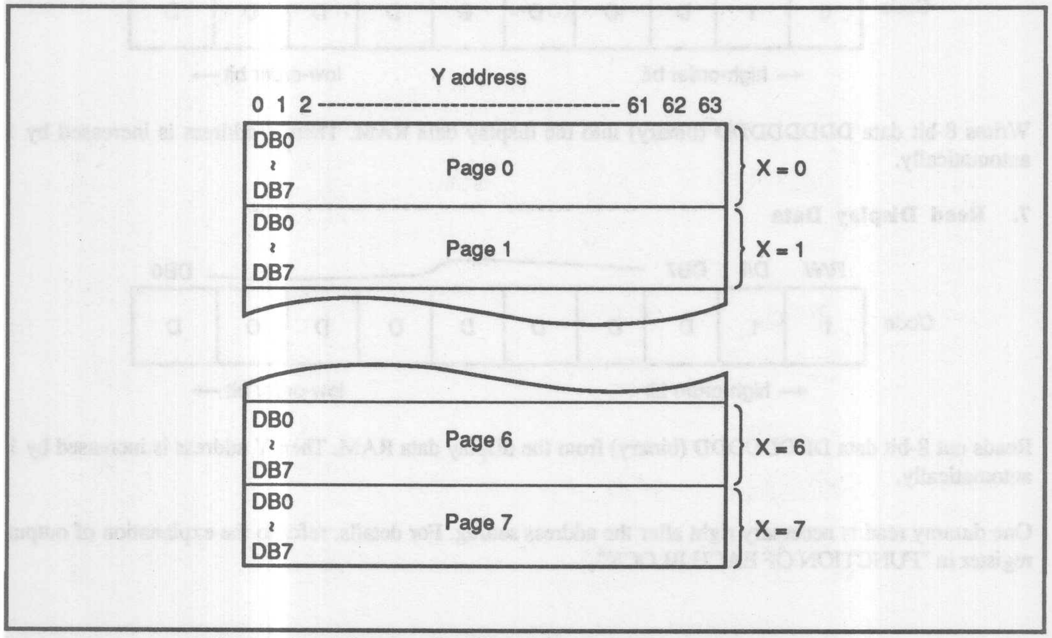


Figure 8 Address Configuration of Display Data RAM

5. Status Read

	R/W	D/I	DB7							DB0
Code	1	0	Busy	0	ON/OFF	RESET	0	0	0	0

← high-order bit low-order bit →

Busy: When Busy is 1, the LSI is executing internal operations. No instructions are accepted while Busy is 1, so you should make sure that Busy is 0 before writing the next instruction.

ON/OFF: Shows the liquid crystal display conditions: on condition or off condition.
When ON/OFF is 1, the display is in off condition.
When ON/OFF is 0, the display is in on condition.

RESET: RESET = 1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted.
RESET = 0 shows that initializing has finished and the system is in the usual operation condition.

6. Write Display Data

	R/W	D/I	DB7							DB0
Code	0	1	D	D	D	D	D	D	D	D

← high-order bit low-order bit →

Writes 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

7. Read Display Data

	R/W	D/I	DB7							DB0
Code	1	1	D	D	D	D	D	D	D	D

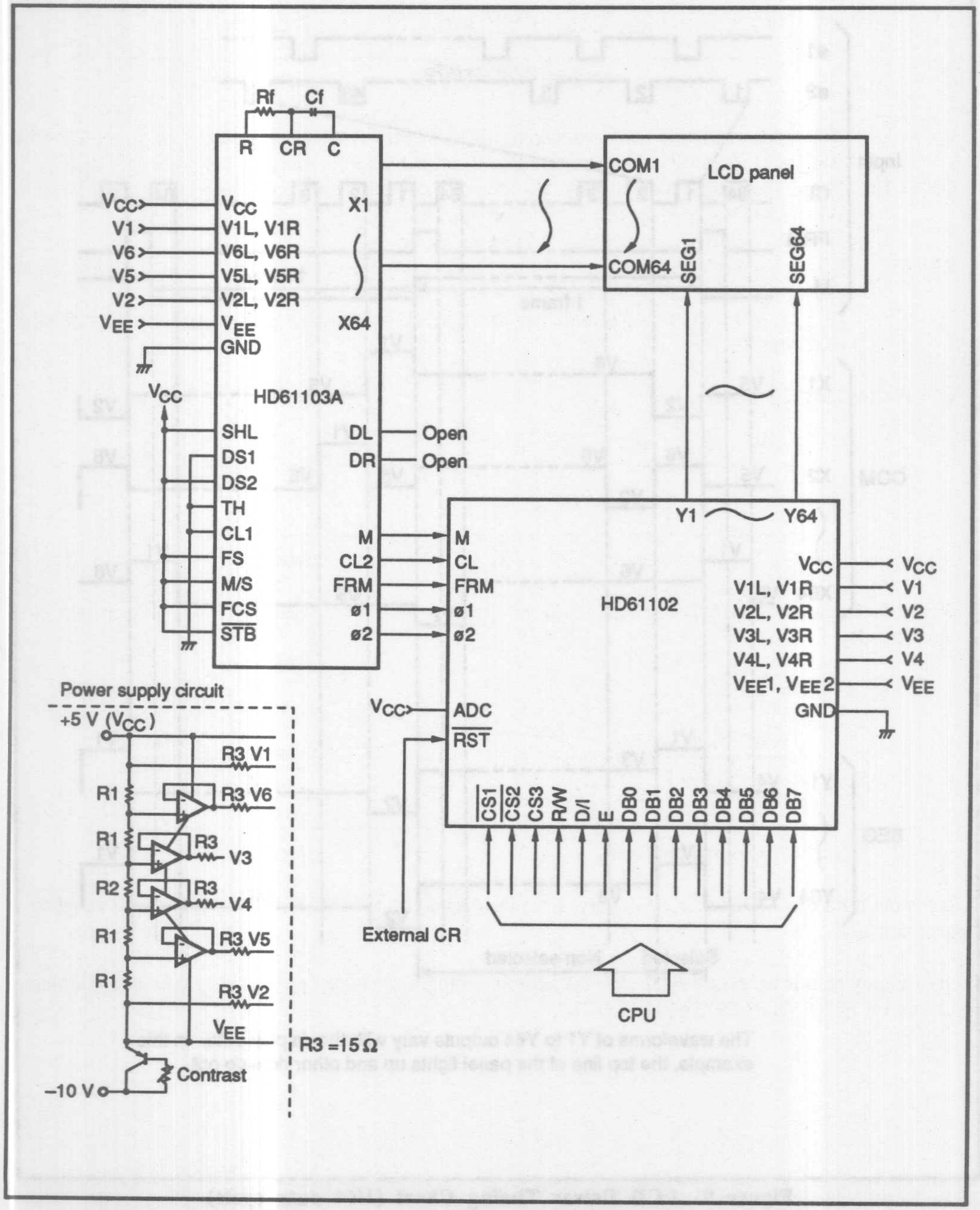
← high-order bit low-order bit →

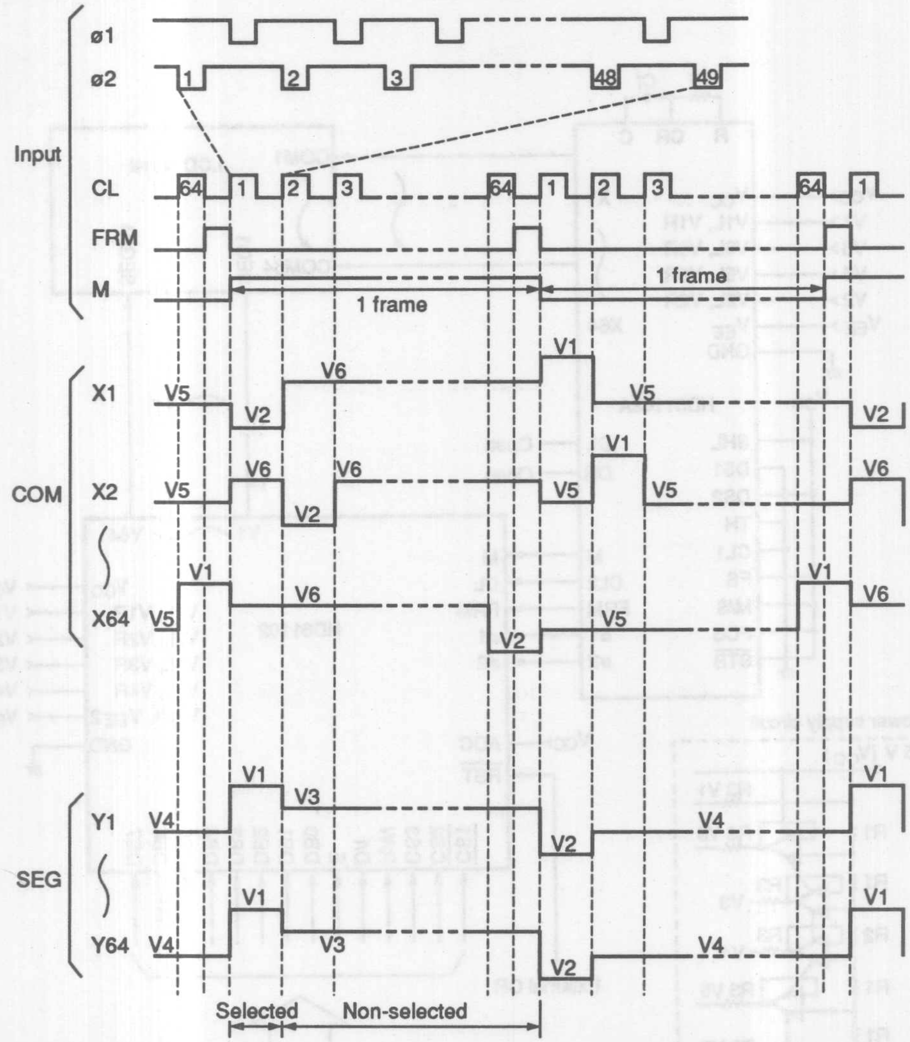
Reads out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.

One dummy read is necessary right after the address setting. For details, refer to the explanation of output register in "FUNCTION OF EACH BLOCK".

Use of HD61102

Interface with HD61103A (1/64 duty cycle)





The waveforms of Y1 to Y64 outputs vary with the display date. In this example, the top line of the panel lights up and other dots do not.

Figure 9 LCD Driver Timing Chart (1/64 duty cycle)

Interface with CPU

1. Example of connection with HD6800

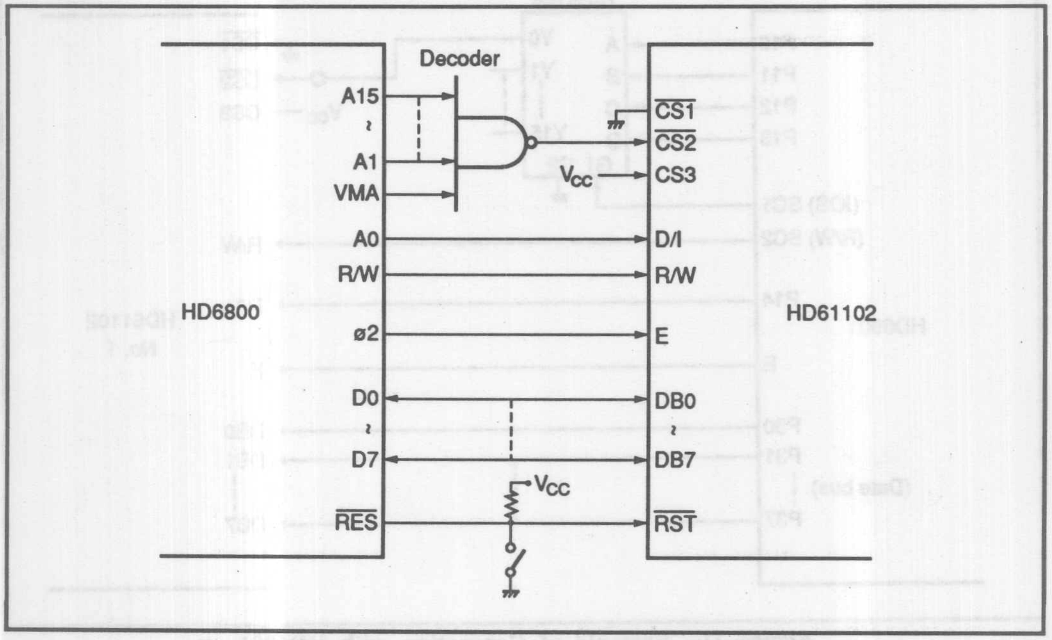


Figure 10 Example of Connection with HD6800 Series

In this decoder (figure 10), addresses of HD61102 in the address area of HD6800 are:

Read/write of the display data	$FFFF
Write of display instruction	$FFFE
Read out of status	$FFFE

Therefore, you can control HD61102 by reading/writing the data at these addresses.

2. Example of connection with HD6801

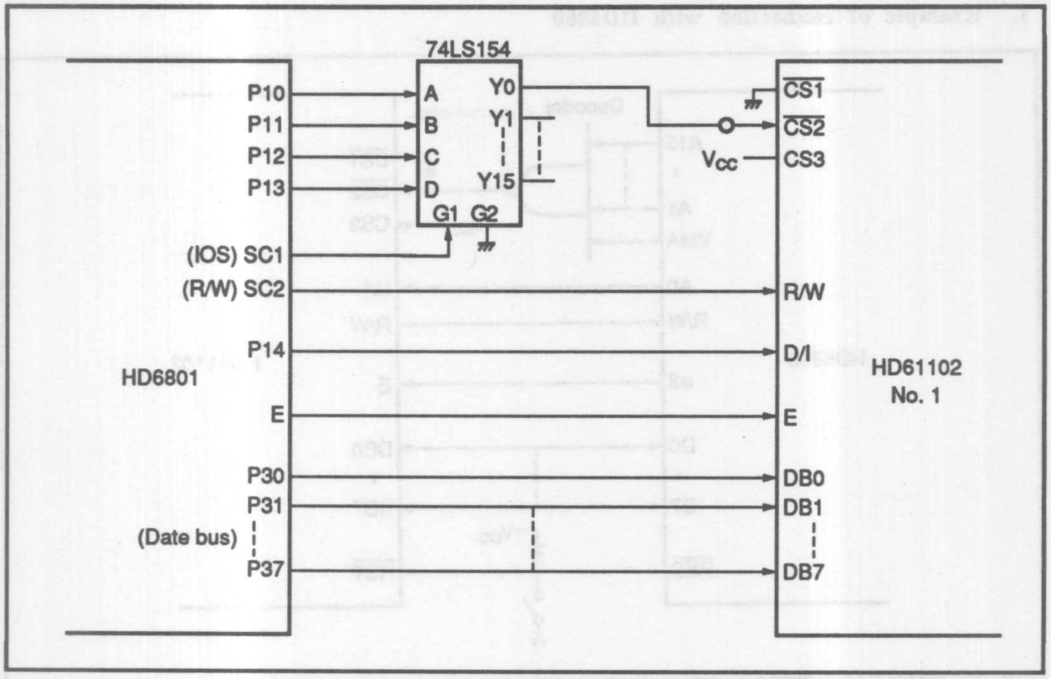


Figure 11 Example of Connection with HD6801

- Set HD6801 to mode 5. P10 to P14 are used as the output port and P30 to P37 as the data bus (table 11).
- 74LS154 4–to–16 decoder generates chip select signal to make specified HD61102 active after decoding 4 bits of P10 to P13.
- Therefore, after enabling the operation by P10 to P13 and specifying D/I signal by P14, read/write from/to the external memory area ($0100 to $01FE) to control HD61102. In this case, IOS signal is output from SC1 and R/W signal from SC2.
- For details of HD6800 and HD6801, refer to their manuals.

Example of Application

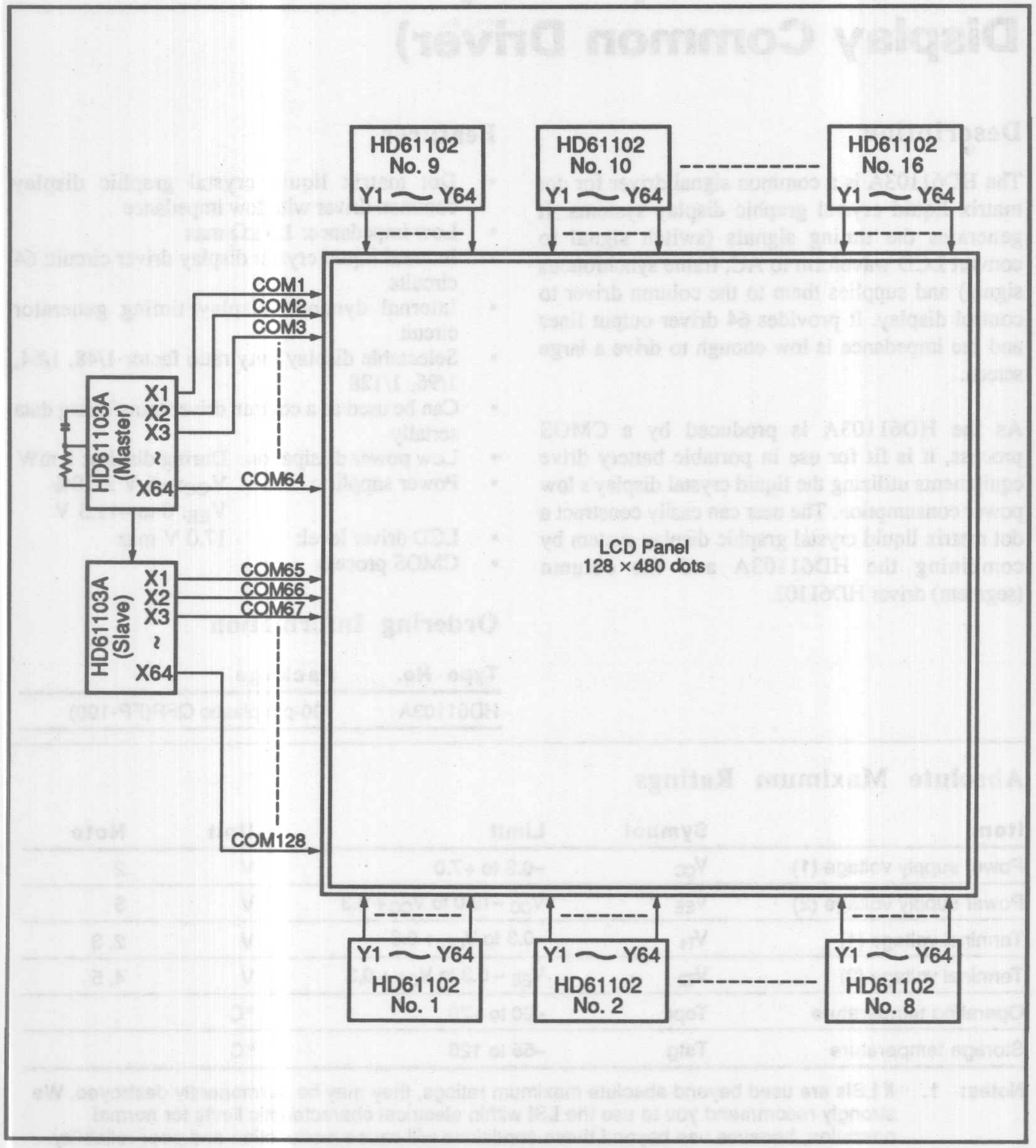


Figure 12 Application Example

Note: In this example (figure 12), two HD61103As output the equivalent waveforms. So, stand-alone operation is possible. In this case, connect COM1 and COM65 to X1, COM2 and COM66 to X2, ..., and COM64 and COM128 to X64. However, for the large screen display, it is better to drive in 2 rows as in this example to guarantee the display quality.

HD61103A
(Dot Matrix Liquid Crystal Graphic Display Common Driver)

Description

The HD61103A is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals (switch signal to convert LCD waveform to AC, frame synchronous signal) and supplies them to the column driver to control display. It provides 64 driver output lines and the impedance is low enough to drive a large screen.

As the HD61103A is produced by a CMOS process, it is fit for use in portable battery drive equipments utilizing the liquid crystal display's low power consumption. The user can easily construct a dot matrix liquid crystal graphic display system by combining the HD61103A and the column (segment) driver HD61102.

Features

- Dot matrix liquid crystal graphic display common driver with low impedance
- Low impedance: 1.5 kΩ max
- Internal liquid crystal display driver circuit: 64 circuits
- Internal dynamic display timing generator circuit
- Selectable display duty ratio factor 1/48, 1/64, 1/96, 1/128
- Can be used as a column driver transferring data serially
- Low power dissipation: During display: 5 mW
- Power supplies: V_{CC}: +5 V ± 10%
  V_{EE}: 0 to –11.5 V
- LCD driver level: 17.0 V max
- CMOS process

Ordering Information

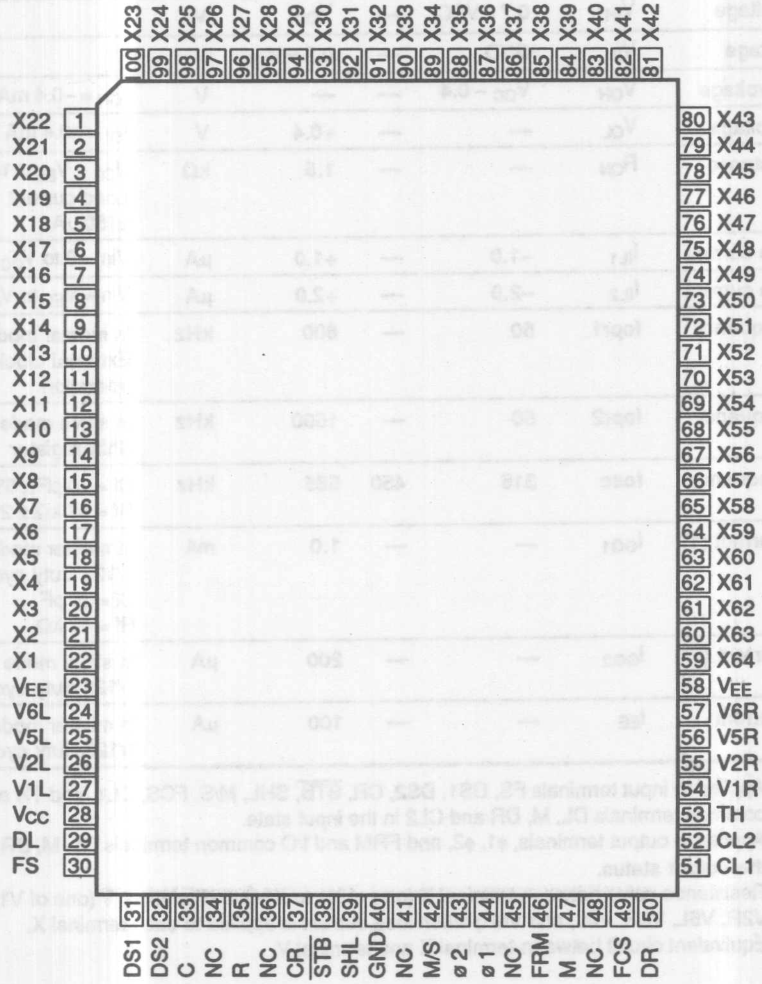
Type No.	Package
HD61103A	100-pin plastic QFP(FP-100)

Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Note
Power supply voltage (1)	V_{CC}	–0.3 to +7.0	V	2
Power supply voltage (2)	V_{EE}	V_{CC} –19.0 to V_{CC} + 0.3	V	5
Terminal voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4, 5
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to 125	°C	

Notes: 1. If LSIs are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend you to use the LSI within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.
2. Based on GND = 0 V.
3. Applies to input terminals (except V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R) and I/O common terminals at high impedance.
4. Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R.
5. Apply the same value of voltages to V1L and V1R, V2L and V2R, V5L and V5R, V6L and V6R, V_{EE} (23 pin) and V_{EE} (58 pin) respectively.
Maintain V_{CC} ≥ V1L = V1R ≥ V6L = V6R ≥ V5L = V5R ≥ V2L = V2R ≥ V_{EE}

Pin Arrangement



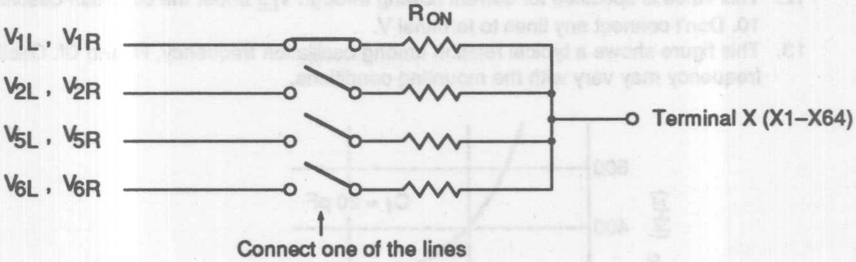
(Top view)

Electrical Characteristics

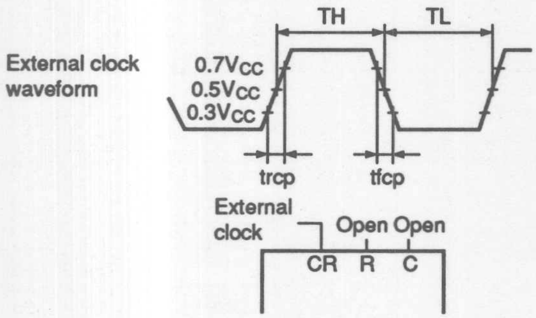
DC Characteristics (V_{CC} = +5 V ± 10%, GND = 0 V, V_{EE} = 0 to –11.5 V, Ta = –20 to +75°C)

Test Item	Symbol	Specifications Min	Specifications Typ	Specifications Max	Unit	Test Conditions	Note
Input high voltage	V_{IH}	0.7 × VCC	—	V_{CC}	V		1
Input low voltage	V_{IL}	GND	—	0.3 × V_{CC}	V		1
Output high voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	2
Output low voltage	V_{OL}	—	—	+0.4	V	I_{Ol} = +0.4 mA	2
Vi-Xj on resistance	R_{ON}	—	—	1.5	kΩ	V_{CC} – V_{EE} = 10 V Load current ±150 µA	3
Input leakage current	I_{IL1}	–1.0	—	+1.0	µA	Vin = 0 to V_{CC}	4
Input leakage current	I_{IL2}	–2.0	—	+2.0	µA	Vin = V_{EE} to V_{CC}	5
Operating frequency	fopr1	50	—	600	kHz	In master mode External clock operation	6
Operating frequency	fopr2	50	—	1500	kHz	In slave mode Shift register	7
Oscillation frequency	fosc	315	450	585	kHz	Cf = 20 pF ± 5% Rf = 47 kΩ ± 2%	8, 13
Dissipation current (1)	I_{GG1}	—	—	1.0	mA	In master mode 1/128 duty cycle Cf = 20 pF Rf = 47 kΩ	9, 10
Dissipation current (2)	I_{GG2}	—	—	200	µA	In slave mode 1/128 duty cycle	9, 11
Dissipation current	I_{EE}	—	—	100	µA	In master mode 1/128 duty cycle	9, 12

Notes:
1. Applies to input terminals FS, DS1, DS2, CR, $\overline{STB}$, SHL, M/S, FCS, CL1, and TH and I/O common terminals DL, M, DR and CL2 in the input state.
2. Applies to output terminals, ϕ1, ϕ2, and FRM and I/O common terminals DL, M, DR, and CL2 in the output status.
3. Resistance value between terminal X (one of X1 to X64) and terminal V (one of V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R) when load current is applied to each terminal X. Equivalent circuit between terminal X and terminal V.



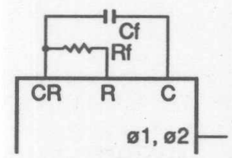
4. Applies to input terminals FS, DS1, DS2, CR, $\overline{\text{STB}}$, SHL, M/S, FCS, CL1, and TH, I/O common terminals DL, M, DR and CL2 in the input status and NC terminals.
5. Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R. Don't connect any lines to X1 to X64.
6. External clock is as follows.



$$\text{Duty cycle} = \frac{TH}{TH + TL} \times 100\%$$

	Min	Typ	Max	Unit
Duty cycle	45	50	55	%
trcp	–	–	50	ns
tfcp	–	–	50	ns

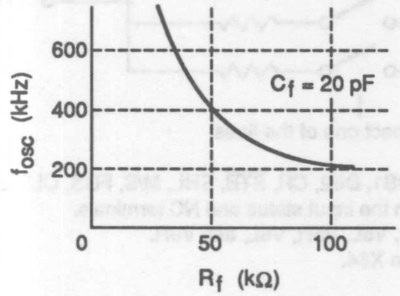
7. Applies to the shift register in the slave mode. For details, refer to AC Characteristics.
8. Connect oscillation resistor (Rf) and oscillation capacitance (Cf) as shown in this figure. Oscillation frequency (f_{OSC}) is twice as much as the frequency ($f\phi$) at ϕ1 or ϕ2.



Cf = 20 pF
Rf = 47 kΩ fosc = 2 × fø

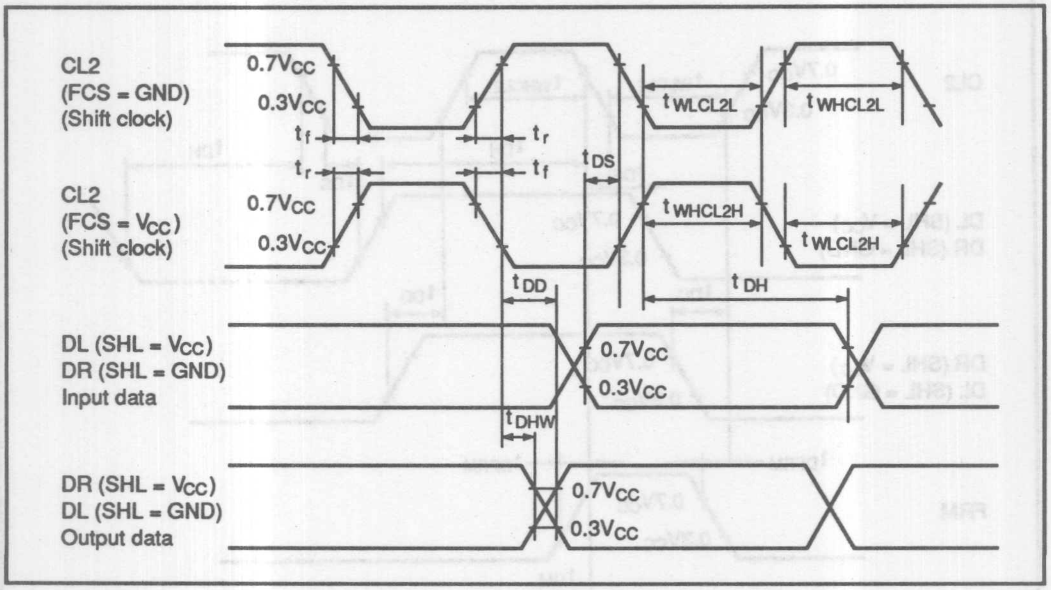
9. No lines are connected to output terminals and current flowing through the input circuit is excluded. This value is specified at $V_{IH} = V_{CC}$ and V_{IL} = GND.
10. This value is specified for current flowing through GND in the following conditions: Internal oscillation circuit is used. Each terminal of DS1, DS2, FS, SHL, M/S, $\overline{\text{STB}}$, and FCS is connected to V_{CC} and each of CL1 and TH to GND. Oscillator is set as described in note 8.
11. This value is specified for current flowing through GND under the following conditions: Each terminals of DS1, DS2, FS, SHL, $\overline{\text{STB}}$, FCS and CR is connected to V_{CC}, CL1, TH, and M/S to GND and the terminals CL2, M, and DL are respectively connected to terminals CL2, M, and DL of the HD61103A under the conditions described in note 10.

12. This value is specified for current flowing through V_{EE} under the condition described in note 10. Don't connect any lines to terminal V.
13. This figure shows a typical relation among oscillation frequency, Rf and Cf. Oscillation frequency may vary with the mounting conditions.



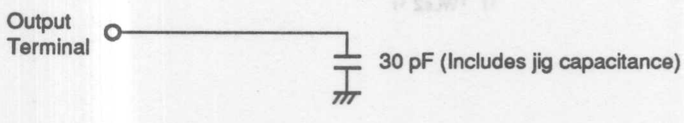
AC Characteristics
(V_{CC} = +5 V ± 10%, GND = 0 V, V_{EE} = 0 to –11.5 V, Ta = –20 to +75°C)

1. Slave Mode (M/S = GND)

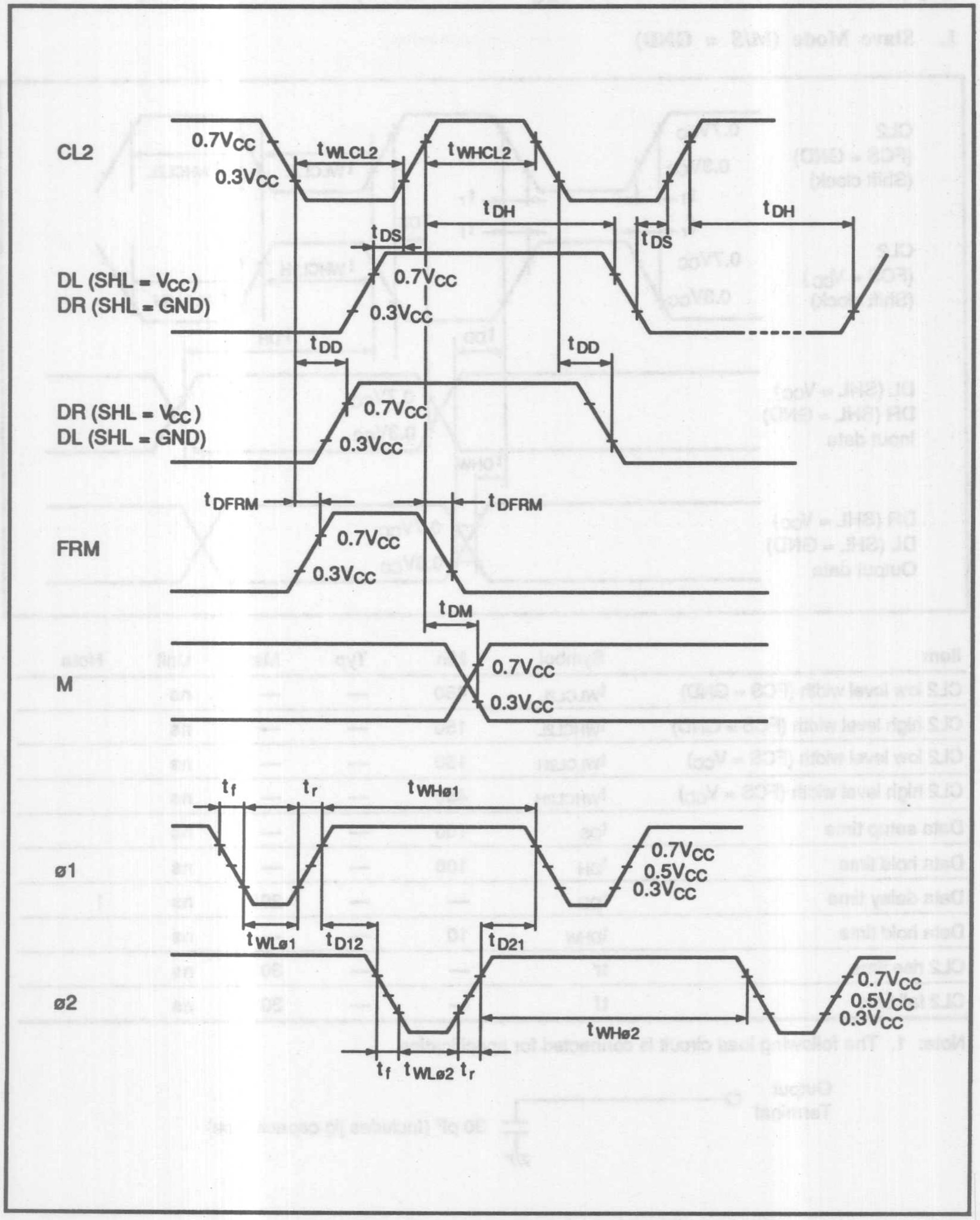


Item	Symbol	Min	Typ	Max	Unit	Note
CL2 low level width (FCS = GND)	t_{WLCL2L}	450	—	—	ns	
CL2 high level width (FCS = GND)	t_{WHCL2L}	150	—	—	ns	
CL2 low level width (FCS = V_{CC})	t_{WLCL2H}	150	—	—	ns	
CL2 high level width (FCS = V_{CC})	t_{WHCL2H}	450	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	100	—	—	ns	
Data delay time	t_{DD}	—	—	200	ns	1
Data hold time	t_{DHW}	10	—	—	ns	
CL2 rise time	tr	—	—	30	ns	
CL2 fall time	tf	—	—	30	ns	

Note: 1. The following load circuit is connected for specification.

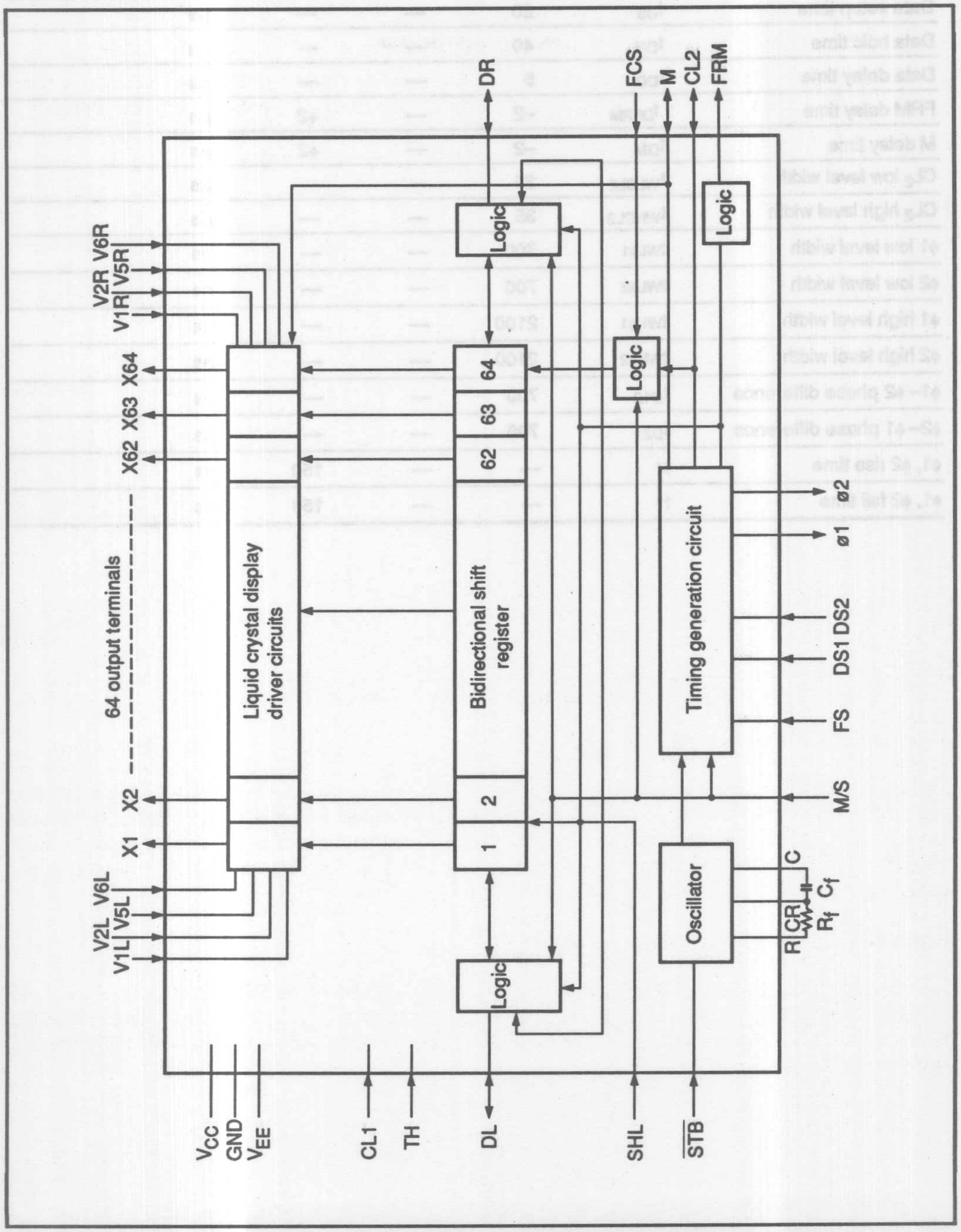


2. **Master Mode (M/S = V_{CC}, FCS = V_{CC}, Cf = 20 pF, Rf = 47 kΩ)**



Item	Symbol	Min	Typ	Max	Unit	Note
Data setup time	t_{DS}	20	—	—	μs	
Data hold time	t_{DH}	40	—	—	μs	
Data delay time	t_{DD}	5	—	—	μs	
FRM delay time	t_{DFRM}	–2	—	+2	μs	
M delay time	t_{DM}	–2	—	+2	μs	
CL_2 low level width	t_{WLCL2}	35	—	—	μs	
CL_2 high level width	t_{WHCL2}	35	—	—	μs	
ϕ1 low level width	$t_{WL\phi1}$	700	—	—	ns	
ϕ2 low level width	$t_{WL\phi2}$	700	—	—	ns	
ϕ1 high level width	$t_{WH\phi1}$	2100	—	—	ns	
ϕ2 high level width	$t_{WH\phi2}$	2100	—	—	ns	
ϕ1– ϕ2 phase difference	t_{D12}	700	—	—	ns	
ϕ2– ϕ1 phase difference	t_{D21}	700	—	—	ns	
ϕ1, ϕ2 rise time	tr	—	—	150	ns	
ϕ1, ϕ2 fall time	tf	—	—	150	ns	

Block Diagram



Block Functions

Oscillator

The CR oscillator generates display timing signals and operating clocks for the HD61102. It is required when the HD61103A is used with the HD61102. An oscillation resistor Rf and an oscillation capacitor Cf are attached as shown in figure 1 and terminal $\overline{\text{STB}}$ is connected to the high level. When using an external clock, input the clock into terminal CR and don't connect any lines to terminal R and C.

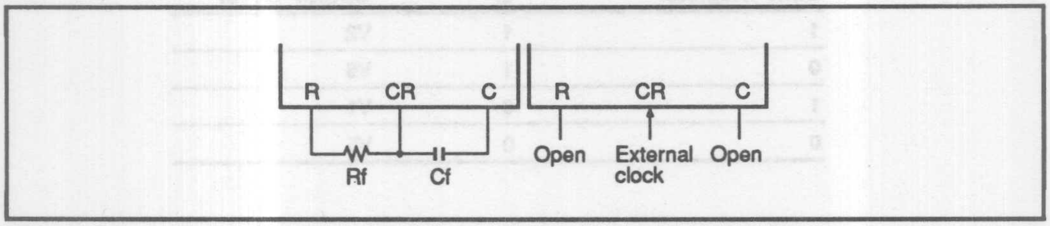


Figure 1 Oscillator Connection with HD61102

The oscillator is not required when the HD61103A is used with the HD61830. Connect terminal CR to the high level and don't connect any lines to terminals R and C (figure 2).

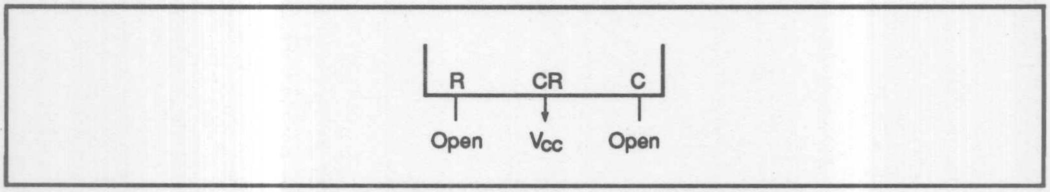


Figure 2 Oscillator Connection with HD61830

Timing Generator Circuit

The timing generator circuit generates display timing and operating clock for the HD61102. This circuit is required when the HD61103A is used with the HD61102. Connect terminal M/S to high level (master mode). It is not necessary when the display timing signal is supplied from other circuits, for example, from HD61830. In this case connect the terminals FS, DS1, and DS2 to high level and M/S to low level (slave mode).

Bidirectional Shift Register

A 64-bit bidirectional shift register. The data is shifted from DL to DR when SHL is at high level and from DR to DL when SHL is at low level. In this case, CL2 is used as shift clock. The lowest order bit of the bidirectional shift register, which is on the DL side, corresponds to X1 and the highest order bit on the DR side corresponds to X64.

Liquid Crystal Display Driver Circuit

The combination of the data from the shift register with the M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to the output terminals (table 1).

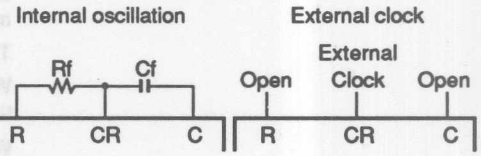
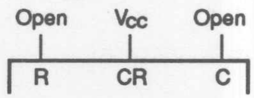
Table 1 Output Levels

Data from the Shift Register	M	Output Level
1	1	V2
0	1	V6
1	0	V1
0	0	V5

HD61103A Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Function
V_{CC} GND V_{EE}	1 1 2		Power supply	V_{CC} – GND: Power supply for internal logic. V_{CC} – V_{EE}: Power supply for driver circuit logic.
V1L, V2L, V5L, V6L, V1R, V2R, V5R, V6R	8		Power supply	Liquid crystal display driver level power supply. V1L (V1R), V2L (V2R): Selected level V5L (V5R), V6L (V6R): Non-selected level Voltages of the level power supplies connected to V1L and V1R should be the same. (This applies to the combination of V2L & V2R, V5L & V5R and V6L & V6R respectively)
M/S	1	I	V_{CC} or GND	Selects master/slave. M/S = V_{CC}: Master mode When the HD61103A is used with the HD61102, timing generation circuit operates to supply display timing signals and operation clock to the HD61102. Each of I/O common terminals DL, DR, CL2, and M is in the output state. M/S = GND: Slave mode The timing operation circuit stops operating. The HD61103A is used in this mode when combined with the HD61830. Even if combined with the HD61102, this mode is used when display timing signals (M, data, CL2, etc.) are supplied by another HD61103A in the master mode. Terminals M and CL2 are in the input state. When SHL is V_{CC}, DL is in the input state and DR is in the output state. When SHL is GND, DL is in the output state and DR is in the input state.
FCS	1	I	V_{CC} or GND	Selects shift clock phase. FCS = V_{CC}: Shift register operates at the rising edge of CL2. Select this condition when HD61103A is used with HD61102 or when MA of the HD61830 connects to CL2 in combination with the HD61830. FCS = GND: Shift register operates at the fall of CL2. Select this condition when CL1 of HD61830 connects to CL2 in combination with the HD61830.

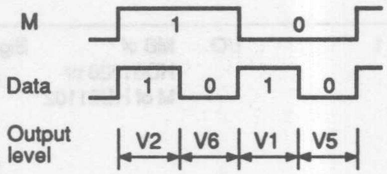
HD61103A Terminal Functions (cont)

<table>
<tr><th>Terminal Name</th><th>Number of Terminals</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>FS</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects frequency.
When the frame frequency is 70 Hz, the oscillation frequency should be:
fosc = 430 kHz at FCS = V_{CC}
fosc = 215 kHz at FCS = GND
This terminal is active only in the master mode. Connect it to V_{CC} in the slave mode.</td></tr>
<tr><td>DS1, DS2</td><td>2</td><td>I</td><td>V_{CC} or GND</td><td>Selects display duty factor.
<table><tr><th>Display Duty Factor</th><th>1/48</th><th>1/64</th><th>1/96</th><th>1/128</th></tr><tr><td>DS1</td><td>GND</td><td>GND</td><td>V_{CC}</td><td>V_{CC}</td></tr><tr><td>DS2</td><td>GND</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td></tr></table>These terminals are valid only in the master mode. Connect them to V_{CC} in the slave mode.</td></tr>
<tr><td>$\overline{STB}$
TH
CL1</td><td>1
1
1</td><td>I</td><td>V_{CC} or GND</td><td>Input terminal for testing.
Connect $\overline{STB}$ to V_{CC}.
Connect TH and CL1 to GND.</td></tr>
<tr><td>CR, R, C</td><td>3</td><td></td><td></td><td>Oscillator.
In the master mode, use these terminals as shown below.
Usage of these terminals in the master mode:

In the slave mode, stop the oscillator as shown below:
</td></tr>
<tr><td>ϕ1, ϕ2</td><td>2</td><td>O</td><td>HD61102</td><td>Operating clock output terminals for the HD61102.
Master mode: Connect these terminals to terminals ϕ1 and ϕ2 of the HD61102 respectively.
Slave mode: Don't connect any lines to these terminals.</td></tr>
</table>

HD61103A Terminal Functions (cont)

<table>
<tr><th>Terminal Name</th><th>Number of Terminals</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>FRM</td><td>1</td><td>O</td><td>HD61102</td><td>Frame signal.
Master mode: Connect this terminal to terminal FRM of the HD61102.
Slave mode: Don't connect any lines to this terminal.</td></tr>
<tr><td>M</td><td>1</td><td>I/O</td><td>MB of HD61830 or M of HD61102</td><td>Signal to convert LCD driver signal into AC.
Master mode: Output terminal
Connect this terminal to terminal M of the HD61102.
Slave mode: Input terminal.
Connect this terminal to terminal MB of the HD61830.</td></tr>
<tr><td>CL2</td><td>1</td><td>I/O</td><td>CL1 or MA of HD61830 or CL of HD61102</td><td>Shift clock.
Master mode: Output terminal
Connect this terminal to terminal CL of the HD61102.
Slave mode: Input terminal
Connect this terminal to terminal CL1 or MA of the HD61830.</td></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Open or FLM of HD61830</td><td>Data I/O terminals of bidirectional shift register.
DL corresponds to X1's side and DR to X64's side.
Master mode: Output common scanning signal. Don't connect any lines to these terminals normally.
Slave mode: Connect terminal FLM of the HD61830 to DL (when SHL = V_{CC}) or DR (when SHL = GND)
<table>
<tr><th>M/S</th><th colspan="2">V_{CC}</th><th colspan="2">GND</th></tr>
<tr><td>SHL</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td><td>GND</td></tr>
<tr><td>DL</td><td>Output</td><td>Output</td><td>Input</td><td>Output</td></tr>
<tr><td>DR</td><td>Output</td><td>Output</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>NC</td><td>5</td><td></td><td>Open</td><td>Not used.
Don't connect any lines to this terminal.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects shift direction of bidirectional shift register.
<table>
<tr><th>SHL</th><th>Shift Direction</th><th>Common Scanning Direction</th></tr>
<tr><td>V_{CC}</td><td>DL → DR</td><td>X1 → X64</td></tr>
<tr><td>GND</td><td>DL ← DR</td><td>X1 ← X64</td></tr>
</table></td></tr>
</table>

HD61103A Terminal Functions (cont)

Terminal Name	Number of Terminals	I/O	Connected to	Function
X1-X64	64	O	Liquid crystal display	Liquid crystal display driver output. Output one of the four liquid crystal display driver levels V1, V2, V5, and V6 with the combination of the dat from the shift register and M signal.  Data 1: Selected level 0: Non–selected level When SHL is V_{CC}, X1 corresponds to COM1 and X64 corresponds to COM64. When SHL is GND, X64 corresponds to COM1 and X1 corresponds to COM64.

Example of Application

HD61103A Connection List

H: V_{CC} } Fixed
L: GND

"—" means "open".

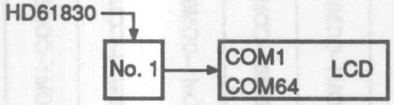
Rf: Oscillation resister
Cf: Oscillation capacitor

	M/S	TH	CL1	FCS	FS	DS1	DS2	$\overline{STB}$	CR	R	C	$\phi1$	$\phi2$	FRM	M	CL2	SHL	DL	DR	X1–X64
A	L	L	L	L	H	H	H	H	H	—	—	—	—	—	from MB of HD61830	from CL1 of HD61830	H	from FLM of HD61830	—	COM1–COM64
																	L	—	from FLM of HD61830	COM64–COM1
B	L	L	L	H	H	H	H	H	H	—	—	—	—	—	from MB of HD61830	from MA of HD61830	H	from FLM of HD61830	to DL/DR of HD61103A No. 2	COM1–COM64
																	L	to DL/DR of HD61103A No. 2	from FLM of HD61830	COM64–COM1
C	L	L	L	H	H	H	H	H	H	—	—	—	—	—	from MB of HD61830	from MA of HD61830	H	from DL/DR of HD61103A No. 1	—	COM65–COM128
																	L	—	from DL/DR of HD61103A No. 1	COM128–COM65
D	H	L	L	H	H	LL or LH		H	Rf Cf	Rf	Cf	to $\phi1$ of HD61102	to $\phi2$ of HD61102	to FRM of HD61102	to M of HD61102	to CL of HD61102	H	—	—	COM1–COM64
																	L	—	—	COM64–COM1
E	H	L	L	H	H	LL or LH		H	Rf Cf	Rf	Cf	to $\phi1$ of HD61102	to $\phi2$ of HD61102	to FRM of HD61102	toM of HD61102 HD61103A	to CL of HD61102 to CL2 of HD61103A	H	—	to DL/DR of HD61103A No. 2	COM1–COM64
																	L	to DL/DR of HD61103A No. 2	—	COM64–COM1
F	L	L	L	H	H	H	H	H	H	—	—	—	—	—	from M of HD61103A No. 1	from CL2 of HD61103A No. 1	H	from DL/DR of HD61103A No. 1	—	COM1–COM64
																	L	—	from DL/DR of HD61103A No. 1	COM64–COM1

Outline of HD61103A System Configuration

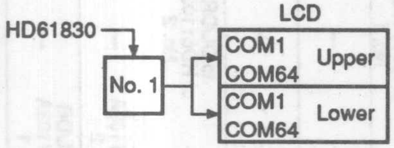
1. Use with HD61830

a. When display duty ratio of LCD is more than 1/64



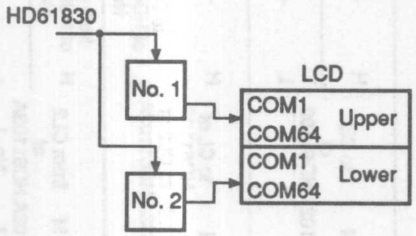
One HD61103A drives common signals.

Refer to Connection list A



One HD61103A drives common signals for upper and lower panels.

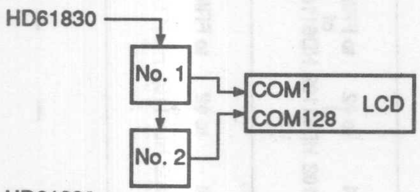
Refer to Connection list A



Two HD61103As drive upper and lower panel separately to ensure the quality of display. No. 1 and No. 2 operate in parallel.

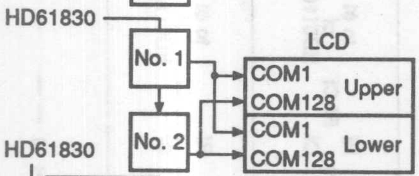
For both of No. 1 and No. 2, refer to Connection list A

b. When display duty ratio of LCD is from 1/65 to 1/128



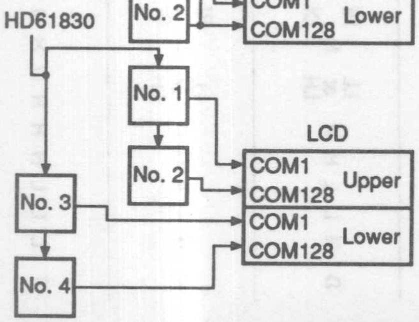
Two HD61103As connected serially drive common signals.

Refer to Connection list B for No. 1.
Refer to Connection list C for No. 2.



Two HD61103As connected serially drive upper and lower panels in parallel.

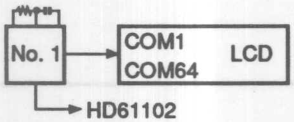
Refer to Connection list B for No. 1.
Refer to Connection list C for No. 2.



Two sets of HD61103As connected serially drive upper and lower panels in parallel to ensure the quality of display.

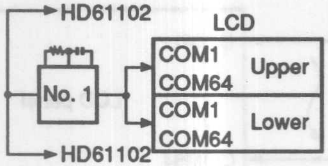
Refer to Connection list B for No. 1 and 3.
Refer to Connection list C for No. 2 and 4.

2. Use with HD61102 (1/64 duty ratio)



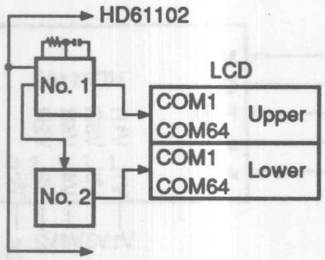
One HD61103A drives common signals and supplies timing signals to the HD61102s.

Refer to Connection list D



One HD61103A drives upper and lower panels and supplies timing signals to the HD61102s.

Refer to Connection list D



Two HD61103As drive upper and lower panels in parallel to ensure the quality of display. No. 1 supplies timing signals to No. 2 and the HD61102s.

Refer to Connection list E for No. 1

Refer to Connection list F for No. 2

Connection Example 1

Use with HD61102 (RAM type segment driver).
a. 1/64 duty ratio (See Connection List D)

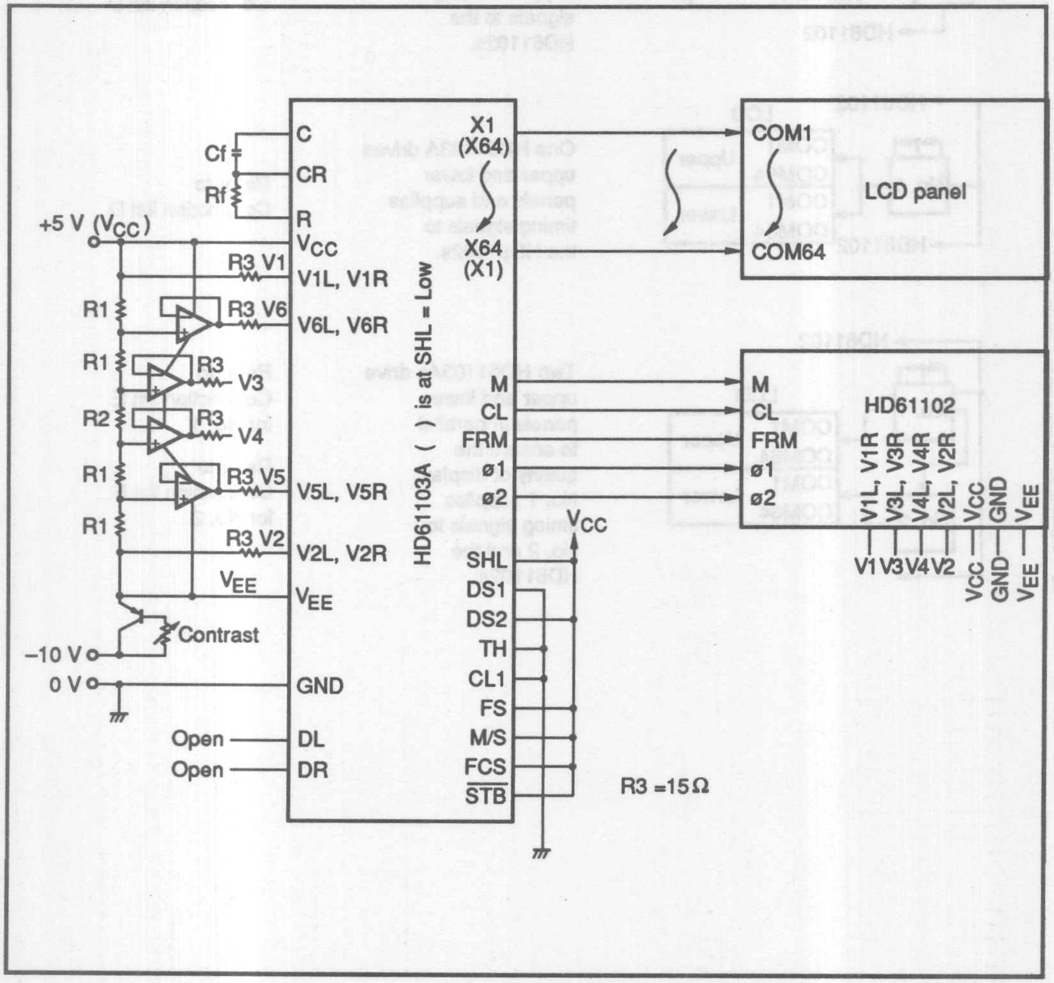


Figure 1 Example 1

Note: 1. The values of R1 and R2 vary with the LCD panel used.
When bias factor is 1/9, the values of R1 and R2 should satisfy

$$\frac{R1}{4R1 + R2} = \frac{1}{9}$$

For example,

R1 = 3 kΩ, R2 = 15 kΩ

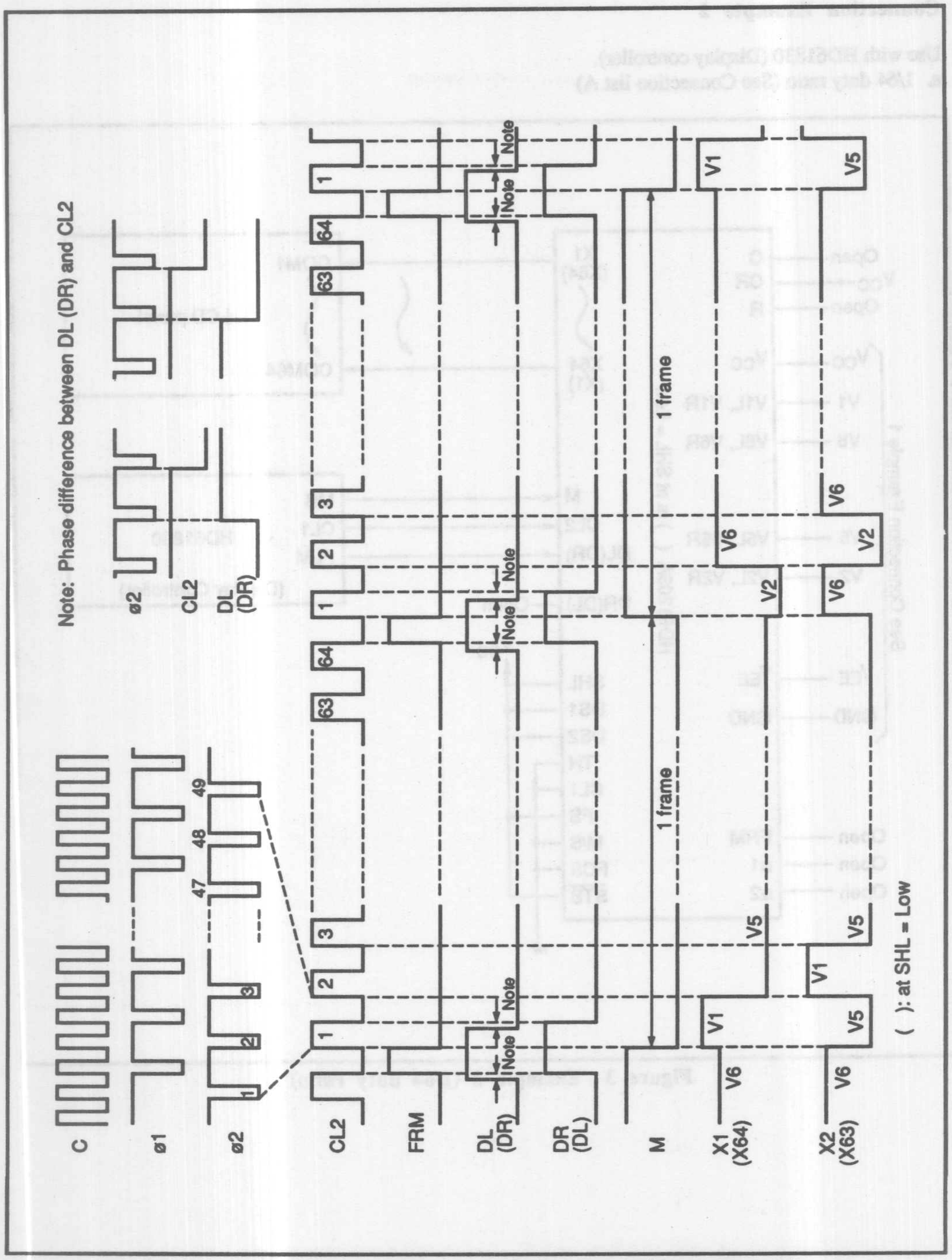


Figure 2 Example 1 Waveform (RAM type, 1/64 duty cycle)

Connection Example 2

Use with HD61830 (Display controller).
a. 1/64 duty ratio (See Connection list A)

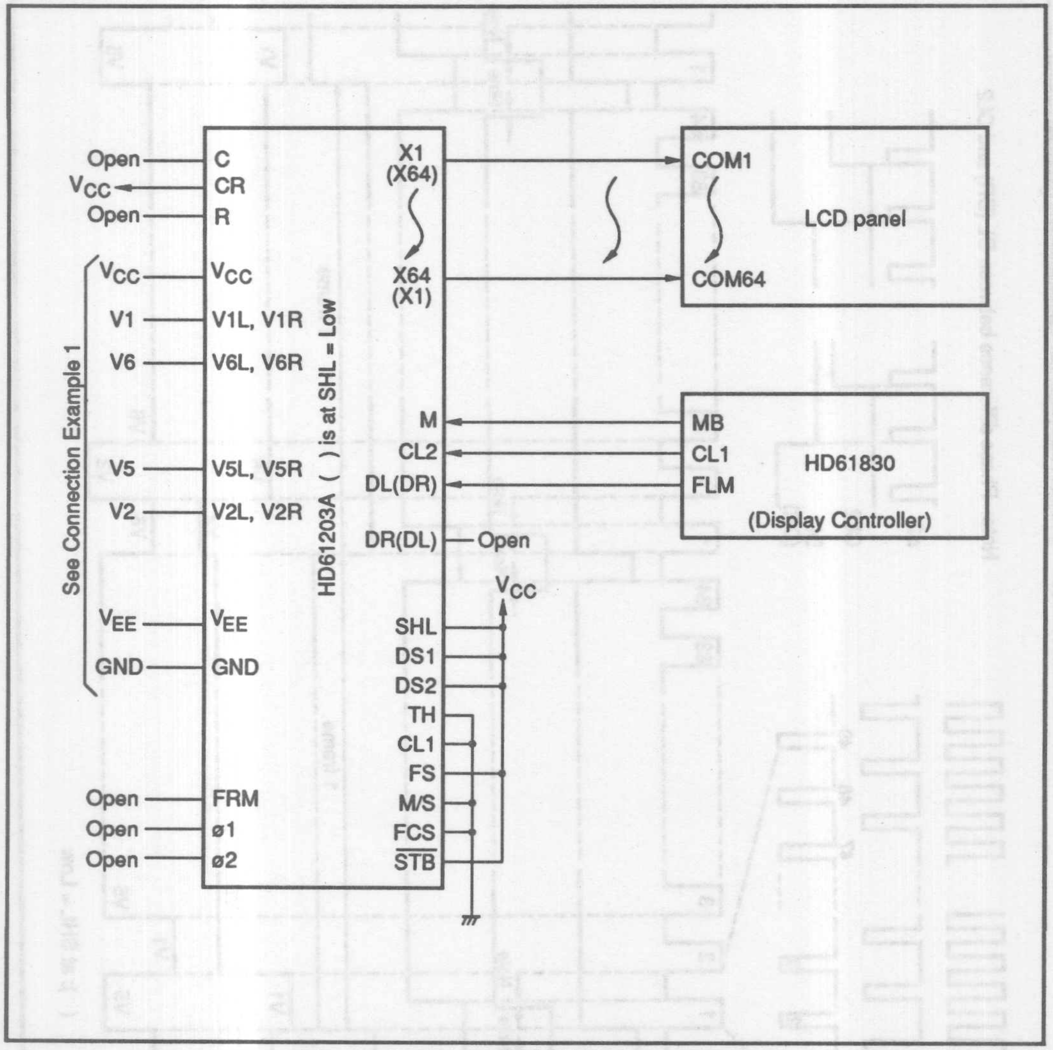


Figure 3 Example 2 (1/64 duty ratio)

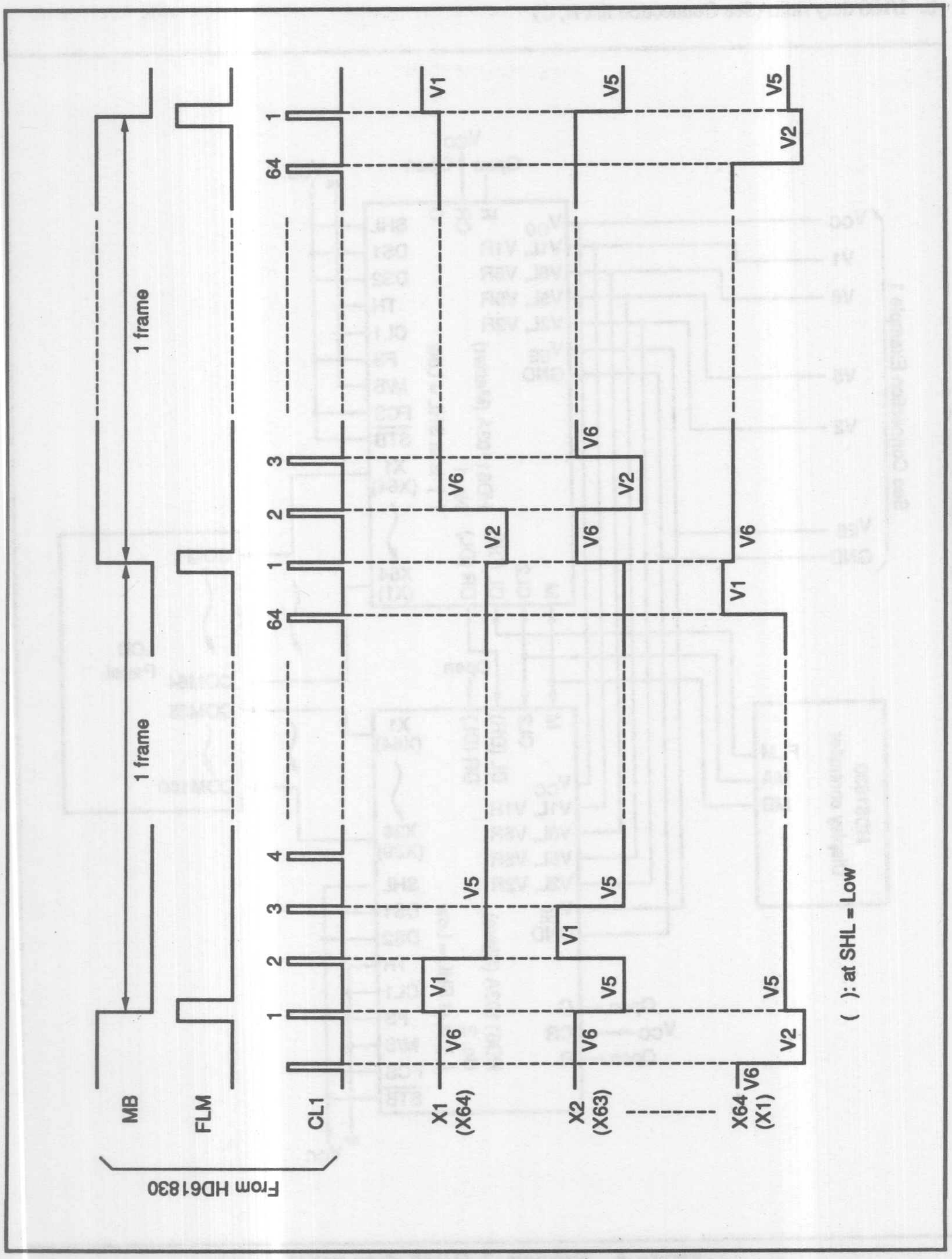


Figure 4 Example 2 Waveform (1/64 duty ratio)

b. 1/100 duty ratio (See Connection list B, C)

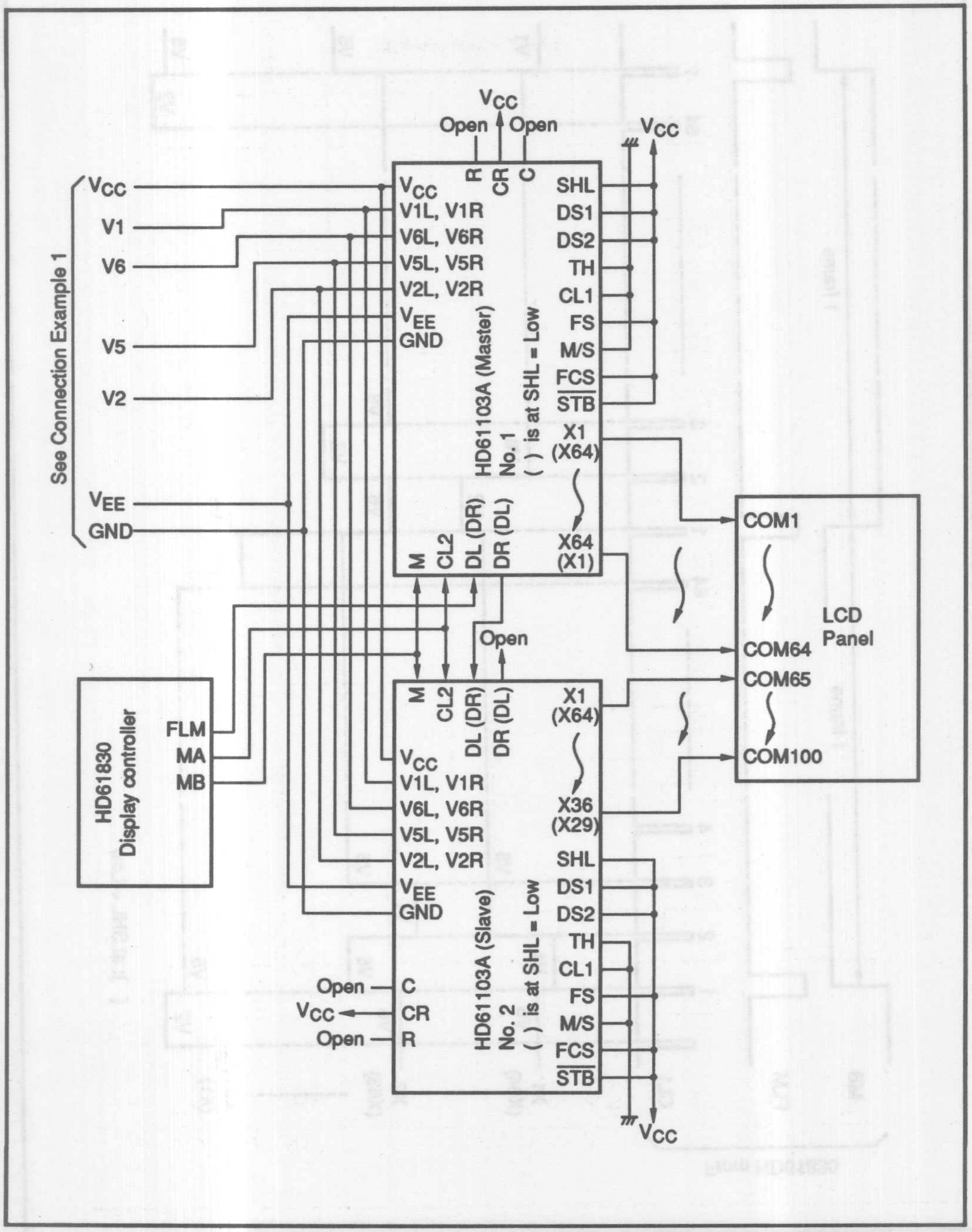


Figure 5 Example 2 (1/100 duty ratio)

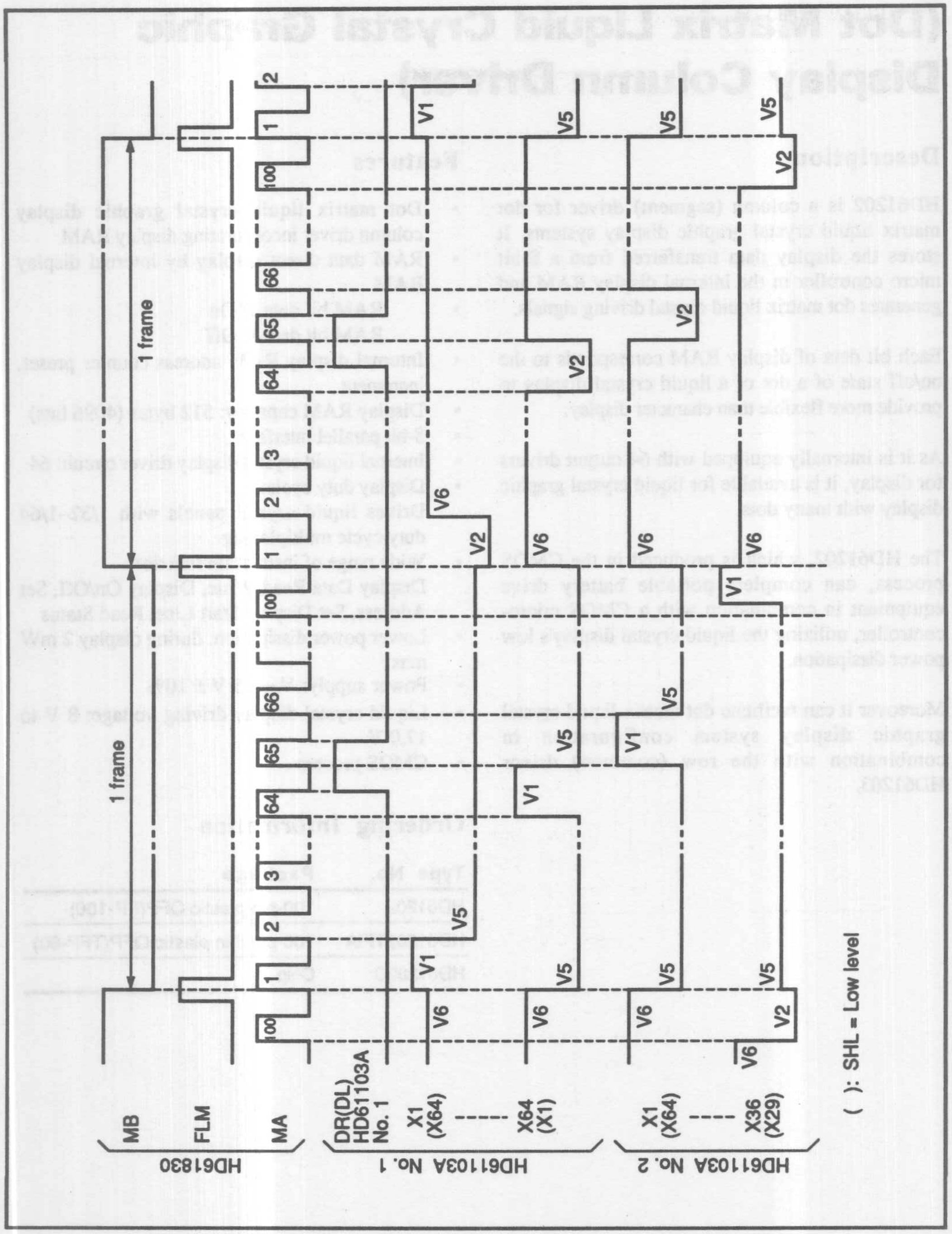


Figure 6 Example 2 (1/100 duty ratio)

HD61202

(Dot Matrix Liquid Crystal Graphic Display Column Driver)

Description

HD61202 is a column (segment) driver for dot matrix liquid crystal graphic display systems. It stores the display data transferred from a 8-bit micro controller in the internal display RAM and generates dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to the on/off state of a dot of a liquid crystal display to provide more flexible than character display.

As it is internally equipped with 64 output drivers for display, it is available for liquid crystal graphic display with many dots.

The HD61202, which is produced in the CMOS process, can complete portable battery drive equipment in combination with a CMOS micro-controller, utilizing the liquid crystal display's low power dissipation.

Moreover it can facilitate dot matrix liquid crystal graphic display system configuration in combination with the row (common) driver HD61203.

Features

- Dot matrix liquid crystal graphic display column driver incorporating display RAM
- RAM data direct display by internal display RAM
- RAM bit data 1: On
  RAM bit data 1: Off
- Internal display RAM address counter preset, increment
- Display RAM capacity: 512 bytes (4096 bits)
- 8-bit parallel interface
- Internal liquid crystal display driver circuit: 64
- Display duty cycle:
  Drives liquid crystal panels with 1/32–1/64 duty cycle multiplexing
- Wide range of instruction function:
  Display Data Read/Write, Display On/Off, Set Address, Set Display Start Line, Read Status
- Lower power dissipation: during display 2 mW max
- Power supply: V_{CC}: 5 V ± 10%
- Liquid crystal display driving voltage: 8 V to 17.0 V
- CMOS process

Ordering Information

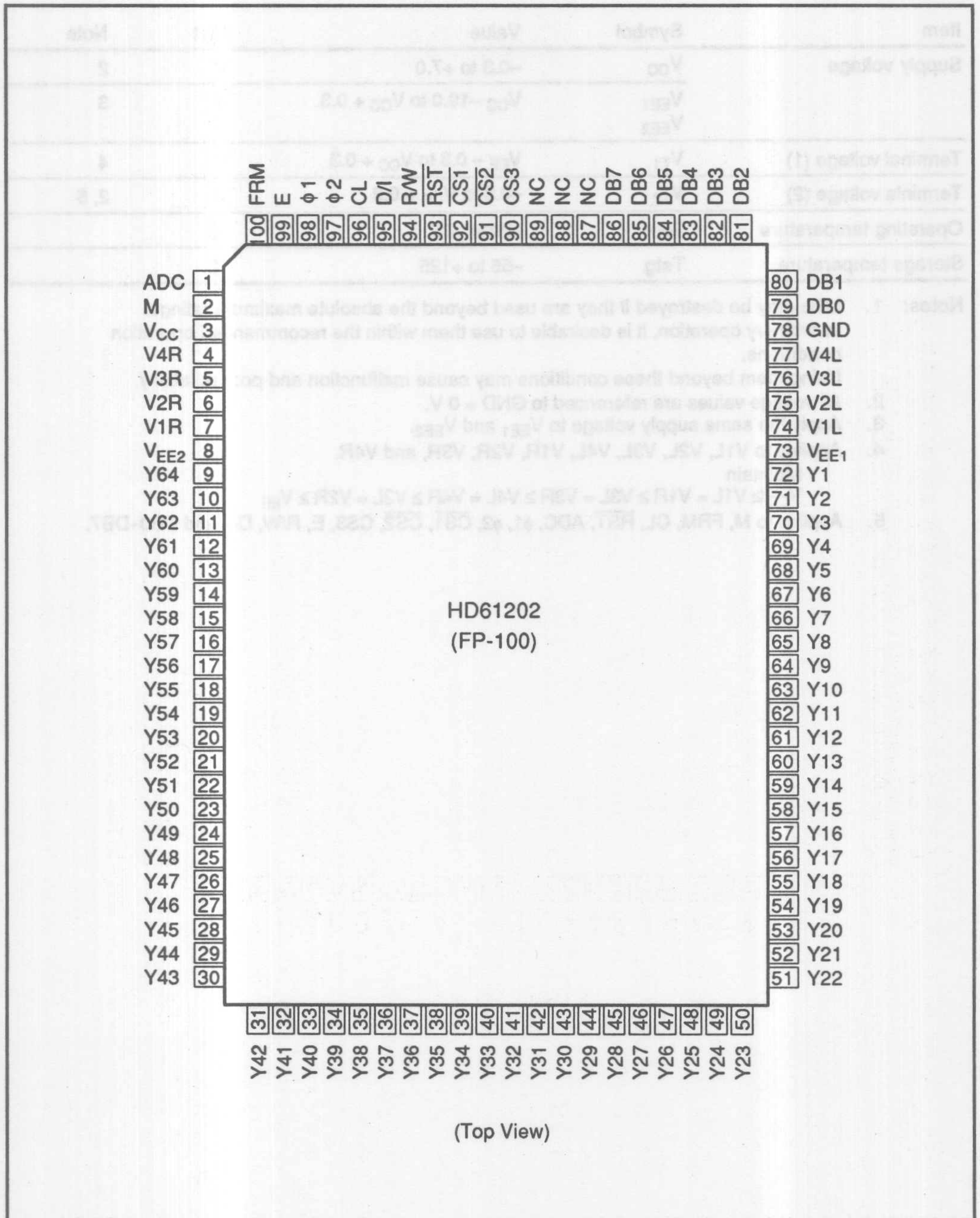
Type No.	Package
HD61202	100-pin plastic QFP(FP-100)
HD61202TFIA	100-pin thin plastic QFP(TFP-60)
HD61202D	Chip

Absolute Maximum Ratings

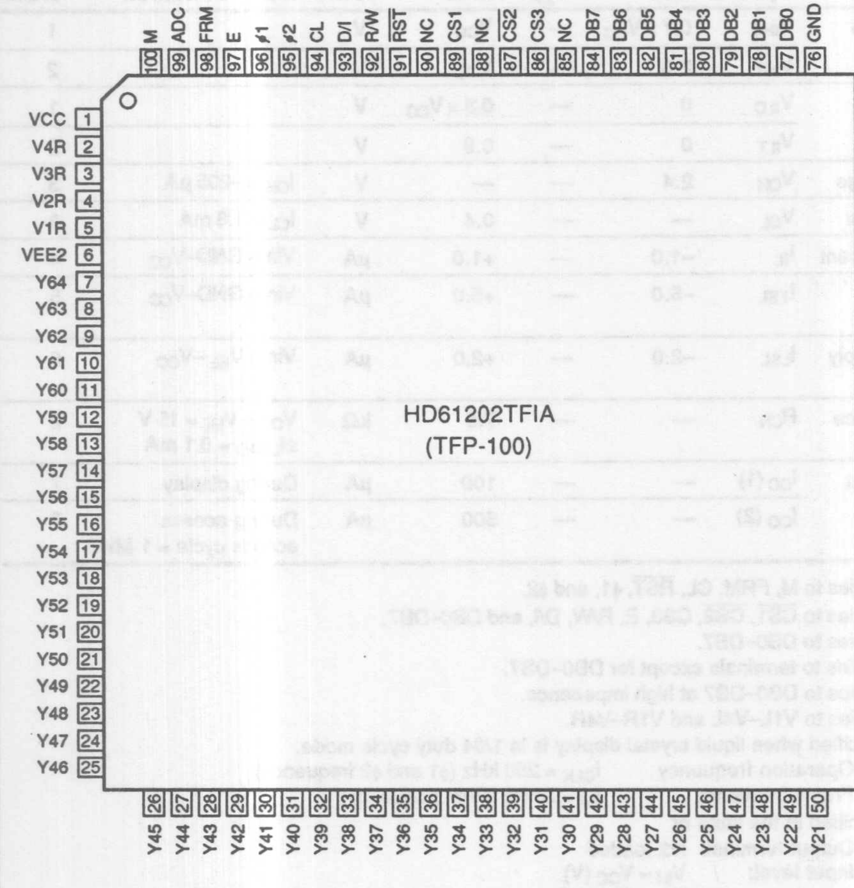
Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	–0.3 to +7.0	V	2
	V_{EE1} V_{EE2}	V_{CC} –19.0 to V_{CC} + 0.3	V	3
Terminal voltage (1)	V_{T1}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Terminla voltage (2)	V_{T2}	–0.3 to V_{CC} + 0.3	V	2, 5
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +125	°C	

Notes:
1. LSIs may be destroyed if they are used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the recommended operation conditions. Using them beyond these conditions may cause malfunction and poor reliability.
2. All voltage values are referenced to GND = 0 V.
3. Apply the same supply voltage to V_{EE1} and V_{EE2}.
4. Applies to V1L, V2L, V3L, V4L, V1R, V2R, V3R, and V4R.
   Maintain
   $V_{CC} \geq V1L = V1R \geq V3L = V3R \geq V4L = V4R \geq V2L = V2R \geq V_{EE}$
5. Applies to M, FRM, CL, $\overline{RST}$, ADC, ϕ1, ϕ2, $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, and DB0–DB7.

Pin Arrangement



(Top View)



100 M
99 ADC
98 FRM
97 E
96 φ1
95 φ2
94 CL
93 D/I
92 R/W
91 RST
90 NC
89 CS1
88 NC
87 CS2
86 CS3
85 NC
84 DB7
83 DB6
82 DB5
81 DB4
80 DB3
79 DB2
78 DB1
77 DB0
76 GND
VCC 1
V4R 2
V3R 3
V2R 4
V1R 5
VEE2 6
Y64 7
Y63 8
Y62 9
Y61 10
Y60 11
Y59 12
Y58 13
Y57 14
Y56 15
Y55 16
Y54 17
Y53 18
Y52 19
Y51 20
Y50 21
Y49 22
Y48 23
Y47 24
Y46 25
75 V4L
74 V3L
73 V2L
72 Y1L
71 VEE1
70 Y1
69 Y2
68 Y3
67 Y4
66 Y5
65 Y6
64 Y7
63 Y8
62 Y9
61 Y10
60 Y11
59 Y12
58 Y13
57 Y14
56 Y15
55 Y16
54 Y17
53 Y18
52 Y19
51 Y20
HD61202TFIA
(TFP-100)
26 Y45
27 Y44
28 Y43
29 Y42
30 Y41
31 Y40
32 Y39
33 Y38
34 Y37
35 Y36
36 Y35
37 Y34
38 Y33
39 Y32
40 Y31
41 Y30
42 Y29
43 Y28
44 Y27
45 Y26
46 Y25
47 Y24
48 Y23
49 Y22
50 Y21

(Top View)

Electrical Characteristics
(GND = 0 V, V_{CC} = 4.5 to 5.5 V, $V_{CC} - V_{EE}$ = 8 to 17.0 V, Ta = –20 to +75°C)

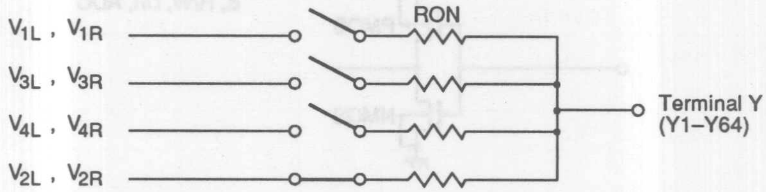
Item	Symbol	Limit Min	Limit Typ	Limit Max	Unit	Test Condition	Note
Input high voltage	V_{IHC}	$0.7 \times V_{CC}$	—	V_{CC}	V		1
	V_{IHT}	2.0	—	V_{CC}	V		2
Input low voltage	V_{ILC}	0	—	$0.3 \times V_{CC}$	V		1
	V_{ILT}	0	—	0.8	V		2
Output high voltage	V_{OH}	2.4	—	—	V	$I_{OH} = -205\ \mu A$	3
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6$ mA	3
Input leakage current	I_{IL}	–1.0	—	+1.0	µA	Vin = GND–V_{CC}	4
Three-state (off) input current	I_{TSL}	–5.0	—	+5.0	µA	Vin = GND–V_{CC}	5
Liquid crystal supply leakage current	I_{LSL}	–2.0	—	+2.0	µA	Vin = V_{EE}–V_{CC}	6
Driver on resistance	R_{ON}	—	—	7.5	kΩ	$V_{CC} - V_{EE} = 15$ V $\pm I_{LOAD} = 0.1$ mA	8
Dissipation current	I_{CC} (1)	—	—	100	µA	During display	7
	I_{CC} (2)	—	—	500	µA	During access access cycle = 1 MHz	7

Notes:
1. Applies to M, FRM, CL, $\overline{RST}$, ϕ1, and ϕ2.
2. Applies to $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, and DB0–DB7.
3. Applies to DB0–DB7.
4. Applies to terminals except for DB0–DB7.
5. Applies to DB0–DB7 at high impedance.
6. Applies to V1L–V4L and V1R–V4R.
7. Specified when liquid crystal display is in 1/64 duty cycle mode.
   Operation frequency f_{CLK} = 250 kHz (ϕ1 and ϕ2 frequency)
   Frame frequency f_M = 70 Hz (FRM frequency)
   Specified in the state of
   Output terminal: not loaded
   Input level: $V_{IH} = V_{CC}$ (V)
   V_{IL} = GND (V)
   Measured at V_{CC} terminal
8. Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L, and V4R) when load current flows through one of the terminals Y1 to Y64. This value is specified under the following condition:

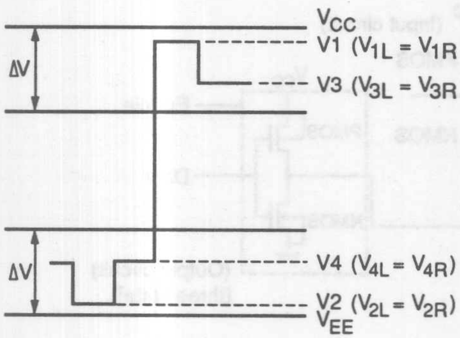
$V_{CC} - V_{EE} = 15.5$ V

$V_{1L} = V_{1R}$, $V_{3L} = V_{3R} = V_{CC} - 2/7\ (V_{CC} - V_{EE})$

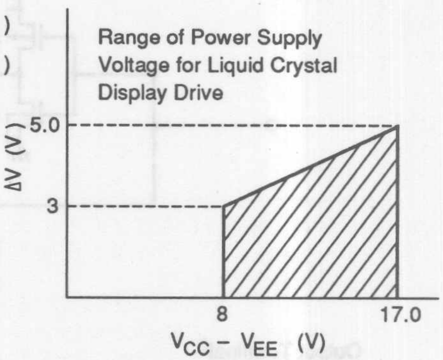
$V_{2L} = V_{2R}$, $V_{4L} = V_{4R} = V_{CC} + 2/7\ (V_{CC} - V_{EE})$



The following is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L = V1R and V3L = V3R and negative voltage to V2L = V2R and V4L = V4R within the ΔV range. This range allows stable impedance on driver output (RON). Notice that ΔV depends on power supply voltage $V_{CC} - V_{EE}$.



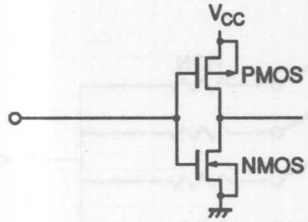
Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage $V_{CC} - V_{EE}$ and ΔV

Terminal Configuration

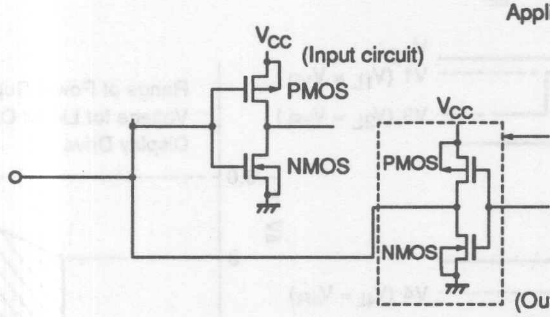
Input Terminal



Applicable terminals :
M, FRM, CL, $\overline{RST}$, ϕ 1, ϕ 2, $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, ADC

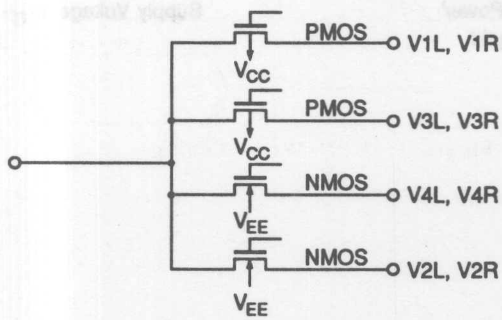
Input/Output Terminal

Applicable terminals: DB0–DB7



Output Terminal

Applicable Terminals:
Y1–Y64



Interface AC Characteristics

MPU Interface
(GND = 0 V, V_{CC} = 4.5 to 5.5 V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Note
E cycle time	t_{CYC}	1000	—	—	ns	1, 2
E high level width	P_{WEH}	450	—	—	ns	1, 2
E low level width	P_{WEL}	450	—	—	ns	1, 2
E rise time	tr	—	—	25	ns	1, 2
E fall time	tf	—	—	25	ns	1, 2
Address setup time	t_{AS}	140	—	—	ns	1, 2
Address hold time	t_{AH}	10	—	—	ns	1, 2
Data setup time	t_{DSW}	200	—	—	ns	1
Data delay time	t_{DDR}	—	—	320	ns	2, 3
Data hold time (Write)	t_{DHW}	10	—	—	ns	1
Data hold time (Read)	t_{DHR}	20	—	—	ns	2

Notes: 1.

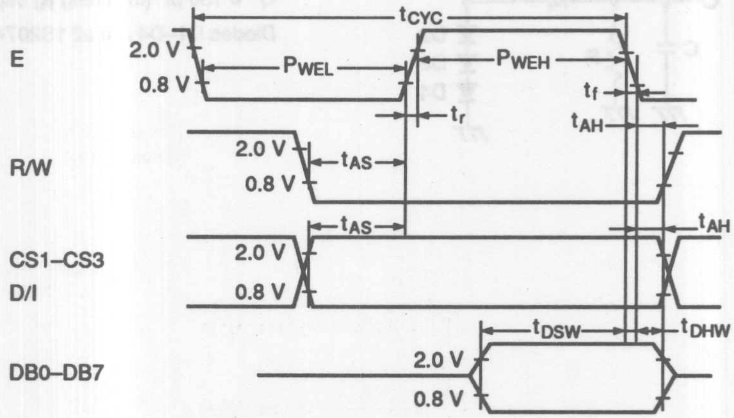


Figure 1 CPU Write Timing

Notes: 2.

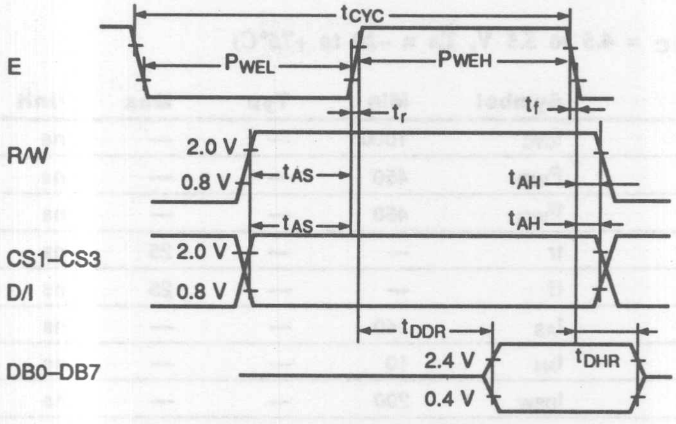
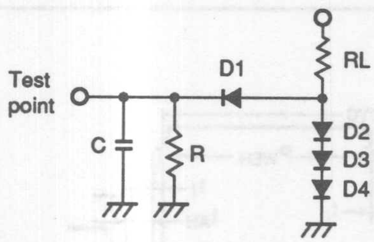


Figure 2 CPU Read Timing

3. DB0–DB7: load circuit



RL = 2.4 k Ω

R = 11 k Ω

C = 130 pF (including jig capacitance)

Diodes D1–D4 are all 1S2074 (H).

Clock Timing
(GND = 0 V, V_{CC} = 4.5 to 5.5 V, Ta = –20 to +75°C)

Item	Symbol	Limit Min	Limit Typ	Limit Max	Unit	Test Condition
ϕ1, ϕ2 cycle time	tcyc	2.5	—	20	µs	Fig. 3
ϕ1 low level width	$t_{WL\phi1}$	625	—	—	ns	Fig. 3
ϕ2 low level width	$t_{WL\phi2}$	625	—	—	ns	Fig. 3
ϕ1 high level width	$t_{WH\phi1}$	1875	—	—	ns	Fig. 3
ϕ2 high level width	$t_{WH\phi2}$	1875	—	—	ns	Fig. 3
ϕ1—ϕ2 phase difference	t_{D12}	625	—	—	ns	Fig. 3
ϕ2—ϕ1 phase difference	t_{D21}	625	—	—	ns	Fig. 3
ϕ1, ϕ2 rise time	tr	—	—	150	ns	Fig. 3
ϕ1, ϕ2 fall time	tf	—	—	150	ns	Fig. 3

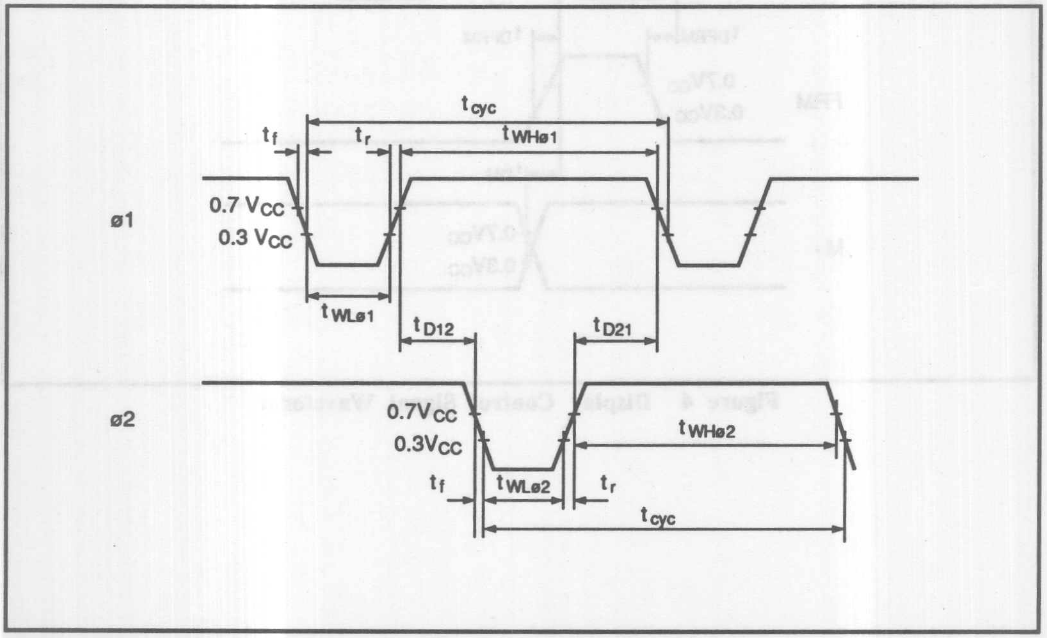


Figure 3 External Clock Waveform

Display Control Timing
(GND = 0V, V_{CC} = 4.5 to 5.5 V, Ta = –20 to +75 °C)

Item	Symbol	Limit Min	Typ	Max	Unit	Test Condition
FRM delay time	t_{DFRM}	–2	—	+2	µs	Fig. 4
M delay time	t_{DM}	–2	—	+2	µs	Fig. 4
CL low level width	t_{WLCL}	35	—	—	µs	Fig. 4
CL high level width	t_{WHCL}	35	—	—	µs	Fig. 4

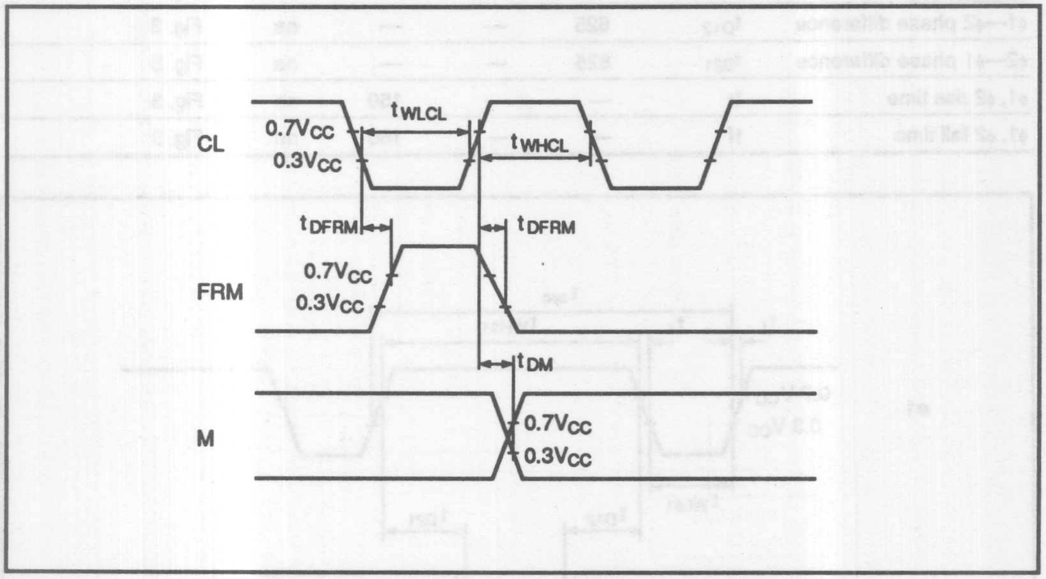
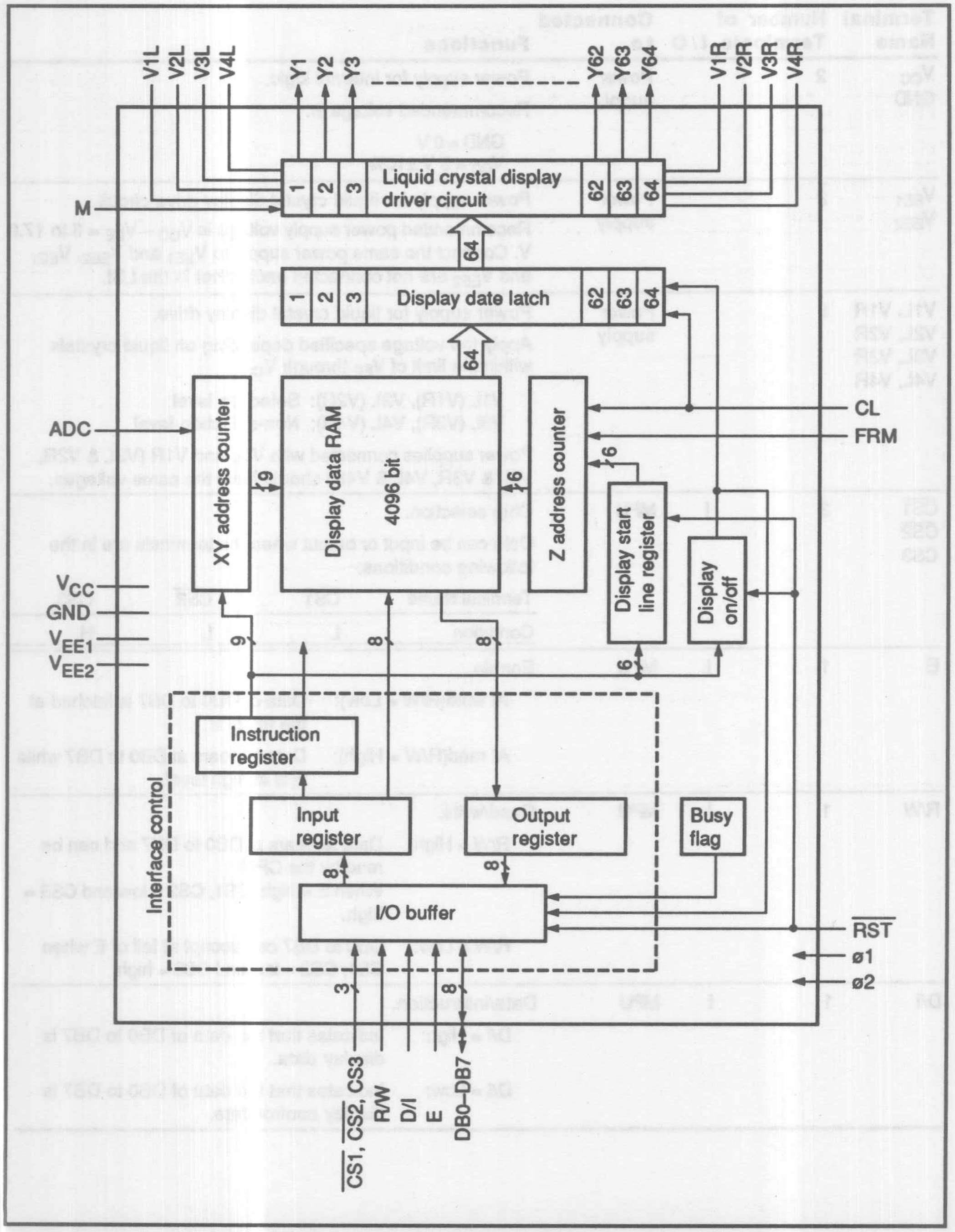


Figure 4 Display Control Signal Waveform

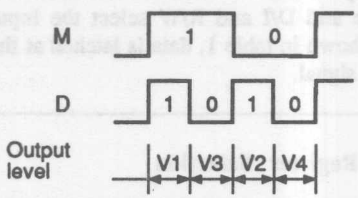
Block Diagram



Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND	2		Power supply	Power supply for internal logic. Recommended voltage is: GND = 0 V V_{CC} = 5 V ±10%
V_{EE1} V_{EE2}	2		Power supply	Power supply for liquid crystal display drive circuit. Recommended power supply voltage is $V_{CC} - V_{EE}$ = 8 to 17.0 V. Connect the same power supply to V_{EE1} and V_{EE2}. V_{EE1} and V_{EE2} are not connected each other in the LSI.
V1L, V1R V2L, V2R V3L, V3R V4L, V4R	8		Power supply	Power supply for liquid crystal display drive. Apply the voltage specified depending on liquid crystals within the limit of V_{EE} through V_{CC}. V1L (V1R), V2L (V2R): Selection level V3L (V3R), V4L (V4R): Non-selection level Power supplies connected with V1L and V1R (V2L & V2R, V3L & V3R, V4L & V4R) should have the same voltages.
$\overline{CS1}$ $\overline{CS2}$ CS3	3	I	MPU	Chip selection. Data can be input or output when the terminals are in the following conditions: Terminal Name: $\overline{CS1}$, $\overline{CS2}$, CS3 Condition: L, L, H
E	1	I	MPU	Enable. At write(R/W = Low): Data of DB0 to DB7 is latched at the fall of E. At read(R/W = High): Data appears at DB0 to DB7 while E is at high level.
R/W	1	I	MPU	Read/write. R/W = High: Data appears at DB0 to DB7 and can be read by the CPU. When E = high, CS1, CS2 = low and CS3 = high. R/W = Low: DB0 to DB7 can accept at fall of E when CS1, CS2 = low and CS3 = high.
D/I	1	I	MPU	Data/instruction. D/I = High: Indicates that the data of DB0 to DB7 is display data. D/I = Low: Indicates that the data of DB0 to DB7 is display control data.

Terminal Functions (cont)

Terminal Name	Number of Terminals	I/O	Connected to	Functions
ADC	1	I	V_{CC}/GND	Address control signal to determine the relation between Y address of display RAM and terminals from which the data is output. ADC = High: Y1: $0, Y64: $63 ADC = Low: Y64: $0, Y1: $63
DB1-DB7	8	I/O	MPU	Data bus, three-state I/O common terminal.
M	1	I	HD61203	Switch signal to convert liquid crystal drive waveform into AC.
FRM	1	I	HD61203	Display synchronous signal (frame signal). Presets the 6-bit display line counter and synchronizes the common signal with the frame timing when the FRM signal becomes high.
CL	1	I	HD61203	Synchronous signal to latch display data. The rising CL signal increments the display output address counter and latches the display data.
$\phi1$, $\phi2$	2	I	HD61203	2-phase clock signal for internal operation. The $\phi1$ and $\phi2$ clocks are used to preform operations (I/O of display data and execution of instructions) other than display.
Y1-Y64	64	O	Liquid crystal display	Liquid crystal display column (segment) drive output. These pins outputs light on level when 1 is in the display RAM, and light off level when 0 is it. Relation among output level, M, and display data (D) is as follows: 
$\overline{RST}$	1	I	CPU or external CR	The following registers can be initialized by setting the $\overline{RST}$ signal to low level. 1. On/off register 0 set (display off) 2. Display start line register line 0 set (displays from line 0) After releasing reset, this condition can be changed only by instruction.
NC	3		Open	Unused terminals. Don't connect any lines to these terminals.

Note: 1 corresponds to high level in positive logic.

Function of Each Block

Interface Control

1. I/O buffer

Data is transferred through 8 data bus lines (DB0–DB7).

DB7: MSB (Most significant bit)

DB0: LSB (Least significant bit)

Data can neither be input nor output unless $\overline{\text{CS1}}$ to CS3 are in the active mode. Therefore, when $\overline{\text{CS1}}$ to CS3 are not in active mode it is useless to switch the signals of input terminals except $\overline{\text{RST}}$ and ADC; that is namely, the internal state is maintained and no instruction excutes. Besides, pay attention to $\overline{\text{RST}}$ and ADC which operate irrespectively of $\overline{\text{CS1}}$ to CS3.

2. Register

Both input register and output register are provided to interface to an MPU whose speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals (table 1).

a. Input register

The input register is used to store data temporarily before writing it into display data RAM.

The data from MPU is written into the input register, then into display data RAM automatically by internal operation. When $\overline{\text{CS1}}$ to CS3 are in the active mode and D/I and R/W select the input register as shown in table 1, data is latched at the fall of the E signal.

b. Output register

The output register is used to store data temporarily that is read from display data RAM. To read out the data from output register, $\overline{\text{CS1}}$ to CS3 should be in the active mode and both D/I and R/W should be 1. With the read display data instruction, data stored in the output register is output while E is high level. Then, at the fall of E, the display data at the indicated address is latched into the output register and the address is increased by 1.

The contents in the output register are rewritten by the read display data instruction, but are held by address set instruction, etc.

Therefore, the data of the specified address cannot be output with the read display data instruction right after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Figure 5 shows the CPU read timing.

Table 1 Register Selection

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register)
1	0	Writes data into input register as internal operation (input register → display data RAM)
0	1	Busy check. Read of status data.
0	0	Instruction

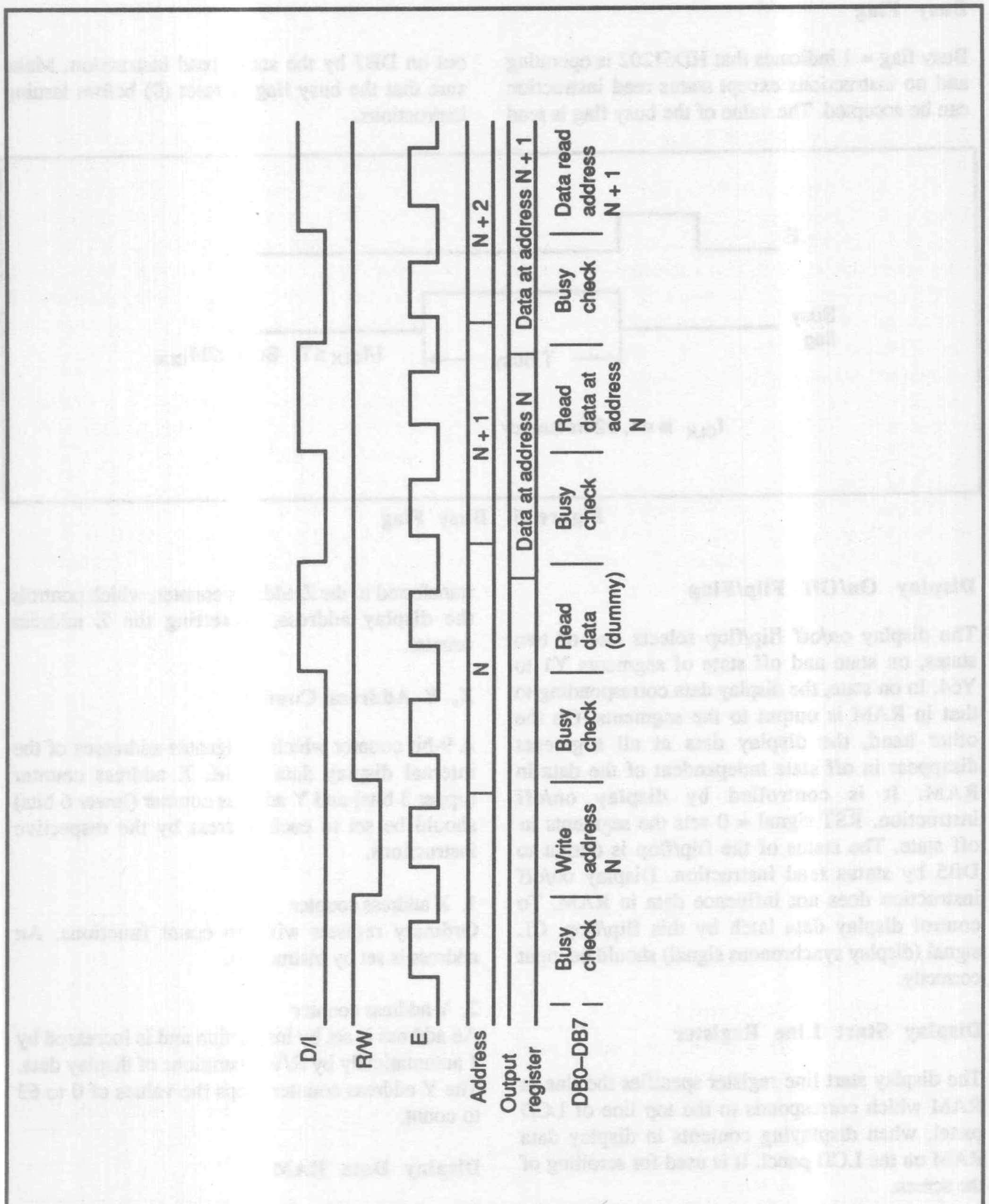


Figure 5 CPU Read Timing

Busy Flag

Busy flag = 1 indicates that HD61202 is operating and no instructions except status read instruction can be accepted. The value of the busy flag is read out on DB7 by the status read instruction. Make sure that the busy flag is reset (0) before issuing instructions.

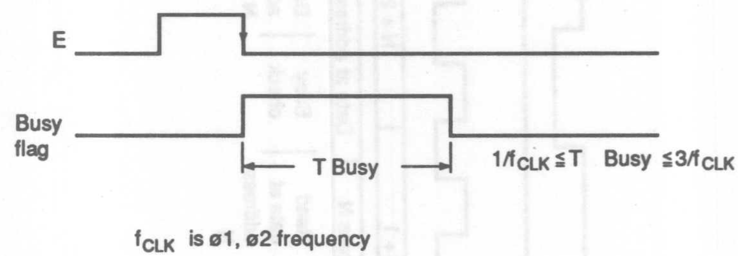


Figure 6 Busy Flag

Display On/Off Flip/Flop

The display on/off flip/flop selects one of two states, on state and off state of segments Y1 to Y64. In on state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in off state independent of the data in RAM. It is controlled by display on/off instruction. $\overline{RST}$ signal = 0 sets the segments in off state. The status of the flip/flop is output to DB5 by status read instruction. Display on/off instruction does not influence data in RAM. To control display data latch by this flip/flop, CL signal (display synchronous signal) should be input correctly.

Display Start Line Register

The display start line register specifies the line in RAM which corresponds to the top line of LCD panel, when displaying contents in display data RAM on the LCD panel. It is used for scrolling of the screen.

6-bit display start line information is written into this register by the display start line set instruction. When high level of the FRM signal starts the display, the information in this register is transferred to the Z address counter, which controls the display address, presetting the Z address counter.

X, Y Address Counter

A 9-bit counter which designates addresses of the internal display data RAM. X address counter (upper 3 bits) and Y address counter (lower 6 bits) should be set to each address by the respective instructions.

1. X address counter
Ordinary register with no count functions. An address is set by instruction.

2. Y address counter
An address is set by instruction and is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

Display Data RAM

Stores dot data for display. 1-bit data of this RAM corresponds to light on (data = 1) and light off (data = 0) of 1 dot in the display panel. The correspondence between Y addresses of RAM and segment pins can be reversed by ADC signal.

As the ADC signal controls the Y address counter, reversing of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore, never fail to connect ADC pin to V_{CC} or GND when using.

Figure 7 shows the relations between Y address of RAM and segment pins in the cases of ADC = 1 and ADC = 0 (display start line = 0, 1/64 duty cycle).

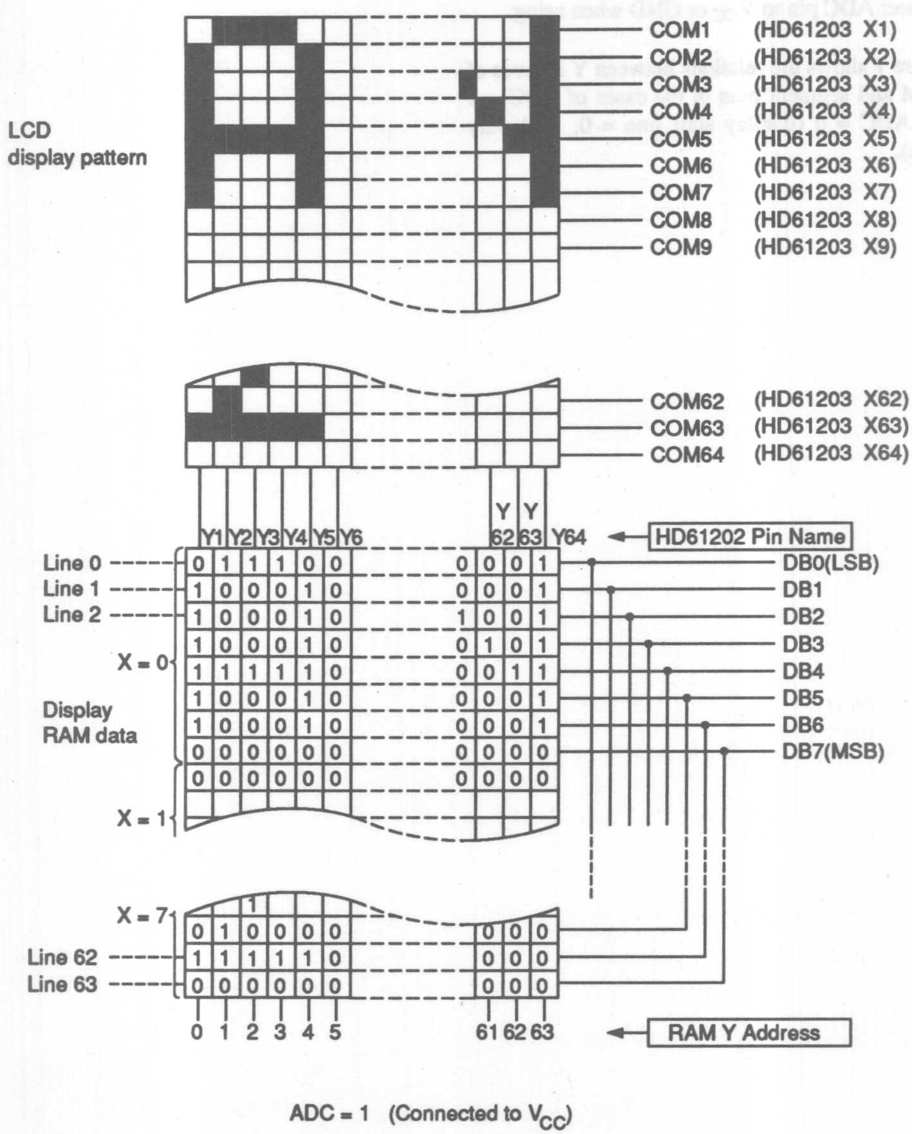


Figure 7 Relation between RAM Data and Display

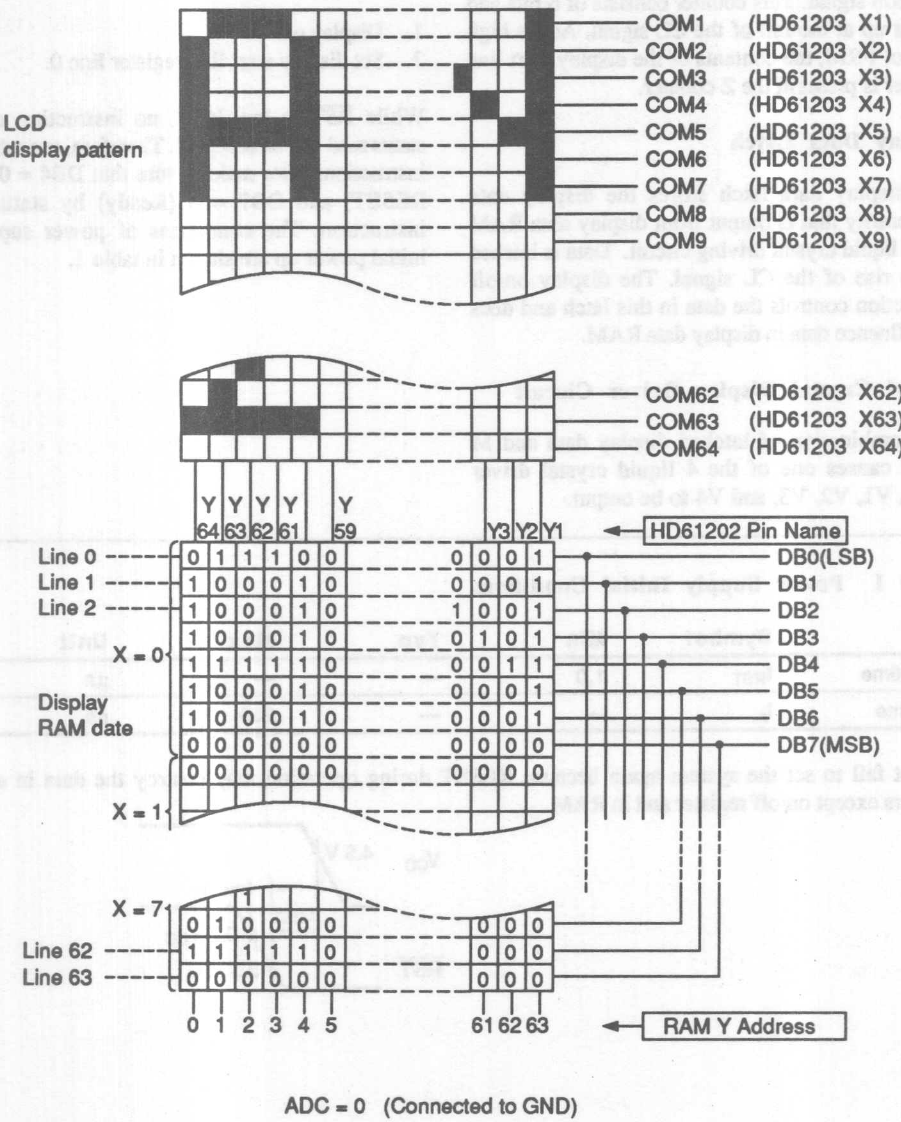


Figure 7 Relation between RAM Data and Display (cont)

Z Address Counter

The Z address counter generates addresses for outputting the display data synchronized with the common signal. This counter consists of 6 bits and counts up at the fall of the CL signal. At the high level of FRM, the contents of the display start line register is preset at the Z counter.

Display Data Latch

The display data latch stores the display data temporarily that is output from display data RAM to the liquid crystal driving circuit. Data is latched at the rise of the CL signal. The display on/off instruction controls the data in this latch and does not influence data in display data RAM.

Liquid Crystal Display Driver Circuit

The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3, and V4 to be output.

Reset

The system can be initialized by setting $\overline{RST}$ terminal at low level when turning power on.

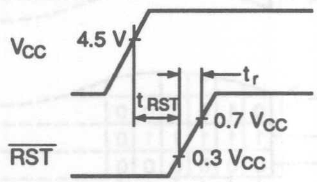
1. Display off
2. Set display start line register line 0.

While $\overline{RST}$ is low level, no instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4 = 0 (clear RESET) and DB7 = 0 (Ready) by status read instruction. The conditions of power supply at initial power up are shown in table 1.

Table 1 Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	—	—	μs
Rise time	t_r	—	—	200	ns

Do not fail to set the system again because RESET during operation may destroy the data in all the registers except on/off register and in RAM.



Display Control Instructions

Outline

Table 2 shows the instructions. Read/write (R/W) signal, data/instruction (D/I) signal, and data bus signals (DB0 to DB7) are also called instructions because the internal operation depends on the signals from the MPU.
These explanations are detailed in the following pages. Generally, there are following three kinds of instructions:

1. Instruction to set addresses in the internal RAM
2. Instruction to transfer data from/to the internal RAM
3. Other instructions

In general use, the second type of instruction is used most frequently. Since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be shortened. During the execution of an instruction, the system cannot accept instructions other than status read instruction. Send instructions from MPU after making sure that the busy flag is 0, which is proof that an instruction is not being excuted.

Table 2 Instructions

Instructions	R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Functions
	Code										
Display on/off	0	0	0	0	1	1	1	1	1	1/0	Controls display on/off. RAM data and internal status are not affected. 1: on, 0: off.
Display start line	0	0	1	1	Display start line (0–63)						Specifies the RAM line displayed at the top of the screen.
Set page (X address)	0	0	1	0	1	1	1	Page (0–7)			Sets the page (X address) of RAM at the page (X address) register.
Set address	0	0	0	1	Y address (0–63)						Sets the Y address in the Y address counter.
Status read	1	0	Busy	0	ON/ OFF	Reset	0	0	0	0	Reads the status. RESET 1: Reset 0: Normal ON/OFF 1: Display off 0: Display on Busy 1: Internal operation 0: Ready
Write display data	0	1	Write data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM. Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
Read display data	1	1	Read data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.

Note: 1. Busy time varies with the frequency (f_{CLK}) of $\phi1$, and $\phi2$.
($1/f_{CLK} \leq T_{BUSY} \leq 3/f_{CLK}$)

Detailed Explanation

Display on/off

	R/W	D/I	DB7							DB0
Code	0	0	0	0	1	1	1	1	1	D

← high-order bit   low-order bit →

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D = 0, it remains in the display data RAM. Therefore, you can make it appear by changing D = 0 into D = 1.

Display start line

	R/W	D/I	DB7							DB0
Code	0	0	1	1	A	A	A	A	A	A

← high-order bit   low-order bit →

Z address AAAAAA (binary) of the display data RAM is set in the display start line register and displayed at the top of the screen. Figure 8 shows examples of display (1/64 duty cycle) when the start line = 0–3. When the display duty cycle is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

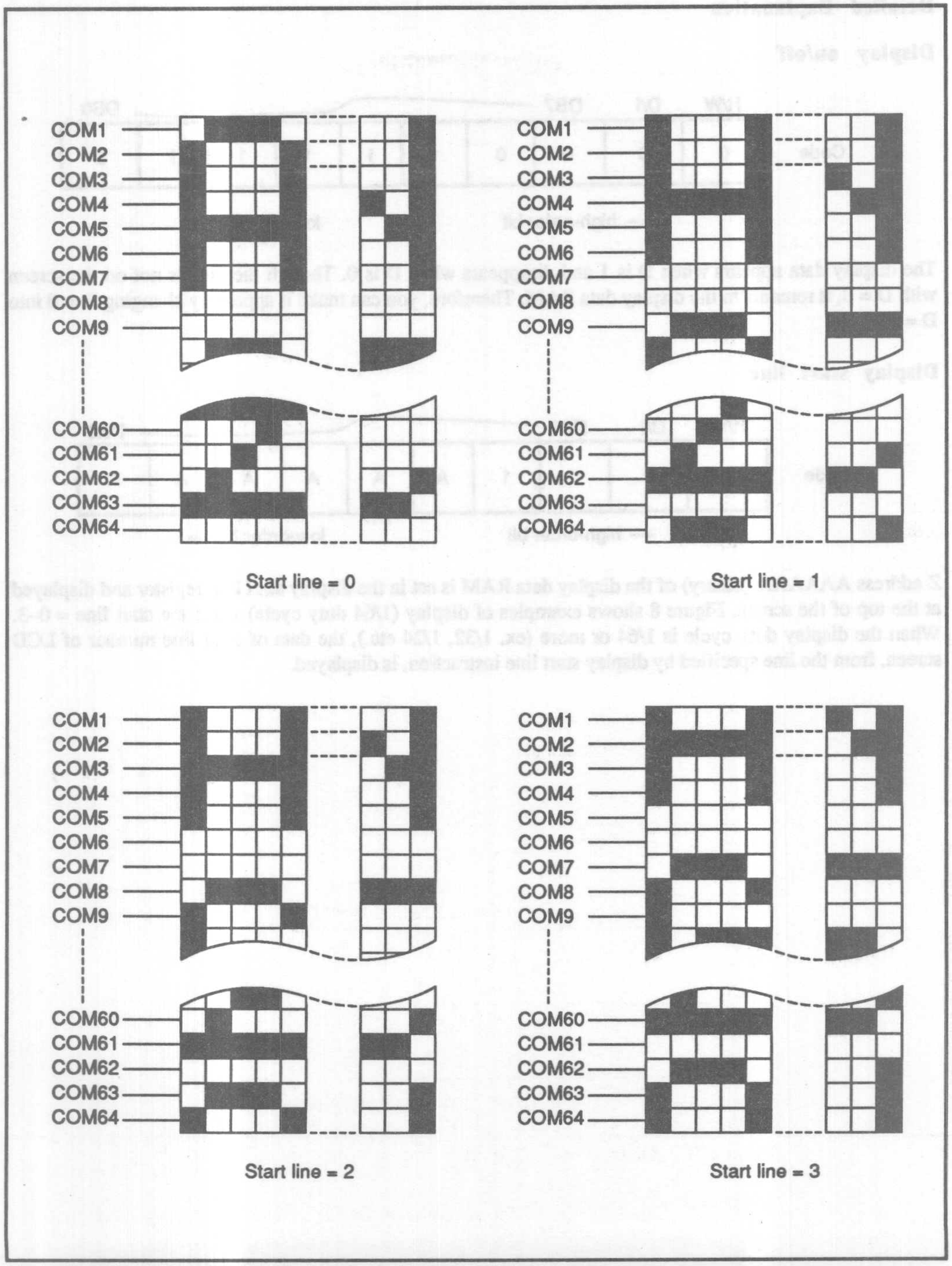


Figure 8 Relation Between Start Line and Display

Set page (X address)

	R/W	D/I	DB7							DB0
Code	0	0	1	0	1	1	1	A	A	A

← high-order bit   low-order bit →

X address AAA (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set. See figure 9.

Set Y address

	R/W	D/I	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← high-order bit   low-order bit →

Y address AAAAAA (binary) of the display data RAM is set in the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

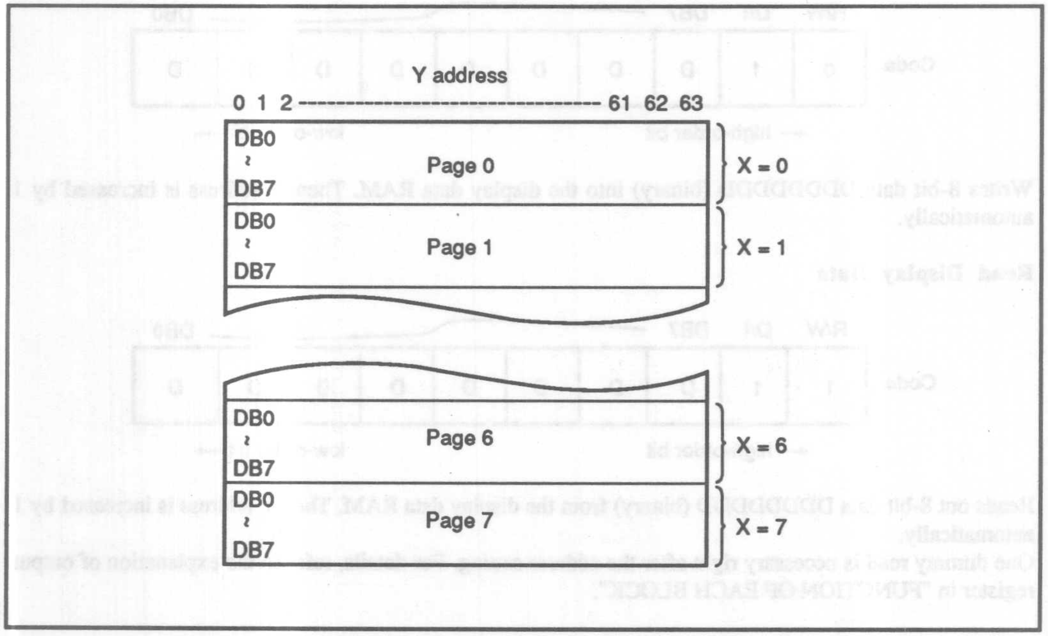


Figure 9 Address Configuration of Display Data RAM

Status Read

	R/W	D/I	DB7							DB0
Code	1	0	Busy	0	ON/ OFF	RESET	0	0	0	0

← high-order bit   low-order bit →

Busy: When Busy is 1, the LSI is executing internal operations. No instructions are accepted while Busy is 1, so you should make sure that Busy is 0 before writing the next instruction.

ON/OFF: Shows the liquid crystal display conditions: on condition or off condition.
When ON/OFF is 1, the display is in off condition.
When ON/OFF is 0, the display is in on condition.

RESET: RESET = 1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted.
RESET = 0 shows that initializing has finished and the system is in the usual operation condition.

Write Display Data

	R/W	D/I	DB7							DB0
Code	0	1	D	D	D	D	D	D	D	D

← high-order bit   low-order bit →

Writes 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

Read Display Data

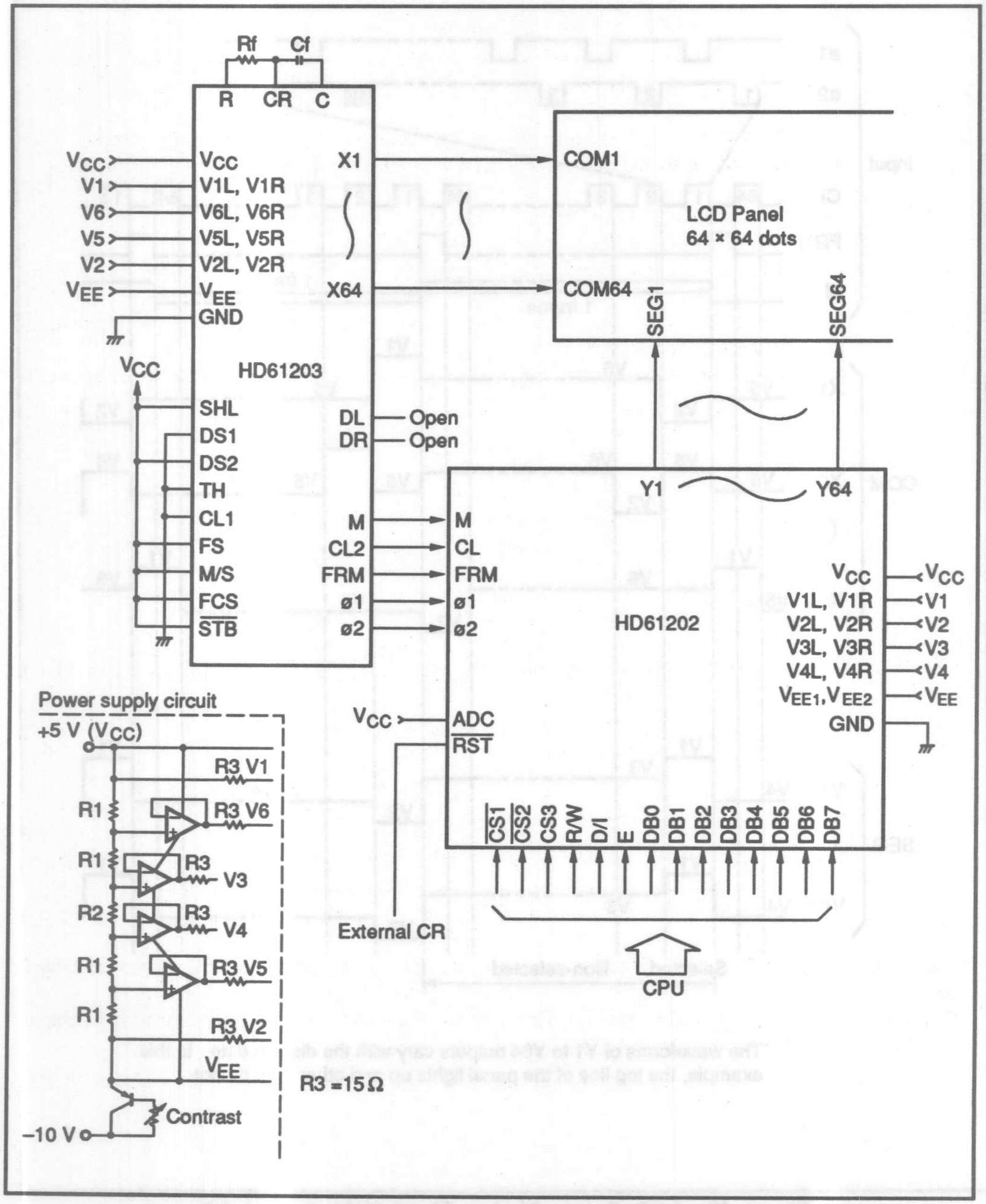
	R/W	D/I	DB7							DB0
Code	1	1	D	D	D	D	D	D	D	D

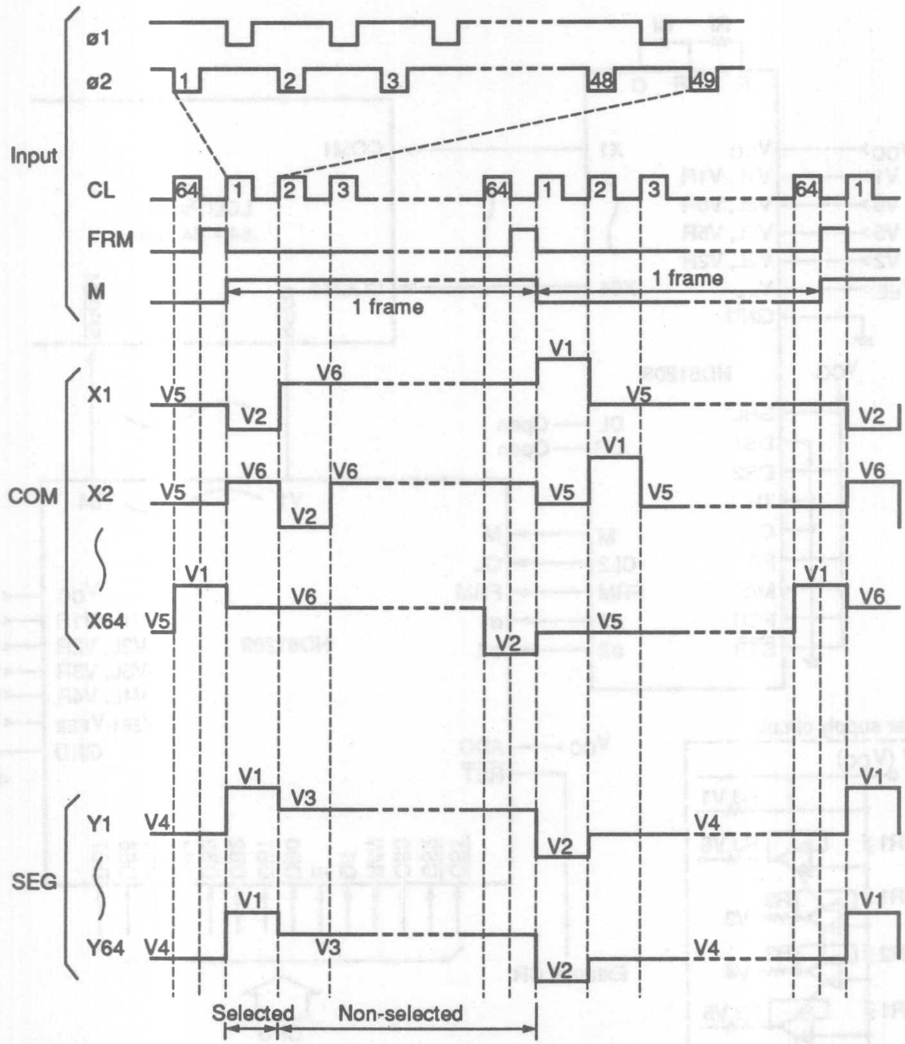
← high-order bit   low-order bit →

Reads out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.
One dummy read is necessary right after the address setting. For details, refer to the explanation of output register in "FUNCTION OF EACH BLOCK".

Use of HD61202

Interface with HD61203 (1/64 duty cycle)





The waveforms of Y1 to Y64 outputs vary with the display date. In this example, the top line of the panel lights up and other dots do not.

Figure 10 LCD Driver Timing Chart (1/64 duty cycle)

Interface with CPU

1. Example of connection with HD6800

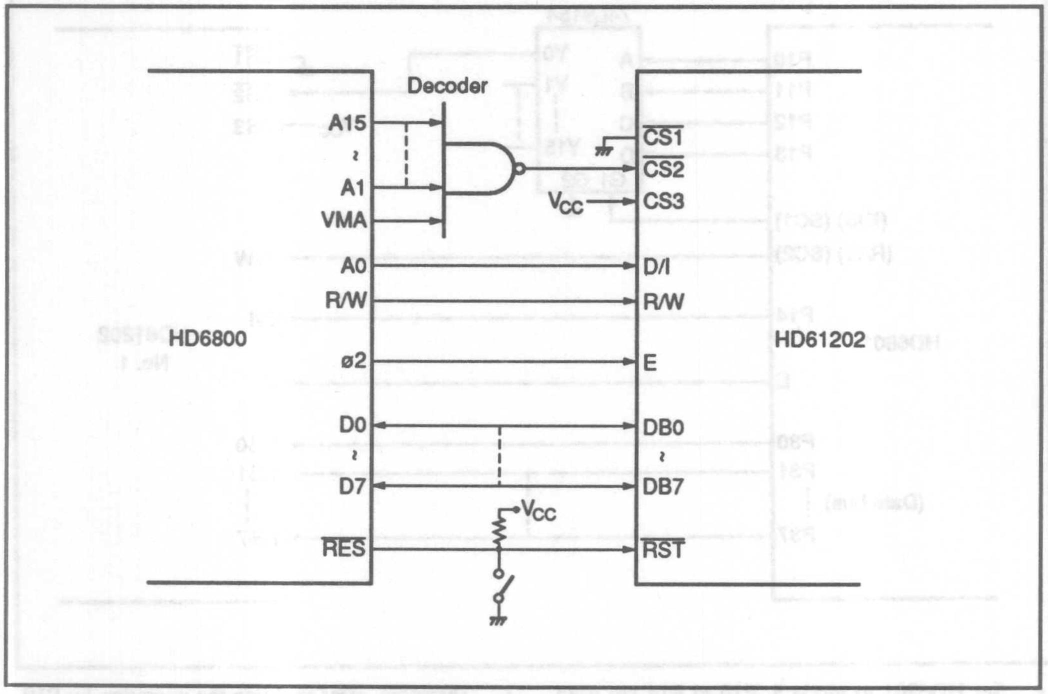


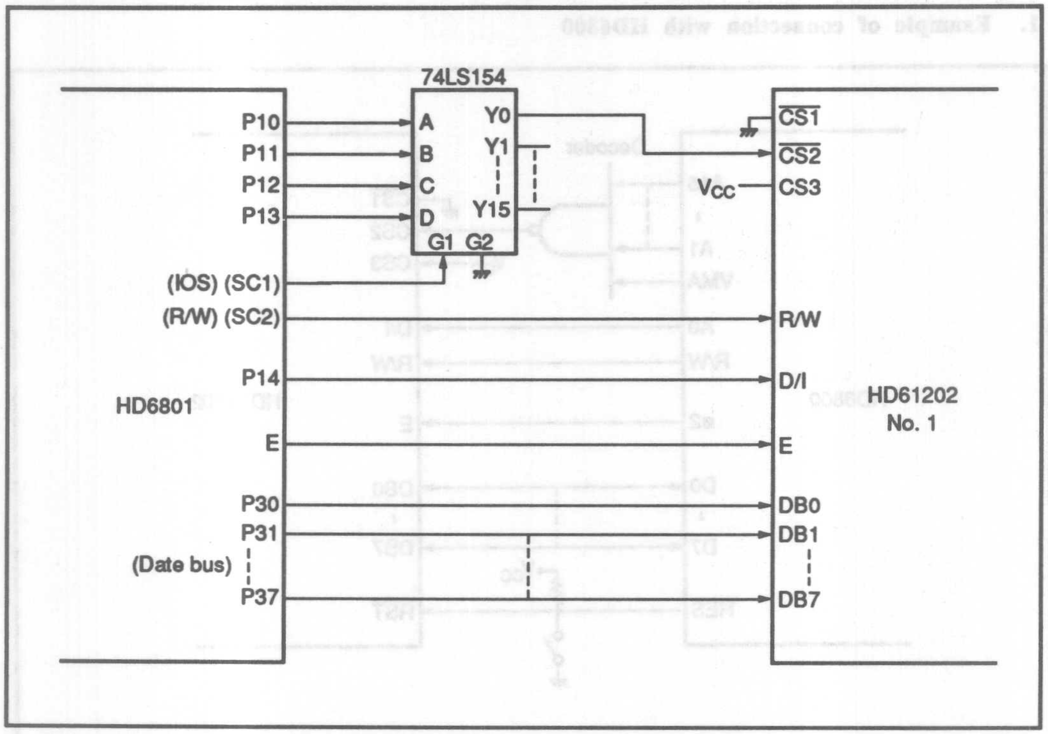
Figure 11 Example of Connection with HD6800 Series

In this decoder, addresses of HD61202 in the address area of HD6800 are:

Read/write of the display data	\$FFFF
write of display instruction	\$FFFE
Read out of status	\$FFFE

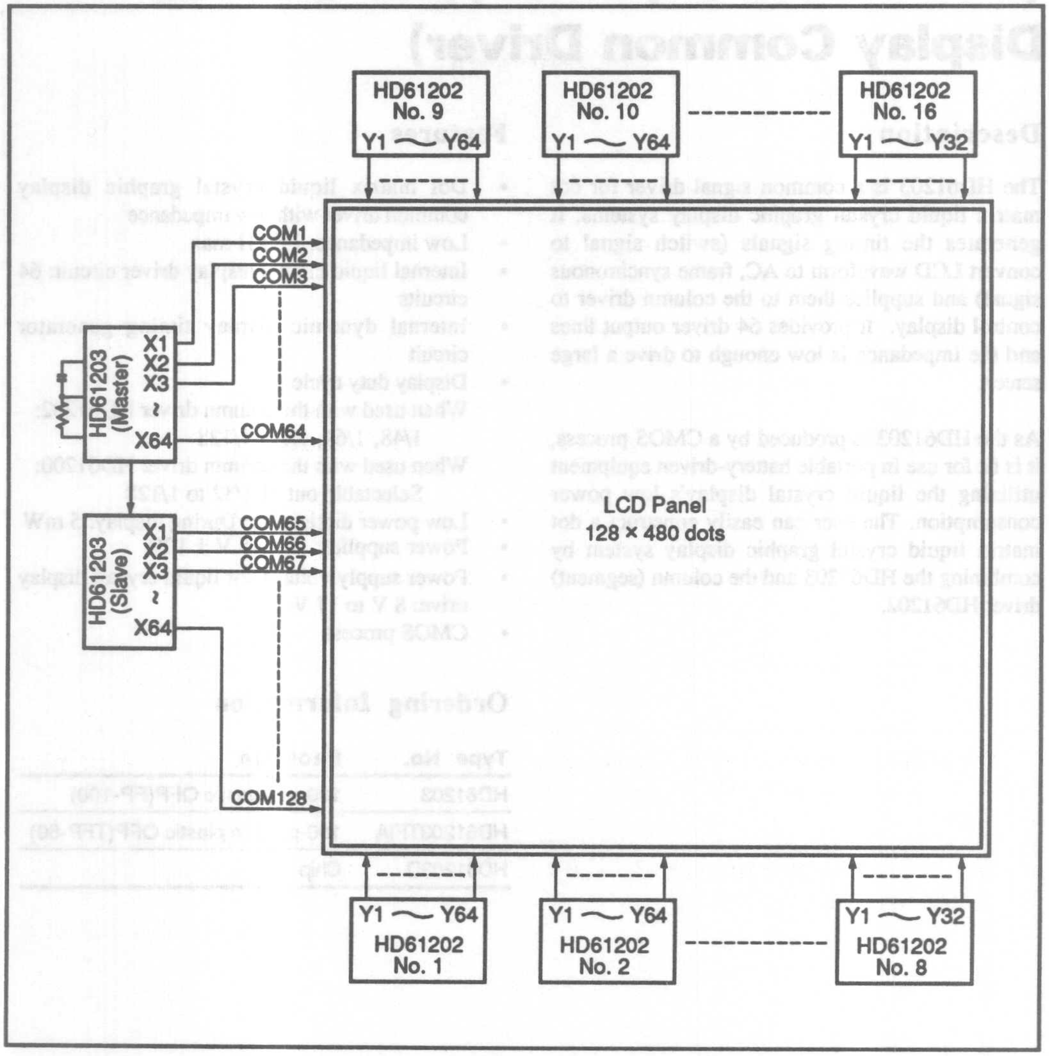
Therefore, you can control HD61202 by reading/writing the data at these addresses.

2. Example of connection with HD6801



- Set HD6801 to mode 5. P10 to P14 are used as the output port and P30 to P37 as the data bus.
- 74LS154 4-to-16 decoder generates chip select signal to make specified HD61202 active after decoding 4 bits of P10 to P13.
- Therefore, after enabling the operation by P10 to P13 and specifying D/I signal by P14, read/write from/to the external memory area ($0100 to $01FE) to control HD61202. In this case, IOS signal is output from SC1 and R/W signal from SC2.
- For details of HD6800 and HD6801, refer to their manuals.

Example of Application



Note: In this example, two HD61203s output the equivalent waveforms. So, stand-alone operation is possible. In this case, connect COM1 and COM65 to X1, COM2 and COM66 to X2, ..., and COM64 and COM128 to X64. However, for the large screen display, it is better to drive in 2 rows as in this example to guarantee the display quality.

HD61203

(Dot Matrix Liquid Crystal Graphic Display Common Driver)

Description

The HD61203 is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals (switch signal to convert LCD waveform to AC, frame synchronous signal) and supplies them to the column driver to control display. It provides 64 driver output lines and the impedance is low enough to drive a large screen.

As the HD61203 is produced by a CMOS process, it is fit for use in portable battery-driven equipment utilizing the liquid crystal display's low power consumption. The user can easily construct a dot matrix liquid crystal graphic display system by combining the HD61203 and the column (segment) driver HD61202.

Features

- Dot matrix liquid crystal graphic display common driver with low impedance
- Low impedance: 1.5 kΩ max
- Internal liquid crystal display driver circuit: 64 circuits
- Internal dynamic display timing generator circuit
- Display duty cycle
  When used with the column driver HD61202:
  1/48, 1/64, 1/96, 1/128
  When used with the column driver HD61200:
  Selectable out of 1/32 to 1/128
- Low power dissipation: During display: 5 mW
- Power supplies: V_{CC}: 5 V ± 10%
- Power supply voltage for liquid crystal display drive: 8 V to 17 V
- CMOS process

Ordering Information

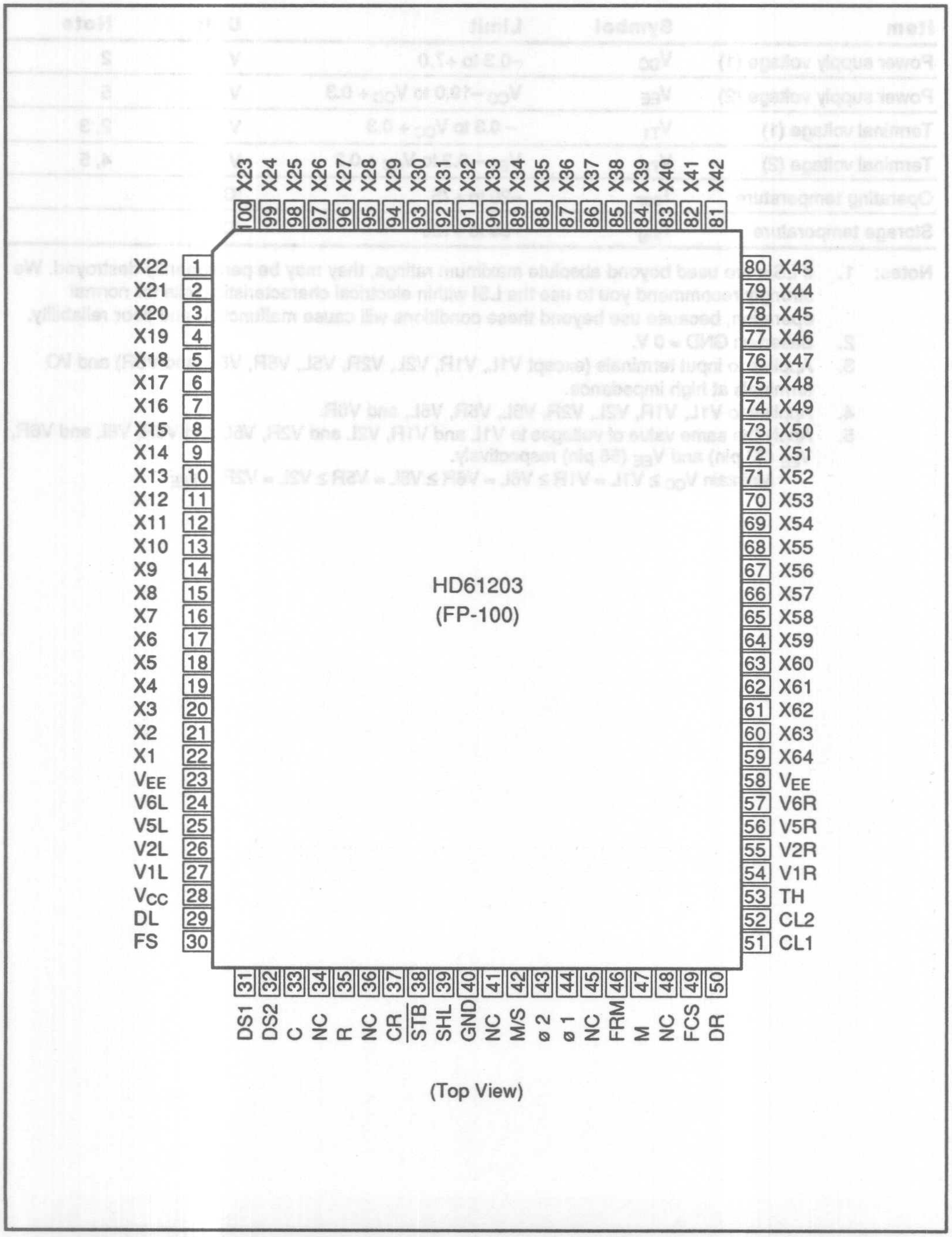
Type No.	Package
HD61203	100-pin plastic QFP(FP-100)
HD61203TFIA	100-pin thin plastic QFP(TFP-60)
HD61203D	Chip

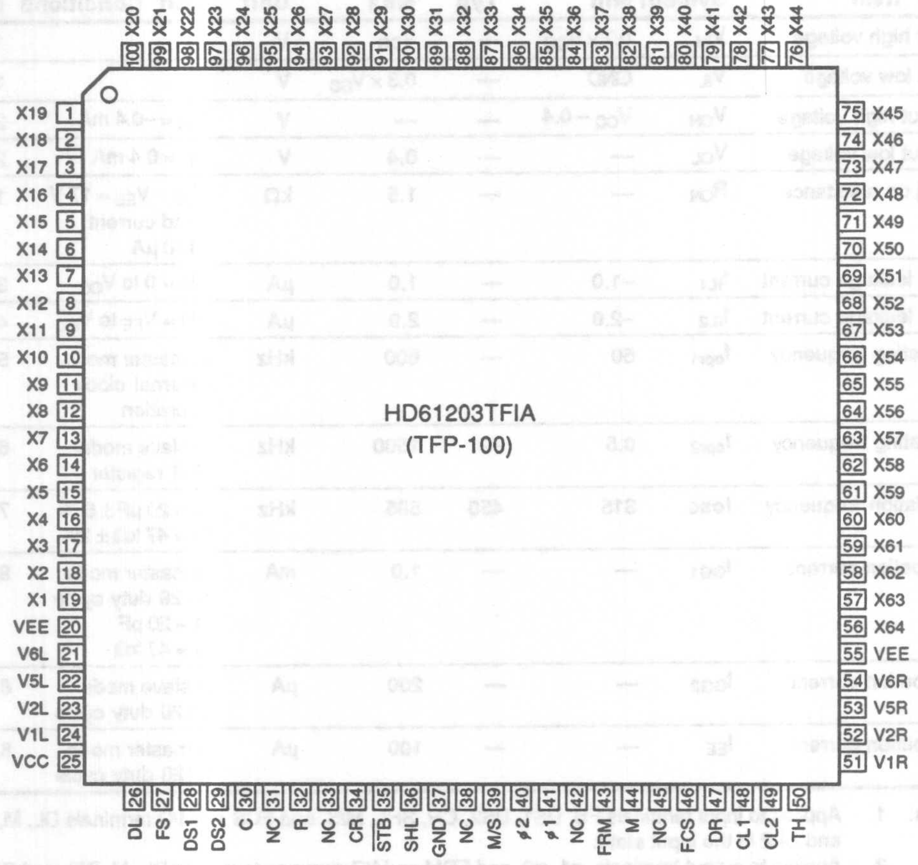
Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Note
Power supply voltage (1)	V_{CC}	–0.3 to +7.0	V	2
Power supply voltage (2)	V_{EE}	V_{CC} –19.0 to V_{CC} + 0.3	V	5
Terminal voltage (1)	V_{T1}	– 0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4, 5
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes:
1. If LSIs are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend you to use the LSI within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.
2. Based on GND = 0 V.
3. Applies to input terminals (except V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R) and I/O terminals at high impedance.
4. Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R.
5. Apply the same value of voltages to V1L and V1R, V2L and V2R, V5L and V5R, V6L and V6R, V_{EE} (23 pin) and V_{EE} (58 pin) respectively.
   Maintain $V_{CC} \geq V1L = V1R \geq V6L = V6R \geq V5L = V5R \geq V2L = V2R \geq V_{EE}$

Pin Arrangement




HD61203TFIA
(TFP-100)
X19 1
X18 2
X17 3
X16 4
X15 5
X14 6
X13 7
X12 8
X11 9
X10 10
X9 11
X8 12
X7 13
X6 14
X5 15
X4 16
X3 17
X2 18
X1 19
VEE 20
V6L 21
V5L 22
V2L 23
V1L 24
VCC 25
26 DL
27 FS
28 DS1
29 DS2
30 C
31 NC
32 R
33 NC
34 CR
35 STB
36 SHL
37 GND
38 NC
39 M/S
40 φ2
41 φ1
42 NC
43 FRM
44 M
45 NC
46 FCS
47 DR
48 CL1
49 CL2
50 TH
51 V1R
52 V2R
53 V5R
54 V6R
55 VEE
56 X64
57 X63
58 X62
59 X61
60 X60
61 X59
62 X58
63 X57
64 X56
65 X55
66 X54
67 X53
68 X52
69 X51
70 X50
71 X49
72 X48
73 X47
74 X46
75 X45
76 X44
77 X43
78 X42
79 X41
80 X40
81 X39
82 X38
83 X37
84 X36
85 X35
86 X34
87 X33
88 X32
89 X31
90 X30
91 X29
92 X28
93 X27
94 X26
95 X25
96 X24
97 X23
98 X22
99 X21
100 X20

(Top View)

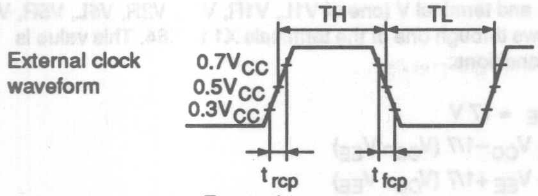
Electrical Characteristics

DC Characteristics

(V_{CC} = 5 V ± 10%, GND = 0 V, $V_{CC} - V_{EE}$ = 8.0 to 17.0 V, Ta = –20 to +75°C)

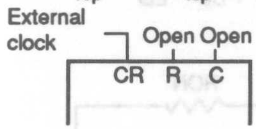
		Specifications					
Test Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Input high voltage	V_{IH}	$0.7 \times V_{CC}$	—	V_{CC}	V		1
Input low voltage	V_{IL}	GND	—	$0.3 \times V_{CC}$	V		1
Output high voltage	V_{OH}	$V_{CC} - 0.4$	—	—	V	I_{OH} = –0.4 mA	2
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 0.4 mA	2
Vi–Xj on resistance	R_{ON}	—	—	1.5	kΩ	$V_{CC} - V_{EE}$ = 17 V Load current ±150 µA	13
Input leakage current	I_{IL1}	–1.0	—	1.0	µA	Vin = 0 to V_{CC}	3
Input leakage current	I_{IL2}	–2.0	—	2.0	µA	Vin = V_{EE} to V_{CC}	4
Operating frequency	f_{opr1}	50	—	600	kHz	In master mode external clock operation	5
Operating frequency	f_{opr2}	0.5	—	1500	kHz	In slave mode shift register	6
Oscillation frequency	fosc	315	450	585	kHz	Cf = 20 pF ± 5 % Rf = 47 kΩ ± 2%	7, 12
Dissipation current (1)	I_{GG1}	—	—	1.0	mA	In master mode 1/128 duty cycle Cf = 20 pF Rf = 47 kΩ	8, 9
Dissipation current (2)	I_{GG2}	—	—	200	µA	In slave mode 1/128 duty cycle	8, 10
Dissipation current	I_{EE}	—	—	100	µA	In master mode 1/128 duty cycle	8, 11

Notes:
1. Applies to input terminals FS, DS1, DS2, CR, SHL, M/S, and FCS and I/O terminals DL, M, DR, and CL2 in the input state.
2. Applies to output terminals, ø1, ø2, and FRM and I/O common terminals DL, M, DR, and CL2 in the output state.
3. Applies to input terminals FS, DS1, DS2, CR, $\overline{\text{STB}}$, SHL, M/S, FCS, CL1, and TH, I/O terminals DL, M, DR, and CL2 in the input state and NC terminals.
4. Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R. Don't connect any lines to X1 to X64.
5. External clock is as follows.

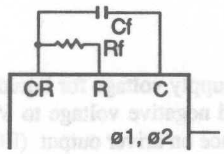


$$\text{Duty Cycle} = \frac{TH}{TH + TL} \times 100\%$$

	Min	Typ	Max	Unit
Duty cycle	45	50	55	%
t_{rcp}	–	–	50	ns
t_{fcp}	–	–	50	ns



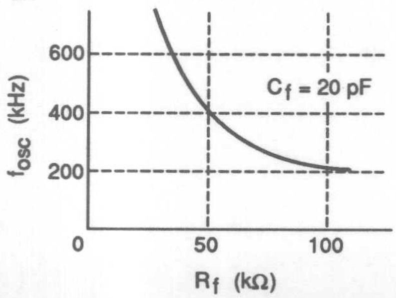
6. Applies to the shift register in the slave mode. For details, refer to AC Characteristics.
7. Connect oscillation resister (Rf) and oscillation capacitance (Cf) as shown in this figure. Oscillation frequency (f_{OSC}) is twice as much as the frequency (fø) at ø1 or ø2.



Cf = 20 pF
Rf = 47 kΩ

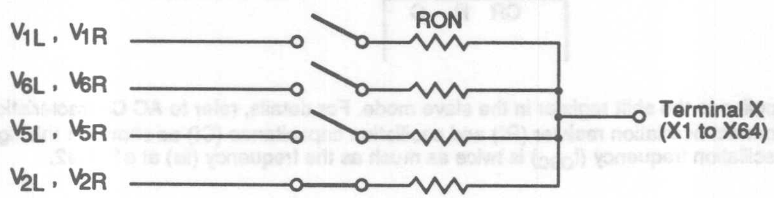
$f_{osc} = 2 \times fø$

8. No lines are connected to output terminals and current flowing through the input circuit is excluded. This value is specified at $V_{IH} = V_{CC}$ and V_{IL} = GND.
9. This value is specified for current flowing through GND in the following conditions: Internal oscillation circuit is used. Each terminal of DS1, DS2, FS, SHL, M/S, $\overline{STB}$, and FCS is connected to V_{CC} and each of CL1 and TH to GND. Oscillator is set as described in note 7.
10. This value is specified for current flowing through GND under the following conditions: Each terminals of DS1, DS2, FS, SHL, $\overline{STB}$, FCS, and CR is connected to V_{CC}, CL1, TH, and M/S to GND and the terminals CL2, M, and DL are respectively connected to terminals CL2, M, and DL of the HD61203 under the condition described in note 9.
11. This value is specified for current flowing through V_{EE} under the condition described in note 9. Don't connect any lines to terminal V.
12. This figure shows a typical relation among oscillation frequency, Rf and Cf. Oscillation frequency may vary with the mounting conditions.

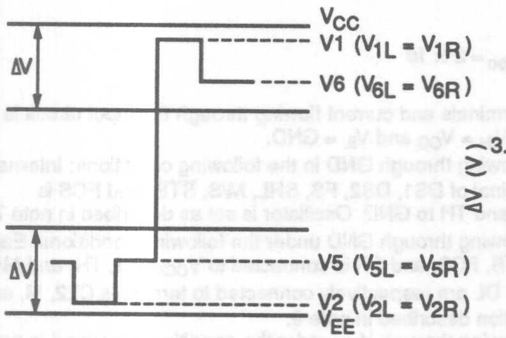


13. Resistance between terminal X and terminal V (one of V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R) when load current flows through one of the terminals X1 to X64. This value is specified under the following conditions:

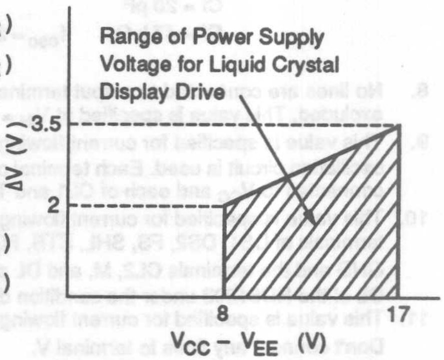
$$V_{CC} - V_{EE} = 17\ \text{V}$$
$$V_{1L} = V_{1R},\ V_{6L} = V_{6R} = V_{CC} - 1/7\ (V_{CC} - V_{EE})$$
$$V_{2L} = V_{2R},\ V_{5L} = V_{5R} = V_{EE} + 1/7\ (V_{CC} - V_{EE})$$



The following is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L = V1R and V6L = V6R and negative voltage to V2L = V2R and V5L = V5R within the ΔV range. This range allows stable impedance on driver output (RON). Notice that ΔV depends on power supply voltage $V_{CC} - V_{EE}$.



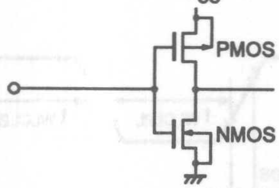
Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage $V_{CC} - V_{EE}$ and ΔV

Terminal Configuration

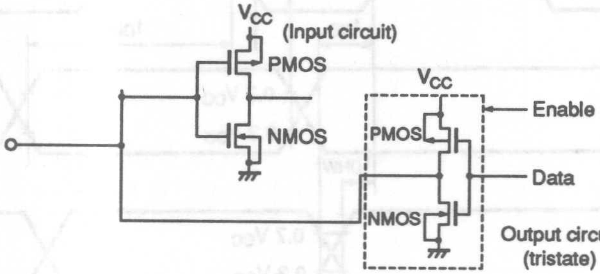
Input Terminal



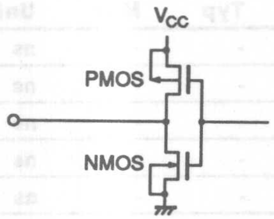
Applicable Terminals :
CR, M/S, SHL, FCS, DS1, DS2, FS

I/O Terminal

Applicable Terminals: DL, DR, CL2, M

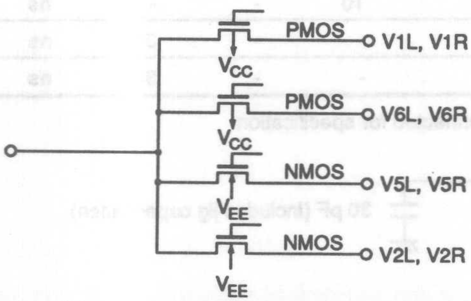


Output Terminal



Applicable Terminals: ø1, ø2, FRM

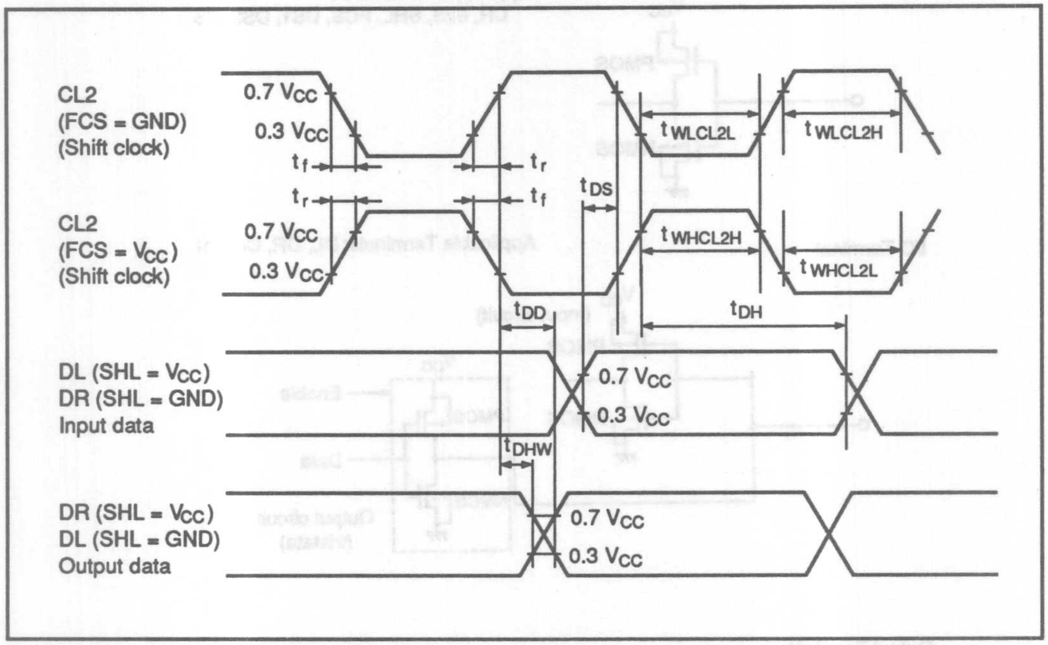
Output Terminal



Applicable Terminals:
X1 to X64

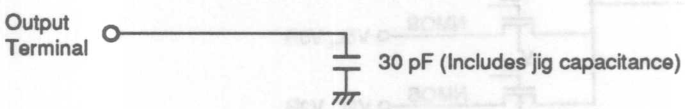
AC Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, Ta = –20 to +75°C)

In the slave mode (M/S = GND)

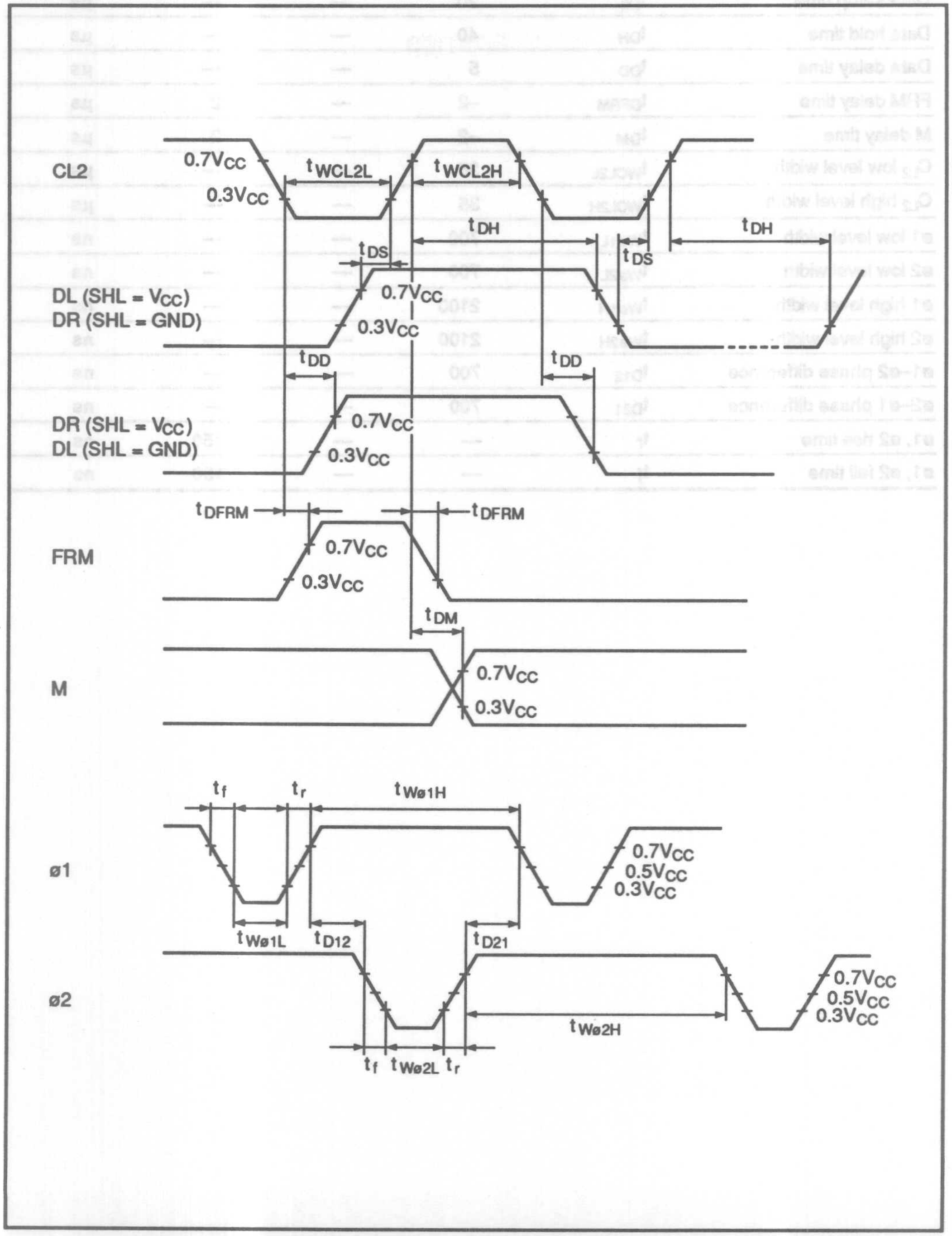


Item	Symbol	Min	Typ	Max	Unit	Note
CL2 low level width (FCS=GND)	t_{WLCL2L}	450	-	-	ns	
CL2 high level width (FCS=GND)	t_{WLCL2H}	150	-	-	ns	
CL2 low level width (FCS=V_{CC})	t_{WHCL2L}	150	-	-	ns	
CL2 high level width (FCS=V_{CC})	t_{WHCL2H}	450	-	-	ns	
Data setup time	t_{DS}	100	-	-	ns	
Data hold time	t_{DH}	100	-	-	ns	
Data delay time	t_{DD}	-	-	200	ns	1
Output data hold time	t_{DHW}	10	-	-	ns	
CL2 rise time	t_r	-	-	30	ns	
CL2 fall time	t_f	-	-	30	ns	

Notes: 1. The following load circuit is connected for specification:

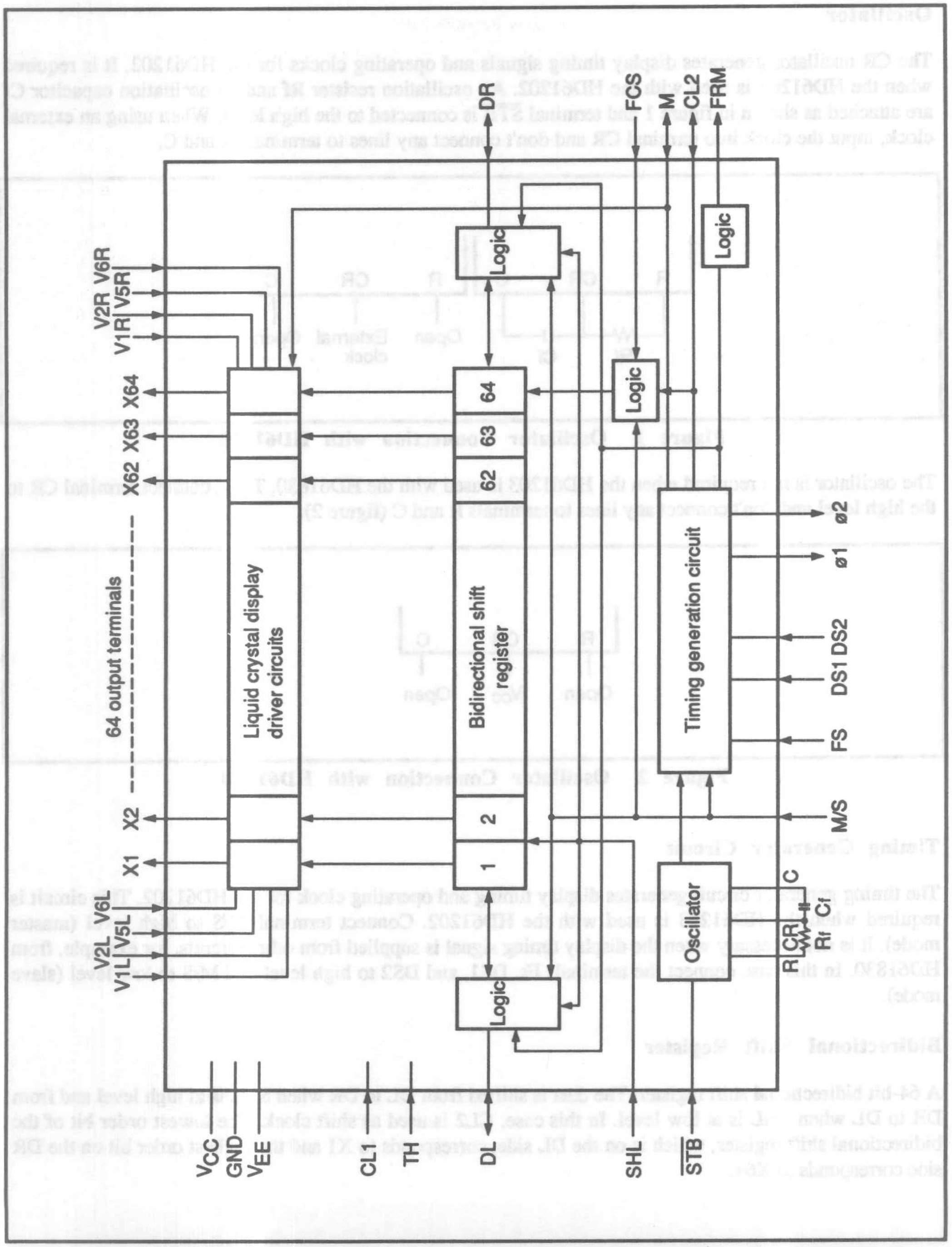


2. In the master mode (M/S = V_{CC}, FCS = V_{CC}, Cf = 20 pF, Rf = 47 kΩ)



Item	Symbol	Min	Typ	Max	Unit
Data setup time	t_{DS}	20	—	—	µs
Data hold time	t_{DH}	40	—	—	µs
Data delay time	t_{DD}	5	—	—	µs
FRM delay time	t_{DFRM}	−2	—	2	µs
M delay time	t_{DM}	−2	—	2	µs
C_{L2} low level width	t_{WCL2L}	35	—	—	µs
C_{L2} high level width	t_{WCL2H}	35	—	—	µs
ø1 low level width	$t_{Wø1L}$	700	—	—	ns
ø2 low level width	$t_{Wø2L}$	700	—	—	ns
ø1 high level width	$t_{Wø1H}$	2100	—	—	ns
ø2 high level width	$t_{Wø2H}$	2100	—	—	ns
ø1–ø2 phase difference	t_{D12}	700	—	—	ns
ø2–ø1 phase difference	t_{D21}	700	—	—	ns
ø1, ø2 rise time	t_r	—	—	150	ns
ø1, ø2 fall time	t_f	—	—	150	ns

Block Diagram



Block Functions

Oscillator

The CR oscillator generates display timing signals and operating clocks for the HD61202. It is required when the HD61203 is used with the HD61202. An oscillation resister Rf and an oscillation capacitor Cf are attached as shown in figure 1 and terminal $\overline{\text{STB}}$ is connected to the high level. When using an external clock, input the clock into terminal CR and don't connect any lines to terminals R and C.

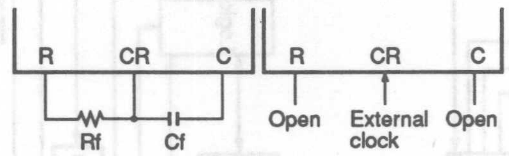


Figure 1 Oscillator Connection with HD61202

The oscillator is not required when the HD61203 is used with the HD61830. Then, connect terminal CR to the high level and don't connect any lines to terminals R and C (figure 2).

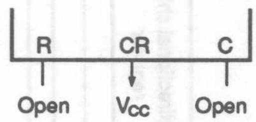


Figure 2 Oscillator Connection with HD61830

Timing Generator Circuit

The timing generator circuit generates display timing and operating clock for the HD61202. This circuit is required when the HD61203 is used with the HD61202. Connect terminal M/S to high level (master mode). It is not necessary when the display timing signal is supplied from other circuits, for example, from HD61830. In this case connect the terminals Fs, DS1, and DS2 to high level and M/S to low level (slave mode).

Bidirectional Shift Register

A 64-bit bidirectional shift register. The data is shifted from DL to DR when SHL is at high level and from DR to DL when SHL is at low level. In this case, CL2 is used as shift clock. The lowest order bit of the bidirectional shift register, which is on the DL side, corresponds to X1 and the highest order bit on the DR side corresponds to X64.

Liquid Crystal Display Driver Circuit

The combination of the data from the shift register with the M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to the output terminals (table 1).

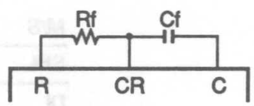
Table 1 Output Levels

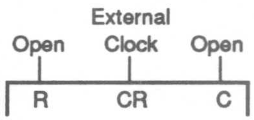
Data from the Shift Register	M	Output Level
1	1	V2
0	1	V6
1	0	V1
0	0	V5

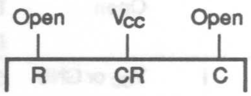
HD61203 Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Function
V_{CC} GND V_{EE}	1 1 2		Power supply	V_{CC}–GND: Power supply for internal logic. V_{CC}–V_{EE}: Power supply for driver circuit logic.
V1L, V2L V5L, V6L V1R, V2R V5R, V6R	8		Power supply	Liquid crystal display driver level power supply. V1L (V1R), V2L (V2R): Selected level V5L (V5R), V6L (V6R): Non-selected level Voltages of the level power supplies connected to V1L and V1R should be the same. (This applies to the combination of V2L & V2R, V5L & V5R and V6L & V6R respectively)
M/S	1	I	V_{CC} or GND	Selects master/slave. M/S = V_{CC}: Master mode When the HD61203 is used with the HD61202, timing generation circuit operates to supply display timing signals and operation clock to the HD61202. Each of I/O common terminals DL, DR, CL2, and M is in the output state. M/S = GND: Slave mode The timing operation circuit stops operating. The HD61203 is used in this mode when combined with the HD61830. Even if combined with the HD61202, this mode is used when display timing signals (M, data, CL2, etc.) are supplied by another HD61203 in the master mode. Terminals M and CL2 are in the input state. When SHL is V_{CC}, DL is in the input state and DR is in the output state. When SHL is GND, DL is in the output state and DR is in the input state.
FCS	1	I	V_{CC} or GND	Selects shift clock phase. FCS = V_{CC}: Shift register operates at the rising edge of CL2. Select this condition when HD61203 is used with HD61202 or when MA of the HD61830 connects to CL2 in combination with the HD61830. FCS = GND: Shift register operates at the fall of CL2. Select this condition when CL1 of HD61830 connects to CL2 in combination with the HD61830.
FS	1	I	V_{CC} or GND	Selects frequency. When the frame frequency is 70 Hz, the oscillation frequency should be: f_{osc} = 430 kHz at FCS = V_{CC} f_{osc} = 215 kHz at FCS = GND This terminal is active only in the master mode. Connect it to V_{CC} in the slave mode.

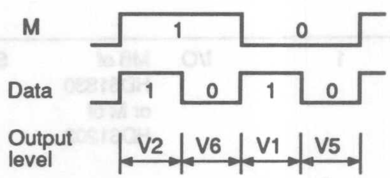
HD61203 Terminal Functions (cont)

<table>
<tr><th>Terminal Name</th><th>Number of Terminals</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>DS1, DS2</td><td>2</td><td>I</td><td>V_{CC} or GND</td><td>Selects display duty factor
<table>
<tr><th>Display Duty Factor</th><th>1/48</th><th>1/64</th><th>1/96</th><th>1/128</th></tr>
<tr><td>DS1</td><td>GND</td><td>GND</td><td>V_{CC}</td><td>V_{CC}</td></tr>
<tr><td>DS2</td><td>GND</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td></tr>
</table>
These terminals are valid only in the master mode.
Connect them to V_{CC} in the slave mode.</td></tr>
<tr><td>$\overline{\text{STB}}$
TH
CL1</td><td>1
1
1</td><td>I</td><td>V_{CC} or GND</td><td>Input terminal for testing.
Connect to $\overline{\text{STB}}$ V_{CC}.
Connect TH and CL1 to GND.</td></tr>
<tr><td>CR, R, C</td><td>3</td><td></td><td></td><td>Oscillator.
In the master mode, use these terminals as shown below:
Internal oscillation


External clock


In the slave mode, stop the oscillator as shown below:

</td></tr>
<tr><td>ø1, ø2</td><td>2</td><td>O</td><td>HD61202</td><td>Operating clock output terminals for the HD61202.
Master mode: Connect these terminals to terminals ø1 and ø2 of the HD61202 respectively.
Slave mode: Don't connect any lines to these terminals.</td></tr>
<tr><td>FRM</td><td>1</td><td>O</td><td>HD61202</td><td>Frame signal.
Master mode: Connect this terminal to terminal FRM of the HD61202.
Slave mode: Don't connect any lines to this terminal.</td></tr>
<tr><td>M</td><td>1</td><td>I/O</td><td>MB of HD61830 or M of HD61202</td><td>Signal to convert LCD driver signal into AC.
Master mode: Output terminal.
Connect this terminal to terminal M of the HD61202.
Slave mode: Input terminal.
Connect this terminal to terminal MB of the HD61830.</td></tr>
</table>

HD61203 Terminal Functions (cont)

<table>
<tr><th>Terminal Name</th><th>Number of Terminals</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>CL2</td><td>1</td><td>I/O</td><td>CL1 or MA of HD61830 or CL of HD61202</td><td>Shift clock
Master mode: Output terminal
Connect this terminal to terminal CL of the HD61202.
Slave mode: Input terminal
Connect this terminal to terminal CL1 or MA of the HD61830.</td></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Open or FLM of HD61830</td><td>Data I/O terminals of bidirectional shift register.
DL corresponds to X1's side and DR to X64's side.
Master mode: Output common scanning signal. Don't connect any lines to these terminals normally.
Slave mode: Connect terminal FLM of the HD61830 to DL (when SHL = V_{CC}) or DR (when SHL = GND)
<table>
<tr><td>M/S</td><td colspan="2">V_{CC}</td><td colspan="2">GND</td></tr>
<tr><td>SHL</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td><td>GND</td></tr>
<tr><td>DL</td><td>Output</td><td>Output</td><td>Input</td><td>Output</td></tr>
<tr><td>DR</td><td>Output</td><td>Output</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>NC</td><td>5</td><td></td><td>Open</td><td>Not used.
Don't connect any lines to this terminal.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects shift direction of bidirectional shift register.
<table>
<tr><th>SHL</th><th>Shift Direction</th><th>Common Scanning Direction</th></tr>
<tr><td>V_{CC}</td><td>DL → DR</td><td>X1 → X64</td></tr>
<tr><td>GND</td><td>DL ← DR</td><td>X1 ← X64</td></tr>
</table></td></tr>
<tr><td>X1–X64</td><td>64</td><td>O</td><td>Liquid crystal display</td><td>Liquid crystal display driver output.
Output one of the four liquid crystal display driver levels V1, V2, V5, and V6 with the combination of the data from the shift register and M signal.

When SHL is V_{CC}, X1 corresponds to COM1 and X64 corresponds to COM64.
When SHL is GND, X64 corresponds to COM1 and X1 corresponds to COM64.</td></tr>
</table>

Example of Application

HD61203 Connection List

H: V_{CC} } Fixed
L: GND

"-" means "open".

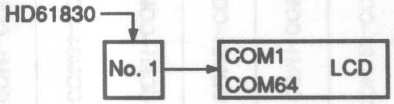
Rf: Oscillation resister
Cf: Oscillation capacitor

	M/S	TH	CL1	FCS	FS	DS1	DS2	$\overline{STB}$	CR	R	C	φ1	φ2	FRM	M	CL2	SHL	DL	DR	X1–X64
A	L	L	L	L	H	H	H	H	H	—	—	—	—	—	from MB of HD61830	from CL1 of HD61830	H	from FLM of HD61830	—	COM1–COM64
																	L	—	from FLM of HD61830	COM64–COM1
B	L	L	L	H	H	H	H	H	H	—	—	—	—	—	from MB of HD61830	from MA of HD61830	H	from FLM of HD61830	to DL/DR of HD61203 No. 2	COM1–COM64
																	L	to DL/DR of HD61203 No. 2	from FLM of HD61830	COM64–COM1
C	L	L	L	H	H	H	H	H	H	—	—	—	—	—	from MB of HD61830	from MA of HD61830	H	from DL/DR of HD61203 No. 1	—	COM65–COM128
																	L	—	from DL/DR of HD61203 No. 1	COM128–COM65
D	H	L	L	H	H	L or L	L or H	H	Rf Cf	Rf	Cf	to φ1 of HD61202	to φ2 of HD61202	to FRM of HD61202	to M of HD61202	to CL of HD61202	H	—	—	COM1–COM64
																	L	—	—	COM64–COM1
E	H	L	L	H	H	L or L	L or H	H	Rf Cf	Rf	Cf	to φ1 of HD61202	to φ2 of HD61202	to FRM of HD61202	toM of HD61202 HD61203	to CL of HD61202 to CL2 of HD61203	H	—	to DL/DR of HD61203 No. 2	COM1–COM64
																	L	to DL/DR of HD61203 No. 2	—	COM64–COM1
F	L	L	L	H	H	H	H	H	H	—	—	—	—	—	from M of HD61203 No. 1	from CL2 of HD61203 No. 1	H	from DL/DR of HD61203 No. 1	—	COM1–COM64
																	L	—	from DL/DR of HD61203 No. 1	COM64–COM1

Outline of HD61203 System Configuration

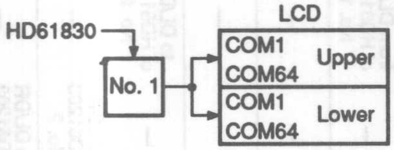
1. Use with HD61830

a. When display duty ratio of LCD is 1/64



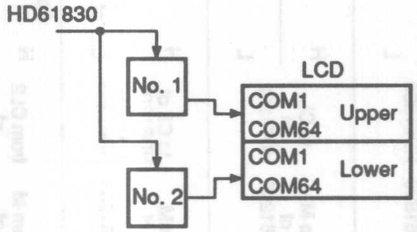
One HD61203 drives common signals.

Refer to Connection list A.



One HD61203 drives common signals for upper and lower panels.

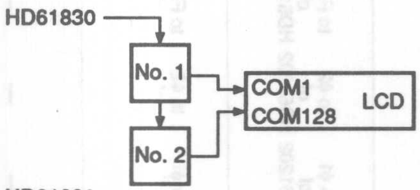
Refer to Connection list A.



Two HD61203s drive upper and lower panels separately to ensure the quality of display. No. 1 and No. 2 operate in parallel.

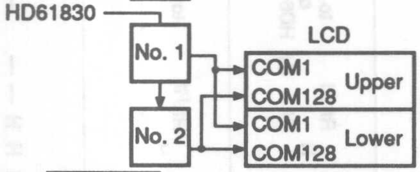
For both of No. 1 and No. 2, refer to Connection list A.

b. When display duty ratio of LCD is from 1/65 to 1/128



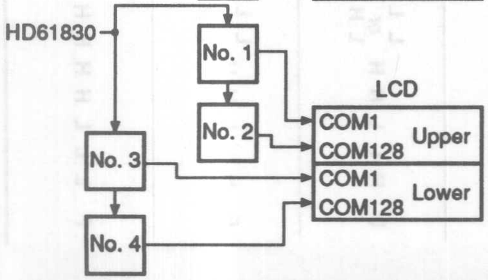
Two HD61203s connected serially drive common signals.

Refer to Connection list B for No. 1. Refer to Connection list C for No. 2.



Two HD61203s connected serially drive upper and lower panels in parallel.

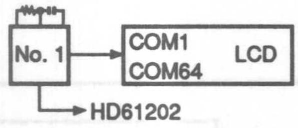
Refer to Connection list B for No. 1. Refer to Connection list C for No. 2.



Two sets of HD61203s connected serially drive upper and lower panels in parallel to ensure the quality of display.

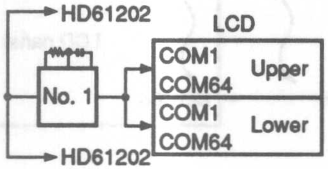
Refer to Connection list B for No. 1 and 3. Refer to Connection list C for No. 2 and 4.

2. Use with HD61202 (1/64 duty ratio)



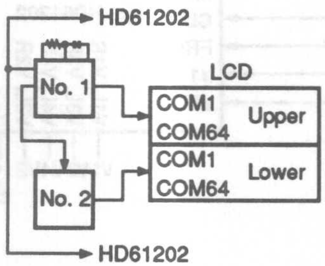
One HD61203 drives common signals and supplies timing signals to the HD61202s.

Refer to Connection list D.



One HD61203 drives upper and lower panels and supplies timing signals to the HD61202s.

Refer to Connection list D.



Two HD61203s drive upper and lower panels in parallel to ensure the quality of display. No. 1 supplies timing signals to No. 2 and the HD61202s.

Refer to Connection list E for No. 1.

Refer to Connection list F for No. 2.

Connection Example 1

Use with HD61202 (RAM type segment driver)

a. 1/64 duty ratio (See Connection List D)

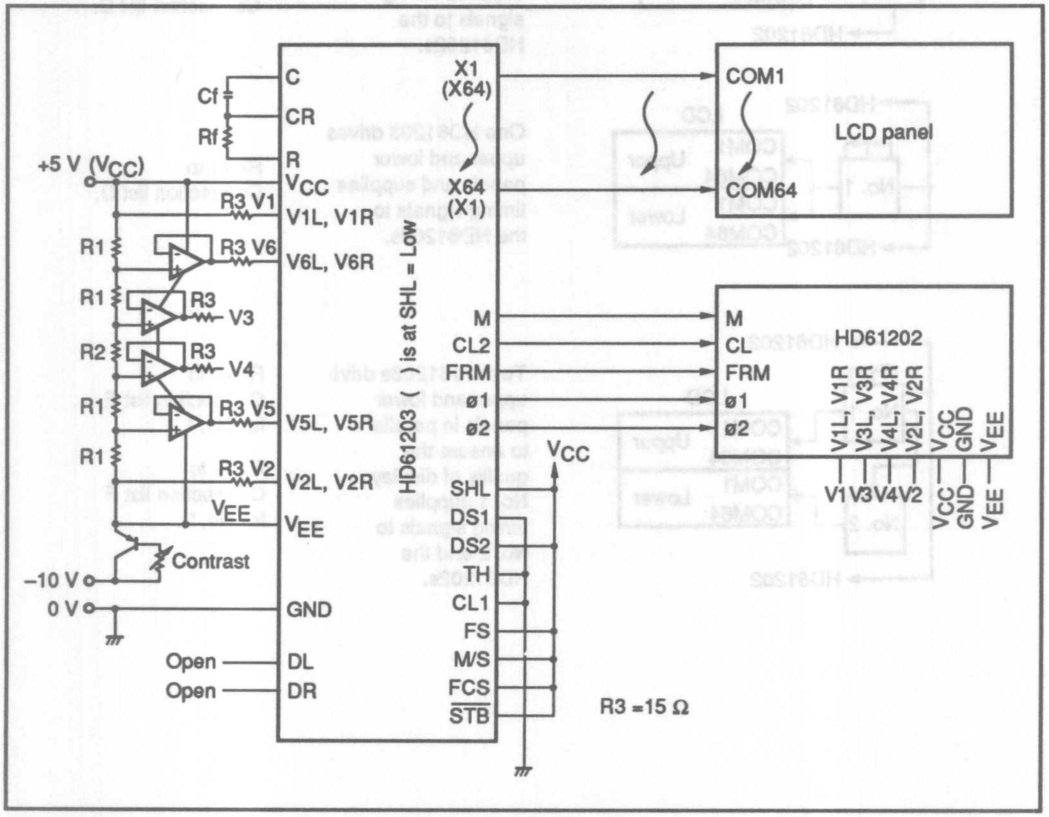


Figure 1 Example 1

Note: The values of R1 and R2 vary with the LCD panel used.
When bias factor is 1/9, the values of R1 and R2 should satisfy

$$\frac{R1}{4R1 + R2} = \frac{1}{9}$$

For example,
R1 = 3 kΩ, R2 = 15 kΩ

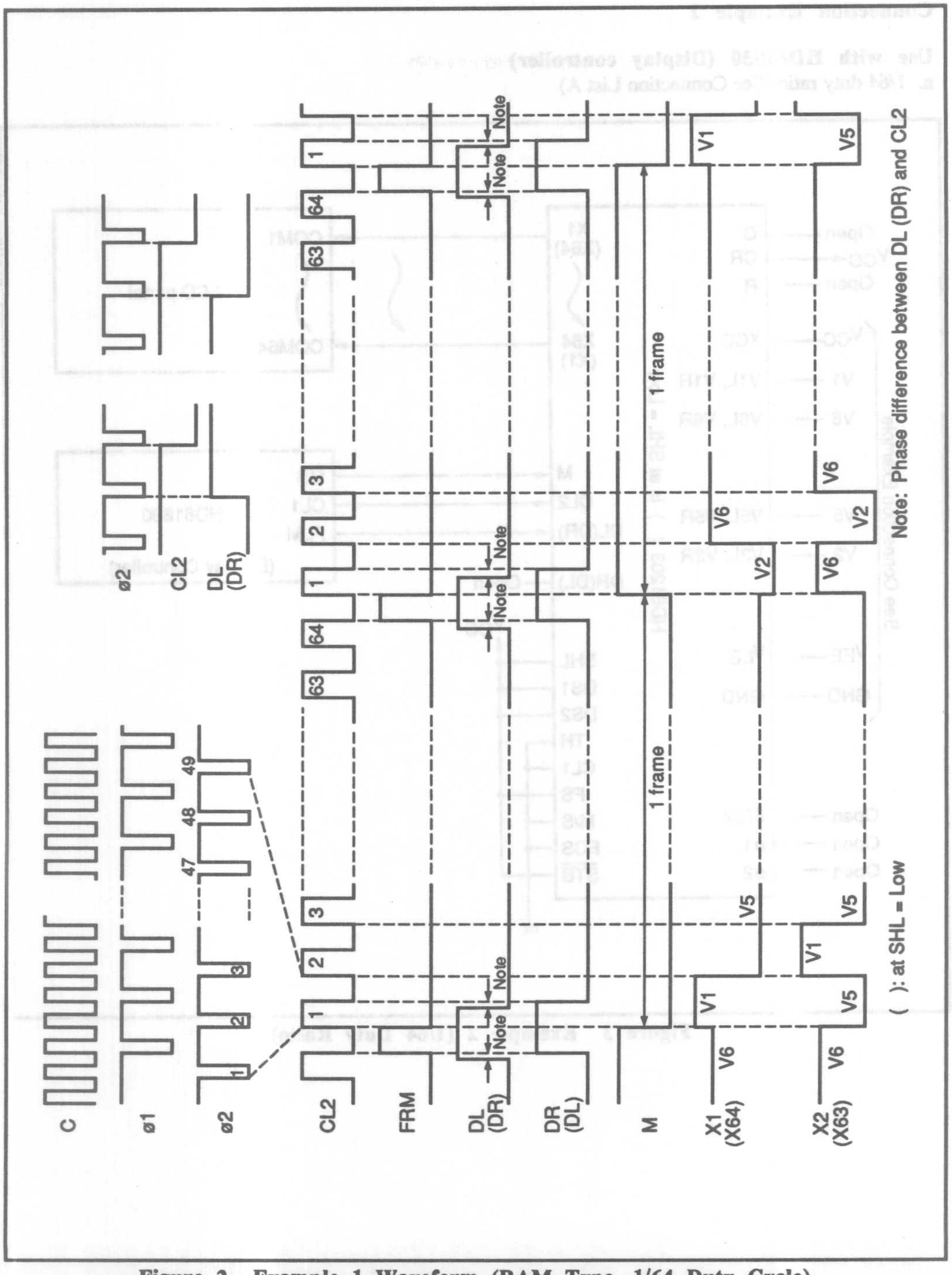


Figure 2 Example 1 Waveform (RAM Type, 1/64 Duty Cycle)

Connection Example 2

Use with HD61830 (Display controller)

a. 1/64 duty ratio (See Connection List A)

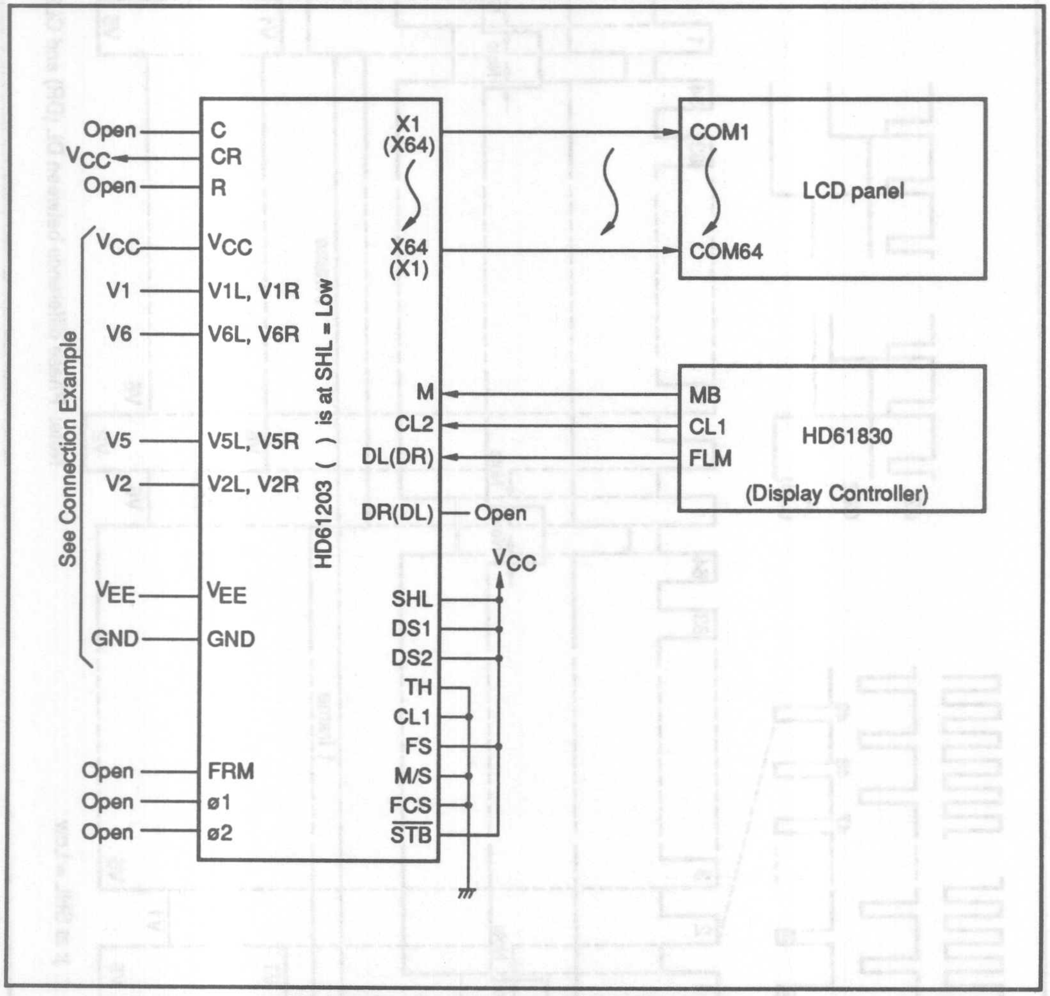


Figure 3 Example 2 (1/64 Duty Ratio)

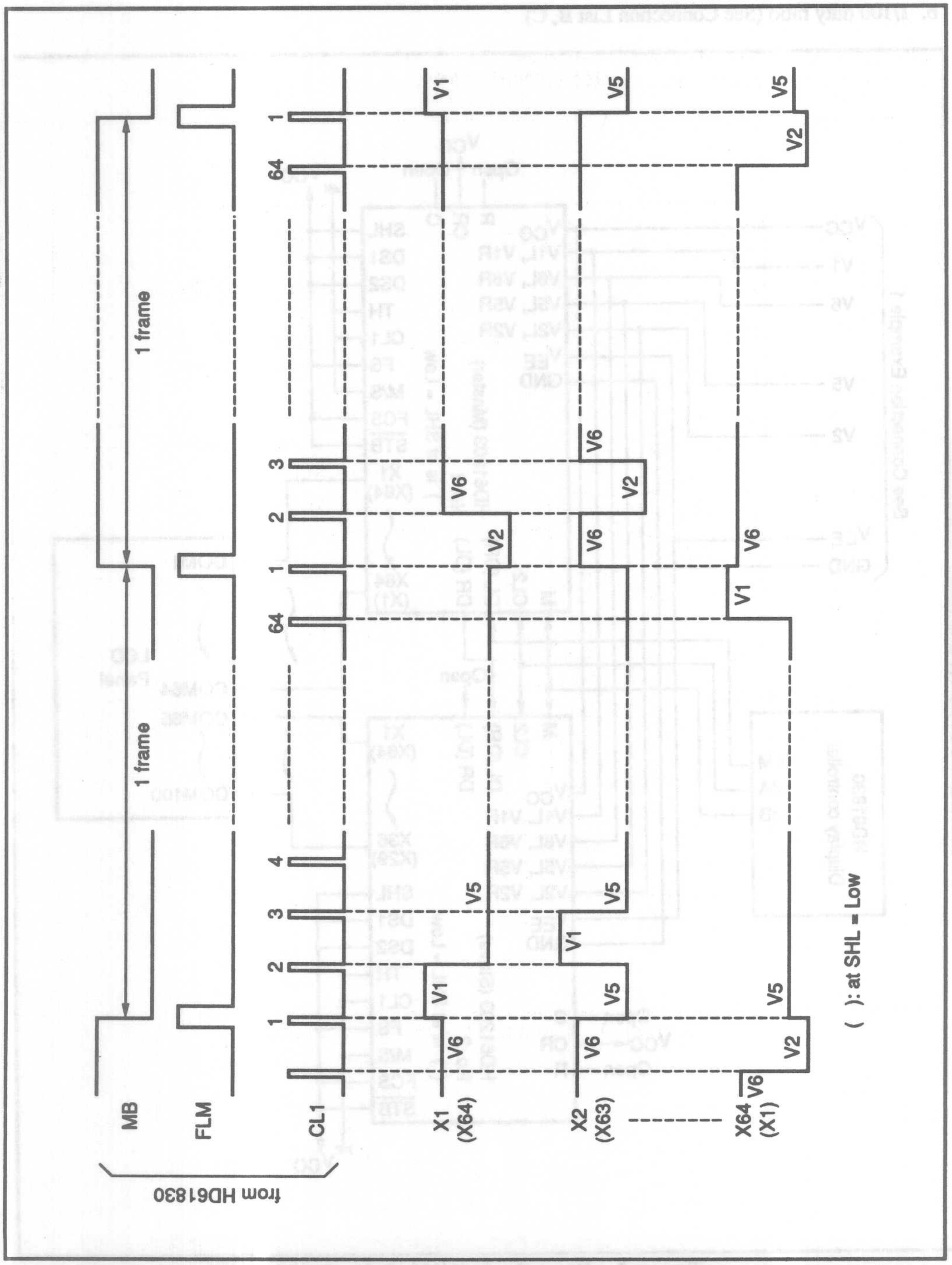


Figure 4 Example 2 Waveform (1/64 Duty Ratio)

b. 1/100 duty ratio (See Connection List B, C)

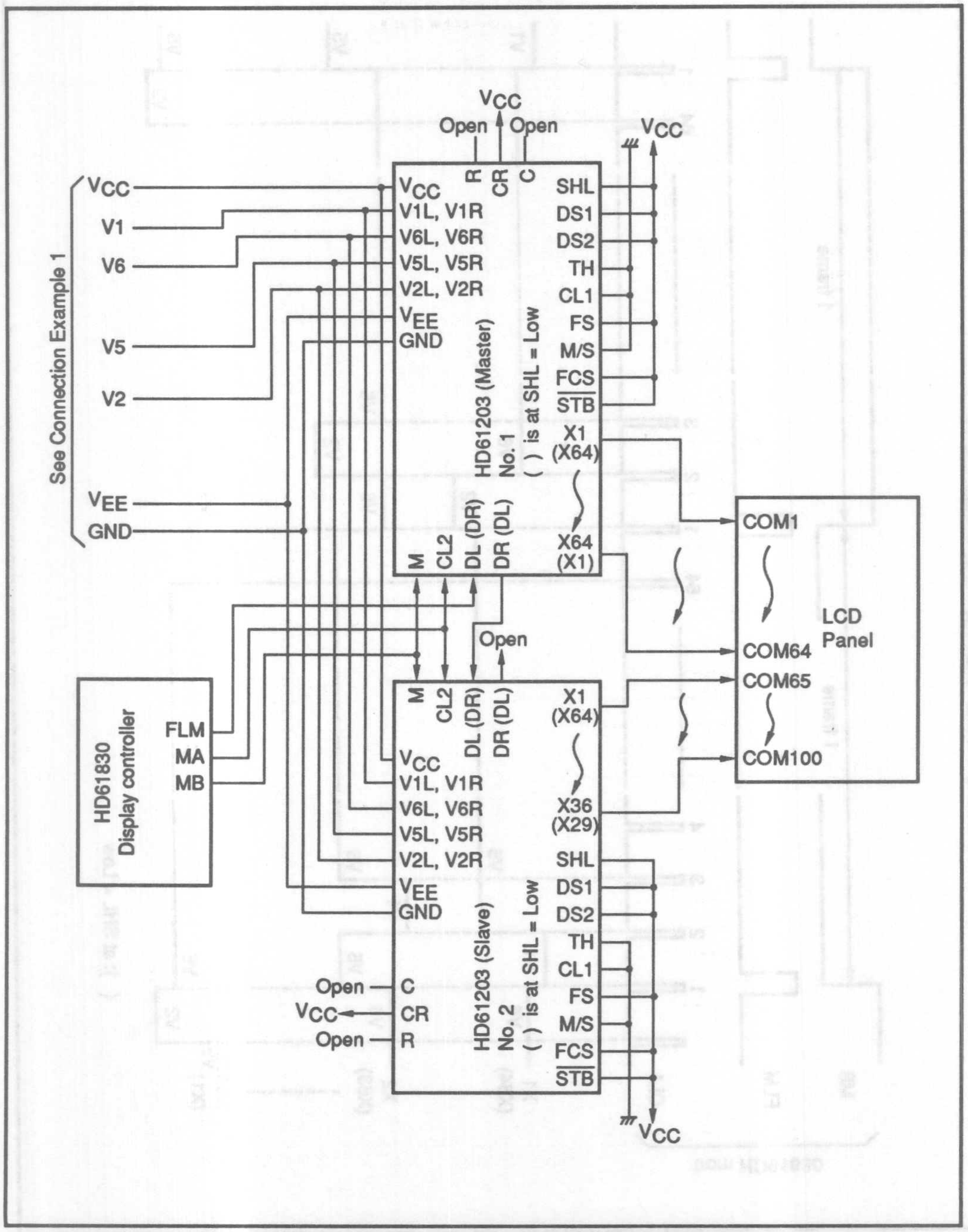


Figure 5 Example 2 (1/100 Duty Ratio)

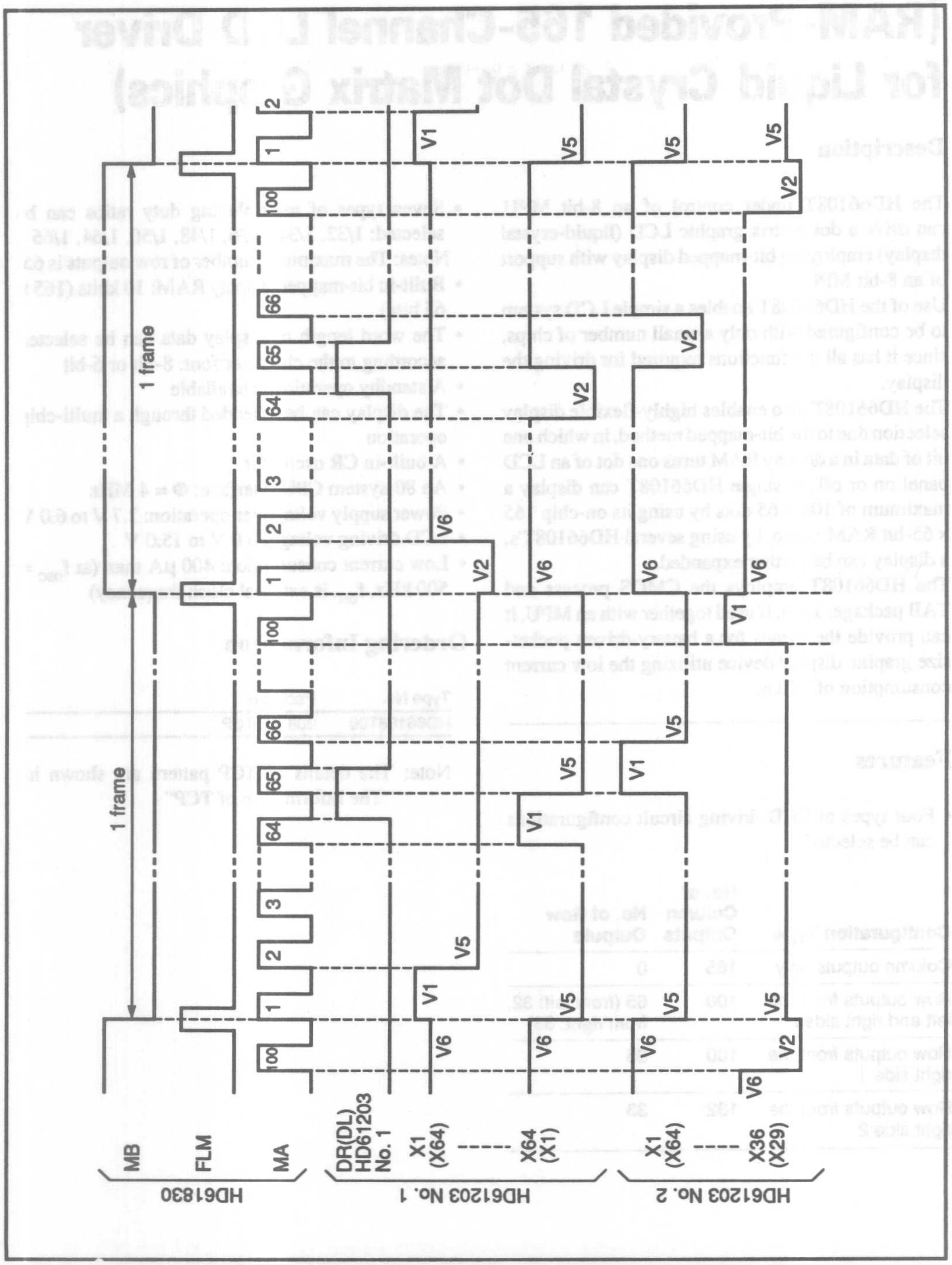


Figure 6 Example 2 Waveform (1/100 Duty Ratio)

HD66108

(RAM-Provided 165-Channel LCD Driver for Liquid Crystal Dot Matrix Graphics)

Description

The HD66108T under control of an 8-bit MPU can drive a dot matrix graphic LCD (liquid-crystal display) employing bit-mapped display with support of an 8-bit MPU.

Use of the HD66108T enables a simple LCD system to be configured with only a small number of chips, since it has all the functions required for driving the display.

The HD66108T also enables highly-flexible display selection due to the bit-mapped method, in which one bit of data in a display RAM turns one dot of an LCD panel on or off. A single HD66108T can display a maximum of 100 × 65 dots by using its on-chip 165 × 65-bit RAM. Also, by using several HD66108T's, a display can be further expanded.

The HD66108T employs the CMOS process and TAB package. Thus, if used together with an MPU, it can provide the means for a battery-driven pocket-size graphic display device utilizing the low current consumption of LCDs.

Features

- Four types of LCD driving circuit configurations can be selected:

Configuration Type	No. of Column Outputs	No. of Row Outputs
Column outputs only	165	0
Row outputs from the left and right sides	100	65 (from left: 32, from right: 33)
Row outputs from the right side 1	100	65
Row outputs from the right side 2	132	33

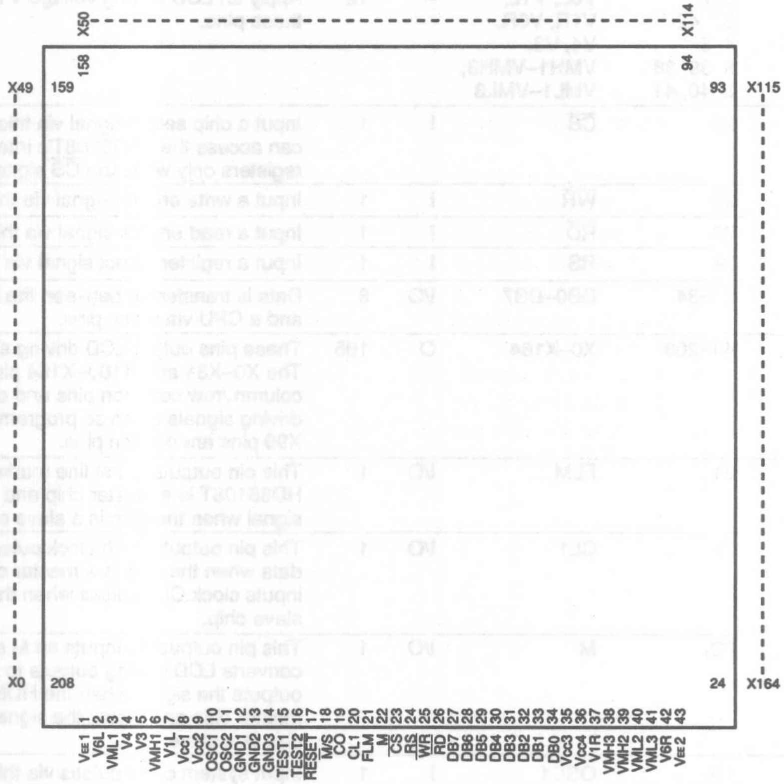
- Seven types of multiplexing duty ratios can be selected: 1/32, 1/34, 1/36, 1/48, 1/50, 1/64, 1/66
  Notes: The maximum number of row outputs is 65.
- Built-in bit-mapped display RAM: 10 kbits (165 × 65 bits)
- The word length of display data can be selected according to the character font: 8-bit or 6-bit
- A standby operation is available
- The display can be extended through a multi-chip operation
- A built-in CR oscillator
- An 80-system CPU interface: Φ = 4 MHz
- Power supply voltage for operation: 2.7 V to 6.0 V
- LCD driving voltage: 6.0 V to 15.0 V
- Low current consumption: 400 µA max (at f_{osc} = 500 kHz, f_{osc} is external clock frequency)

Ordering Information

Type No.	Package
HD66108T00	208 pin TCP

Note: The details of TCP pattern are shown in "The Information of TCP"

Chip terminals

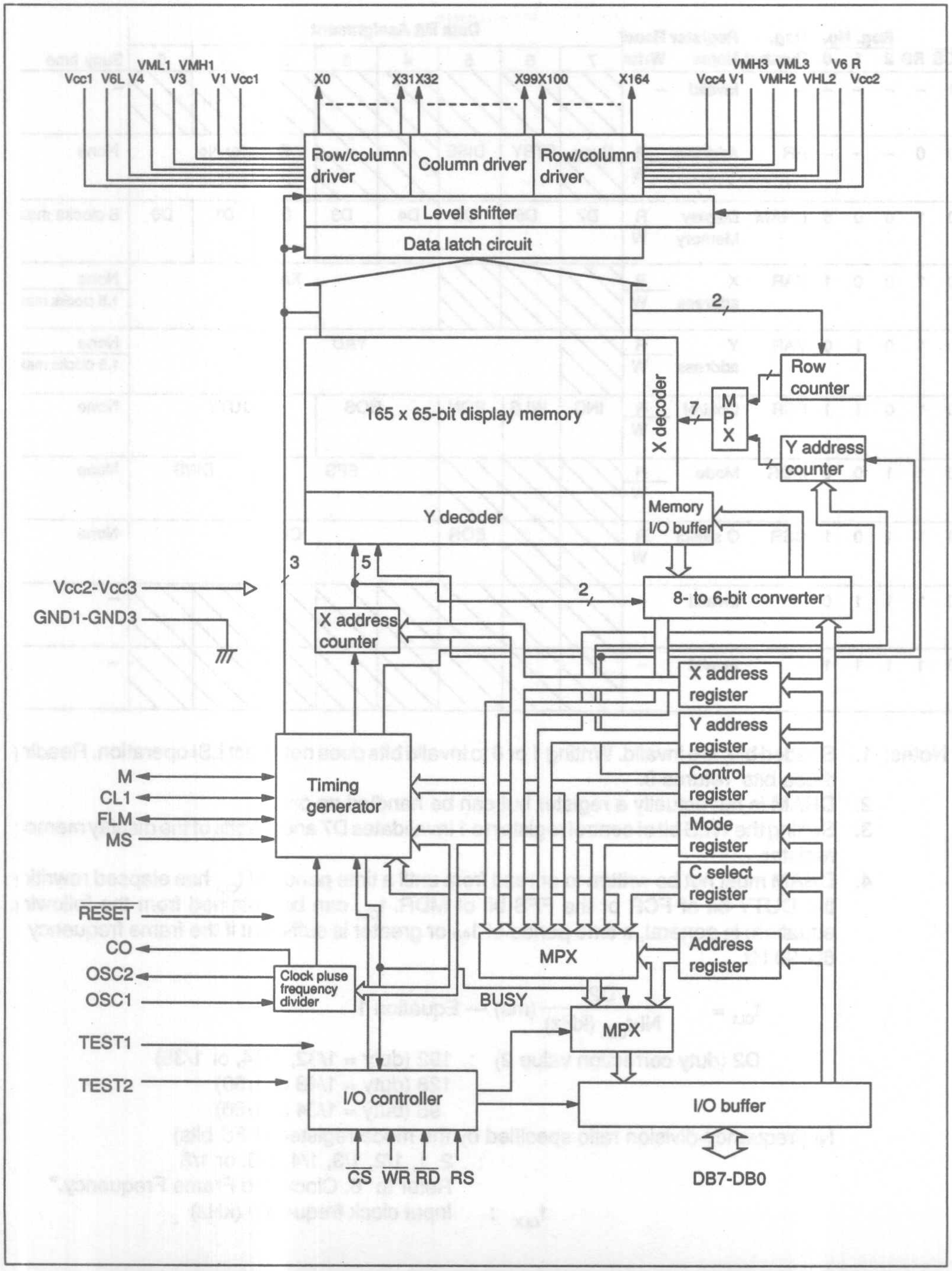


Note: The above view is seen from the grinded surface of the chip, not TCP.

Pin Description

Classification	No. of Pins	Symbol	I/O	No. of Pins	Function
Power Supply	8, 9, 35, 36	$V_{CC}1$–$V_{CC}4$	–	4	Connect these pins to V_{CC}.
	12 ~ 14	GND1–GND3	–	3	Ground these pins.
	1, 43	$V_{EE}1$, $V_{EE}2$	–	2	These pins supply power to the LCD driving circuits and should usually be set to the V6 level.
	2, 7 37, 42 4, 5 6, 39, 38 3, 40, 41	V6L, V1L, V1R, V6R, V4, V3, VMH1–VMH3, VML1–VML3	–	12	Apply an LCD driving voltage V1 to V6 to these pins.
CPU Interface	23	$\overline{CS}$	I	1	Input a chip select signal via this pin. A CPU can access the HD66108T's internal registers only while the $\overline{CS}$ signal is low.
	25	$\overline{WR}$	I	1	Input a write enable signal via this pin.
	26	$\overline{RD}$	I	1	Input a read enable signal via this pin.
	24	RS	I	1	Input a register select signal via this pin.
	27~34	DB0–DB7	I/O	8	Data is transferred between the HD66108T and a CPU via these pins.
LCD Driving Output	44~208	X0–X164	O	165	These pins output LCD driving signals. The X0–X31 and X100–X164 pins are column /row common pins and output row driving signals when so programmed. X32–X99 pins are column pins.
LCD Interface	21	FLM	I/O	1	This pin outputs a first line marker when the HD66108T is a master chip and inputs the signal when the chip is a slave chip.
	20	CL1	I/O	1	This pin outputs latch clock pulses of display data when the chip is a master chip and inputs clock CL1 pulses when the chip is a slave chip.
	22	M	I/O	1	This pin outputs or inputs an M signal, which converts LCD driving outputs to AC; it outputs the signal when the HD66108T is a master chip and inputs the signal when the chip is a slave chip.
Control Signals	10	OSC1	I	1	Input system clock pulses via this pin.
	11	OSC2	O	1	This pin outputs clock pulses generated by the internal CR oscillator.
	19	CO	O	1	This pin outputs the same clock pulses as the system clock pulses, the OSC1 pin of a slave chip. Connect with the OSC1 pin of a slave chip.
	18	$\overline{M}$/S	I	1	This pin specifies master/slave. Set this pin low when the HD66108T is a master chip and set high when the chip is a slave chip; must not be changed after power-on.
	17	$\overline{RESET}$	I	1	Input a reset signal via this pin. Setting this pin low initializes the HD66108T.
	15, 16	TEST1, TEST2	I	2	These pins input a test signal and should usually be set low.

Internal Block Diagram



Register List

CS	RS	Reg. No. 2	1	0	Reg. Symbol	Register Name	Read/Write	Data Bit Assignment 7	6	5	4	3	2	1	0	Busy time
1	–	–	–	–	–	Invalid	–									–
0	0	–	–	–	AR	Address	R W	Busy	STBY	DISE			Register No.			None
0	1	0	0	0	DRAM	Display Memory	R W	D7	D6	D5	D4	D3	D2	D1	D0	8 clocks max
0	1	0	0	1	XAR	X address	R W				XAD					None 1.5 clocks max
0	1	0	1	0	YAR	Y address	R W		YAD							None 1.5 clocks max
0	1	0	1	1	FCR	Control	R W	INC	WLS	PON	ROS		DUTY			None
0	1	1	0	0	MDR	Mode	R W				FFS			DWS		None
0	1	1	0	1	CSR	C select	R W			EOR	CLN					None
0	1	1	1	0	–	Invalid	–									–
0	1	1	1	1	–	Invalid	–									–

Notes:
1. Shaded bits are invalid. Writing 1 or 0 to invalid bits does not affect LSI operation. Readin[g] these bits returns 0.
2. DRAM is not actually a register but can be handled as one.
3. Setting the WLS bit of control register to 1 invalidates D7 and D6 bits of the display memor[y] register.
4. DRAM must not be written to or read from until a time period of t_{CL1} has elapsed rewritin[g] the DUTY bit of FCR or the FFS bit of MDR. t_{CL1} can be obtained from the followin[g] equation; in general, a time period of 1ms or greater is sufficient if the frame frequency i[s] 60–90 Hz.

$$t_{CL1} = \frac{D2}{Ni \cdot f_{CLK}\ (kHz)}\ (ms) \text{ --- Equation 1}$$

D2 (duty correction value 2) : 192 (duty = 1/32, 1/34, or 1/36)
128 (duty = 1/48 or 1/50)
96 (duty = 1/64 or 1/66)

Ni (frequency-division ratio specified by the mode register's FFS bits)
: 2, 1, 1/2, 1/3, 1/4, 1/6, or 1/8
Refer to "6. Clock and Frame Frequency."

f_{CLK} : Input clock frequency (kHz)

System Description

The HD66108T can assign a maximum of 65 out of 165 channels to row outputs for LCD driving . It also incorporates a timing generator and display memory, which are necessary to drive an LCD.

If connected to an MPU and supplied with LCD driving voltage, one HD66108T chip can be used to configure an LCD system with a 100 x 65 dot panel (figure 1). In this case, clock pulses should be supplied by the internal CR oscillator or the MPU.

Using LCD expansion signals CL1, FLM, and M enables the display size to be expanded. In this case, LCD expansion signal pins output corresponding signals when pin $\overline{M}$/S is set low for master mode and conversely input corresponding signals when pin $\overline{M}$/S is set high for slave mode; LCD expansion signal pins of both master chip and slave chips must be mutually connected. Figure 2 shows a basic system configuration using two HD66108T chips.

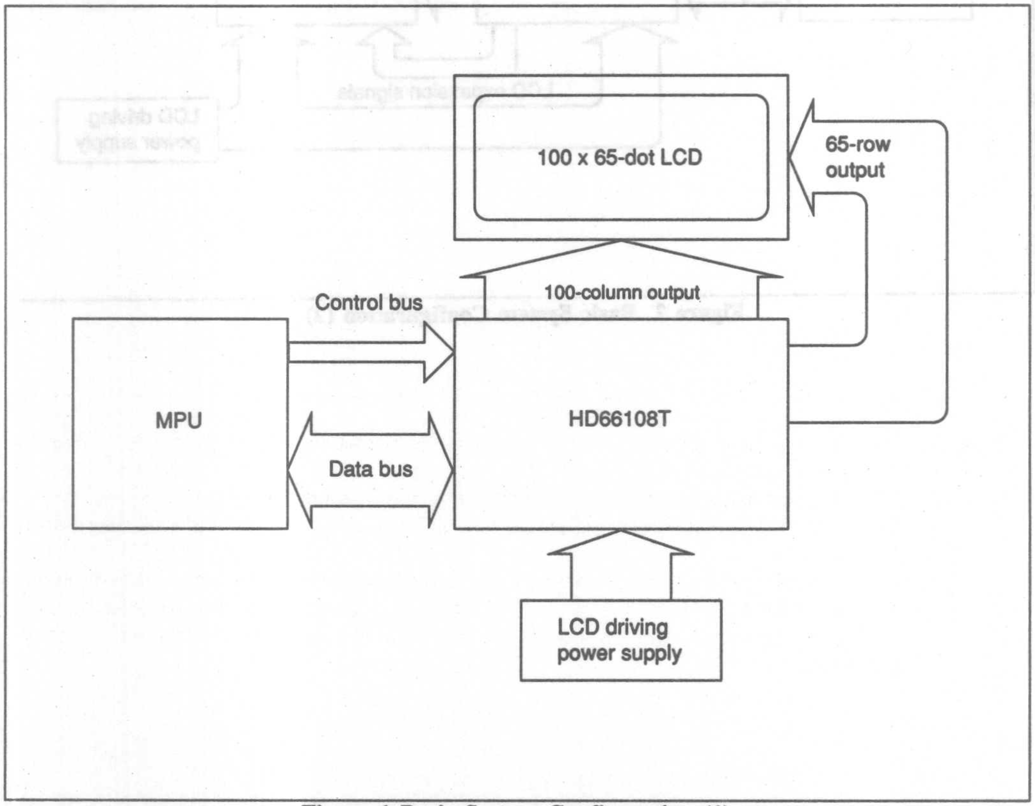


Figure 1 Basic System Configuration (1)

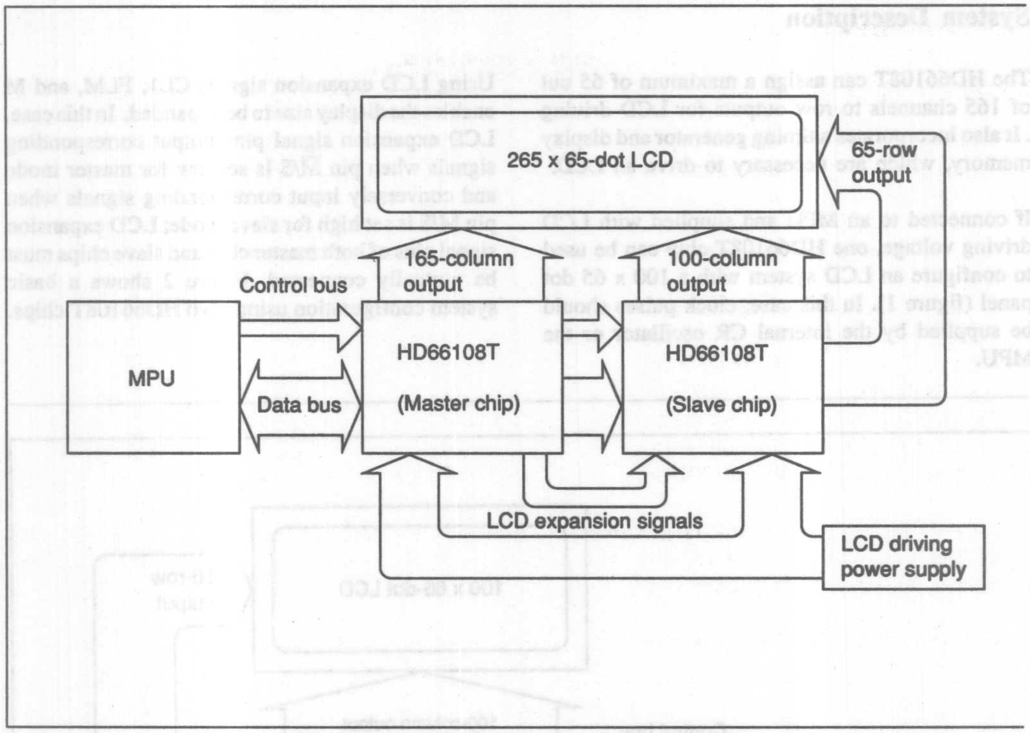


Figure 2 Basic System Configuration (2)

Functional Description

1. Display Size Programming

A variety of display sizes can be programmed by changing the system configuration and internal register settings.

(1) System Configuration Using 1 HD66108T Chip

When the 65-row-output mode is selected by internal register settings, a maximum of 100 dots in the X direction can be displayed (figure 3 (a)). Display size in the Y direction can be selected from 32 , 34, 36, 48, 50, 64 , and 65 dots according to display duty setting. Note that Y direction settings does not affect those in the X direction (100 dots).

When the 33-row-output mode is selected by internal register settings, a maximum of 132 dots in the X direction can be displayed (figure 3 (b)).

Table 1 shows the relationship between display sizes and the control register's (FCR) ROS and DUTY bits. ROS and DUTY bit settings determine the function of X pins. For more details, refer to " 4.1 Row Output Pin Selection."

(2) System Configuration Using 1 HD66108T Chip and 1 HD61203 Chip as Row Driver

A maximum of 64 dots in the Y direction and 165 dots in the X direction can be displayed. 48 or 64 dots in the Y direction can be selected by HD61203 pin settings (figure 3 (c)).

(3) System Configuration Using 2 or more HD66108T Chips

X direction size can be expanded by 165 dots per chip. Figure 3 (d) shows a 265 x 65-dot display. Y direction size can be expanded up to 130 dots with 2 chips; a 100 x 130-dot display provided by 2 chips is shown in figure 3 (e).

Table 1 Relationship between Display Size and Register Settings (No. of Dots)

ROS Bit Setting (X0-X164 Pin Function)	Duty Bit Setting (Multiplexing Duty Ratio) 1/32	1/34	1/36	1/48	1/50	1/64	1/66
165-column-output	Specified by a row driver						
65-row-output from the right side	X: 100 Y: 32	X: 100 Y: 34	X: 100 Y: 36	X: 100 Y: 48	X: 100 Y: 50	X: 100 Y: 64	X: 100 Y: 65
65-row-output from the left and right sides	X: 100 Y: 32	X: 100 Y: 34	X: 100 Y: 36	X: 100 Y: 48	X:100 Y: 50	X: 100 Y: 64	X: 100 Y: 65
33-row-output from the right side	X: 132 Y: 32	X: 132 Y: 33	X: 132 Y: 33	X: 132 Y: 33	X: 132 Y: 33	X: 132 Y: 33	X: 132 Y: 33

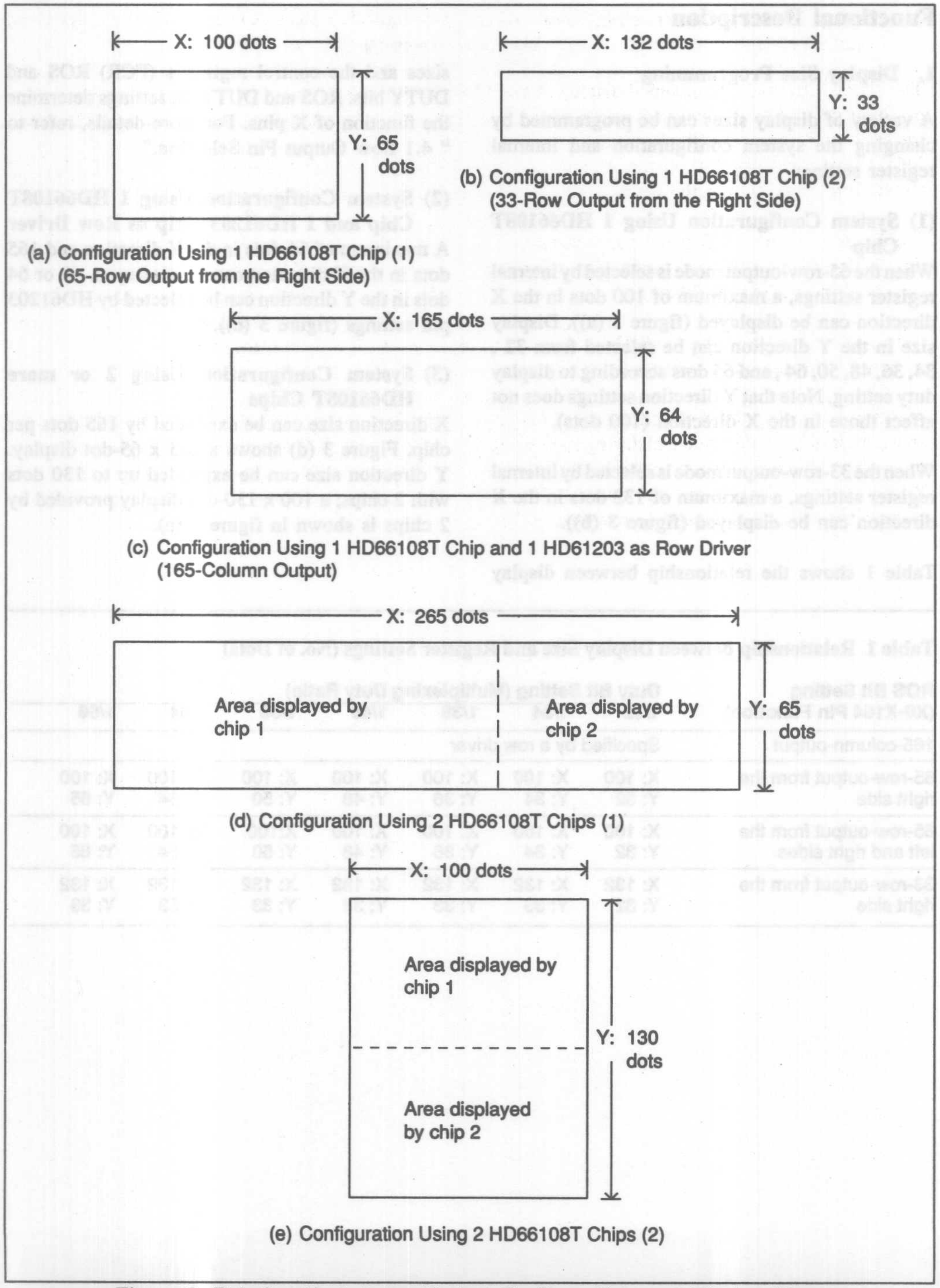


Figure 3 Relationship between System Configurations and Display Sizes

2. Display Memory Construction and Word Length Setting

The HD66108T has a bit-mapped display memory of 165 x 65 bits. As shown in figure 4, data from the MPU is stored in the display memory, with the MSB (most significant bit) on the left and the LSB (least significant bit) on the right.

The sections on the LCD panel corresponding to the display memory bits in which 1's are written will be displayed as on (black).

Display area size of the internal RAM is determined by control register (FCR) settings (refer to table 1).

The start address in the Y direction for the display area is always Y0, independent of the register setting. In contrast, the start address in the X direction is X0 in the modes for 165-column-output, 65 -row-output from the right side, and 33-row-output from the right side, and is X32 in the 65-row-output mode from the left and right sides.

Each display area contains the number of dots shown in table 1, beginning from each start address.

For more detail, refer to " 4.2 Row Output Data Setting, " figures 15 to 19.

In the display memory, one X address is assigned to each word of 8 or 6 bits long in X direction. (Either 8 or 6 bits can be selected as word length of display data.) Similarly, one Y address is assigned to each row in Y direction.

Accordingly, X address 20 in the case of 8-bit word and X address 27 in the case of 6-bit word have 5 and 3 bits of display data, respectively. Nevertheless, data is also stored here with the MSB on the left (figure 5).

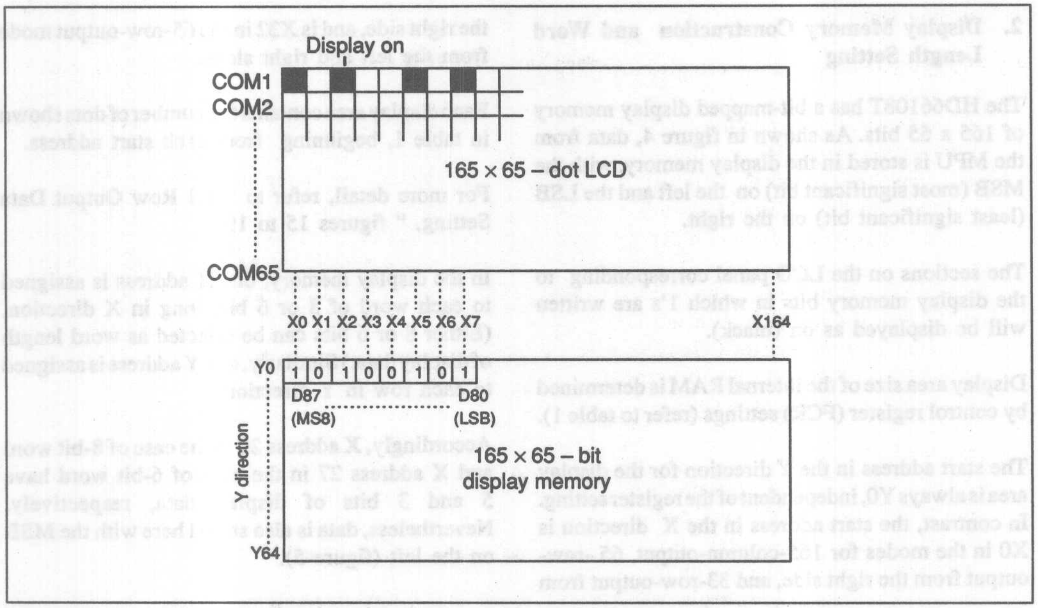


Figure 4 Relationship between Memory Construction and Display

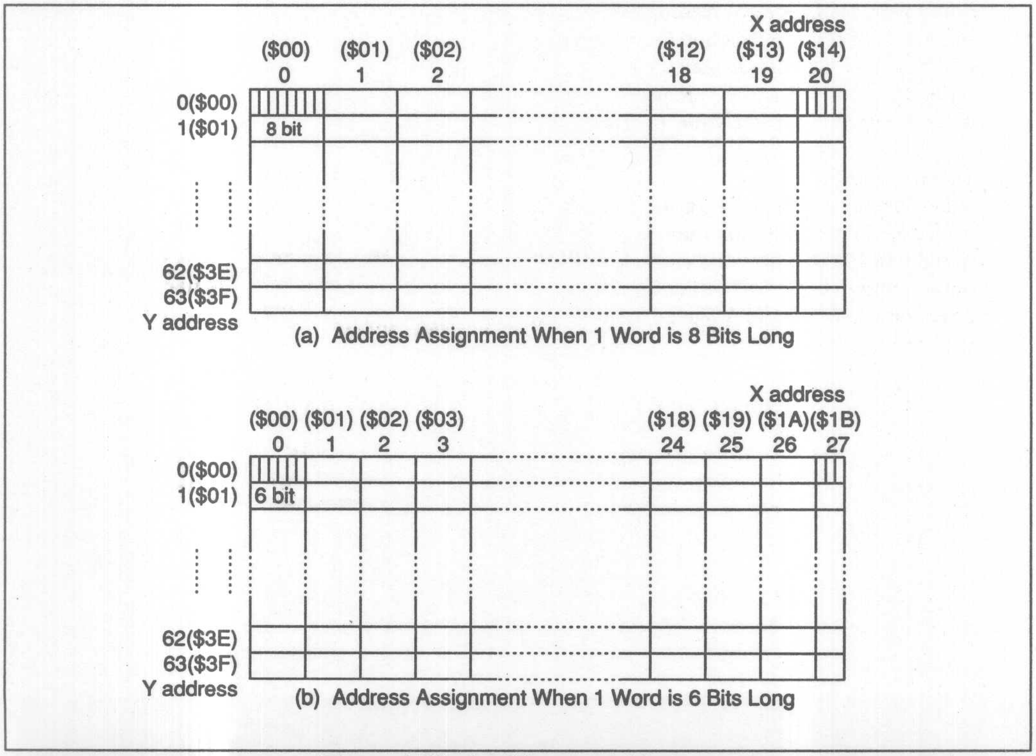


Figure 5 Display Memory Addresses

3. Display Data Write

3.1 Display Memory and Data Register Accesses

(1) Access

Figure 6 shows the relationship between the address register (AR) and internal registers and display memory in the HD66108T. Display memory shall be referred to as a data register since it can be handled as other registers.

To access a data register, the register address assigned to the desired register must be written into the address register's Register No.bits. The MPU will access only that register until the register address is updated.

(2) Busy Check

A busy time period appears after display memory read/write or X or Y address register write, since post-access processing is performed synchronously with internal clock pulses. Updating data in registers other than the address register is disabled during this time. Subsequent data must be input after confirming ready mode by reading the address register. The busy time period is a maximum of 8 clock pulses after display memory read/write and a maximum of 1.5 clock pulses after X or Y address register write (figure 7).

(3) Dummy Read

When reading out display data, the data which is read out immediately after setting the X and Y addresses is invalid. Valid data can be read out after one dummy read, which is performed after setting the X and Y addresses desired (figure 8).

(4) Limitations on Access

As shown in figure 9, the display memory must not be rewritten until a time period of t_{CL1} or longer has elapsed after rewriting the control register's DUTY bits or the mode register's FFS bits. However, display memory and registers other than the control register and mode register can be accessed even during this time period. t_{CL1} can be obtained from the following equation. If using an LSI with a frame frequency of 60 Hz or greater, a time period of 1 ms should be sufficient.

$$t_{CL1} = \frac{D2}{Ni \cdot f_{CLK}\ (\mathrm{kHz})} \quad (\mathrm{ms}) \quad \ldots \quad \text{Equation 1}$$

D2 (duty correction value 2) :
192 (duty = 1/32, 1/34, or 1/36)
128 (duty = 1/48 or 1/50)
96 (duty = 1/64 or 1/66)

Ni (frequency-division ratio specified by the mode register's FFS bits)
: 2, 1, 1/2, 1/3, 1/4, 1/6, or 1/8

f_{CLK} : Input clock frequency (kHz)

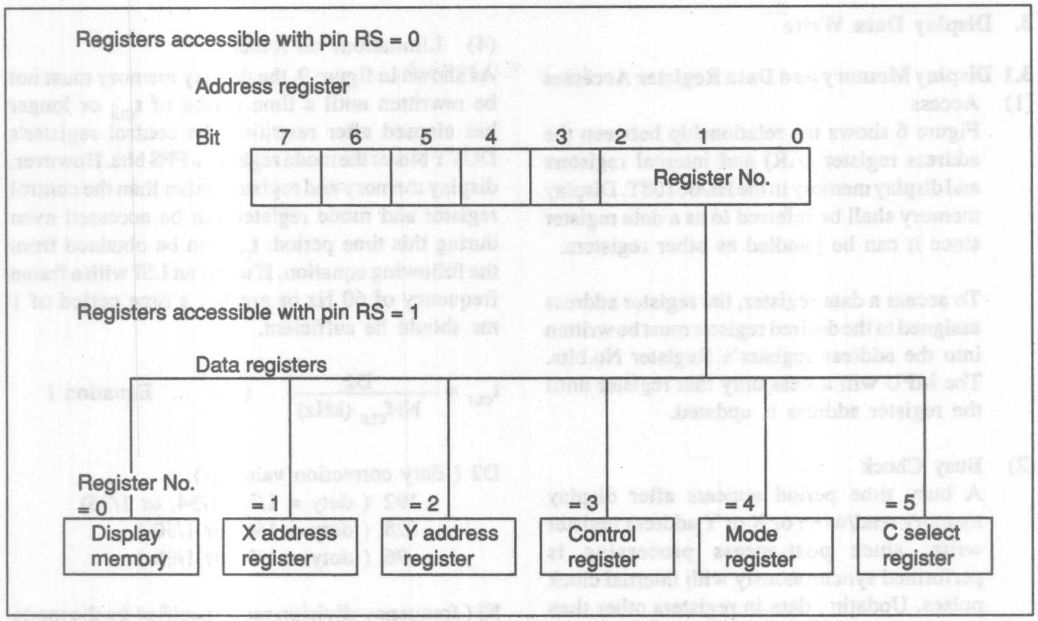


Figure 6 Relationship between Address Register and Register No.

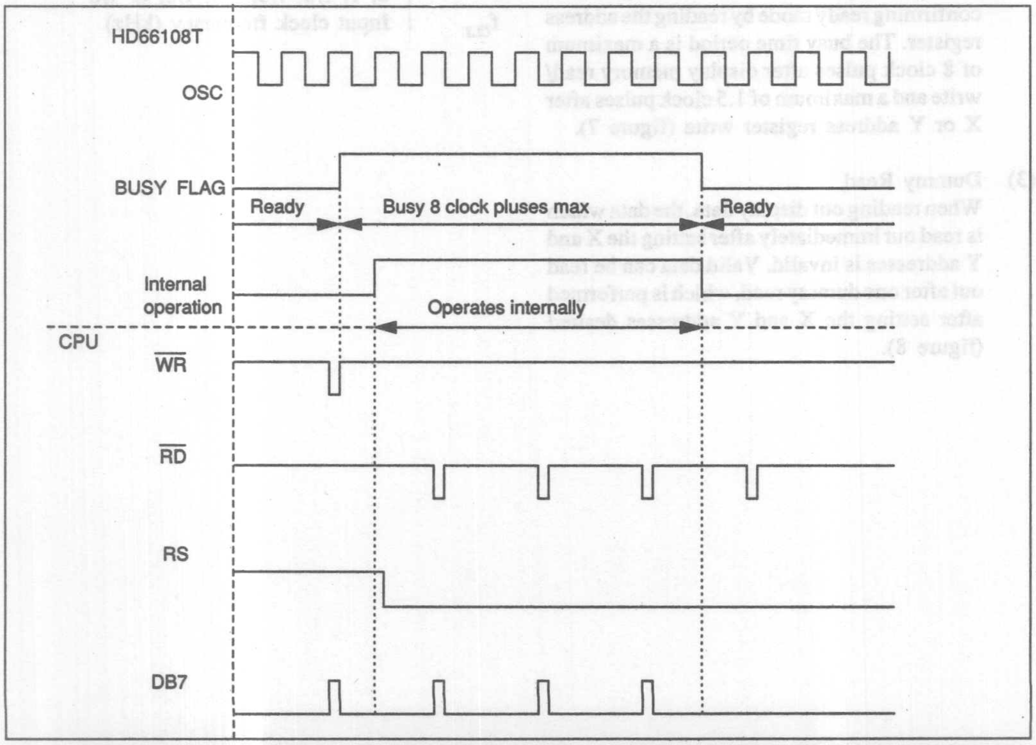


Figure 7 Relationship between Clock Pulses and Busy Time (Updating Display Data)

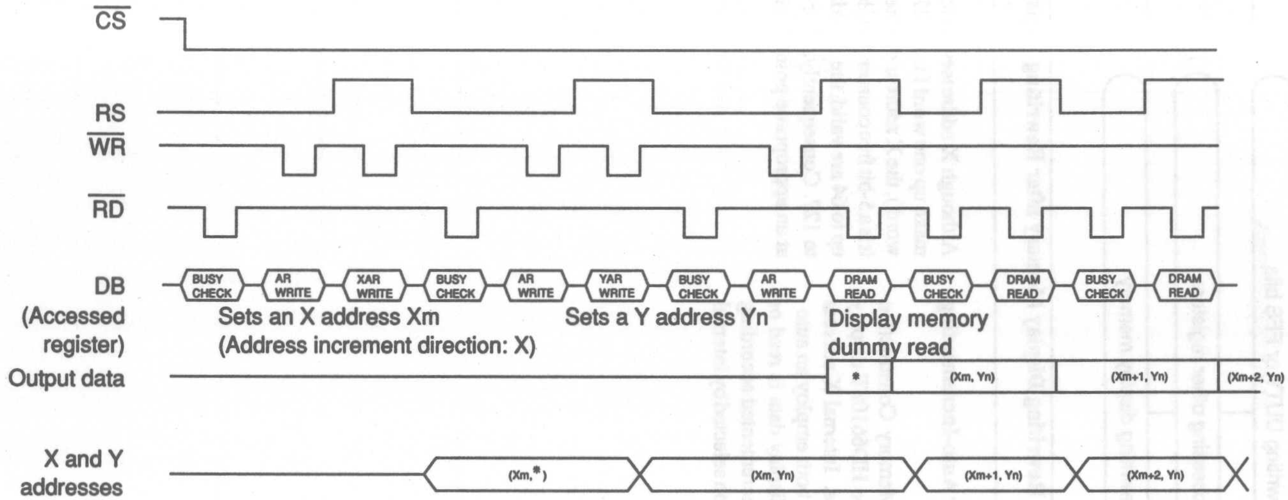


Figure 8 Display Memory Reading

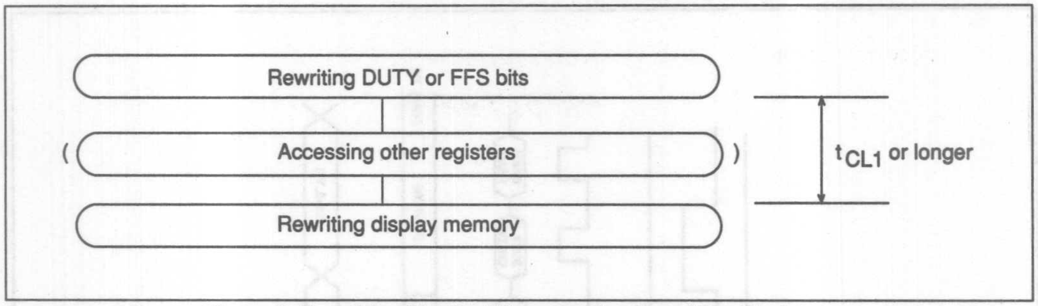
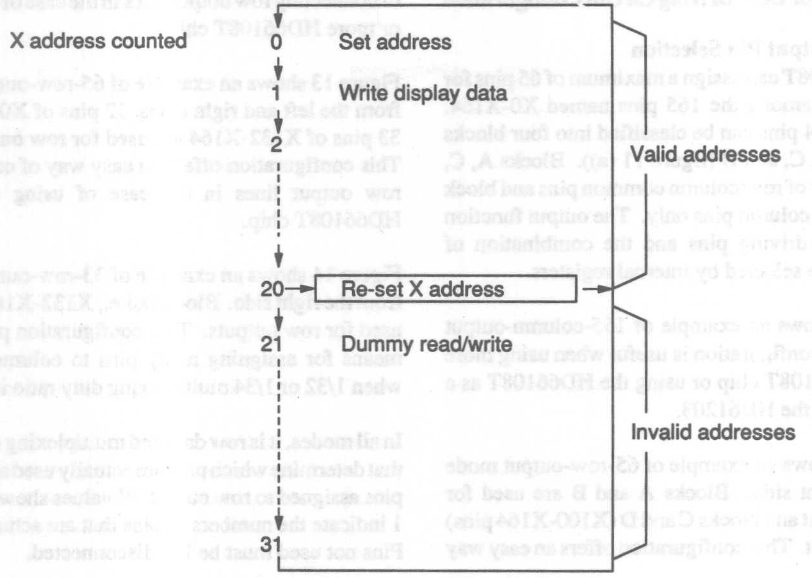


Figure 9 Rewriting Display Memory after Rewriting Registers

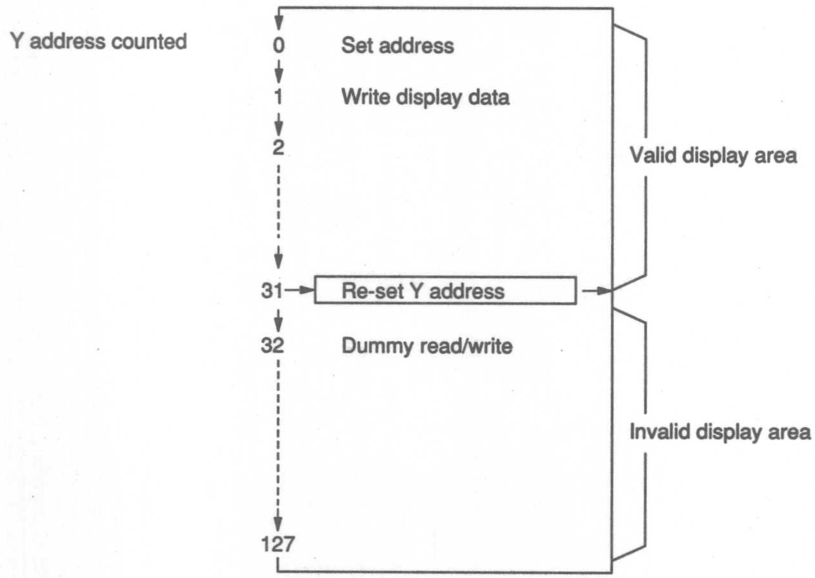
3.2 X and Y Address Counter Auto-Incrementing Function

As described in "2. Display Memory Construction and Word Length Setting, " the HD66108T display memory has X and Y addresses. Internal X address counter and Y address counter both employ an auto-incrementing function. After display data is read or written, the X or Y address is incremented according to the address increment direction selected by internal register.

Although X addresses up to 20 are valid when 8 bits make up one word (up to 27 when 6 bits make up one word), the X address counter can count up to 31 since it is a 5-bit free counter. Similarly, although Y addresses up to 64 are valid, the Y address counter can count up to 127. Consequently, X or Y address must be re-set at an appropriate point as shown in figure 10.



(1) Example of X Address Counter Increment
(Word Length: 8 bits)



(2) Example of Y Address Counter Increment
(Multiplexing duty ratio: 1/32)

Figure 10 X/Y Address Counter Increment

4. Selection for LCD Driving Circuit Configuration

4.1 Row Output Pin Selection

The HD 66108T can assign a maximum of 65 pins for row outputs among the 165 pins named X0-X164. The X0-X164 pins can be classified into four blocks labeled A, B, C, and D (figure 11 (a)). Blocks A, C, and D consist of row/column common pins and block B consists of column pins only. The output function of the LCD driving pins and the combination of blocks can be selected by internal registers.

Figure 11 shows an example of 165-column-output mode. This configuration is useful when using more than 1 HD66108T chip or using the HD66108T as a slave chip of the HD61203.

Figure 12 shows an example of 65-row-output mode from the right side. Blocks A and B are used for column output and blocks C and D (X100-X164 pins) for row output. This configuration offers an easy way of connecting row output lines in the case of using one or more HD66108T chips.

Figure 13 shows an example of 65-row-output mode from the left and right sides. 32 pins of X0-X31 and 33 pins of X132-X164 are used for row output here. This configuration offers an easy way of connecting row output lines in the case of using only one HD66108T chip.

Figure 14 shows an example of 33-row-output mode from the right side. Block D, i.e., X132-X164 pins, is used for row outputs. This configuration provides a means for assigning many pins to column outputs when 1/32 or 1/34 multiplexing duty ratio is desired.

In all modes, it is row data and multiplexing duty ratio that determine which pins are actually used among the pins assigned to row output. Y values shown in table 1 indicate the numbers of pins that are actually used. Pins not used must be left disconnected.

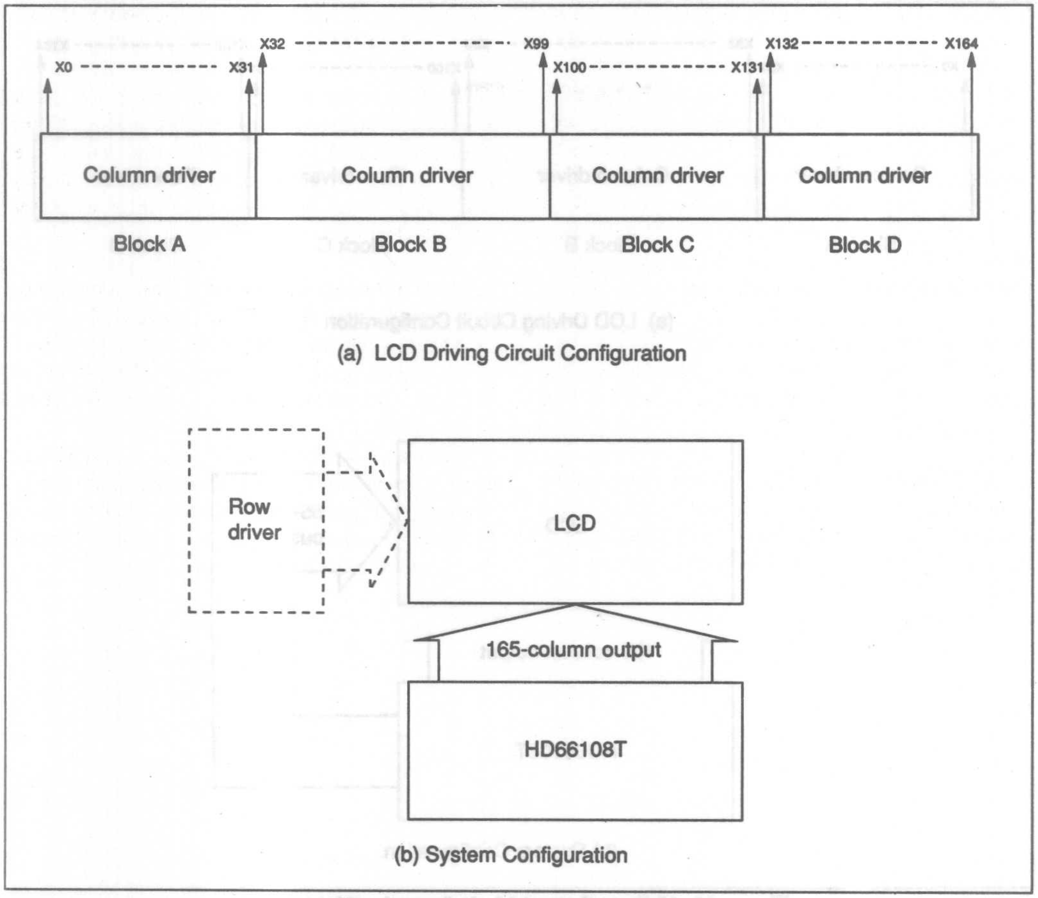


Figure 11 165-Column-Output Mode

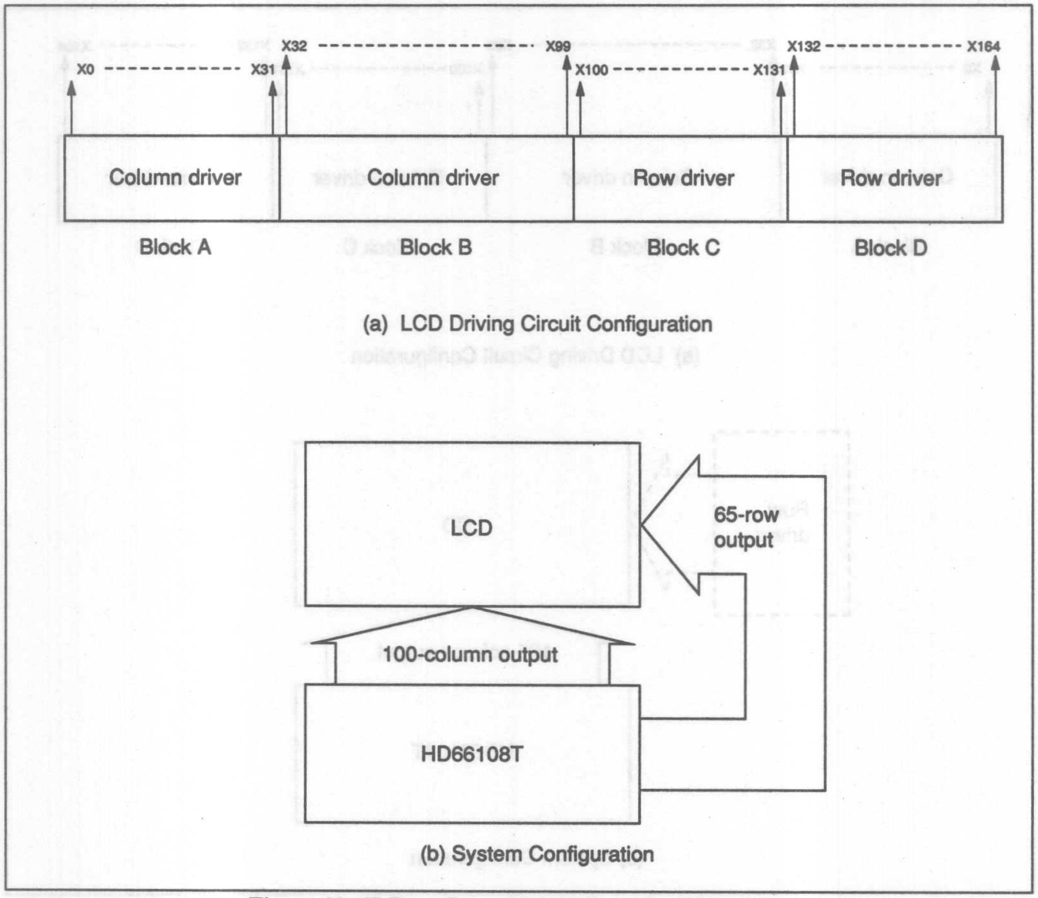


Figure 12 65-Row-Output Mode from the Right Side

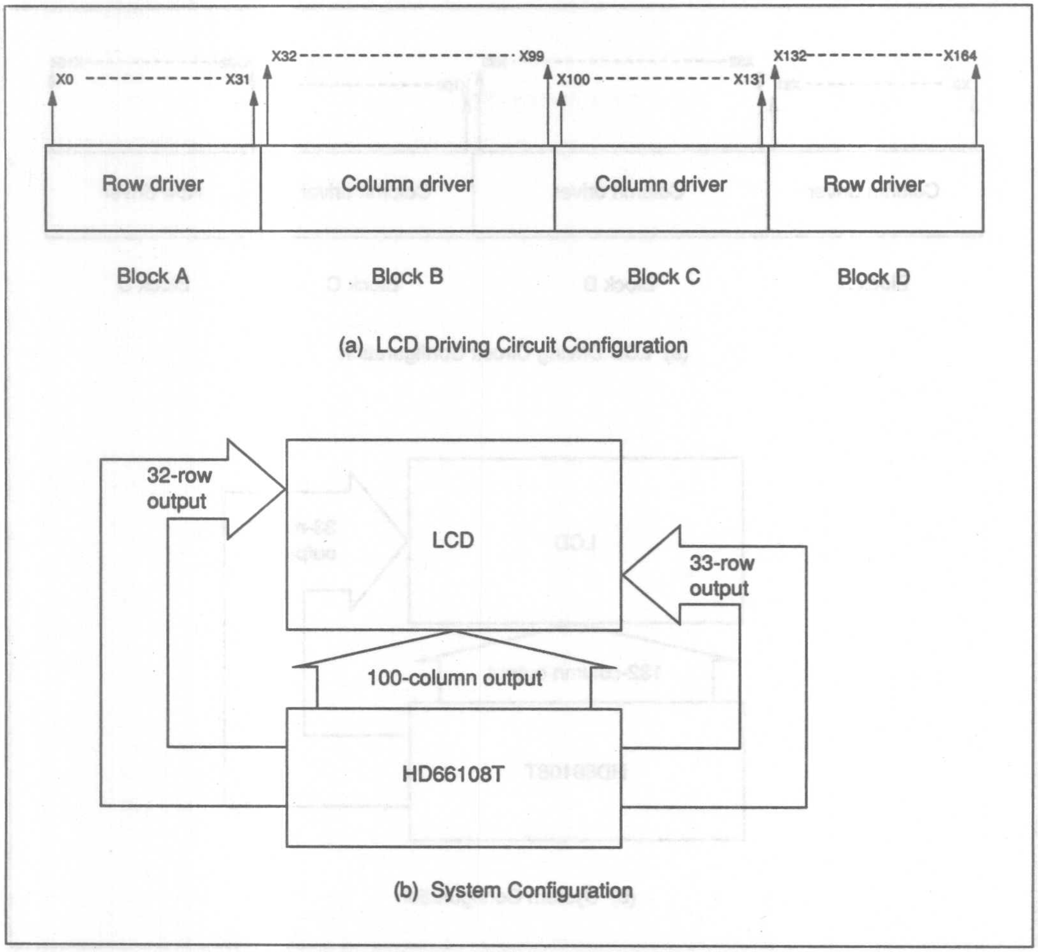


Figure 13 65-Row-Output Mode from the Left and Right Sides

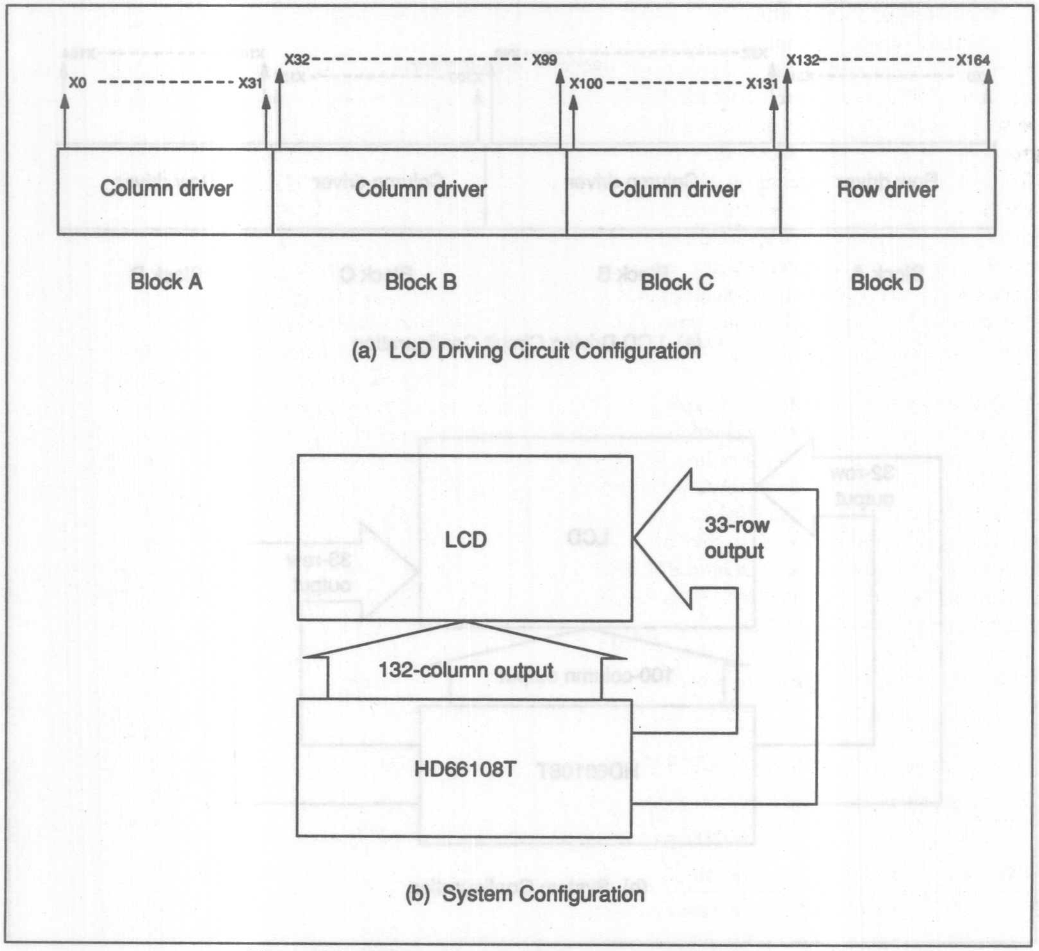


Figure 14 33-Row-Output-Mode from the Right Side

4.2 Row Output Data Setting

If certain LCD driving output pins are assigned to row output, data must be written to display memory for row output. The specific area to which this data must be written depends on the row-output mode and the procedure of writing row data to the display memory (0 or 1 to which bits?) depends on which X pin drives which line of the LCD. Row data area is determined by the control register's (FCR) ROS and DUTY bits and is identical to the protected area, which will be described below. (165-column-output mode has no protected area, thus requiring no row data to be written (figure 15).)

Procedure of writing row data to the display memory is as follows. First, 1 must be written to the bit at the intersection between line Yj and line (column) Xi (column). Line Yj is filled with data to be displayed on the first line of the LCD and line Xi is connected to pin Xn, which drives the first line of the LCD. Following this, 0s must be written to the remaining bits on line Yj in the row data area. This rule applies to subsequent lines on the LCD.

Table 2 shows the relationship between FCR settings and protected areas.

Figure 16 shows the relationship between row data and display. Here the mode is 65-row output from the right side. Display data on Y0 is displayed on the first line of the LCD and data on Y64 is displayed on the 65th line of the LCD. If X164 is connected to the first line of the LCD and X100 is connected to the 65th line of the LCD, 1s must be written to the bits on the diagonal line between coordinates (X164, Y0) and (X100, Y64) and 0s to the remaining bits. Row data protect function must be turned off before writing row data and be turned on after writing row data. Turning on the row data protect function disables read/write of display memory area corresponding to the row output pins, i.e., prevents row data from being destroyed. In figure 16, display memory area corresponding to pins X100 to X164 is protected.

Figures 17 to 19 show examples of row data settings. Some multiplexing duty ratios result in invalid display areas. Although an invalid display area can be read from or written to, it will not be displayed.

Table 2 Relationship between FCR Settings and Protected Areas

Control Register (FCR)					
	ROS			LCD Driving Signal Output Pins Connected to	
PON	4	3	Mode	Protected Area of Display Memory	Figures
1	0	0	165-column	No area protected	15
1	0	1	65-row (R)	X100-X164	16, 19
1	1	0	65-row (L/R)	X0-X31 and X132-X164	17
1	1	1	33-row (R)	X132-X164	18

65-row (R) : 65-row-output mode from the right side
65-row (L/R) : 65-row-output mode from the left and right sides
33-row (R) : 33-row-output mode from the right side

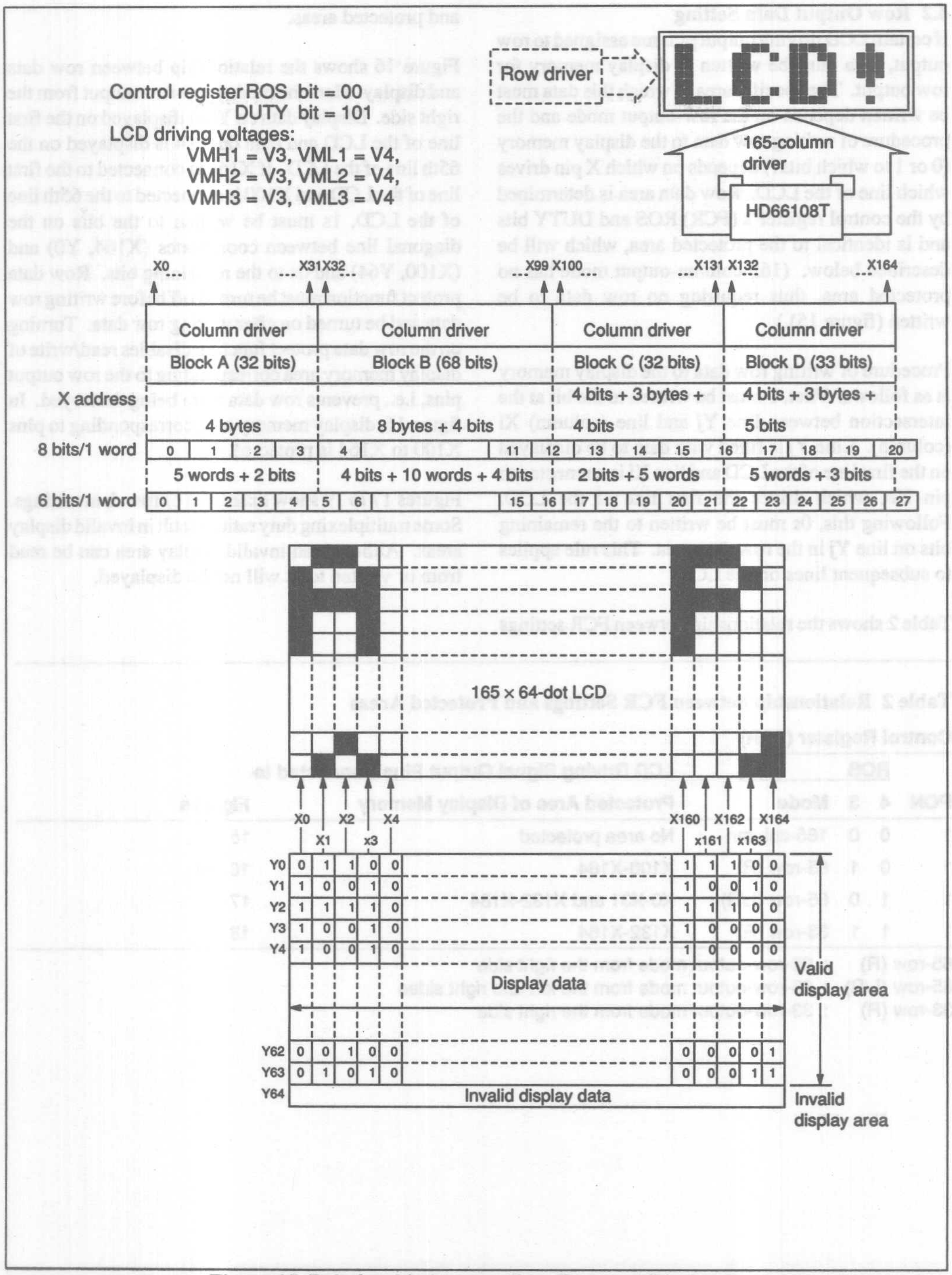


Figure 15 Relationship between Row Data and Display (165-Column Output, 1/64 Multiplexing Duty Ratio)

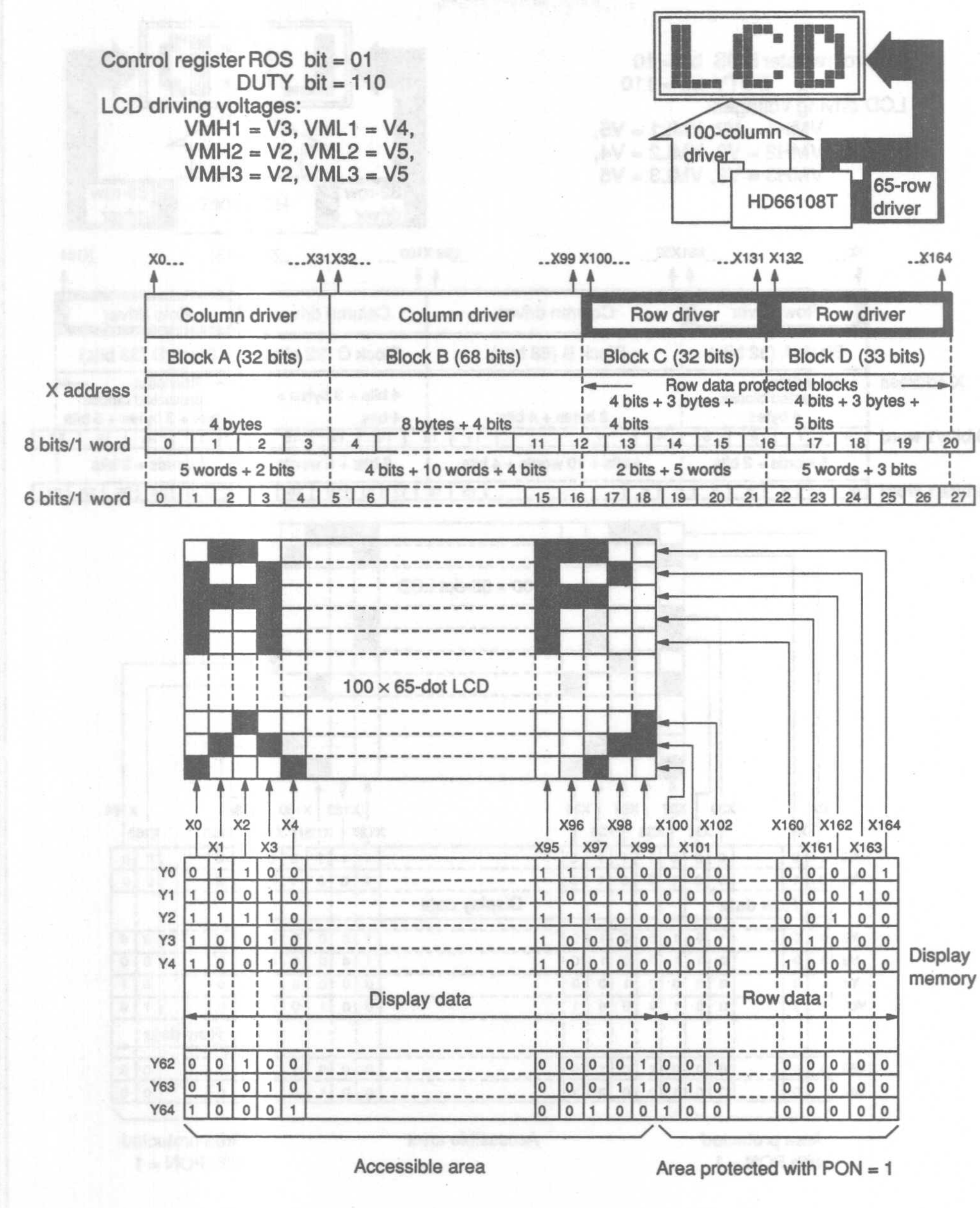


Figure 16 Relationship between Row Data and Display (65-Row Output from the Right Side, 1/66 Multiplexing Duty Ratio)

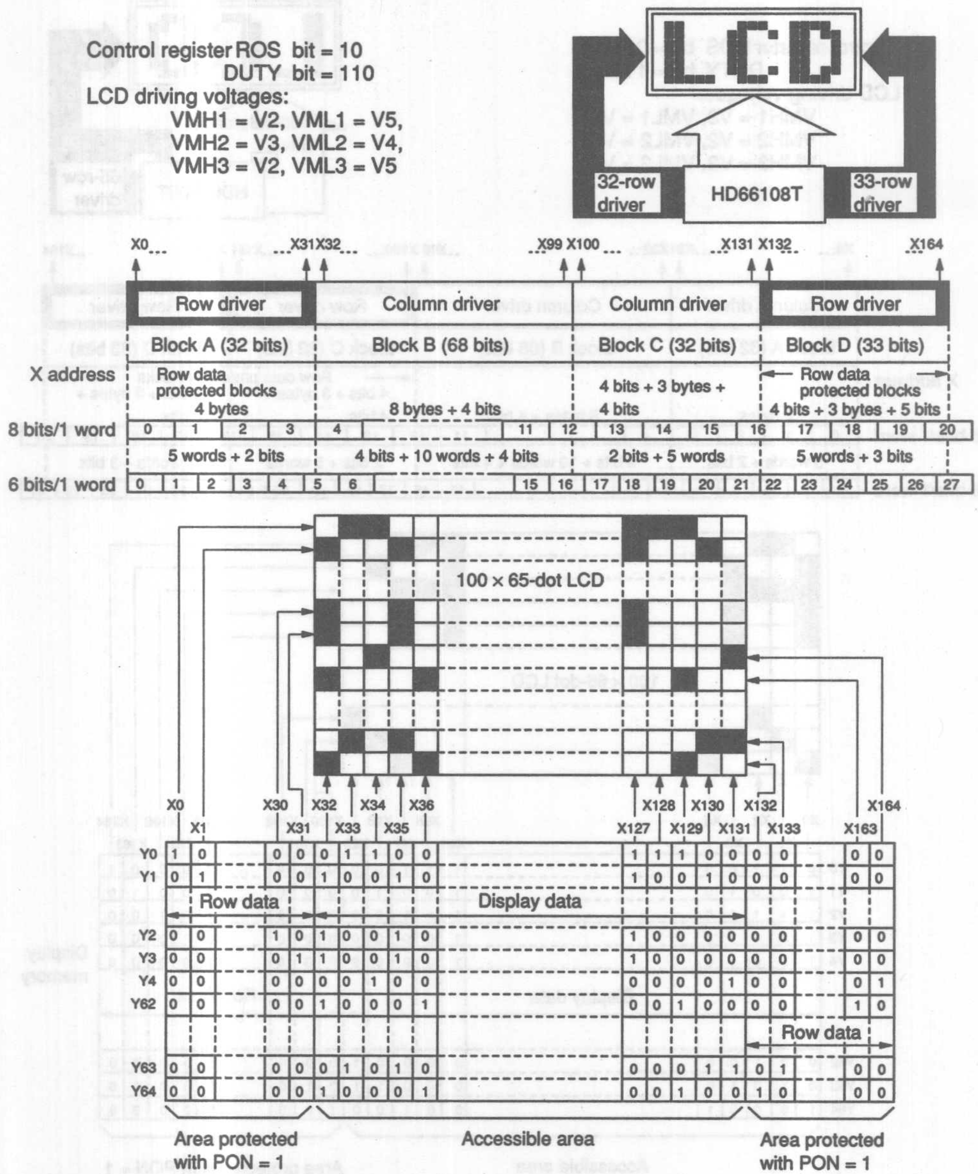


Figure 17 Relationship between Row Data and Display (65-Row Output from the Left and Right Sides, 1/66 Multiplexing Duty Ratio)

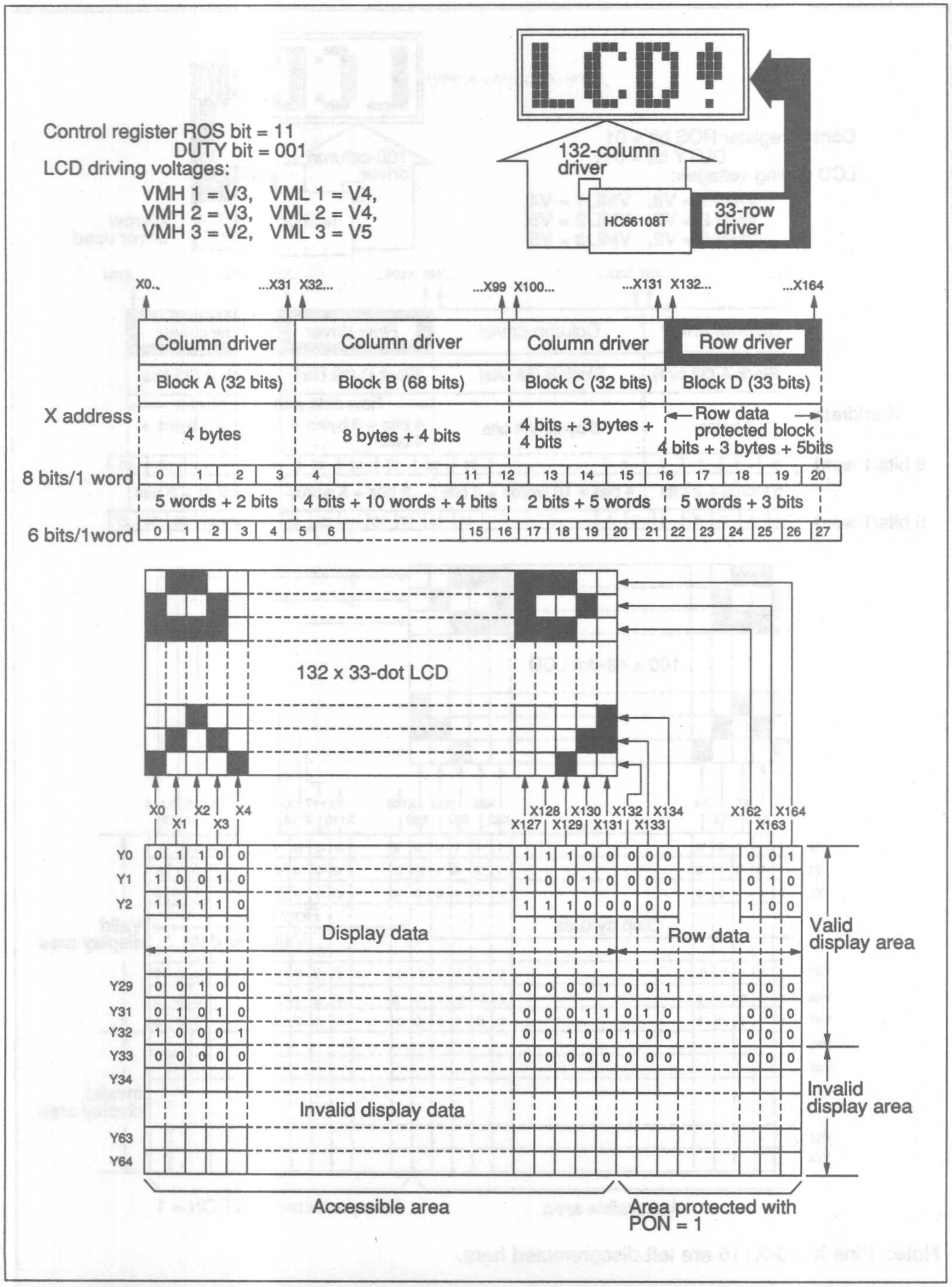


Figure 18 Relationship between Row Data and Display (33-Row Output from the Right Side, 1/34 Multiplexing Duty Ratio)

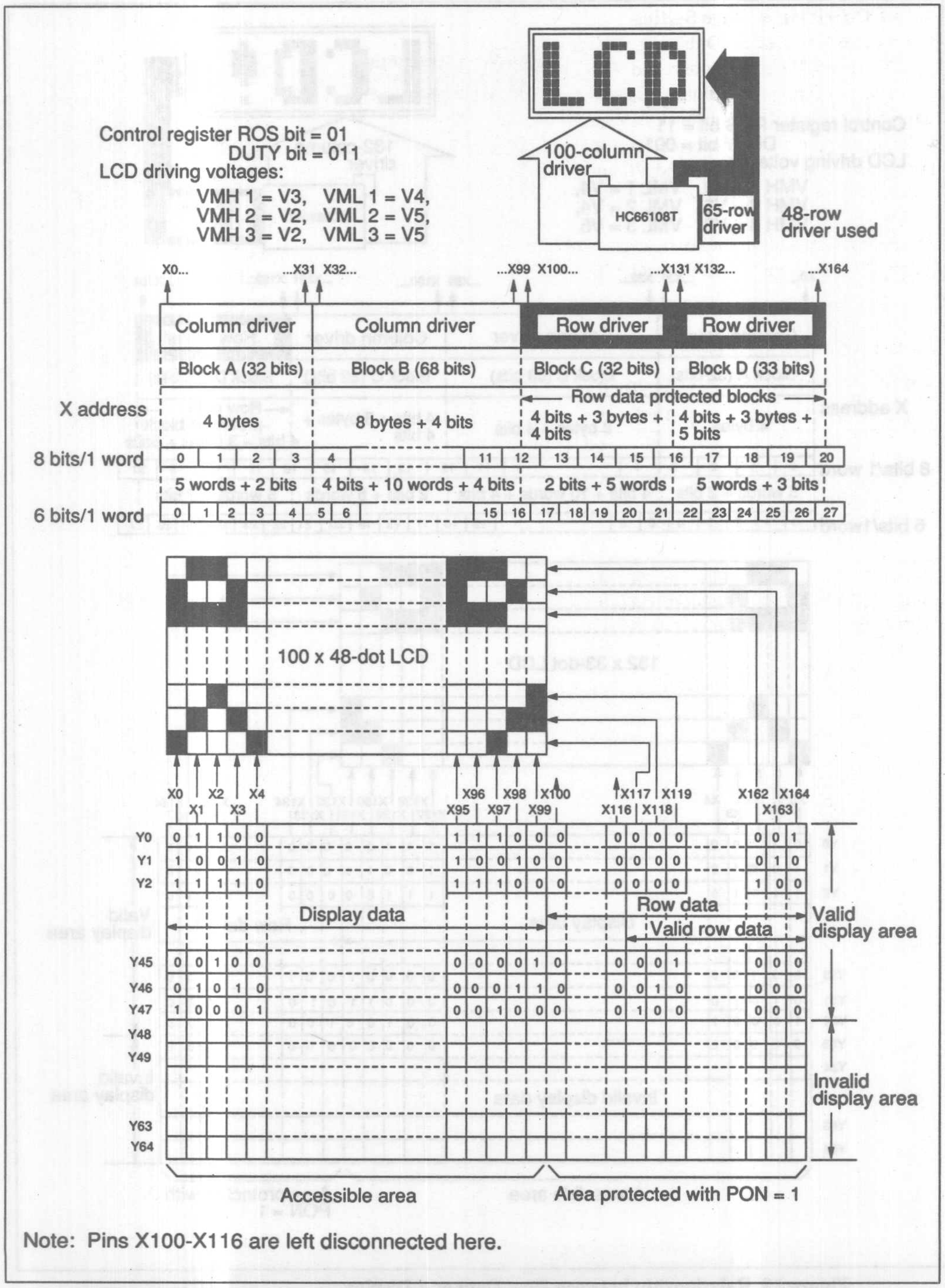


Figure 19 Relationship between Row Data and Display (65-Row Output from the Right Side, 1/48 Multiplexing Duty Ratio)

4.3 LCD Driving Voltage Setting

There are 6 levels of LCD driving voltages ranging from V1 to V6; V1 is the highest and V6 is the lowest. As shown in figure 20, column output waveform is made up of a combination of V1, V3, V4, and V6 while row output waveform is made up of V1, V2, V5, and V6. This means that V1 and V6 are common to both waveforms while mid-voltages are different.

To accommodate this situation, each block of the HD66108T is provided with power supply pins for mid-voltages as shown in figure 21. Each pair of V1R and V1L and V6R and V6L are internally connected and must be applied the same level of voltage. Block B is fixed for column output and must be applied V3 and V4 as mid-voltages. The other blocks must be applied different levels of voltages according to the function of their LCD driving output pins; if the LCD driving output pins are set for row output, VMHn and VMLn must be applied V2 and V5, respectively, while they must be applied V3 and V4, respectively, if the pins are set for column output (n = 1 to 3).

Table 3 Relationship between FCR settings and LCD Driving Voltages

Control Register (FCR)			LCD Driving Voltage Pins									
ROS4	**ROS3**	**Mode**	**VIR/VIL**	**V3**	**V4**	**VMH1**	**VML1**	**VMH2**	**VML2**	**VMH3**	**VML3**	**V6R/V6L**
0	0	165-column	V1	V3	V4	V3	V4	V3	V4	V3	V4	V6
0	1	65-row (R)	V1	V3	V4	V3	V4	V2	V5	V2	V5	V6
1	0	65-row (L/R)	V1	V3	V4	V2	V5	V3	V4	V2	V5	V6
1	1	33-row (R)	V1	V3	V4	V3	V4	V3	V4	V2	V5	V6

65-row (R) : 65-row-output mode from the right side
65-row (L/R) : 65-row-output mode from the left and right sides
33-row (R) : 33-row-output mode from the right side

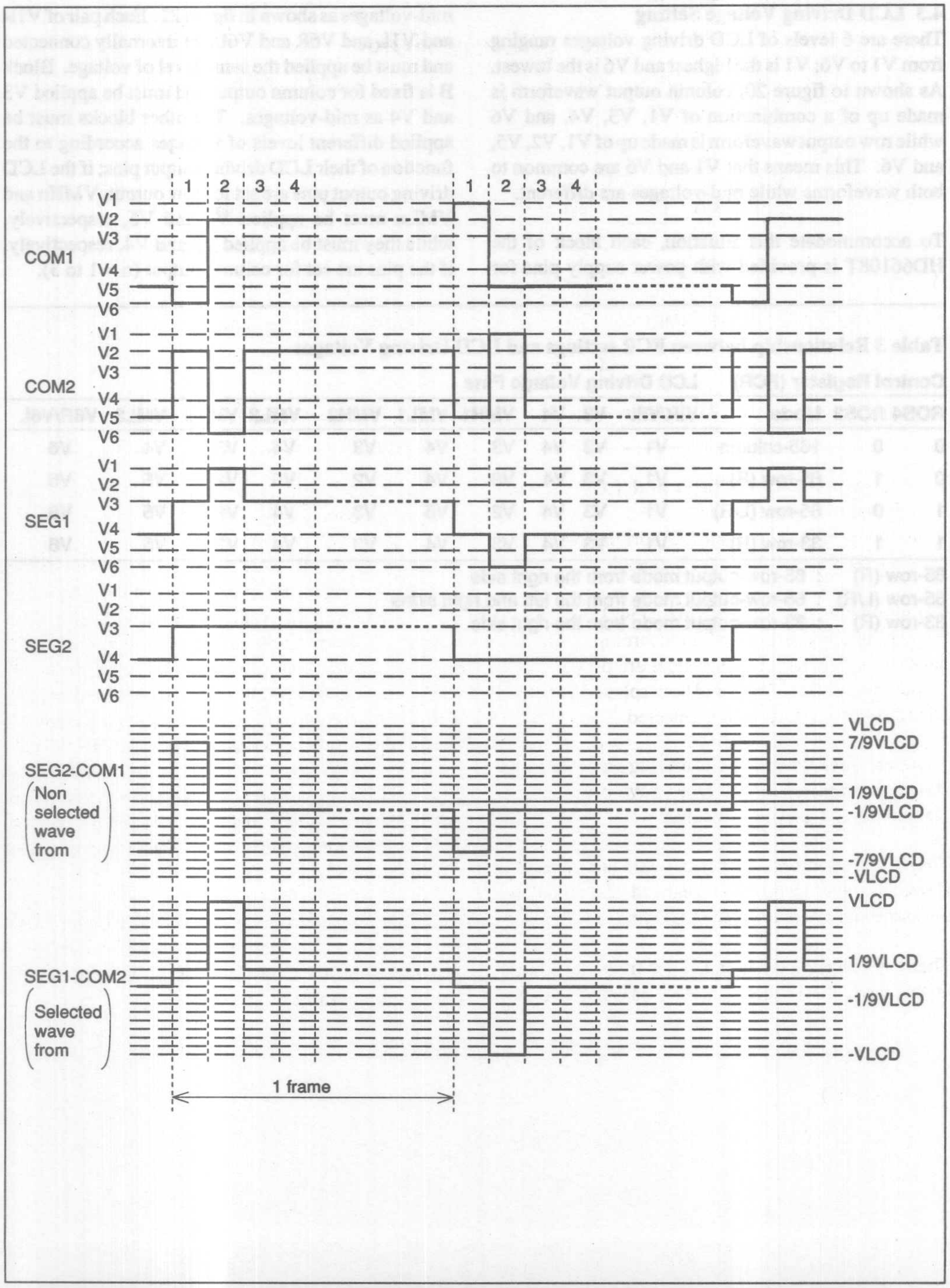


Figure 20 LCD Driving Voltage Waveforms

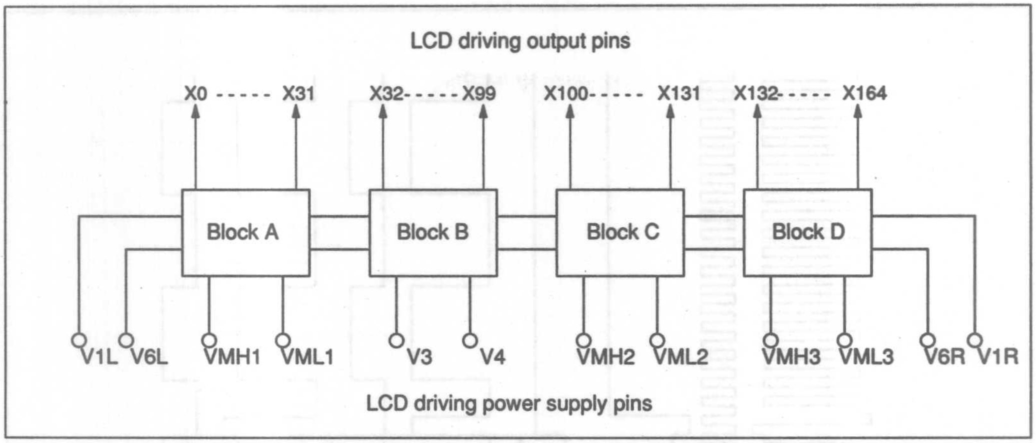


Figure 21 Relationship between Blocks and LCD Driving Voltages

5. Multiplexing Duty Ratio and LCD Driving Waveform Settings

A multiplexing duty ratio and LCD driving waveform can be selected via internal registers.

A multiplexing duty ratio of 1/32, 1/34, 1/36, 1/48, 1/50, 1/64, or 1/66 can be selected according to the LCD panel used. However, since there are only 65 row-output pins, only 65 lines will be displayed even if 1/66 multiplexing duty ratio is selected.

There are three types of LCD driving waveforms, as shown in figure 22: A-type waveform, B-type waveform, and C-type waveform.

The A-type waveform is called per-half-line inversion. Here, the waveforms of M signal and CL1 signal are the same and alternate every LCD line.

The B-type waveform is called per-frame inversion; in this case, the M signal inverts its polarity every frame so as to alternate every two LCD frames. This is the most common type.

The C-type waveform is called per-n-line inversion and inverts its polarity every n lines (n can be set as needed within 1 to 31 via the internal registers). The C-type waveform combines the advantages of the A- and B-types of waveforms. However, some lines will not be alternated depending on the multiplexing duty ratio and n. To avoid this, another C-type waveform is available which is generated from the EOR of the C-type waveform M signal mentioned above and the B-type waveform M signal. Since the relationship between n and display quality usually depends on the LCD panel, n must be determined by observing actual display results.

The B-type waveform should be used if the LCD panel specifies no particular type of waveform. However, in some cases, the C-type waveform may create a better display.

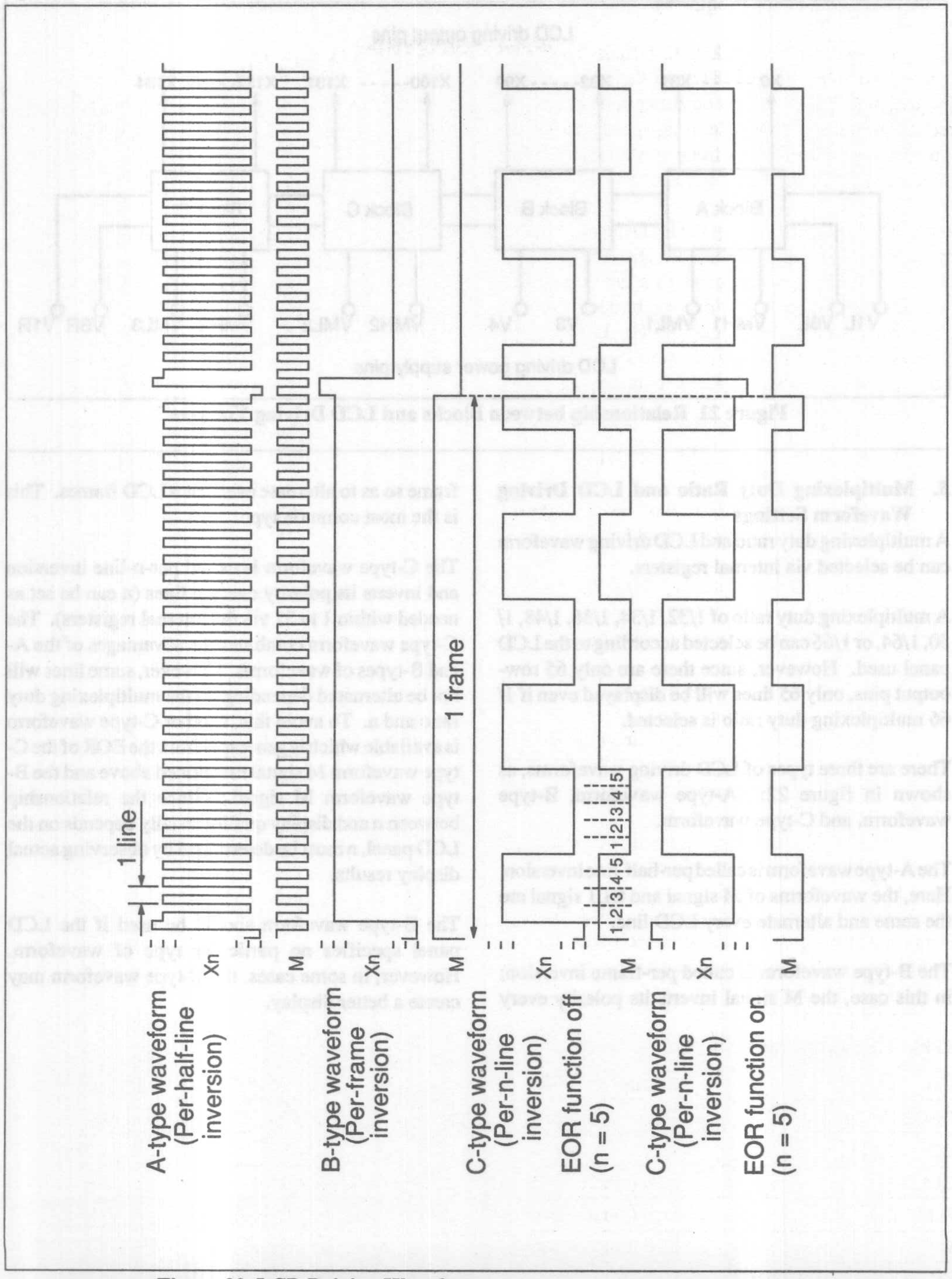


Figure 22 LCD Driving Waveforms (Row Output with a 1/32 Multiplexing Duty Ratio)

6. Clock and Frame Frequency

An input clock with a 200-kHz to 4-MHz frequency can be used for the HD66108T. Note that raising clock frequency increases current consumption although it reduces busy time and enables high-speed operations. An optimum system clock frequency should thus be selected within 200 kHz to 4 MHz.

The clock frequency driving the LCD panel (= frame frequency) is usually 70 Hz to 90 Hz. Accordingly, the HD66108T is so designed that the frequency-division ratio of the input clock can be selected. The HD66108T generates around 80-Hz LCD frame frequency if the frequency-division ratio is 1. The frequency-division ratio can be obtained from the following equation.

$$Ni = \frac{f_F}{f_{CLK}} \times \frac{500}{80} \times D1$$

Ni : Frequency-division ratio
f_F : Frame frequency required for the LCD panel (Hz)
f_{CLK} : Input clock frequency (kHz)
D1 : Duty correction value 1
D1 = 1 when multiplexing duty ratio is 1/32, 1/48 or 1/64
D1 = 32/34 when multiplexing duty ratio is 1/34
D1 = 32/36 when multiplexing duty ratio is 1/36
D1 = 48/50 when multiplexing duty ratio is 1/50
D1 = 64/66 when multiplexing duty ratio is 1/66

The frequency-division ratio nearest the value obtained from the above equation must be selected; selectable frequency-division ratios by internal registers are 2, 1, 1/2, 1/3, 1/4, 1/6, and 1/8.

7. Display Off function

The HD66108T has a display off function which turns off display by rewriting the contents of the internal register. This prevents random display at power-on until display memory is initialized.

8. Standby Function

The HD66108T has a standby function provinding low-power dissipation. Writing a 1 to bit 6 of the address register starts up the standby function.

The LCD driving voltages, ranking from V1 to V6, must be set to V_{CC} to prevent DC voltage from beging applied to an LCD panel during standby state.

The HD66108T operates as follows in standby mode.

(1) Stops oscillation and external clock input
(2) Resets all registers to 0's except the STBY bit

Here, note that the display memory will not preserve data if the standby function is turned on; the display memory as well as registers must be set again after the standby function is terminated.

Table 4 shows the standby status of pins and table 5 shows the status of registers after standby function termination.

Writing a 0 to bit 6 of the address register terminates the standby function. Writing values into the DISP and Register No. bits at this time is ignored; these bits need to be set after the standby function has been completely terminated.

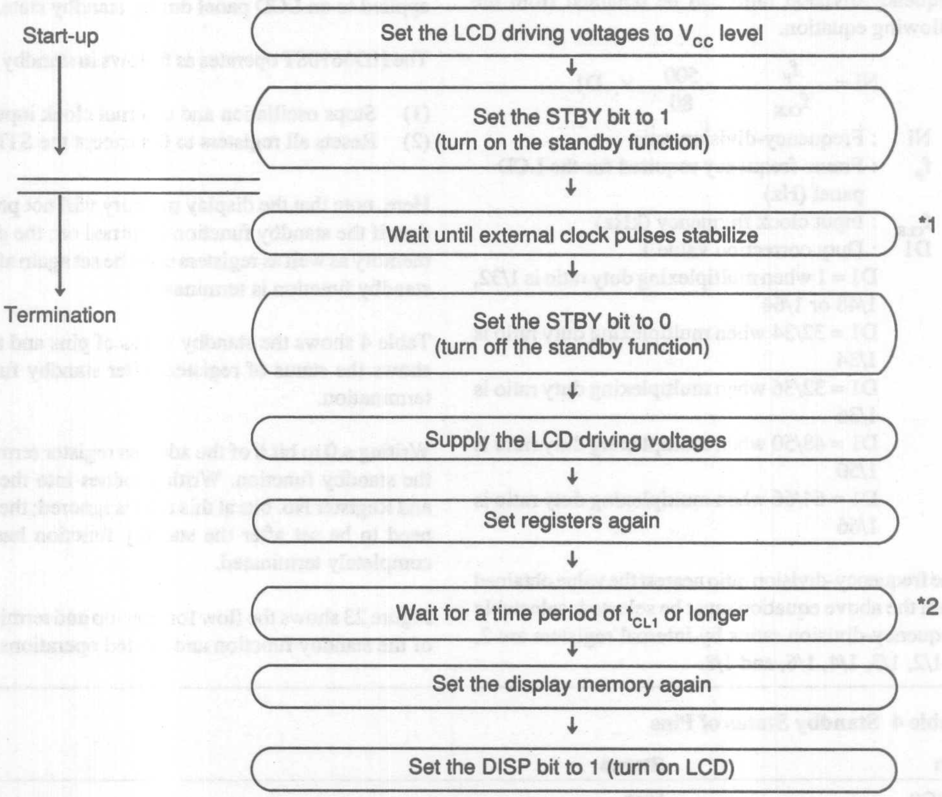
Figure 23 shows the flow for start-up and termination of the standby function and related operations.

Table 4 Standby Status of Pins

Pin	Status
OSC2	High
CO	Low
CL1	Low (master chip) or high-impedance (slave chip)
FLM	Low (master chip) or high-impedance (slave chip)
M	Low (master chip) or high-impedance (slave chip)
Xn (column output pins)	V4
Xn' (row output pins)	V5

Table 5 Register Status after Standby Function Termination

Register Name	Status after Standby Function Termination
Address register	Reset to 0's except for the STBY bit
X address register	Reset to 0's
Y address register	Reset to 0's
Control register	Reset to 0's
Mode register	Reset to 0's
C select register	Reset to 0's
Display memory	Data not preserved



Notes: 1. Not necessary in the case of using internal oscillation
2. Refer to equation 1 (section 3.1).

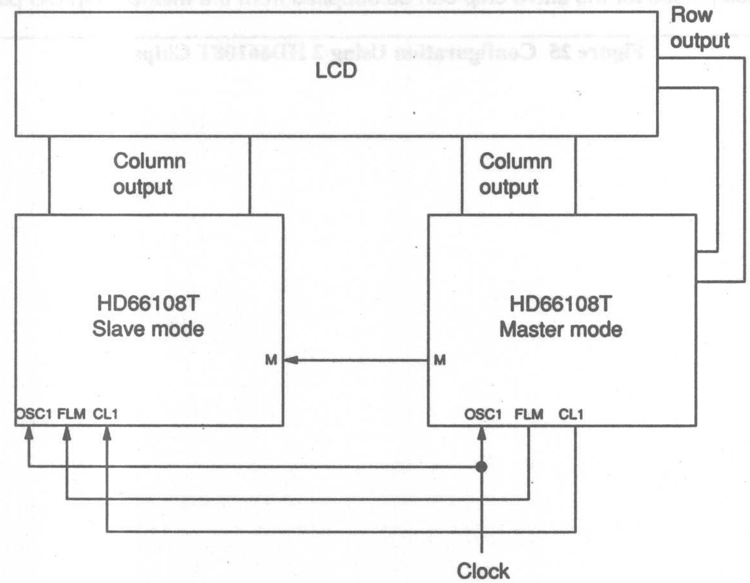
Figure 23 Start-Up and Termination of Standby Function and Related Operations

9. Multi-Chip Operation

Using multiple HD66108T chips (= multi-chip operation) provides the means for extending the number of disply dots. Note the following items when using the multi-chip operation.

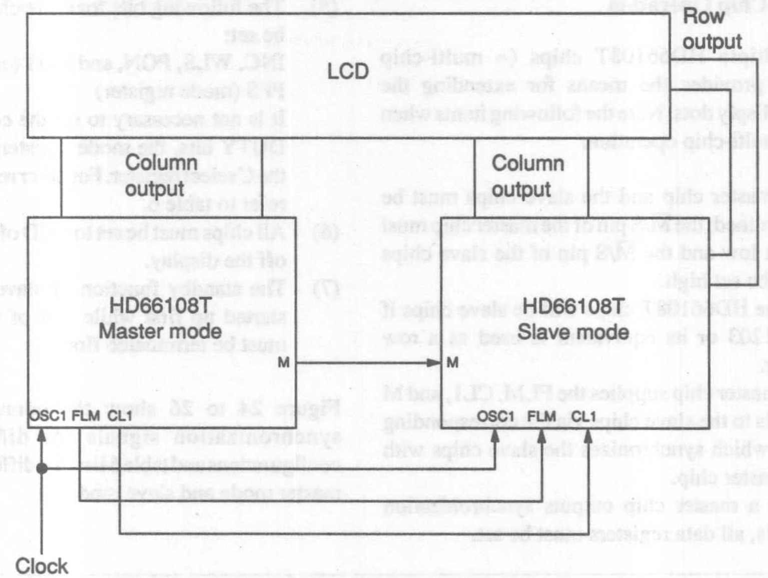
(1) The master chip and the slave chips must be determined; the $\overline{M}$/S pin of the master chip must be set low and the $\overline{M}$/S pin of the slave chips must be set high.
(2) All the HD66108T chips will be slave chips if HD61203 or its equivalent is used as a row driver.
(3) The master chip supplies the FLM, CL1, and M signals to the slave chips via the corresponding pins, which synchronizes the slave chips with the master chip.
(4) Since a master chip outputs synchronization signals, all data registers must be set.
(5) The following bits for slave chips must always be set:
INC, WLS, PON, and ROS (control register)
FFS (mode register)
It is not necessary to set the control register's DUTY bits, the mode register's DWS bits, or the C select register. For other registers' settings, refer to table 6.
(6) All chips must be set to LCD off in order to turn off the display.
(7) The standby function of slave chips must be started up first while that of the master chip must be terminated first.

Figure 24 to 26 show the connections of the synchronization signals for different system configurations and table 6 lists the differences between master mode and slave mode.



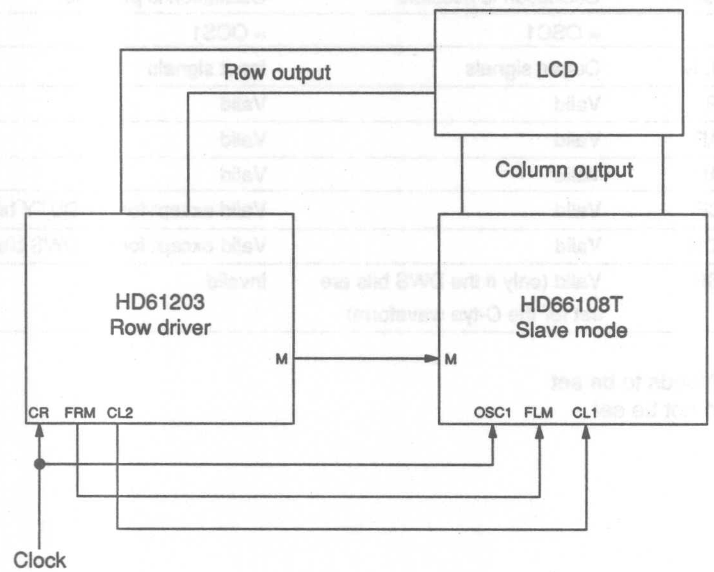
Note: Clock pulses for the slave chip can be supplied from the master chip CO pin.

Figure 24 Configuration Using 2 HD66108T Chips (1)



Note: Clock pulses for the slave chip can be supplied from the master chip CO pin.

Figure 25 Configuration Using 2 HD66108T Chips (2)



Note: 1. The slave chip can oscillate CR clock pulses. In this case, the clock pulses must be supplied to the HD61203 from the HD66108T's CO pin.
2. The HD61203's control pins must be set in accordance with the type of RAMs.

Figure 26 Configuration Using 1 HD66108T Chip with Another Row Driver (HD61203)

Table 6 Comparison between Master and Slave Mode

Item		Master Mode	Slave Mode
Pin:	$\overline{M}$/S	Must be set low	Must be set high
	OSC1, OSC2	Oscillation is possible	Oscillation is possible
	CO	= OSC1	= OCS1
	FLM, CL1, M	Output signals	Input signals
Register:	AR	Valid	Valid
	XAR	Valid	Valid
	YAR	Valid	Valid
	FCR	Valid	Valid except for the DUTY bits
	MDR	Valid	Valid except for the DWS bits
	CSR	Valid (only if the DWS bits are set for the C-tye waveform)	Invalid

Notes
- Valid : Needs to be set
- Invaid: Need not be set

Internal Registers

All HD66108T's registers can be read from and written into. However, the BUSY FLAG and invalid bits cannot be written to and reading invalid bits or registers returns 0's.

1. Address Register (AR) (Accessed with RS = 0)

This register (figure 27) contains Register No. bits, BUSY FLAG bit, STBY bit, and DISP bit. Register No. bits select one of the data registers according to the register number written. The BUSY FLAG bit indicates the internal operation state if read. The STBY bit activates the standby function. The DISP bit turns the display on or off. This register is selected when RS pin is 0.

Bits D4 and D3 are invalid.

D7	D6	D5	D4	D3	D2	D1	D0
BUSY FLAG	STBY	DISP	—		Register No.		

(1) STBY
- 1: Standby function on
- 0: Normal (standby function off)

* When standby function is on, all registers are reset to 0's

(2) DISP
- 1: LCD on
- 0: LCD off

(3) Register No.

No.	Bit 2	1	0	Register
0	0	0	0	Display memory
1	0	0	1	X address register
2	0	1	0	Y address register
3	0	1	1	Control register
4	1	0	0	Mode register
5	1	0	1	C select register

(4) BUSY FLAG (Can be read only)
- 1: Busy state
- 0: Ready state

Figure 27 Address Register

2. **Display Memory (DRAM) (Accessed with RS = 1, register number = $(000)_2$)**

Although display memory (figure 28) is not a register, it can be handled as one. 8- or 6-bit data can be selected by the control register WLS bit according to the character font in use. If 6-bit data is selected, D7 and D6 bits are invalid.

3. **X Address Register (XAR) (Accessed with RS = 1, register number = $(001)_2$)**

This register (figure 29) contains 3 invalid bits (D7 to D5) and 5 valid bits (D4 to D0). It sets X addresses and confirms X addresses after writing or reading to or from the display memory.

4. **Y Address Register (YAR) (Accessed with RS = 1, register number = $(010)_2$)**

This register (figure 30) contains 1 invalid bit (D7) and 7 valid bits (D6 to D0). It sets Y addresses and confirms Y addresses after writing or reading to or from the display memory.

D7	D6	D5	D4	D3	D2	D1	D0
8-Bit Data							
*	*	6-Bit Data					

Reading bits marked with * return 0s and writing them is invalid.

Figure 28 Display Memory

D7	D6	D5	D4	D3	D2	D1	D0
—			XAD				

XAD: 0 to 20 (\$00 to \$14) when display data is 8 bits long and 0 to 27 (\$00 to \$1B) when display data is 6 bits long. A maximum of \$1F is programmable.

Figure 29 X Address Register

D7	D6	D5	D4	D3	D2	D1	D0
—	YAD						

YAD: 0 to 128 (\$00 to \$7F)

Figure 30 Y Address Register

5. Control Register (FCR) (Accessed with RS = 1, register number = $(011)_2$)

This register (figure 31), containing eight bits, has a variety of functions such as specifying the method for accessing RAM, determining RAM valid area, and selecting the function of the LCD driving signal output pins. It must be initialized as soon as possible after power-on since it determines the overall operation of the HD66108T. The PON bit may have to be re-set afterwards. If the DUTY bits are rewritten after initialization at power-on (if values other than the initial values are desired), the display memory will not preserve data; the display memory must be set again after a time period of t_{CL1} or longer. For determining t_{CL1}, refer to equation 1 (section 3.1).

D7	D6	D5	D4	D3	D2	D1	D0
INC	WLS	PON	ROS		DUTY		

(1) INC (Address increment direction select)
- 1: X address is incremented
- 0: Y address is incremented

(2) WLS (Word length (of display data) select)
- 1: 6-bit word
- 0: 8-bit word

(3) PON (Row data protect on)
- 1: Protect function on
- 0: Pretect function off

(4) ROS (Row output (function of LCD driving output pins) select)

No.	Bit 4 3	Contents
0	0 0	165 column outputs
1	0 1	65 row outputs from the right side
2	1 0	65 row outputs from the left and right sides
3	1 1	33 row outputs from the right side

(5) DUTY (Multiplexing duty ratio)

No.	Bit 2	1	0	Multiplexing Duty Ratio
0	0	0	0	1/32
1	0	0	1	1/34
2	0	1	0	1/36
3	0	1	1	1/48
4	1	0	0	1/50
5	1	0	1	1/64
6	1	1	0	1/66
7	1	1	1	Testing mode

Figure 31 Control Register

6. Mode Register (MDR) (Accessed with RS = 1, register number = $(100)_2$)

This register (figure 32), containing 3 invalid bits (D7 to D5) and 5 valid bits (D4 to D0), selects a system clock and type of LCD driving waveform. It must also be initialized after power-on since it determines overall HD66108T operation like the FCR register. If the FFS bits are rewritten after initialization at power-on (if values other than the initial values are desired), the display memory will not preserve data; the display memory must be set again after a time period of t_{CL1} or longer. For determining t_{CL1}, refer to equation 1 (section 3.1).

D7	D6	D5	D4	D3	D2	D1	D0
—			FFS			DWS	

(1) FFS (Frame frequency select)

No.	Bit 4	Bit 3	Bit 2	Frequency-Division Ratio
0	0	0	0	1
1	0	0	1	1/2
2	0	1	0	1/3
3	0	1	1	1/4
4	1	0	0	1/6
5	1	0	1	1/8
6	1	1	0	2
7	1	1	1	—

(2) DWS (LCD driving waveform select)

No.	Bit 1	Bit 0	Driving Waveform
0	0	0	A-type waveform
1	0	1	B-type waveform
2	1	0	C-type waveform
3	1	1	—

Figure 32 Mode Register

7. C Select Register (CSR) (Accessed with RS = 1, register number = $(101)_2$)

This register (figure 33) contains 2 invalid bits (D7 and D6) and 5 valid bits (D5 to D0). It controls C-type waveforms and is activated only when MDR register's DWS bits are set for this type of waveform.

D7	D6	D5	D4	D3	D2	D1	D0
—		EOR	CLN				

(1) EOR (B-type waveform M signal ⊕ no. of counting lines on/off)
- 1: EOR function on
- 0: EOR function off

(2) CLN (No. of counting lines in C-type waveform)
1 to 31 should be set in these bits; 0 must not be set.

Figure 33 C Select Register

Reset Function

The $\overline{\text{RESET}}$ pin starts the HD66108T after power-on. A $\overline{\text{RESET}}$ signal must be input via this pin for at least 20 µs to prevent system failure due to excessive current created after power-on. Figure 34 shows the reset definition.

(1) **Reset Status of Pins**
Table 7 shows the reset status of output pins. The pins return to normal operation after reset.

(2) **Reset Status of Registers**
The $\overline{\text{RESET}}$ signal has no effect on registers or register bits except for the address register's STBY bit and the X and Y address registers, which are reset to 0's by the signal. Table 8 shows the reset status of registers.

(3) **Status after Reset**
The display memory does not preserve data which has been written to it before reset; it must be set again after reset.

A $\overline{\text{RESET}}$ signal terminates the standby mode.

Table 7 Reset Status of Pins

Pin	Status
OSC2	Outputs clock pulses or oscillates
CO	Outputs clock pulses
CL1	Low (master chip) or high-impedance (slave chip)
FLM	Low (master chip) or high-impedance (slave chip)
M	Low (master chip) or high-impedance (slave chip)
Xn(column output pins)	V4
Xn' (Row output pins)	V5

Table 8 Reset Status of Registers

Register	Status
Address register	Pre-reset status with the STBY bit reset to 0
X address register	Reset to 0's
Y address register	Reset to 0's
Control register	Pre-reset status
Mode register	Pre-reset status
C select register	Pre-reset status
Display memory	Preserves no pre-reset data

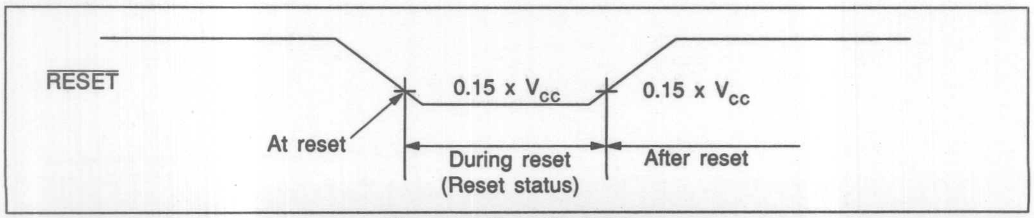


Figure 34 Reset Definition

Precautionary Notes When Using the HD66108T

(1) Install a 0.1-µF bypass capacitor as close to the LSI as possible to reduce power supply impedance (V_{CC}-GND and V_{CC}-V_{EE}).

(2) Do not leave input pins open since the HD66108T is a CMOS LSI; refer to "Pin Functions" on how to deal with each pin.

(3) When using the internal oscillation clock, attach an oscillation resistor as close to the LSI as possible to reduce coupling capacitance.

(4) Make sure to input the reset signal at power-on so that internal units operate as specified.

(5) Maintain the LCD driving power at V_{CC} during standby state so that DC is not applied to an LCD, in which Xn pins are fixed at V4 or V5 level.

Programming Restrictions

(1) After busy time is terminated, an X or Y address is not incremented until 0.5-clock time has passed. If an X or Y address is read during this time period, non-updated data will be read. (The addresses are incremented even in this case.) In addition, the address increment direction should not be changed during this time since it will cause malfunctions.

(2) Although the maximum output rows is 33 when 33-row-output mode from the right side is specified, any multiplexing duty ratio can be specified. Therefore, row output data sufficient to fill the specified duty must be input in the Y direction. Figure 35 shows how to set row data in the case of 1/34 multiplexing duty ratio. In this case, 0s must be set in Y33 since data for the 34th row (Y33) are not output.

(3) Do not set the C select register's CLN bits to 0 for the M signal of C-type waveform.

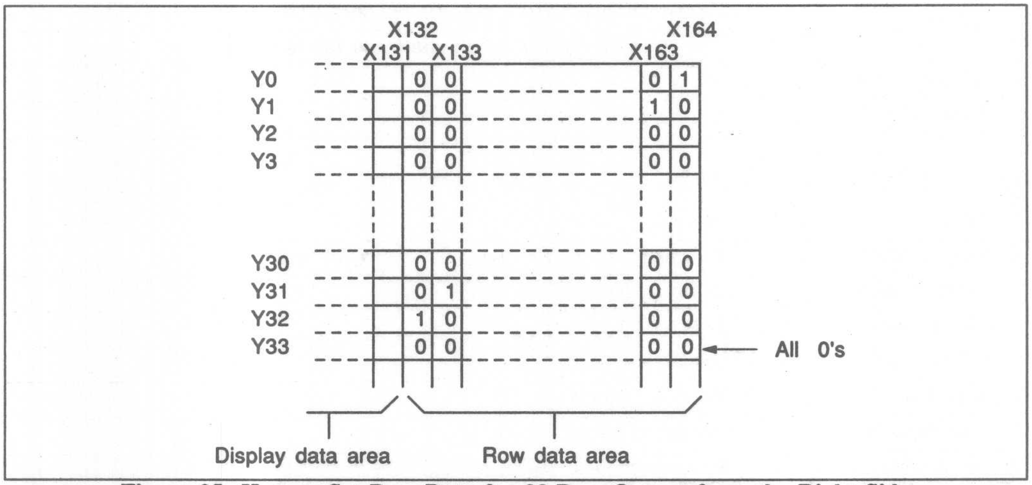


Figure 35 How to Set Row Data for 33-Row Output from the Right Side

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power Supply Voltage (1)	$V_{CC}1$ to $V_{CC}3$	–0.3 to +7.0	V
Power Supply Voltage (2)	$V_{CC} - V_{EE}$	–0.3 to +16.5	V
Input Voltage	V_{in}	–0.3 to VCC + 0.3	V
Operating Temperature	T_{op}	–20 to + 75	°C
Storage Temperature	T_{stg}	–20 to +85	°C

Notes: 1. Permanent LSI damage may occur if the maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 2.7 to 6.0 V, GND = 0 V, Ta = –20 to + 75°C). If these conditions are exceeded, LSI malfunctions could occur.

2. Power supply voltages are referenced to GND = 0 V. Power supply voltage (2) indicates the difference between V_{CC} and V_{EE}.

Electrical Characteristics

DC Characteristics (1) (V_{CC} = 5 V ±20%, GND = 0 V, $V_{CC} - V_{EE}$ = 6.0 to 15 V, Ta = –20 to+75°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Input High Voltage	OSC1	$V_{IH}1$	$0.8 \times V_{CC}$	–	$V_{CC} + 0.3$	V		
	$\overline{M}$/S, CL1, FLM, M, TEST1, TEST2	$V_{IH}2$	$0.7 \times V_{CC}$	–	$V_{CC} + 0.3$	V		
	$\overline{RESET}$	$V_{IH}3$	$0.85 \times V_{CC}$	–	$V_{CC} + 0.3$	V		
	The other inputs	$V_{IH}4$	2.0	–	$V_{CC} + 0.3$	V	V_{CC} = 5 V ±10%	5
Input Low Voltage	OSC1	$V_{IL}1$	–0.3	–	$0.2 \times V_{CC}$	V		
	$\overline{M}$/S, CL1, FLM, M, TEST1, TEST2	$V_{IL}2$	–0.3	–	$0.3 \times V_{CC}$	V		
	$\overline{RESET}$	$V_{IL}3$	–0.3	–	$0.15 \times V_{CC}$	V		
	The other inputs	$V_{IL}4$	–0.3	–	0.8	V	V_{CC} = 5V ±10%	6
Output High Voltage	CO, CL1, FLM, M	$V_{OH}1$	$0.9 \times V_{CC}$	–	–	V	$-I_{OH}$ = 0.1 mA	
	DB7–DB0	$V_{OH}2$	2.4	–	–	V	$-I_{OH}$ = 0.2 mA V_{CC} = 5 V ±10%	7
Output Low Voltage	CO, CL1, FLM, M	$V_{OL}1$	–	–	$0.1 \times V_{CC}$	V	I_{OL} = 0.1 mA	
	DB7–DB0	$V_{OL}2$	–	–	0.4	V	I_{OL} = 1.6 mA V_{CC} = 5 V ±10%	8
Input Leakage Current	All except DB7–DB0, CL1, FLM, M	I_{IIL}	–2.5	–	2.5	µA	V_{in} = 0 to V_{CC}	
Tri-State Leakage Current	DB7–DB0, CL1, FLM, M	I_{TSL}	–10	–	10	µA	V_{in} = 0 to V_{CC}	
V Pins Leakage Current	V1, V3, V4, V6, VMHn, VMLn	I_{VL}	–10	–	10	µA	$V_{in} = V_{EE}$ to V_{CC}	
Current Consumption	During display	$I_{CC}1$	–	–	400	µA	External clock f_{OSC} = 500 kHz	1
		$I_{CC}2$	–	–	1.0	mA	Internal oscillation Rf = 91 kΩ	1
	During standby data	I_{SB}	–	–	10	µA		1, 2
ON Resistance between Vi and Xj	X0–X164	R_{ON}	–	–	10	kΩ	$\pm I_{LD}$ = 50 µA $V_{CC} - V_{EE}$ = 10 V	3
V Pins Voltage Range		ΔV	–	–	35	%		4
Oscillating Frequency		f_{OSC}	315	450	585	kHz	Rf = 91 kΩ	

Notes:
1. When voltage applied to input pins is fixed to V_{CC} or to GND and output pins have no load capacity.
2. When the LSI is not exposed to light and Ta = 0 to 40°C with the STBY bit = 1. If using external clock pulses, input pins must be fixed high or low. Exposing the LSI to light increases current consumption.
3. I_{LD} indicates the current supplied to one measured pin.
4. $\Delta V = 0.35 \times (V_{CC} - V_{EE})$. For levels V1, V2, and V3, the voltage employed should fall between the V_{CC} and the ΔV and for levels V4, V5, and V6, the voltage employed should fall between the V_{EE} and the ΔV (figure 36).
5. $V_{IH}3$ (min) = $0.7 \times V_{CC}$ when used under conditions other than V_{CC} = 5 v ±10%.
6. $V_{IL}3$ (max) = $0.15 \times V_{CC}$ when used under conditions other than V_{CC} = 5 V ±10%.
7. $V_{OH}2$ (min) = $0.9 \times V_{CC}$ ($-I_{OH}$ = 0.1 mA) when used under conditions other than V_{CC} = 5 V ±10%.
8. $V_{OL}2$ (max) = $0.1 \times V_{CC}$ (I_{OL} = 0.1 mA) when used under conditions other than V_{CC} = 5 V ±10%.

DC Characteristics (2) (V_{CC} = 2.7 to 4.0 V, GND = 0 V, $V_{CC} - V_{EE}$ = 6.0 to 15 V, Ta = –20 to +75°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Input High Voltage	$\overline{\text{RESET}}$	$V_{IH}1$	$0.85 \times V_{CC}$	–	$V_{CC} + 0.3$	V		
	The other inputs	$V_{IH}2$	$0.7 \times V_{CC}$	–	$V_{CC} + 0.3$	V		
Input Low Voltage	$\overline{\text{M}}$/S, OSC1, CL1, FLM, TEST1, TEST2, M	$V_{IL}1$	–0.3	–	$0.3 \times V_{CC}$	V		
	The other inputs	$V_{IL}2$	–0.3	–	$0.15 \times V_{CC}$	V		
Output High Voltage		$V_{OL}1$	$0.9 \times V_{CC}$	–	–	V	$-I_{OH} = 50\ \mu A$	
Output Low Voltage		$V_{OL}1$	–	–	$0.1 \times V_{CC}$	V	$I_{OL} = 50\ \mu A$	
Input Leakage Current	All except DB7–DB0, CL1, FLM, M	I_{IIL}	–2.5	–	2.5	µA	V_{in} = 0 to V_{CC}	
Tri-State Leakage Current	DB7–DB0, CL1, FLM, M	I_{TSL}	–10	–	10	µA	V_{in} = 0 to V_{CC}	
V Pins Leakage Current	V1, V3, V4, V6, VMHn, VMLn	I_{VL}	–10	–	10	µA	$V_{in} = V_{EE}$ to V_{CC}	
Current Consumption	During display	$I_{CC}1$	–	–	260	µA	External clock f_{OSC} = 500 kHz	1
		$I_{CC}2$	–	–	700	µA	Internal oscillation Rf = 75 kΩ	1
	During standby state	I_{SB}	–	–	10	µA		1, 2
ON Resistance between Vi and Xj	X0–X164	R_{ON}	–	–	10	kΩ	$\pm I_{LD} = 50\ \mu A$, $V_{CC} - V_{EE}$ = 10 V	3
V Pins Voltage Range		ΔV	–	–	35	%		4
Oscillating Frequency		f_{OSC}	315	450	585	kHz	Rf = 75 kΩ	

Notes:
1. When voltage applied to input pins is fixed to V_{CC} or to GND and output pins have no load capacity. Exposing the LSI to light increases current consumption.
2. When the LSI is not exposed to light and Ta = 0 to 40°C with the STBY bit = 1. If using external clock pulses, input pins must be fixed high or low.
3. I_{LD} indicates the current supplied to one measured pin.
4. $\Delta V = 0.35 \times (V_{CC} - V_{EE})$. For levels V1, V2, and V3, the voltage employed should fall between the V_{CC} and the ΔV and for levels V4, V5, and V6, the voltage employed should fall between the V_{EE} and the ΔV (figure 36).

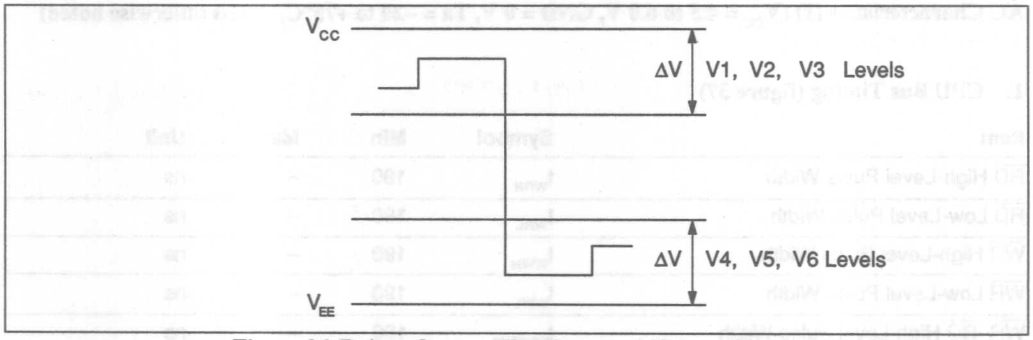


Figure 36 Driver Output Waveform and Voltage Levels

AC Characteristics (1) (V_{CC} = 4.5 to 6.0 V, GND = 0 V, Ta = –20 to +75°C, unless otherwise noted)

1. CPU Bus Timing (figure 37)

Item	Symbol	Min	Max	Unit	
$\overline{RD}$ High-Level Pulse Width	t_{WRH}	190	–	ns	
$\overline{RD}$ Low-Level Pulse Width	t_{WRL}	190	–	ns	
$\overline{WR}$ High-Level Pulse Width	t_{WWH}	190	–	ns	
$\overline{WR}$ Low-Level Pulse Width	t_{WWL}	190	–	ns	
$\overline{WR}$–$\overline{RD}$ High-Level Pulse Width	t_{WWRH}	190	–	ns	
$\overline{CS}$, RS Setup Time	t_{AS}	0	–	ns	
$\overline{CS}$, RS Hold Time	t_{AH}	0	–	ns	
Write Data Setup Time	t_{DSW}	100	–	ns	
Write Data Hold Time	t_{DHW}	0	–	ns	
Read Data Output Delay Time	t_{DDR}	–	150	ns	Note
Read Data Hold Time	t_{DHR}	20	–	ns	Note
External Clock Cycle Time	t_{CYC}	0.25	5.0	µs	
External Clock High-Level Pulse Width	t_{WCH}	0.1	–	µs	
External Clock Low-Level Pulse Width	t_{WCL}	0.1	–	µs	
External Clock Rise and Fall time	tr, tf	–	20	ns	

Note: Measured by test circuit 1 (figure 39).

2. LCD Interface Timing (figure 38)

Item			Symbol	Min	Max	Notes
$\overline{M}$/S = 0	CL1	High-Level Pulse Width	$t_{WCH}1$	35	–	1, 4, 5
	CL1	Low-Level Pulse Width	$t_{WCL}1$	35	–	1, 4, 5
	FLM	Delay Time	$t_{DFL}1$	–2.0	+2.0	4, 5
	FLM	Hold Time	$t_{HFL}1$	–2.0	+2.0	4, 5
	M Output Delay Time		$t_{DMO}1$	–2.0	+2.0	4, 5
$\overline{M}$/S = 1	CL1	High-Level Pulse Width	$t_{WCH}2$	35	–	4, 5
	CL1	Low-Level Pulse Width	$t_{WCL}2$	$11 \times t_{CYC}$	–	2, 4, 5
	FLM	Delay Time	$t_{DFL}2$	–2.0	$1.5 \times t_{CYC}$	3, 4, 5
	FLM	Hold Time	$t_{HFL}2$	–2.0	+2.0	4, 5
	M Delay Time		t_{DMI}	–2.0	+2.0	4, 5

Notes:
1. When R_{OSC} is 91 kΩ (V_{CC} = 4.0 to 6 V) or 75 kΩ (V_{CC} = 2.0 to 4.0 V) and bits FFS are set for 1.
2. When bits FFS are set for 1 or 2. The value is $19 \times t_{CYC}$ in other cases.
3. When bitgs FFS are set for 1 or 2. The value is $8.5 \times t_{CYC}$ in other cases.
4. Measured by test circuit 2 (figure 39).
5. Units are µs.

AC Characteristics (2) (V_{CC} = 2.7 to 4.5 V, GND = 0 V, Ta = –20 to +75°C, unless otherwise noted)

1. CPU Bus Timing (figure 37)

Item	Symbol	Min	Max	Unit	
$\overline{RD}$ High-Level Pulse Width	t_{WRH}	1.0	–	µs	
$\overline{RD}$ Low-Level Pulse Width	t_{WRL}	1.0	–	µs	
$\overline{WR}$ High-Level Pulse Width	t_{WWH}	1.0	–	µs	
$\overline{WR}$ Low-Level Pulse Width	t_{WWL}	1.0	–	µs	
$\overline{WR}$–$\overline{RD}$ High-Level Pulse Width	t_{WWRH}	1.0	–	µs	
$\overline{CS}$, RS Setup Time	t_{AS}	0.5	–	µs	
$\overline{CS}$, RS Hold Time	t_{AH}	0.1	–	µs	
Write Data Setup Time	t_{DSW}	1.0	–	µs	
Write Data Hold Time	t_{DHW}	0	–	µs	
Read Data Output Delay Time	t_{DDR}	–	0.5	µs	Note
Read Data Hold Time	t_{DHR}	20	–	ns	Note
External Clock Cycle Time	t_{CYC}	1.6	5.0	µs	
External Clock High-Level Pulse Width	t_{WCH}	0.7	–	µs	
External Clock Low-Level Pulse Width	t_{WCL}	0.7	–	µs	
External Clock Rise and Fall time	tr, tf	–	0.1	µs	

Note: Measured by test circuit 2 (figure 39).

2. LCD Interface Timing (figure 38)

Item			Symbol	Min	Max	Notes
$\overline{M}$/S = 0	CL1	High-Level Pulse Width	$t_{WCH}1$	35	–	1, 4, 5
	CL1	Low-Level Pulse Width	$t_{WCL}1$	35	–	1, 4, 5
	FLM	Delay Time	$t_{DFL}1$	–2.0	+2.0	4, 5
	FLM	Hold Time	$t_{HFL}1$	–2.0	+2.0	4, 5
	M Output Delay Time		$t_{DMO}1$	–2.0	+2.0	4, 5
$\overline{M}$/S = 1	CL1	High-Level Pulse Width	$t_{WCH}2$	35	–	4, 5
	CL1	Low-Level Pulse Width	$t_{WCL}2$	$11 \times t_{CYC}$	–	2, 4, 5
	FLM	Delay Time	$t_{DFL}2$	–2.0	$1.5 \times t_{CYC}$	3, 4, 5
	FLM	Hold Time	$t_{HFL}2$	–2.0	+2.0	4, 5
	M Delay Time		t_{DMI}	–2.0	+2.0	4, 5

Notes:
1. When R_{OSC} is 91 kΩ (V_{CC} = 4.0 to 6 V) or 75 kΩ (V_{CC} = 2.7 to 4.0 V) and bits FFS are set for 1.
2. When bits FFS are set for 1 or 2. The value is $19 \times t_{CYC}$ in other cases.
3. When bits FFS are set for 1 or 2. The value is $8.5 \times t_{CYC}$ in other cases.
4. Measured by test circuit 2 (figure 39).
5. Units are µs.

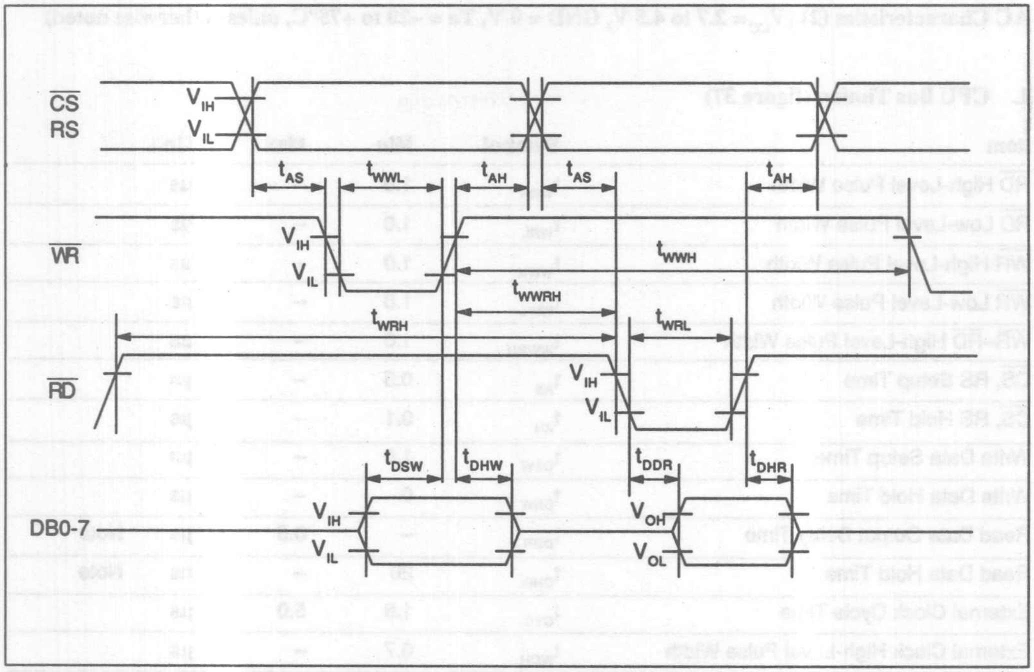


Figure 37 CPU Bus Timing

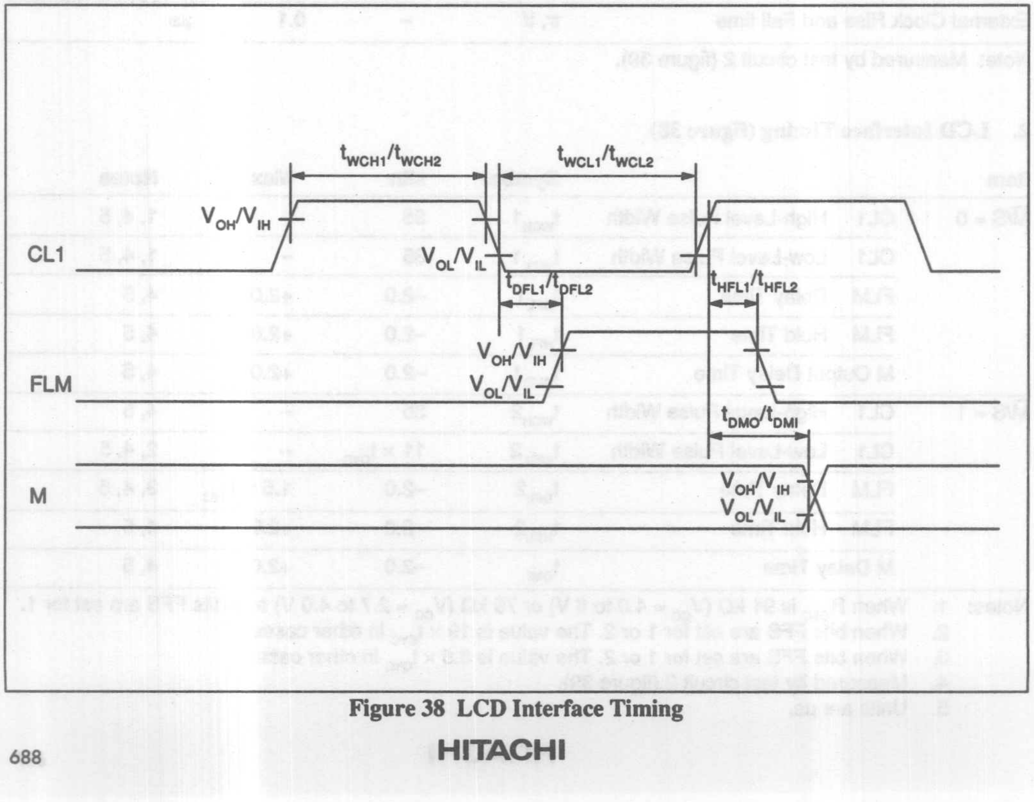
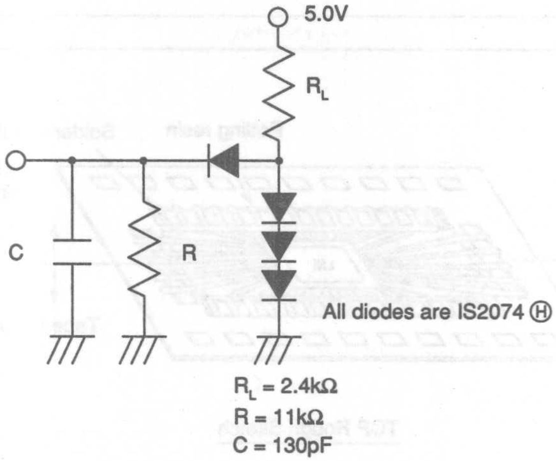
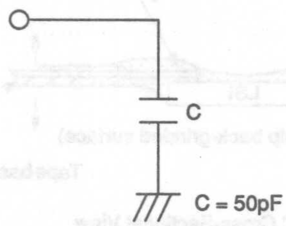


Figure 38 LCD Interface Timing



Test Circuit 1

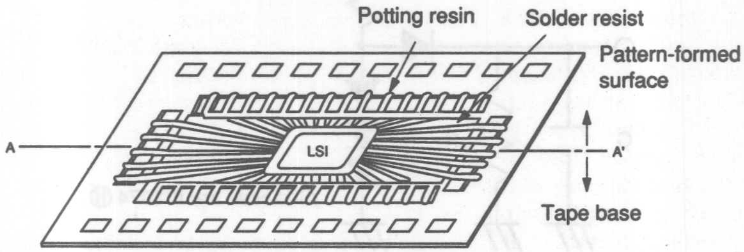


Test Circuit 2

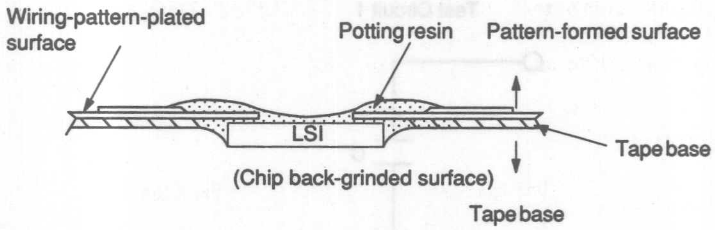
Figure 39 Load Circuits

TCP Sketches and Mounting

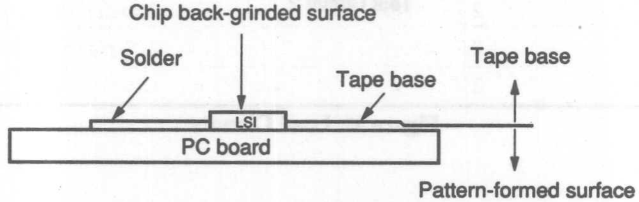
The following shows TCP sketches and TCP mounting on a printed circuit board. These drawings do not restrict TCP shape.



TCP Rough Sketch



A-A' Cross-Sectional View



TCP Mounting on PC Board

HD66204

(Dot Matrix Liquid Crystal Graphic Display Column Driver with 80-Channel Outputs)

Description

The HD66204F/HD66204FL/HD66204TF/HD 66204TFL, the column driver for a large liquid crystal graphic display, features as many as 80 LCD outputs powered by 80 internal LCD drive circuits. This device latches 4-bit parallel data sent from an LCD controller, and generates LCD drive signals. In standby mode provided by its internal standby function, only one drive circuit operates, lowering power dissipation. The HD66204 has a complete line-up: the HD66204F, a standard device powered by 5 V ± 10%; the HD66204FL, a 2.7–5.5 V, low power dissipation device suitable for battery-driven portable equipment such as "notebook" personal computers and palm-top personal computers; and the HD66204TF and HD66204TFL, thin package devices powered by 5 V ± 10% and 2.7–5.5 V, respectively.

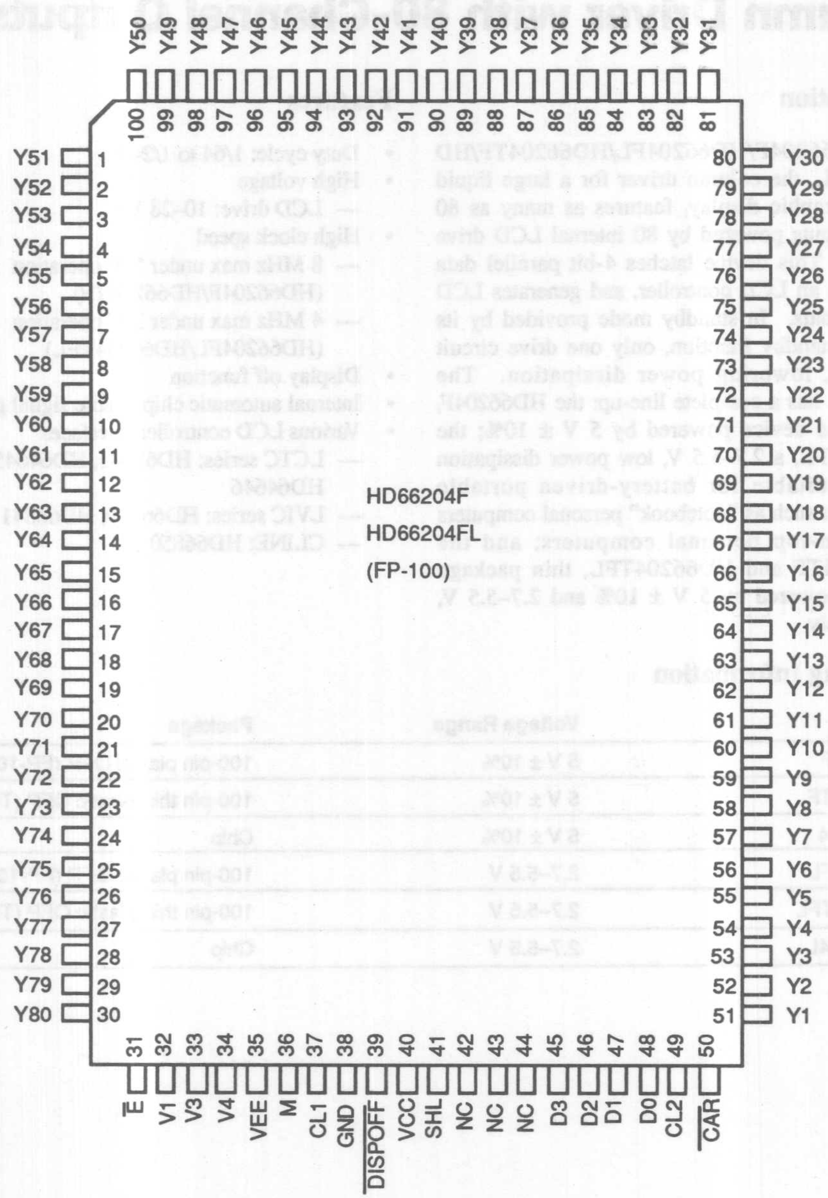
Features

- Duty cycle: 1/64 to 1/240
- High voltage
  — LCD drive: 10–28 V
- High clock speed
  — 8 MHz max under 5-V operation (HD66204F/HD66204TF)
  — 4 MHz max under 3-V operation (HD66204FL/HD66204TFL)
- Display off function
- Internal automatic chip enable signal generator
- Various LCD controller interfaces
  — LCTC series: HD63645, HD64645, HD64646
  — LVIC series: HD66840, HD66841
  — CLINE: HD66850

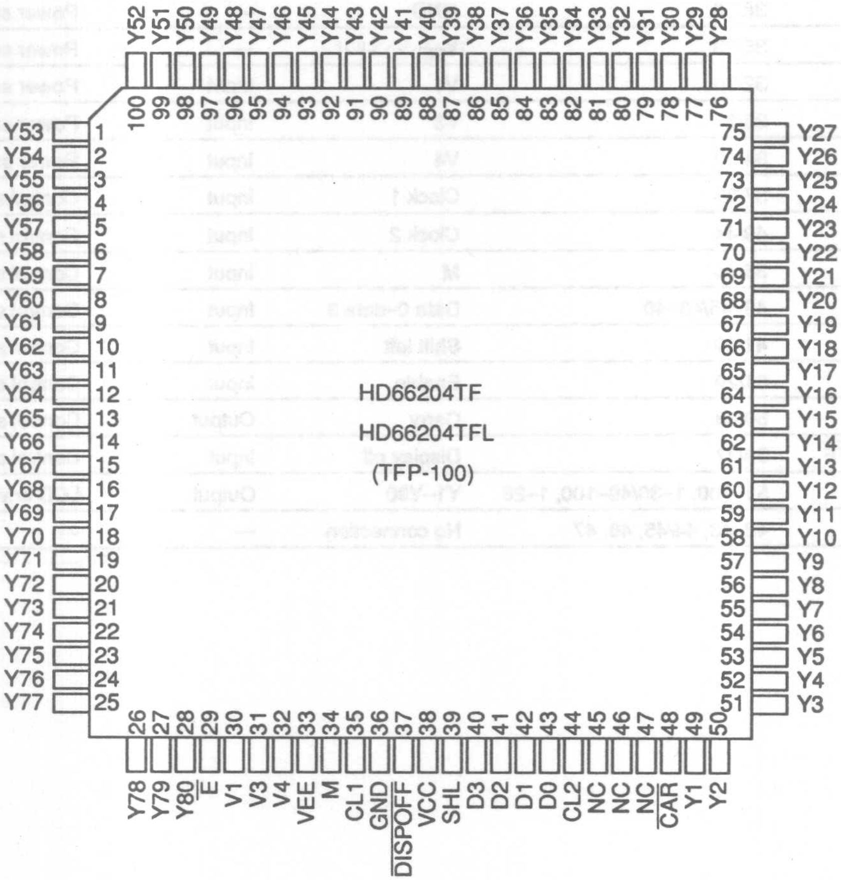
Ordering Information

Type No.	Voltage Range	Package
HD66204F	5 V ± 10%	100-pin plastic QFP (FP-100)
HD66204TF	5 V ± 10%	100-pin thin plastic QFP (TFP-100)
HCD66204	5 V ± 10%	Chip
HD66204FL	2.7–5.5 V	100-pin plastic QFP (FP-100)
HD66204TFL	2.7–5.5 V	100-pin thin plastic QFP (TFP-100)
HCD66204L	2.7–5.5 V	Chip

Pin Arrangement



(Top View)


HD66204TF
HD66204TFL
(TFP-100)
1 Y53
2 Y54
3 Y55
4 Y56
5 Y57
6 Y58
7 Y59
8 Y60
9 Y61
10 Y62
11 Y63
12 Y64
13 Y65
14 Y66
15 Y67
16 Y68
17 Y69
18 Y70
19 Y71
20 Y72
21 Y73
22 Y74
23 Y75
24 Y76
25 Y77
26 Y78
27 Y79
28 Y80
29 E
30 V1
31 V3
32 V4
33 VEE
34 M
35 CL1
36 GND
37 DISPOFF
38 VCC
39 SHL
40 D3
41 D2
42 D1
43 D0
44 CL2
45 NC
46 NC
47 NC
48 CAR
49 Y1
50 Y2
51 Y3
52 Y4
53 Y5
54 Y6
55 Y7
56 Y8
57 Y9
58 Y10
59 Y11
60 Y12
61 Y13
62 Y14
63 Y15
64 Y16
65 Y17
66 Y18
67 Y19
68 Y20
69 Y21
70 Y22
71 Y23
72 Y24
73 Y25
74 Y26
75 Y27
76 Y28
77 Y29
78 Y30
79 Y31
80 Y32
81 Y33
82 Y34
83 Y35
84 Y36
85 Y37
86 Y38
87 Y39
88 Y40
89 Y41
90 Y42
91 Y43
92 Y44
93 Y45
94 Y46
95 Y47
96 Y48
97 Y49
98 Y50
99 Y51
100 Y52

(Top View)

Pin Description

Symbol	Pin No. (FP-100/TFP-100)	Pin Name	Input/Output	Classification
V_{CC}	40/38	V_{CC}	—	Power supply
GND	38/36	GND	—	Power supply
V_{EE}	35/33	V_{EE}	—	Power supply
V1	32/30	V1	Input	Power supply
V3	33/31	V3	Input	Power supply
V4	34/32	V4	Input	Power supply
CL1	37/35	Clock 1	Input	Control signal
CL2	49/44	Clock 2	Input	Control signal
M	36/34	M	Input	Control signal
D_0–D_3	48–45/43–40	Data 0–data 3	Input	Control signal
SHL	41/39	Shift left	Input	Control signal
$\overline{E}$	31/29	Enable	Input	Control signal
$\overline{CAR}$	50/48	Carry	Output	Control signal
$\overline{DISPOFF}$	39/37	Display off	Input	Control signal
Y_1–Y_{80}	51–100, 1–30/49–100, 1–28	Y1–Y80	Output	LCD drive output
NC	42, 43, 44/45, 46, 47	No connection	—	—

Pin Functions

Power Supply

V_{CC}, V_{EE}, GND: V_{CC}–GND supplies power to the internal logic circuits. V_{CC}–V_{EE} supplies power to the LCD drive circuits.

V1, V3, V4: Supply different levels of power to drive the LCD. V1 and V_{EE} are selected levels, and V3 and V4 are non-selected levels. See figure 1.

Control Signal

CL1: Inputs display data latch pulses for the line data latch circuit. The line data latch circuit latches display data input from the 4-bit latch circuit, and outputs LCD drive signals corresponding to the latched data, both at the falling edge of each CL1 pulse.

CL2: Inputs display data latch pulses for the 4-bit latch circuit. The 4-bit latch circuit latches display data input via D_0–D_3 at the falling edge of each CL2 pulse.

M: Changes LCD drive outputs to AC.

D_0–D_3: Input display data. High-voltage level of data corresponds to a selected level and turns an LCD pixel on, and low-voltage level data corresponds to a non-selected level and turns an LCD pixel off.

SHL: Shifts the destinations of display data output. See figure 2.

$\overline{E}$: A low $\overline{E}$ enables the chip, and a high $\overline{E}$ disables the chip.

$\overline{CAR}$: Outputs the $\overline{E}$ signal to the next HD66204 if HD66204s are connected in cascade.

$\overline{DISPOFF}$: A low $\overline{DISP}$ sets LCD drive outputs Y_1–Y_{80} to V1 level.

LCD Drive Output

Y_1–Y_{80}: Each Y outputs one of the four voltage levels V1, V3, V4, or V_{EE}, depending on a combination of the M signal and display data levels. See figure 3.

NC: Must be open.

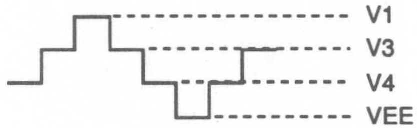


Figure 1 Different Power Supply Voltage Levels for LCD Drive Circuits

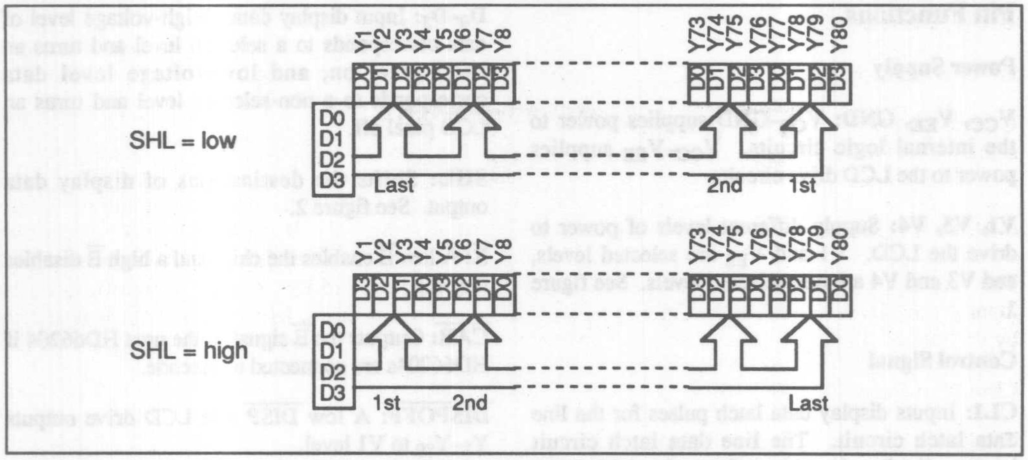


Figure 2 Selection of Destinations of Display Data Output

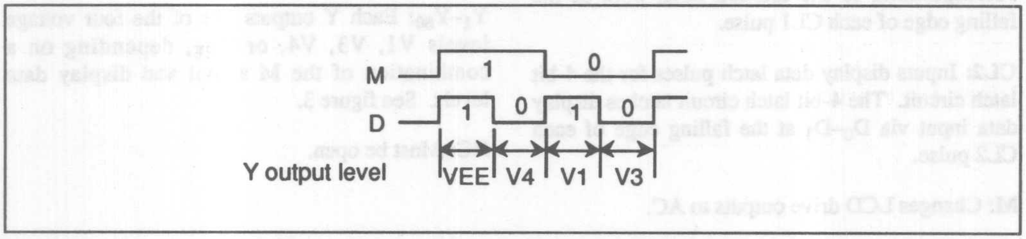


Figure 3 Selection of LCD Drive Output Level

Block Functions

LCD Drive Circuit

Controller: The controller generates the latch signal at the falling edge of each CL2 pulse for the 4-bit latch circuit.

4-Bit Latch Circuit

The 4-bit latch circuit latches 4-bit parallel data input via the D_0 to D_3 pins at the timing generated by the control circuit.

Line Data Latch Circuit

The 80-bit line data latch circuit latches data input from the 4-bit latch circuit, and outputs the latched data to the level shifter, both at the falling edge of each clock 1 (CL1) pulse.

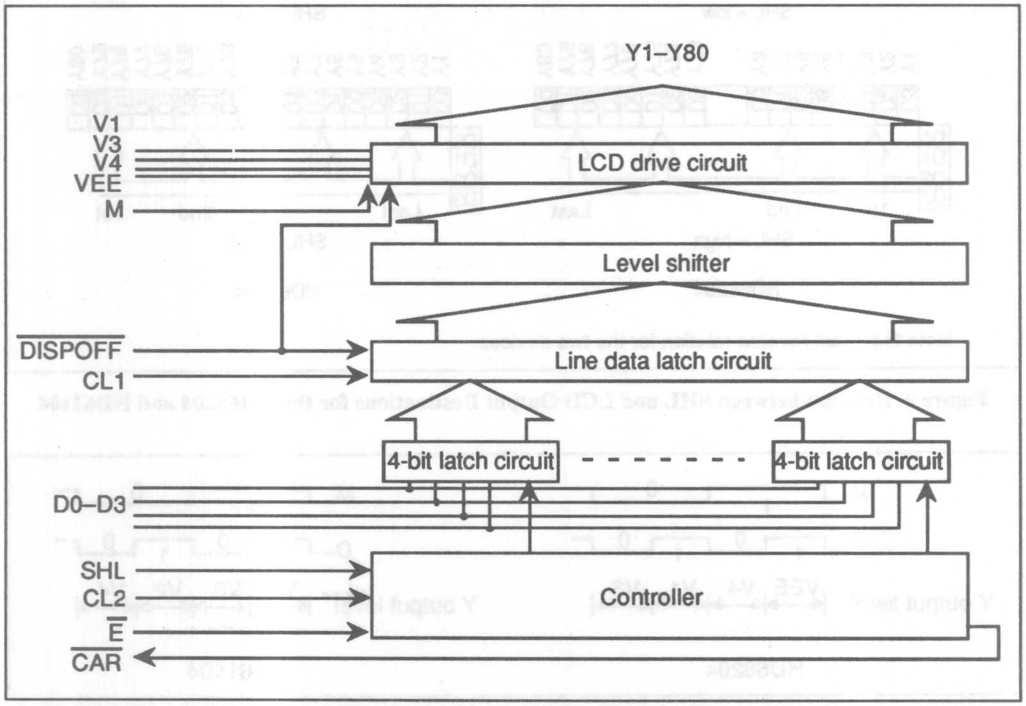
Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

LCD Drive Circuit

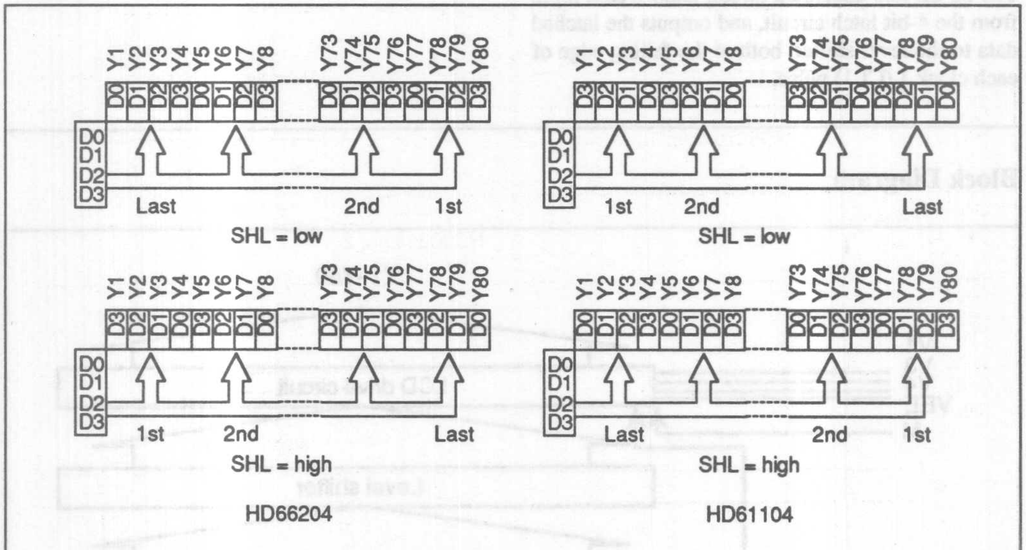
The 80-bit LCD drive circuit generates four voltage levels V1, V3, V4, and VEE, for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on a combination of the M signal and the data in the line data latch circuit.

Block Diagram



Comparison of the HD66204 with the HD61104

Item	HD66204	HD61104
Clock speed	8.0 MHz max.	3.5 MHz max.
Display off function	Provided	Not provided
LCD drive voltage range	10–28 V	10–26 V
Relation between SHL and LCD output destinations	See figure 4	See figure 4
Relation between LCD output levels, M, and data	See figure 5	See figure 5
LCD drive V pins	V1, V3, V4 (V2 level is the same as VEE level)	V1, V2, V3, V4



Note the exact reverse relation for the two devices.

Figure 4 Relation between SHL and LCD Output Destinations for the HD66204 and HD61104

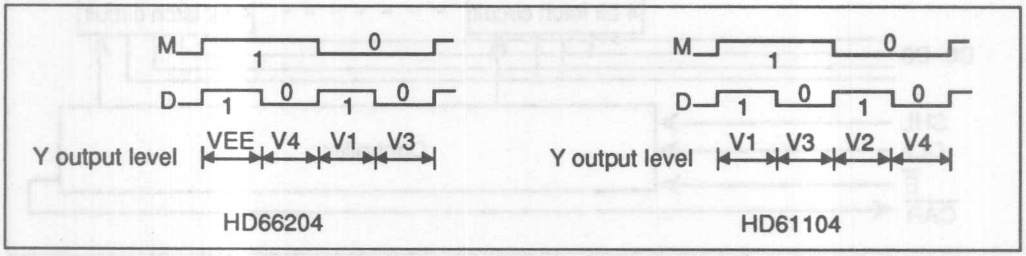
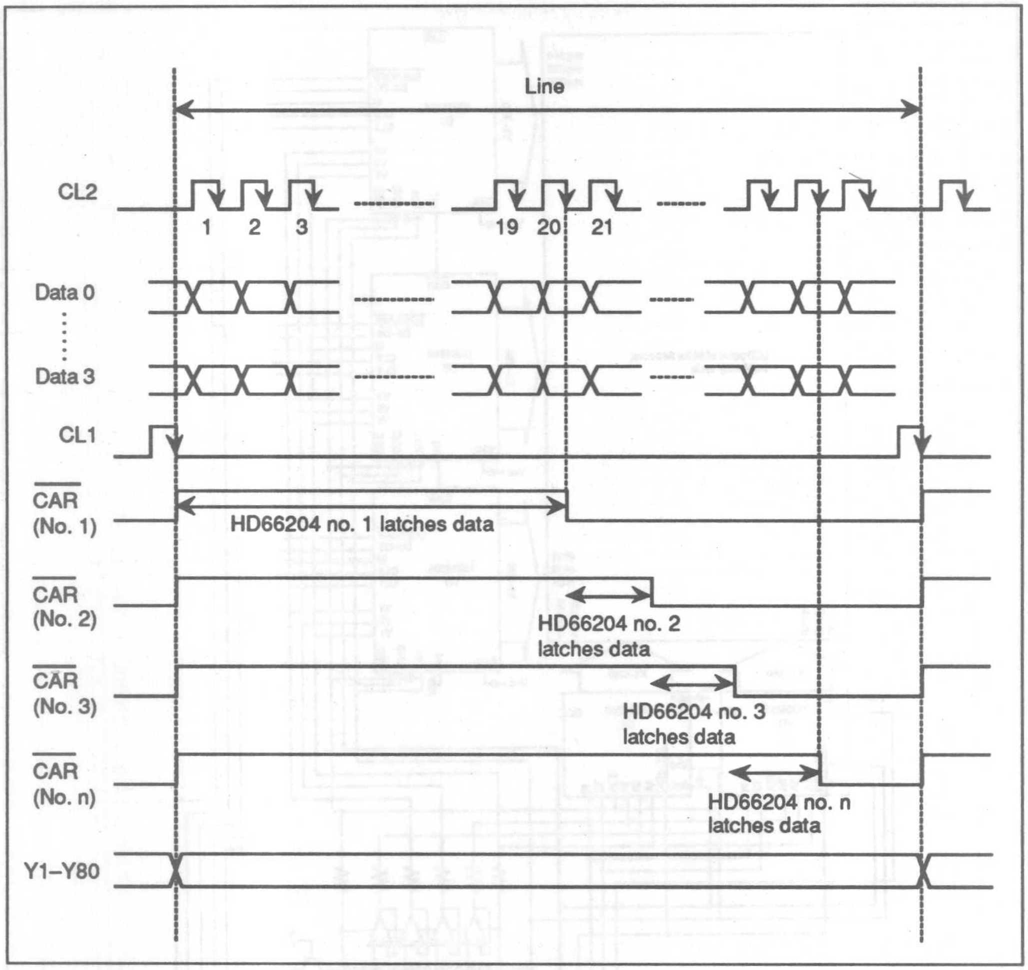
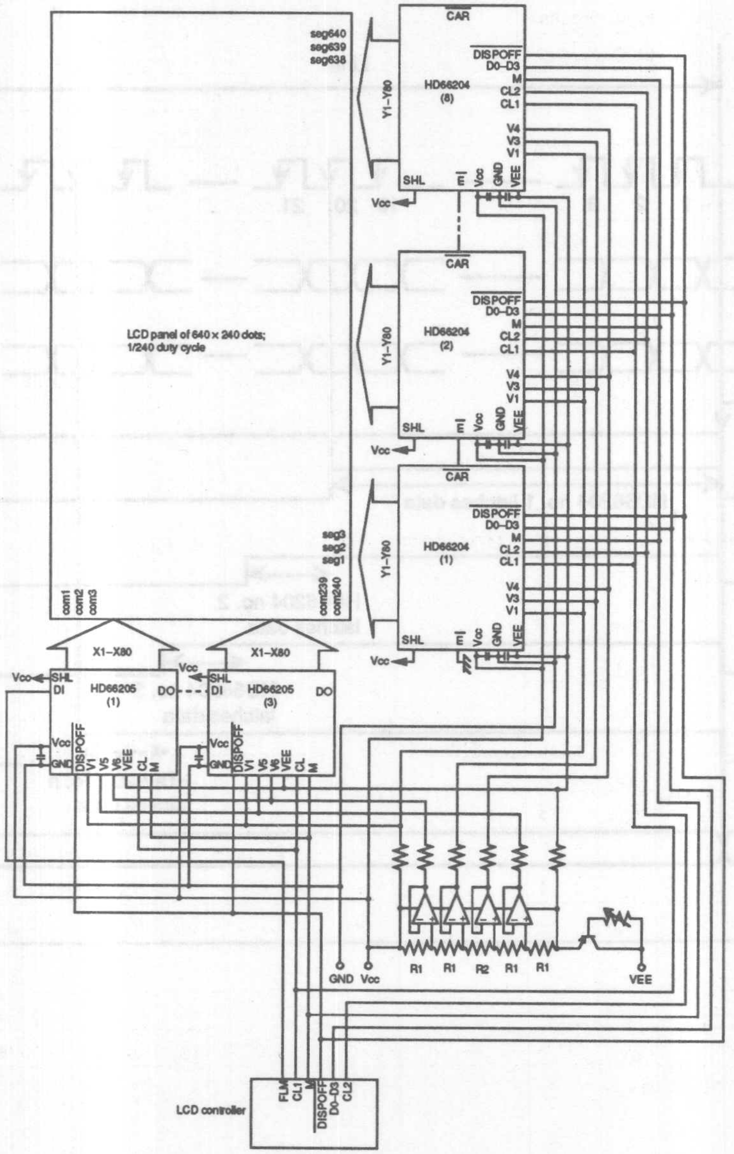


Figure 5 Relation between LCD Output Levels, M, and Data for the HD66204 and HD61104

Operation Timing



Application Example



Notes: 1. The resistances of R1 and R2 depend on the type of the LCD panel used. For example, for an LCD panel with a 1/15 bias, R1 and R2 must be 3 kΩ and 33 kΩ, respectively. That is, R1/(4 • R1 + R2) should be 1/15.

2. To stabilize the power supply, place two 0.1-µF capacitors near each LCD driver: one between the V_{CC} and GND pins, and the other between the V_{CC} and V_{EE} pins.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1
Power supply voltage for LCD drive circuits	V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3	V	
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	1, 3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. The reference point is GND (0 V).
2. Applies to pins CL1, CL2, M, SHL, $\overline{E}$, D_0–D_3, $\overline{DISPOFF}$.
3. Applies to pins V1, V3, and V4.
4. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

Electrical Characteristics

DC Characteristics for the HD66204F/HD66204TF (V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – V_{EE} = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Typ.	Max.	Unit	Condition	Notes
Input high voltage	V_{IH}	1	0.7 × V_{CC}	—	V	V		
Input low voltage	V_{IL}	1	0	—	0.3 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	—	4.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	—	1.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	—	25	µA	V_{IN} = V_{CC} to V_{EE}	
Current consumption 1	I_{GND}	—	—	—	3.0	mA	f_{CL2} = 8.0 MHz f_{CL1} = 20 kHz V_{CC} – V_{EE} = 28 V	2
Current consumption 2	I_{EE}	—	—	150	500	µA	Same as above	2
Current consumption 3	I_{ST}	—	—	—	200	µA	Same as above	2, 3

Pins and notes on next page.

DC Characteristics for the HD66204FL/HD66204TFL (V_{CC} = 2.7 to 5.5 V, GND = 0 V, $V_{CC} - V_{EE}$ = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Condition	Notes
Input high voltage	V_{IH}	1	$0.7 \times V_{CC}$	V_{CC}	V		
Input low voltage	V_{IL}	1	0	$0.3 \times V_{CC}$	V		
Output high voltage	V_{OH}	2	$V_{CC} - 0.4$	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	4.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	1.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	25	µA	V_{IN} = V_{CC} to V_{EE}	
Current consumption 1	I_{GND}	—	—	1.0	mA	f_{CL2} = 4.0 MHz f_{CL1} = 16.8 kHz f_M = 35 Hz V_{CC} = 3.0 V $V_{CC} - V_{EE}$ = 28 V Checker-board pattern	2
Current consumption 2	I_{EE}	—	—	500	µA	Same as above	2
Current consumption 3	I_{ST}	—	—	50	µA	Same as above	2, 3

Pins:
1. CL1, CL2, M, SHL, E, D_0–D_3, $\overline{\text{DISPOFF}}$
2. $\overline{\text{CAR}}$
3. Y_1–Y_{80}, V1, V3, V4
4. V1, V3, V4

Notes:
1. Indicates the resistance between one pin from Y_1–Y_{80} and another pin from V1, V3, V4, and V_{EE}, when load current is applied to the Y pin; defined under the following conditions.

   V_{CC} – GND = 28 V

   V1, V3 = V_{CC} – {2/10($V_{CC} - V_{EE}$)}

   V4 = V_{EE} + {2/10($V_{CC} - V_{EE}$)}

   V1 and V3 should be near V_{CC} level, and V4 should be near V_{EE} level (figure 6). All voltage must be within ΔV. ΔV is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage V_{CC}–V_{EE} (figure 7).
2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.
3. Applies to standby mode.

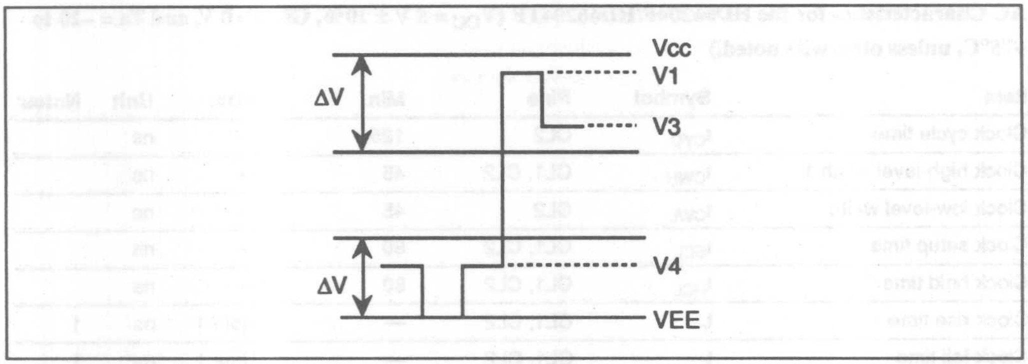


Figure 6 Relation between Driver Output Waveform and Level Voltages

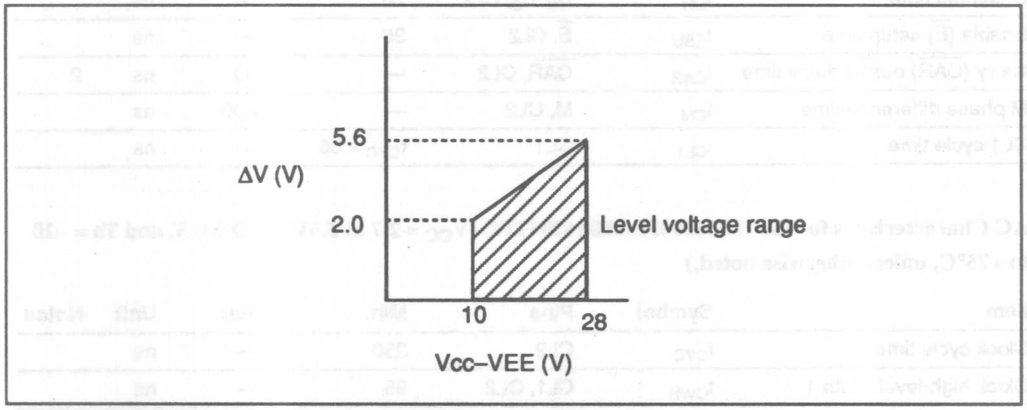


Figure 7 Relation between $V_{CC} - V_{EE}$ and ΔV

AC Characteristics for the HD66204F/HD66204TF (V_{CC} = 5 V ± 10%, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Notes
Clock cycle time	t_{CYC}	CL2	125	—	ns	
Clock high-level width 1	t_{CWH}	CL1, CL2	45	—	ns	
Clock low-level width	t_{CWL}	CL2	45	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	80	—	ns	
Clock rise time	t_r	CL1, CL2	—	Note 1	ns	1
Clock fall time	t_f	CL1, CL2	—	Note 1	ns	1
Data setup time	t_{DS}	D_0–D_3, CL2	20	—	ns	
Data hold time	t_{DH}	D_0–D_3, CL2	20	—	ns	
Enable ($\overline{E}$) setup time	t_{ESU}	$\overline{E}$, CL2	30	—	ns	
Carry ($\overline{CAR}$) output delay time	t_{CAR}	$\overline{CAR}$, CL2	—	80	ns	2
M phase difference time	t_{CM}	M, CL2	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	

AC Characteristics for the HD66204FL/HD66204TFL (V_{CC} = 2.7 to 5.5V, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Notes
Clock cycle time	t_{CYC}	CL2	250	—	ns	
Clock high-level width 1	t_{CWH}	CL1, CL2	95	—	ns	
Clock low-level width	t_{CWL}	CL2	95	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	80	—	ns	
Clock rise time	t_r	CL1, CL2	—	Note 1	ns	1
Clock fall time	t_f	CL1, CL2	—	Note 1	ns	1
Data setup time	t_{DS}	D_0–D_3, CL2	50	—	ns	
Data hold time	t_{DH}	D_0–D_3, CL2	50	—	ns	
Enable ($\overline{E}$) setup time	t_{ESU}	$\overline{E}$, CL2	65	—	ns	
Carry ($\overline{CAR}$) output delay time	t_{CAR}	$\overline{CAR}$, CL2	—	155	ns	2
M phase difference time	t_{CM}	M, CL2	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	

Notes: 1. t_r, t_f < (t_{CYC} – t_{CWH} – t_{CWL})/2 and t_r, $t_f \le 50$ ns

2. The load circuit shown in figure 8 is connected.

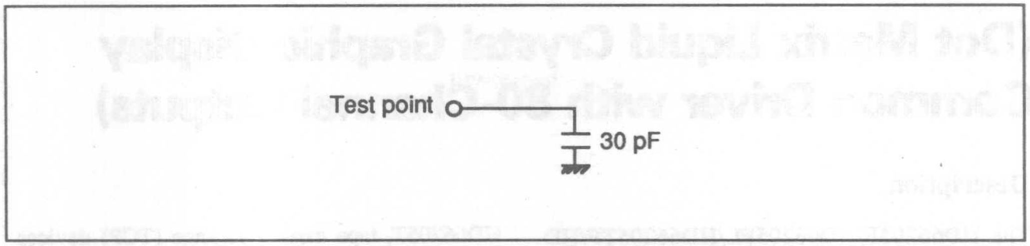


Figure 8 Load Circuit

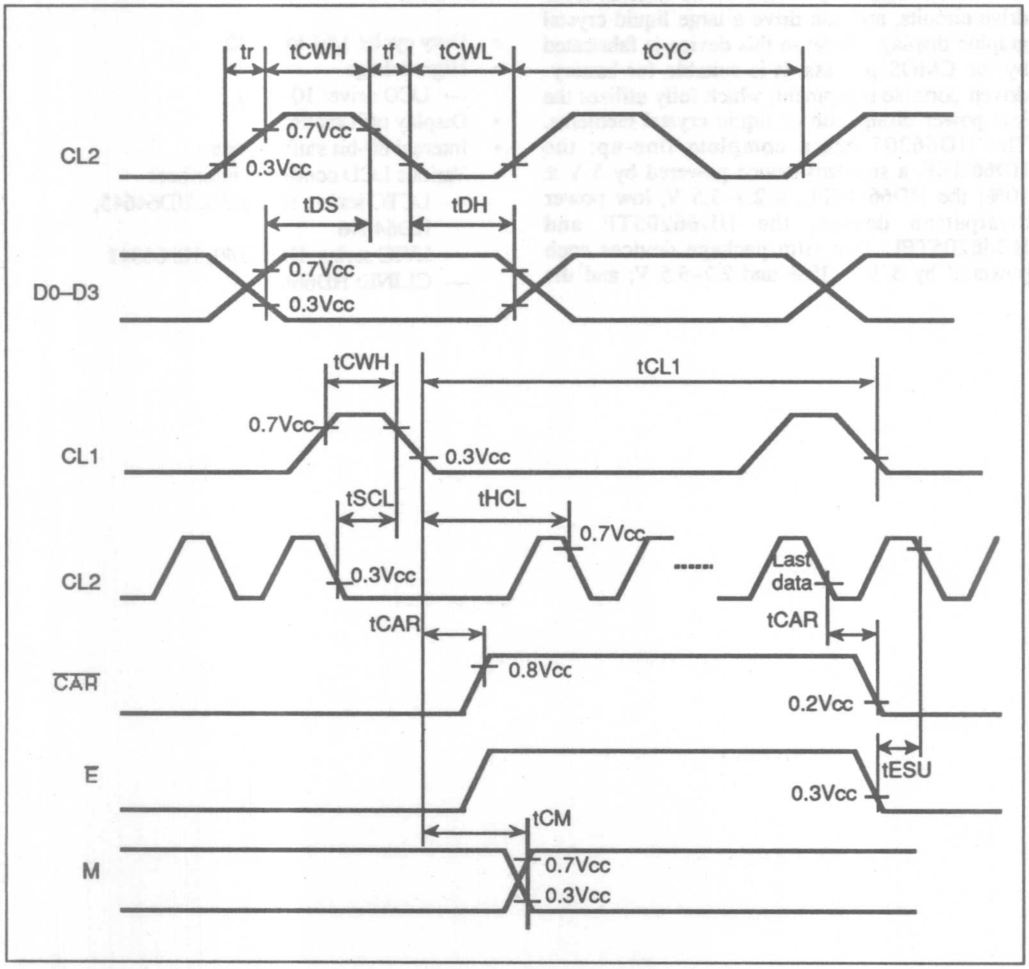


Figure 9 LCD Controller Interface Timing

HD66205

(Dot Matrix Liquid Crystal Graphic Display Common Driver with 80-Channel Outputs)

Description

The HD66205F/HD66205FL/HD66205TF/HD 66205TFL/HD66205T/HD66205TL, the row LCD driver, features low output impedance and as many as 80 LCD outputs powered by 80 internal LCD drive circuits, and can drive a large liquid crystal graphic display. Because this device is fabricated by the CMOS process, it is suitable for battery-driven portable equipment, which fully utilizes the low power dissipation of liquid crystal elements. The HD66205 has a complete line-up: the HD66205F, a standard device powered by 5 V ± 10%; the HD66205FL, a 2.7–5.5 V, low power dissipation device; the HD66205TF and HD66205TFL, thin film package devices each powered by 5 V ± 10% and 2.7–5.5 V; and the HD66205T, tape carrier package (TCP) devices powered by 2.7–5.5 V, respectively.

Features

- Duty cycle: 1/64 to 1/240
- High voltage
  - — LCD drive: 10–28 V
- Display off function
- Internal 80-bit shift register
- Various LCD controller interfaces
  - — LCTC series: HD63645, HD64645, HD64646
  - — LVIC series: HD66840, HD66841
  - — CLINE: HD66850

Ordering Information 1 (Flat package and die shipment)

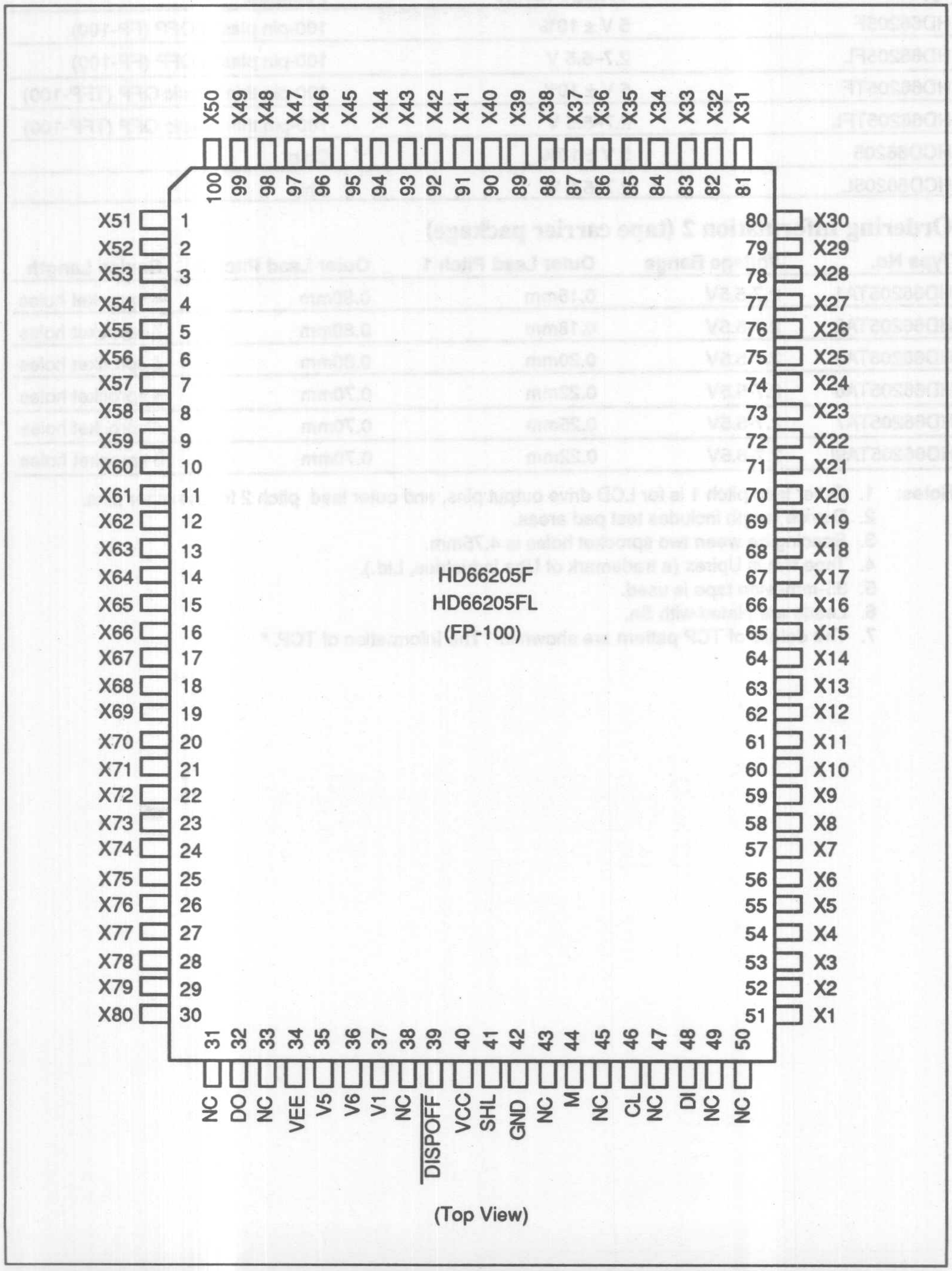
Type No.	Voltage Range	Package
HD66205F	5 V ± 10%	100-pin plastic QFP (FP-100)
HD66205FL	2.7–5.5 V	100-pin plastic QFP (FP-100)
HD66205TF	5 V ± 10%	100-pin thin plastic QFP (TFP-100)
HD66205TFL	2.7–5.5 V	100-pin thin plastic QFP (TFP-100)
HCD66205	5 V ± 10%	Chip
HCD66205L	2.7–5.5 V	Chip

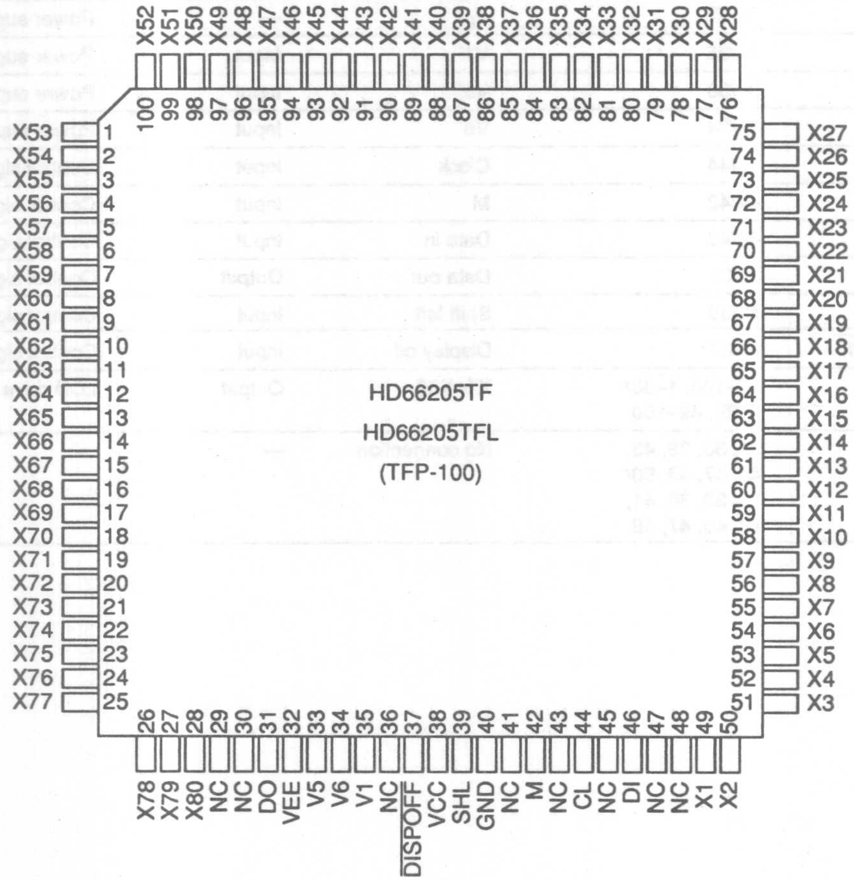
Ordering Information 2 (tape carrier package)

Type No.	Voltage Range	Outer Lead Pitch 1	Outer Lead Pitch 2	Device Length
HD66205TA1	2.7-5.5V	0.15mm	0.80mm	4 sprocket holes
HD66205TA2	2.7-5.5V	0.18mm	0.80mm	4 sprocket holes
HD66205TA3	2.7-5.5V	0.20mm	0.80mm	4 sprocket holes
HD66205TA6	2.7-5.5V	0.22mm	0.70mm	4 sprocket holes
HD66205TA7	2.7-5.5V	0.25mm	0.70mm	4 sprocket holes
HD66205TA9L	2.7-5.5V	0.22mm	0.70mm	3 sprocket holes

Notes:
1. Outer lead pitch 1 is for LCD drive output pins, and outer lead pitch 2 for the other pins.
2. Device length includes test pad areas.
3. Spacing between two sprocket holes is 4.75mm.
4. Tape film is Upirex (a trademark of Ube industries, Ltd.).
5. 35-mm-wide tape is used.
6. Leads are plated with Sn.
7. The details of TCP pattern are shown in " The Information of TCP. "

Pin Arrangement




HD66205TF
HD66205TFL
(TFP-100)
X52 X51 X50 X49 X48 X47 X46 X45 X44 X43 X42 X41 X40 X39 X38 X37 X36 X35 X34 X33 X32 X31 X30 X29 X28
100 99 98 97 96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80 79 78 77 76
X53 1
X54 2
X55 3
X56 4
X57 5
X58 6
X59 7
X60 8
X61 9
X62 10
X63 11
X64 12
X65 13
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66 X18
65 X17
64 X16
63 X15
62 X14
61 X13
60 X12
59 X11
58 X10
57 X9
56 X8
55 X7
54 X6
53 X5
52 X4
51 X3
26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
X78 X79 X80 NC NC DO VEE V5 V6 V1 NC DISPOFF VCC SHL GND NC M NC CL NC DI NC NC X1 X2

(Top View)

Pin Description

Symbol	Pin No. (FP-100 / TFP-100)	Pin Name	Input/Output	Classification
V_{CC}	40/38	V_{CC}	—	Power supply
GND	42/40	GND	—	Power supply
V_{EE}	34/32	V_{EE}	—	Power supply
V1	37/35	V1	Input	Power supply
V5	35/33	V5	Input	Power supply
V6	36/34	V6	Input	Power supply
CL	46/44	Clock	Input	Control signal
M	44/42	M	Input	Control signal
DI	48/46	Data in	Input	Control signal
DO	32/31	Data out	Output	Control signal
SHL	41/39	Shift left	Input	Control signal
$\overline{\text{DISPOFF}}$	39/37	Display off	Input	Control signal
X_1–X_{80}	51–100, 1–30/ 1–28, 49–100	X1–X80	Output	LCD drive output
NC	31, 33, 38, 43, 45, 47, 49, 50/ 29, 30, 36, 41, 43, 45, 47, 48	No connection	—	—

Pin Functions

Power Supply

V_{CC}, V_{EE}, GND: V_{CC}–GND supplies power to the internal logic circuits. V_{CC}–V_{EE} supplies power to the LCD drive circuits.

V1, V5, V6: Supply different levels of power to drive the LCD. V1 and V_{EE} are selected levels, and V5 and V6 are non-selected levels. See figure 1.

Control Signal

CL: Inputs data shift clock pulses for the shift register. At the falling edge of each CL pulse, the shift register shifts display data input via the DI pin.

M: Changes LCD drive outputs to AC.

DI: Inputs display data. DI of the first HD66205 must be connected to an LCD controller, and those of the other HD66205s must be connected to DI of the previous HD66205.

DO: Outputs display data. DO of the last HD66205 must be open, and those of the other HD66205s must be connected to DI of the next HD66205.

SHL: Selects the data shiftt direction for the shift register. See figure 2.

$\overline{\text{DISPOFF}}$: A low $\overline{\text{DISP}}$ sets LCD drive outputs X_1–X_{80} to V1 level.

LCD Drive Output

X_1–X_{80}: Each X outputs one of the four voltage levels V1, V5, V6, or V_{EE}, depending on a combination of the M signal and display data levels. See figure 3.

Other

NC: Must be open.

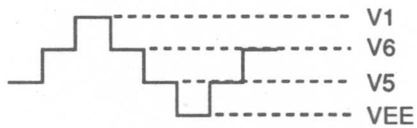


Figure 1 Different Power Supply Voltage Levels for LCD Drive Circuits

SHL level	Data shift direction	Common signal scan direction
Low	DI ➔ SR1 ➔ SR2 ➔ SR80	X1 ➔ X80
High	DI ➔ SR80 ➔ SR79 ➔ SR1	X80 ➔ X1

Figure 2 Selection of Display Data Shift Direction

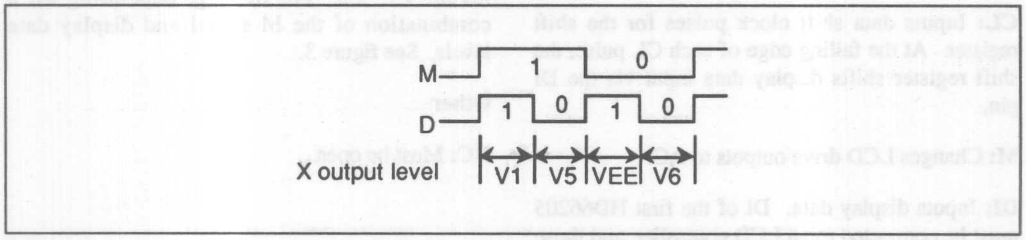


Figure 3 Selection of LCD Drive Output Level

Block Functions

LCD Drive Circuit

The 80-bit LCD drive circuit generates four voltage levels V1, V5, V6, and V_{EE}, for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on a combination of the M signal and the data in the shift register

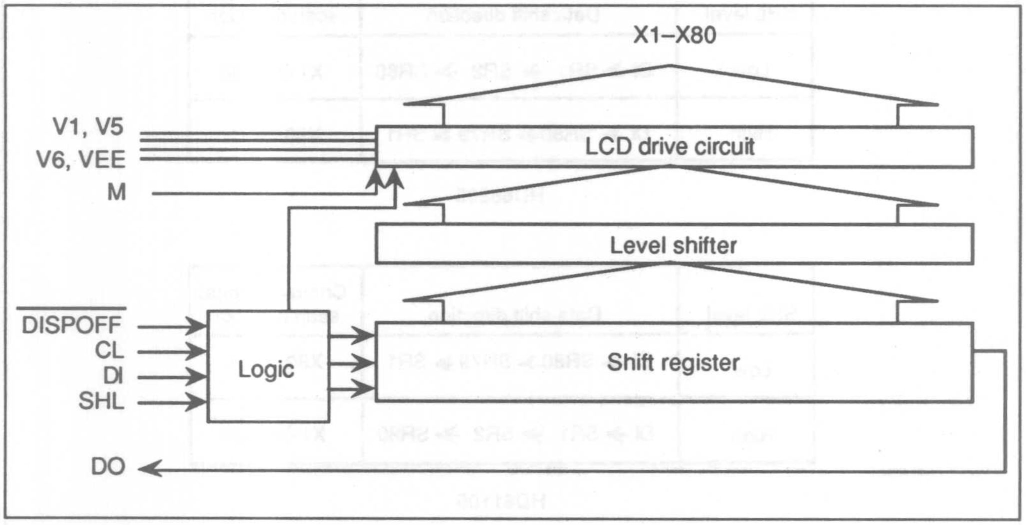
Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

Shift Register

The 80-bit shift register shifts data input via the DI pin by one bit, and the one bit of shifted-out data is output from the DO pin. Both actions occur simultaneously at the falling edge of each shift clock (CL) pulse

Block Diagram



Comparison of the HD66205 with the HD61105

Item	HD66205	HD61105
Display off function	Provided	Not provided
LCD drive voltage range	10–28 V	10–26 V
Shift clock phase selection function	Not provided	Provided (FCS pin)
Relation between SHL and LCD output destinations	See figure 4	See figure 4
Relation between LCD output levels, M, and data	See figure 5	See figure 5
LCD drive V pins	V1, V5, V6 (V2 level is the same as V_{EE} level)	V1, V2, V5, V6

SHL level	Data shift direction	Common signal scan direction
Low	DI → SR1 → SR2 → SR80	X1 → X80
High	DI → SR80 → SR79 → SR1	X80 → X1

HD66205

SHL level	Data shift direction	Common signal scan direction
Low	DI → SR80 → SR79 → SR1	X80 → X1
High	DI → SR1 → SR2 → SR80	X1 → X80

HD61105

Note the exact reverse relation for the two devices.

Figure 4 Relation between SHL and LCD Output Destinations for the HD66205 and HD61105

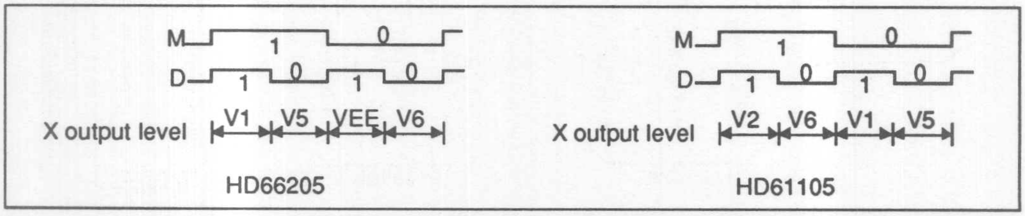


Figure 5 Relation between LCD Output Levels, M, and Data for the HD66205 and HD61105

Operation Timing

Figure 6 shows the operation timing for the Application Example.

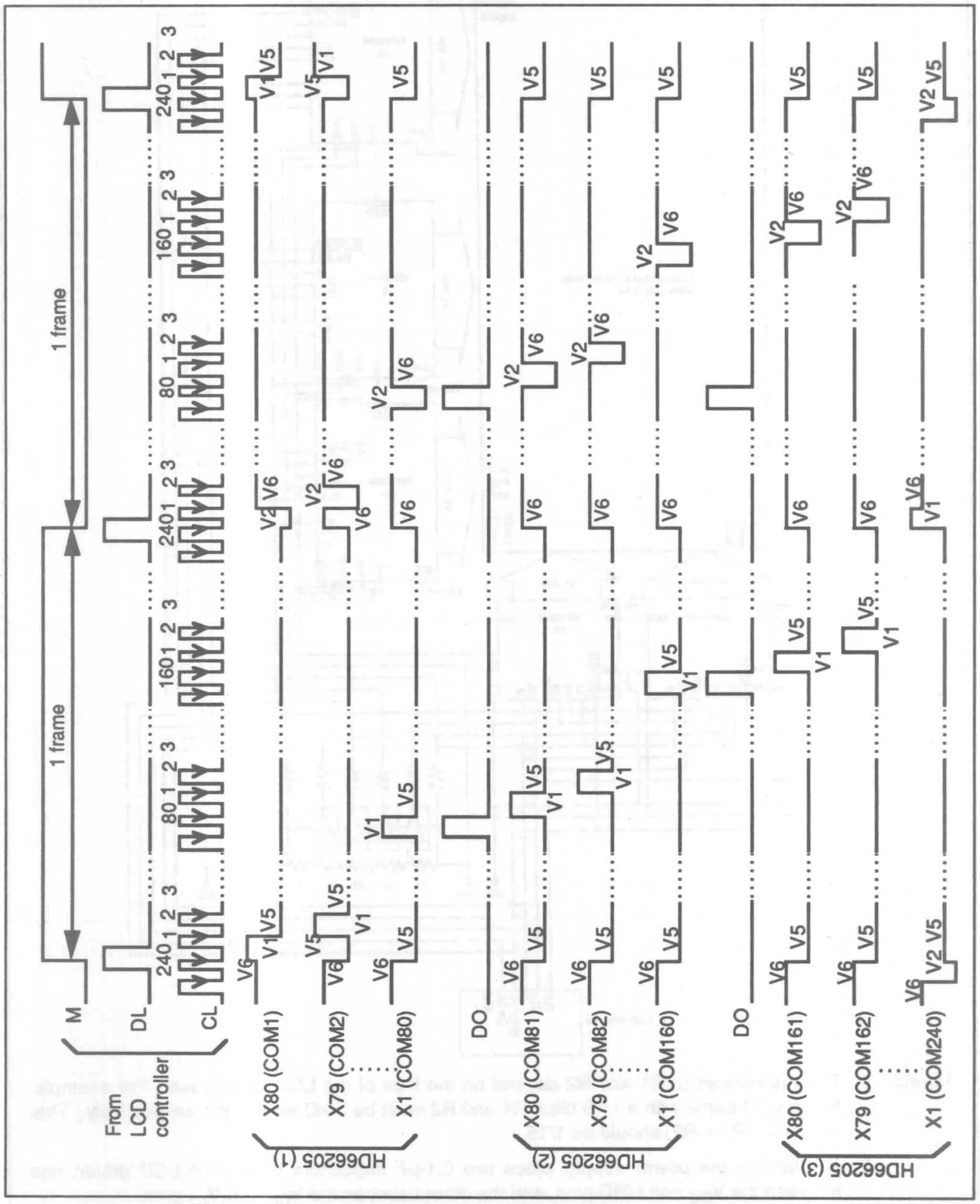
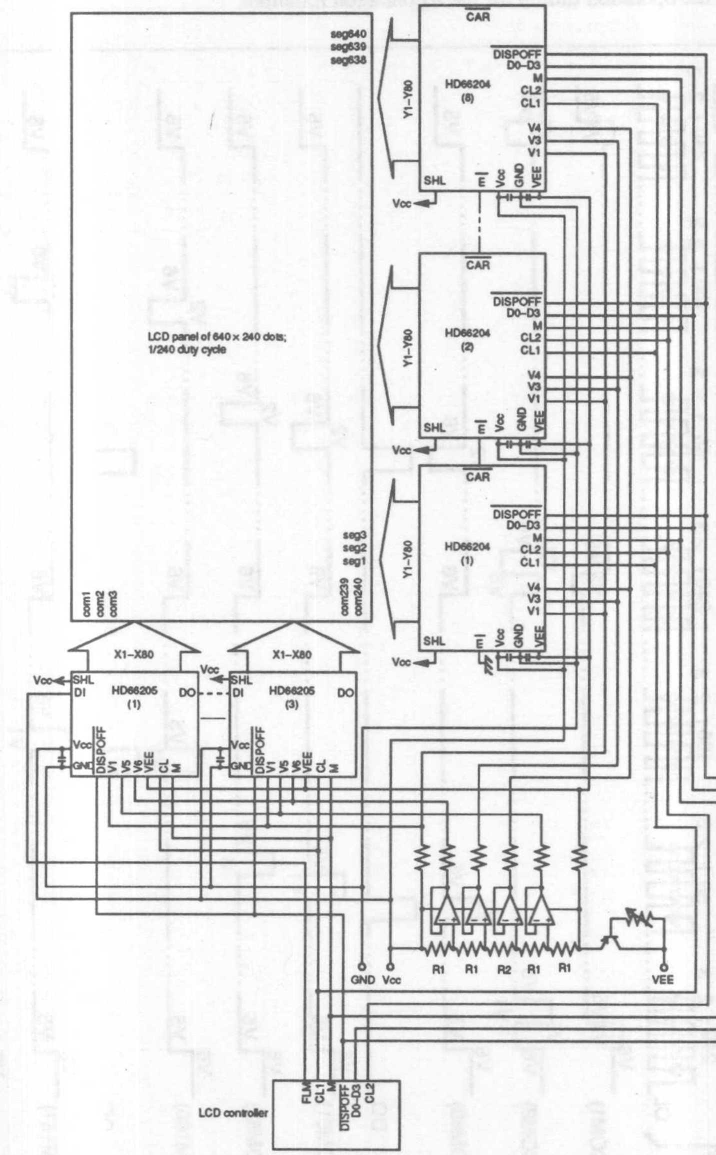


Figure 6 Relation between SHL and LCD Output Destinations

Application Example



Notes: 1. The resistances of R1 and R2 depend on the type of the LCD panel used. For example, for an LCD panel with a 1/15 bias, R1 and R2 must be 3 kΩ and 33 kΩ, respectively. That is, R1/(4 • R1 + R2) should be 1/15.

2. To stabilize the power supply, place two 0.1-µF capacitors near each LCD driver: one between the V_{CC} and GND pins, and the other between the V_{CC} and V_{EE} pins.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1
Power supply voltage for LCD drive circuits	V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3	V	
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	1, 3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	4

Notes:
1. The reference point is GND (0 V).
2. Applies to pins CL, M, SHL, DI, $\overline{DISPOFF}$.
3. Applies to pins V1, V5, and V6.
4. –40 to +125°C for TCP devices.
5. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

Electrical Characteristics

DC Characteristics for the HD66205F/HD66205TF (V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – V_{EE} = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Typ.	Max.	Unit	Condition	Notes
Input high voltage	V_{IH}	1	0.7 × V_{CC}	—	V_{CC}	V		
Input low voltage	V_{IL}	1	0	—	0.3 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	—	2.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	—	1.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	—	25	µA	V_{IN} = V_{CC} to V_{EE}	
Current consumption 1	I_{GND}	—	—	—	100	µA	f_{CL} = 20 kHz V_{CC} – V_{EE} = 28 V	2
Current consumption 2	I_{EE}	—	—	150	500	µA	Same as above	2

Pins and notes on next page.

DC Characteristics for the HD66204FL/HD66204TFL/HD66204T (V_{CC} = 2.7 to 5.5 V, GND = 0 V, $V_{CC} - V_{EE}$ = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Condition	Notes
Input high voltage	V_{IH}	1	0.7 × V_{CC}	V_{CC}	V		
Input low voltage	V_{IL}	1	0	0.3 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	2.0	kΩ	I_{ON} = 100 mA	1
Input leakage current 1	I_{IL1}	1	–1.0	1.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	25	µA	V_{IN} = V_{CC0} to V_{EE}	
Current consumption 1	I_{GND}	—	—	100	µA	f_{CL} = 16.8 kHz f_M = 35 Hz V_{CC} = 3.0 V $V_{CC} - V_{EE}$ = 28 V	2
Current consumption 2	I_{EE}	—	—	250	µA	Same as above	2

Pins:
1. CL, M, SHL, DI, $\overline{\text{DISPOFF}}$
2. DO
3. X_1–X_{80}, V1, V5, V6
4. V1, V5, V6

Notes:
1. Indicates the resistance between one pin from X_1–X_{80} and another pin from V1, V5, V6, and V_{EE}, when load current is applied to the X pin; defined under the following conditions.

   $V_{CC} - V_{EE}$= 28 V

   V1, V6 = $V_{CC} - \{1/10(V_{CC} - V_{EE})\}$

   V5 = $V_{EE} + \{1/10(V_{CC} - V_{EE})\}$

   V1 and V6 should be near V_{CC} level, and V5 should be near V_{EE} level (figure 7). All voltage must be within ΔV. ΔV is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage V_{CC}–V_{EE} (figure 8).
2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.
3. Applies to standby mode.

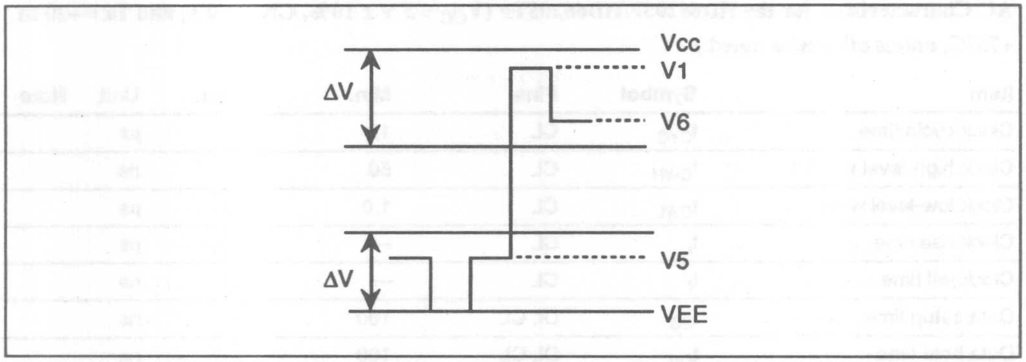


Figure 7 Relation between Driver Output Waveform and Level Voltages

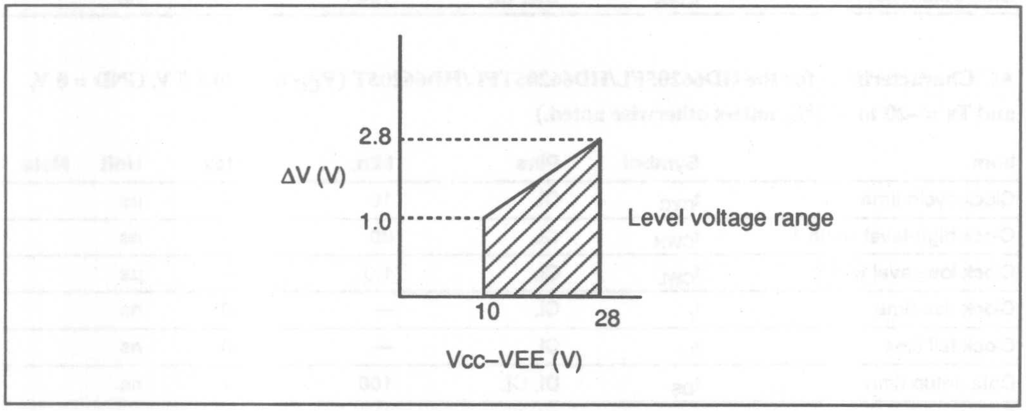


Figure 8 Relation between $V_{CC} - V_{EE}$ and ΔV

AC Characteristics for the HD66205F/HD66205TF (V_{CC} = 5 V ± 10%, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL	10	—	µs	
Clock high-level width 1	t_{CWH}	CL	50	—	ns	
Clock low-level width	t_{CWL}	CL	1.0	—	µs	
Clock rise time	t_r	CL	—	30	ns	
Clock fall time	t_f	CL	—	30	ns	
Data setup time	t_{DS}	DI, CL	100	—	ns	
Data hold time	t_{DH}	DI, CL	100	—	ns	
Data output delay time	t_{DD}	DO, CL	—	3.0	µs	1
Data output hold time	t_{DHW}	DO, CL	100	—	ns	

AC Characteristics for the HD66205FL/HD66205TFL/HD66205T (V_{CC} = 2.7 to 5.5 V, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL	10	—	µs	
Clock high-level width 1	t_{CWH}	CL	80	—	ns	
Clock low-level width	t_{CWL}	CL	1.0	—	µs	
Clock rise time	t_r	CL	—	30	ns	
Clock fall time	t_f	CL	—	30	ns	
Data setup time	t_{DS}	DI, CL	100	—	ns	
Data hold time	t_{DH}	DI, CL	100	—	ns	
Data output delay time	t_{DD}	DO, CL	—	7.0	µs	1
Data output hold time	t_{DHW}	DO, CL	100	—	ns	

Notes: 1. The load circuit shown in figure 9 is connected.

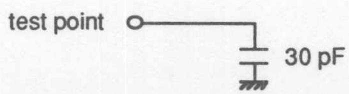


Figure 9 Load Circuit

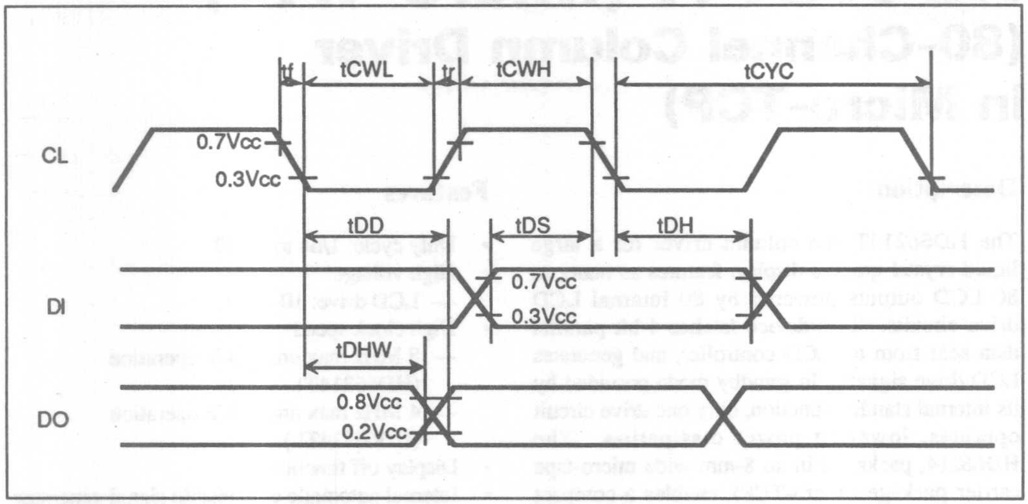


Figure 10 LCD Controller Interface Timing

HD66214T (Micro-TAB)
(80-Channel Column Driver in Micro-TCP)

Description

The HD66214T, the column driver for a large liquid crystal graphic display, features as many as 80 LCD outputs powered by 80 internal LCD drive circuits. This device latches 4-bit parallel data sent from an LCD controller, and generates LCD drive signals. In standby mode provided by its internal standby function, only one drive circuit operates, lowering power dissipation. The HD66214, packaged in an 8-mm-wide micro-tape carrier package (micro-TCP), enables a compact LCD system with a narrower frame (peripheral areas for LCD drivers) —about half as large as that os an existing system. The HD66214T is a low power dissipation device powered by 2.7–5.5 V suitable for battery-driven portable equipment such as notebook personal computers and palm-top personal computers.

Features

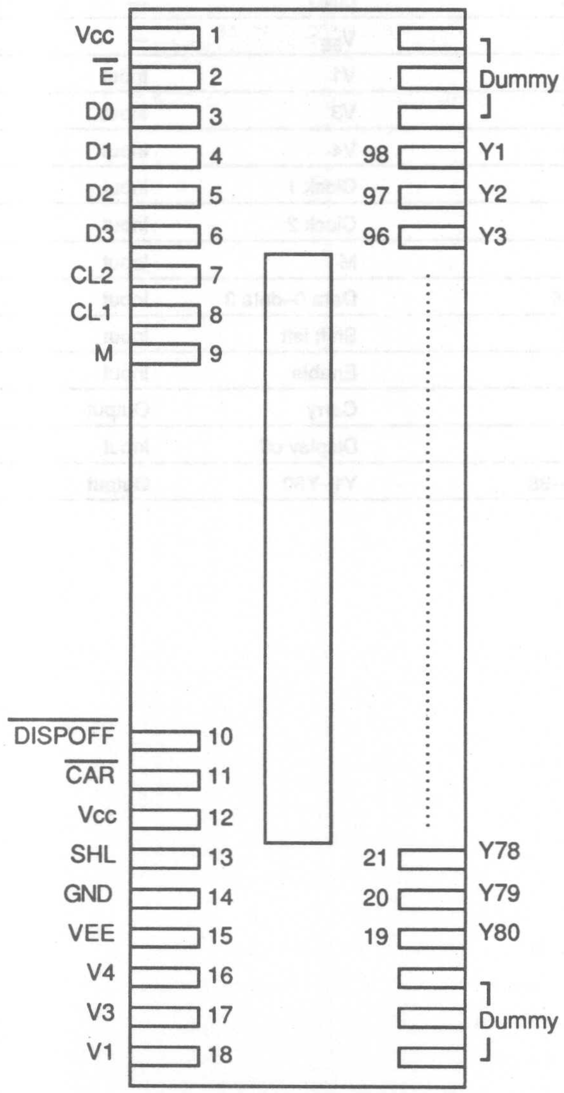
- Duty cycle: 1/64 to 1/240
- High voltage
  - — LCD drive: 10–28 V
- High clock speed
  - — 8 MHz max under 5-V operation (HD66214T)
  - — 4 MHz max under 3-V operation (HD66214TL)
- Display off function
- Internal automatic chip enable signal generator
- Various LCD controller interfaces
  - — LCTC series: HD63645, HD64645, HD64646
  - — LVIC series: HD66840, HD66841
  - — CLINE: HD66850
- 98–pin TCP

Ordering Information

Type No.	Voltage Range	Outer Lead Pitch 1	Outer Lead Pitch 2	Device Length
HD66214TA1	2.7–5.5 V	0.15 mm	0.80 mm	3 sprocket holes
HD66214TA2	2.7–5.5 V	0.18 mm	0.80 mm	3 sprocket holes
HD66214TA3	2.7–5.5 V	0.20 mm	0.80 mm	3 sprocket holes
HD66214TA6	2.7–5.5 V	0.20 mm	0.45 mm	3 sprocket holes
HD66214TA9L	2.7–5.5 V	0.22 mm	0.45 mm	2 sprocket holes

Notes:
1. Outer lead pitch 1 is for LCD drive output pins, and outer lead pitch 2 for the other pins.
2. Device length includes test pad areas.
3. Spacing between two sprocket holes is 4.75 mm.
4. Tape film is Upirex (a trademark of Ube Industries, Ltd.).
5. 35-mm-wide tape is used.
6. Leads are plated with Sn.
7. The details of TCP pattern are shown in " The Information of TCP. "

Pin Arrangement



Top view

Pin Description

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{CC}	1, 12	V_{CC}	—	Power supply
GND	14	GND	—	Power supply
V_{EE}	15	V_{EE}	—	Power supply
V1	18	V1	Input	Power supply
V3	17	V3	Input	Power supply
V4	16	V4	Input	Power supply
CL1	8	Clock 1	Input	Control signal
CL2	7	Clock 2	Input	Control signal
M	9	M	Input	Control signal
D_0–D_3	3–6	Data 0–data 3	Input	Control signal
SHL	13	Shift left	Input	Control signal
$\overline{E}$	2	Enable	Input	Control signal
$\overline{CAR}$	11	Carry	Output	Control signal
$\overline{DISPOFF}$	10	Display off	Input	Control signal
Y_1–Y_{80}	19–98	Y1–Y80	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, V_{EE}, GND: V_{CC}–GND supplies power to the internal logic circuits. Vcc–VEE supplies power to the LCD drive circuits.

V1, V3, V4: Supply different levels of power to drive the LCD. V1 and V_{EE} are selected levels, and V3 and V4 are non-selected levels. See figure 1.

Control Signal

CL1: Inputs display data latch pulses for the line data latch circuit. The line data latch circuit latches display data input from the 4-bit latch circuit, and outputs LCD drive signals corresponding to the latched data, both at the falling edge of each CL1 pulse.

CL2: Inputs display data latch pulses for the 4-bit latch circuit. The 4-bit latch circuit latches display data input via D_0–D_3 at the falling edge of each CL2 pulse.

M: Changes LCD drive outputs to AC.

D_0–D_3: Input display data. High-voltage level of data corresponds to a selected level and turns an LCD pixel on, and low-voltage level data corresponds to a non-selected level and turns an LCD pixel off.

SHL: Shifts the destinations of display data output. See figure 2.

$\overline{E}$: A low $\overline{E}$ enables the chip, and a high $\overline{E}$ disables the chip.

$\overline{CAR}$: Outputs the $\overline{E}$ signal to the next HD66214 if HD66214s are connected in cascade.

$\overline{DISPOFF}$: A low $\overline{DISP}$ sets LCD drive outputs Y_1–Y_{80} to V1 level.

LCD Drive Output

Y_1–Y_{80}: Each Y outputs one of the four voltage levels V1, V3, V4, or V_{EE}, depending on a combination of the M signal and display data levels. See figure 3.

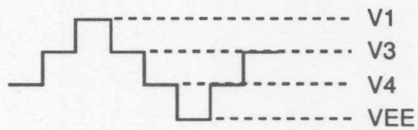


Figure 1 Different Power Supply Voltage Levels for LCD Drive Circuits

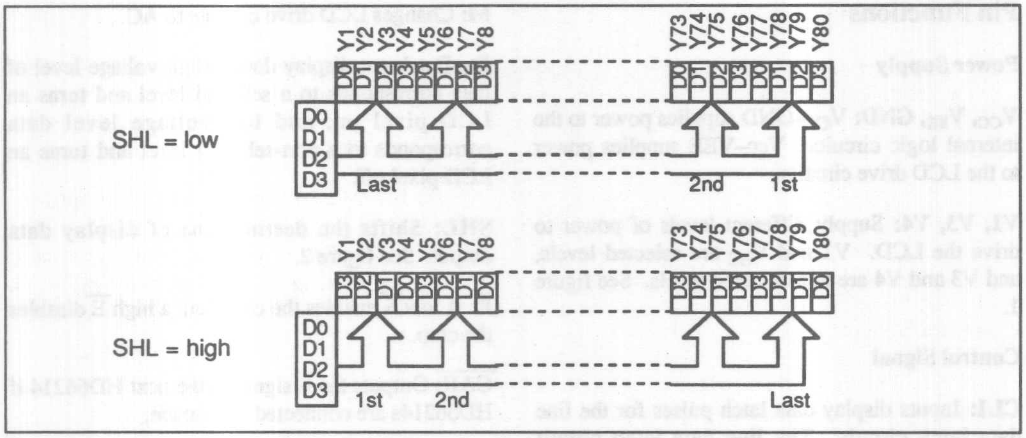


Figure 2 Selection of Destinations of Display Data Output

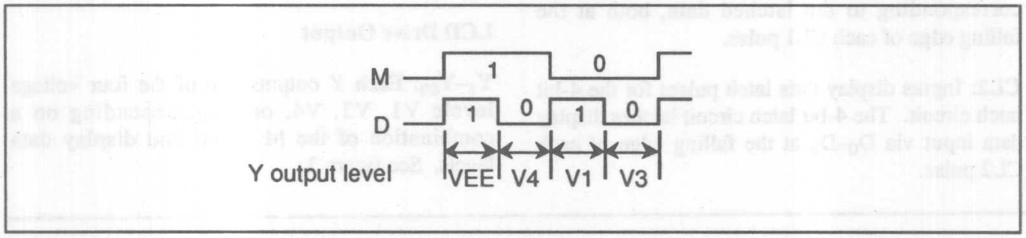


Figure 3 Selection of LCD Drive Output Level

Block Functions

Controller: The controller generates the latch signal at the falling edge of each CL2 pulse for the 4-bit latch circuit.

4-Bit Latch Circuit

The 4-bit latch circuit latches 4-bit parallel data input via the D0 to D3 pins at the timing generated by the control circuit.

Line Data Latch Circuit

The 80-bit line data latch circuit latches data input from the 4-bit latch circuit, and outputs the latched data to the level shifter, both at the falling edge of each clock 1 (CL1) pulse.

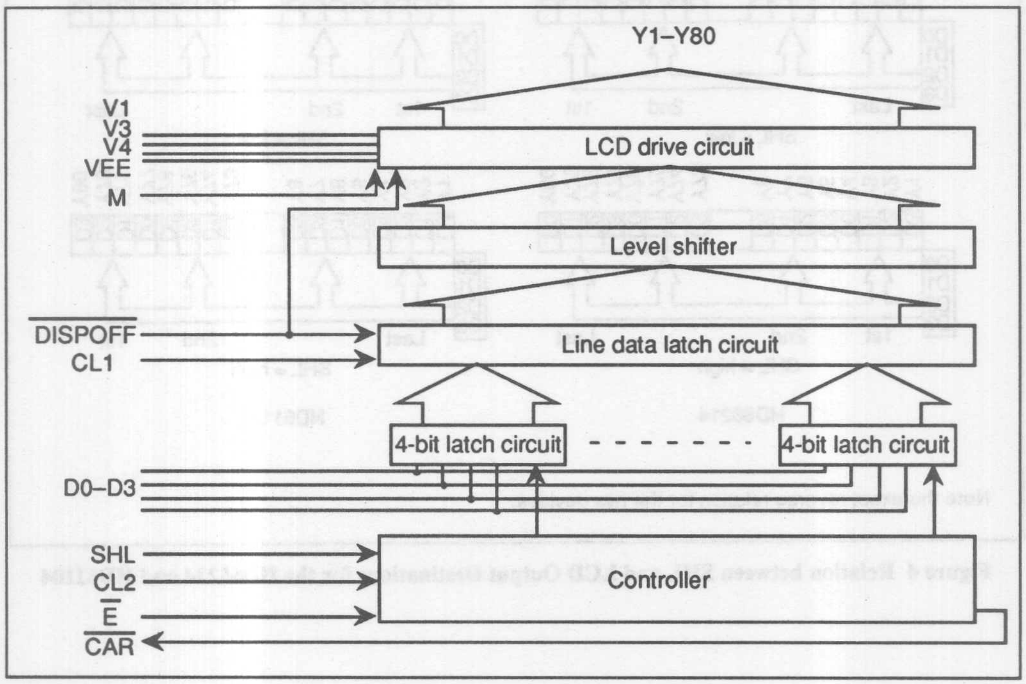
Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

LCD Drive Circuit

The 80-bit LCD drive circuit generates four voltage levels V1, V3, V4, and VEE, for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on a combination of the M signal and the data in the line data latch circuit.

Block Diagram



Comparison of the HD66214 with the HD61104

Item	HD66214	HD61104
Clock speed	8.0 MHz max.	3.5 MHz max.
Display off function	Provided	Not provided
LCD drive voltage range	10–28 V	10–26 V
Relation between SHL and LCD output destinations	See figure 4	See figure 4
Relation between LCD output levels, M, and data	See figure 5	See figure 5
LCD drive V pins	V1, V3, V4 (V2 level is the same as VEE level)	V1, V2, V3, V4
Storage temperature	–40 to 125°C	–55 to 125°C
Package	TCP (tape carrier package)	QFP (quad flat package)

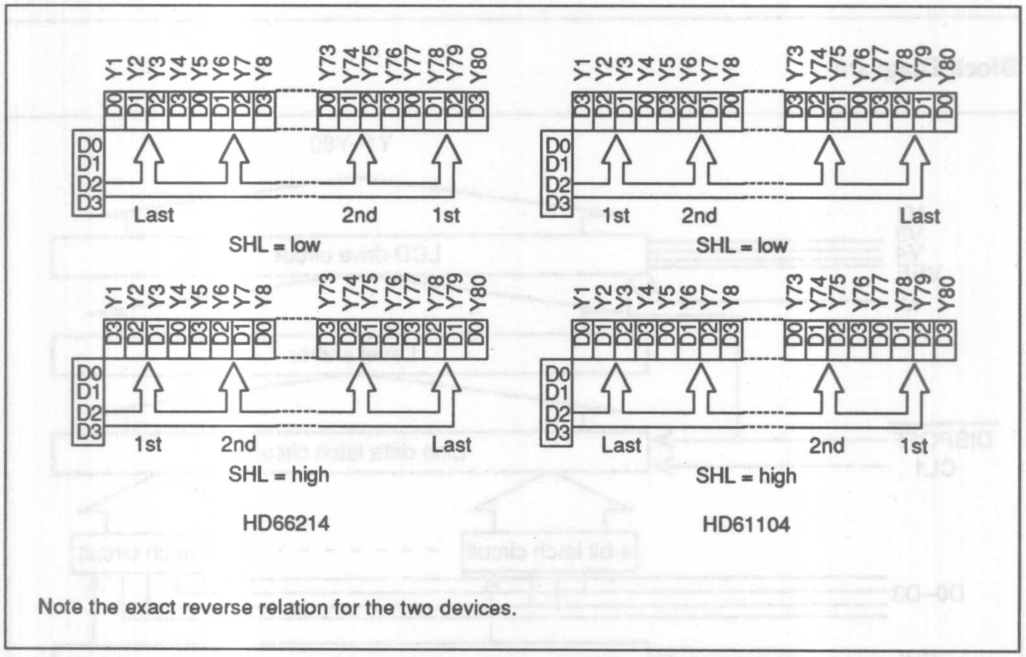


Figure 4 Relation between SHL and LCD Output Destinations for the HD66214 and HD61104

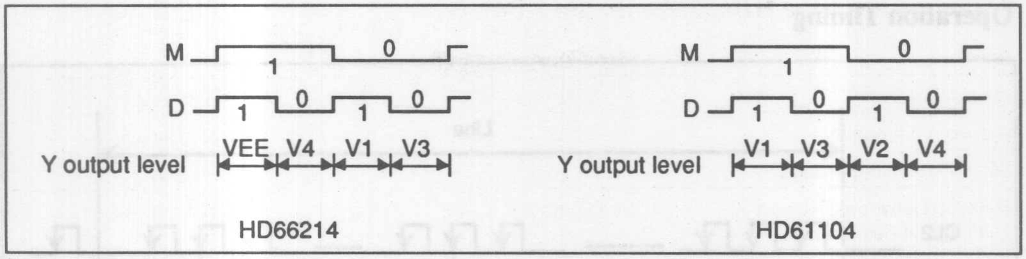
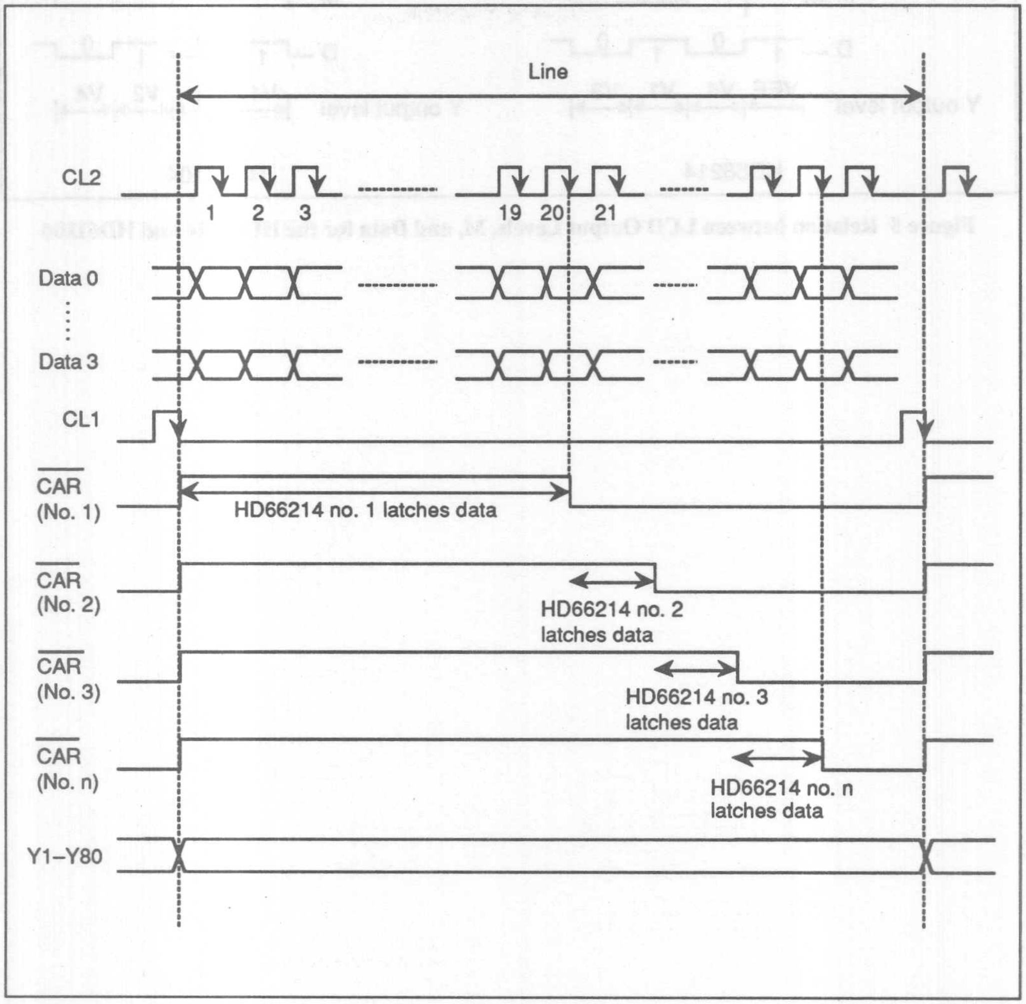
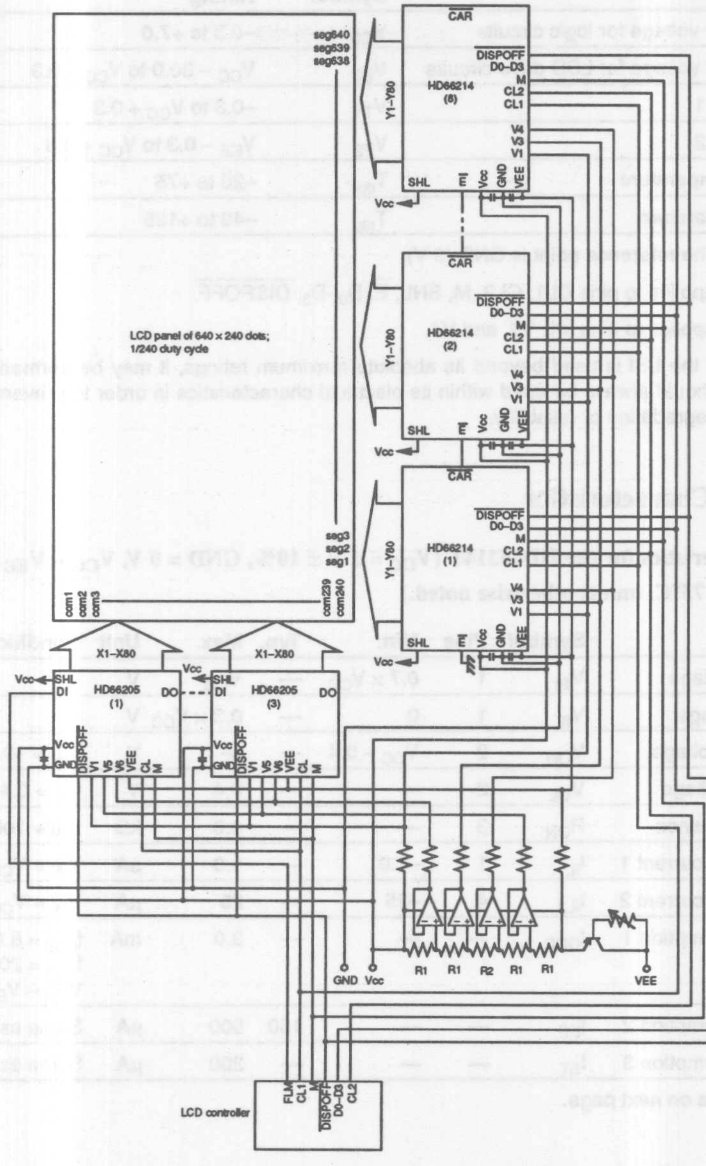


Figure 5 Relation between LCD Output Levels, M, and Data for the HD66214 and HD61104

Operation Timing



Application Example



Notes: 1. The resistances of R1 and R2 depend on the type of the LCD panel used. For example, for an LCD panel with a 1/15 bias, R1 and R2 must be 3 kΩ and 33 kΩ, respectively. That is, R1/(4 • R1 + R2) should be 1/15.

2. To stabilize the power supply, place two 0.1-µF capacitors near each LCD driver: one between the V_{CC} and GND pins, and the other between the V_{CC} and V_{EE} pins.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1
Power supply voltage for LCD drive circuits	V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3	V	
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	1, 3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

Notes:
1. The reference point is GND (0 V).
2. Applies to pins CL1, CL2, M, SHL, $\overline{E}$, D_0–D_3, $\overline{DISPOFF}$.
3. Applies to pins V1, V3, and V4.
4. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

Electrical Characteristics

DC Characteristics for the HD66214T (V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – V_{EE} = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Typ.	Max.	Unit	Condition	Notes
Input high voltage	V_{IH}	1	0.7 × V_{CC}	—	V_{CC}	V		
Input low voltage	V_{IL}	1	0	—	0.3 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	—	4.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	—	1.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	—	25	µA	V_{IN} = V_{CC} to V_{EE}	
Current consumption 1	I_{GND}	—	—	—	3.0	mA	f_{CL2} = 8.0 MHz f_{CL1} = 20 kHz V_{CC} – V_{EE} = 28 V	2
Current consumption 2	I_{EE}	—	—	150	500	µA	Same as above	2
Current consumption 3	I_{ST}	—	—	—	200	µA	Same as above	2, 3

Pins and notes on next page.

DC Characteristics for the HD66214T (V_{CC} = 2.7 to 5.5 V, GND = 0 V, $V_{CC} - V_{EE}$ = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Condition	Notes
Input high voltage	V_{IH}	1	$0.7 \times V_{CC}$	V_{CC}	V		
Input low voltage	V_{IL}	1	0	$0.3 \times V_{CC}$	V		
Output high voltage	V_{OH}	2	$V_{CC} - 0.4$	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	4.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	1.0	µA	$V_{IN} = V_{CC}$ to GND	
Input leakage current 2	I_{IL2}	4	–25	25	µA	$V_{IN} = V_{CC}$ to V_{EE}	
Current consumption 1	I_{GND}	—	—	1.0	mA	f_{CL2} = 4.0 MHz f_{CL1} = 16.8 kHz f_M = 35 Hz V_{CC} = 3.0 V $V_{CC} - V_{EE}$ = 28 V Checker-board pattern	2
Current consumption 2	I_{EE}	—	—	500	µA	Same as above	2
Current consumption 3	I_{ST}	—	—	50	µA	Same as above	2, 3

Pins:
1. CL1, CL2, M, SHL, $\overline{E}$, D_0–D_3, $\overline{DISPOFF}$
2. $\overline{CAR}$
3. Y_1–Y_{80}, V1, V3, V4
4. V1, V3, V4

Notes:
1. Indicates the resistance between one pin from Y_1–Y_{80} and another pin from V1, V3, V4, and V_{EE}, when load current is applied to the Y pin; defined under the following conditions.

   V_{CC} – GND = 28 V

   V1, V3 = $V_{CC} - \{2/10(V_{CC} - V_{EE})\}$

   V4 = $V_{EE} + \{2/10(V_{CC} - V_{EE})\}$

   V1 and V3 should be near Vcc level, and V4 should be near V_{EE} level (figure 6). All voltage must be within ΔV. ΔV is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage V_{CC}–V_{EE} (figure 7).
2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.
3. Applies to standby mode.

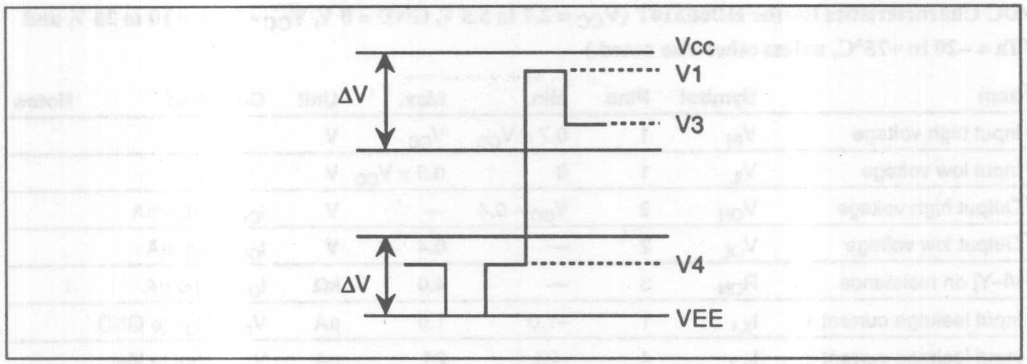


Figure 6 Relation between Driver Output Waveform and Level Voltages

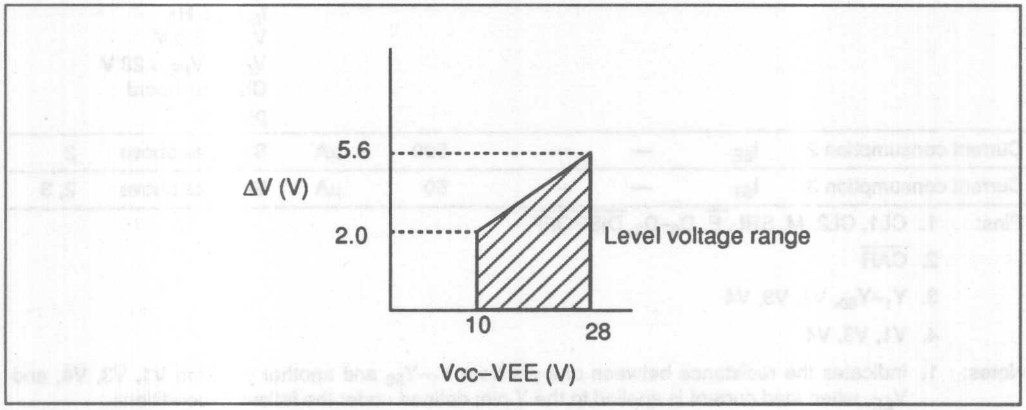


Figure 7 Relation between $V_{CC} - V_{EE}$ and ΔV

AC Characteristics for the HD66214T (V_{CC} = 5 V ± 10%, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Notes
Clock cycle time	t_{CYC}	CL2	125	—	ns	
Clock high-level width 1	t_{CWH}	CL1, CL2	45	—	ns	
Clock low-level width	t_{CWL}	CL2	45	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	80	—	ns	
Clock rise time	t_r	CL1, CL2	—	*1	ns	1
Clock fall time	t_f	CL1, CL2	—	*1	ns	1
Data setup time	t_{DS}	D_0–D_3, CL2	20	—	ns	
Data hold time	t_{DH}	D_0–D_3, CL2	20	—	ns	
Enable ($\overline{E}$) setup time	t_{ESU}	$\overline{E}$, CL2	30	—	ns	
Carry ($\overline{CAR}$) output delay time	t_{CAR}	$\overline{CAR}$, CL2	—	80	ns	2
M phase difference time	t_{CM}	M, CL2	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	

AC Characteristics for the HD66214T (V_{CC} = 2.7 to 5.5 V, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Notes
Clock cycle time	t_{CYC}	CL2	250	—	ns	
Clock high-level width 1	t_{CWH}	CL1, CL2	95	—	ns	
Clock low-level width	t_{CWL}	CL2	95	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	120	—	ns	
Clock rise time	t_r	CL1, CL2	—	*1	ns	1
Clock fall time	t_f	CL1, CL2	—	*1	ns	1
Data setup time	t_{DS}	D_0–D_3, CL2	50	—	ns	
Data hold time	t_{DH}	D_0–D_3, CL2	50	—	ns	
Enable ($\overline{E}$) setup time	t_{ESU}	$\overline{E}$, CL2	65	—	ns	
Carry ($\overline{CAR}$) output delay time	t_{CAR}	$\overline{CAR}$, CL2	—	155	ns	2
M phase difference time	t_{CM}	M, CL2	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	

Notes: 1. t_r, t_f < $(t_{CYC} - t_{CWH} - t_{CWL})/2$ and t_r, $t_f \leq 50$ ns

2. The load circuit shown in figure 8 is connected.

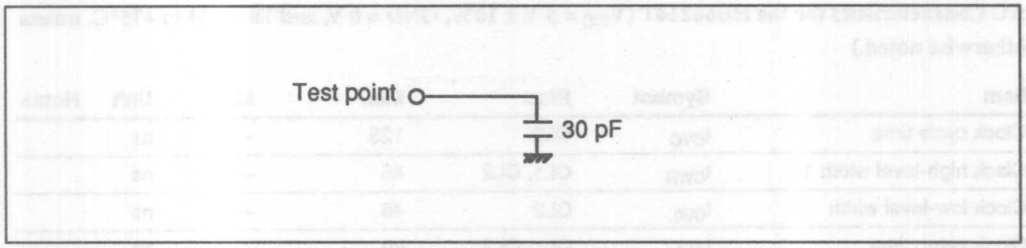


Figure 8 Load Circuit

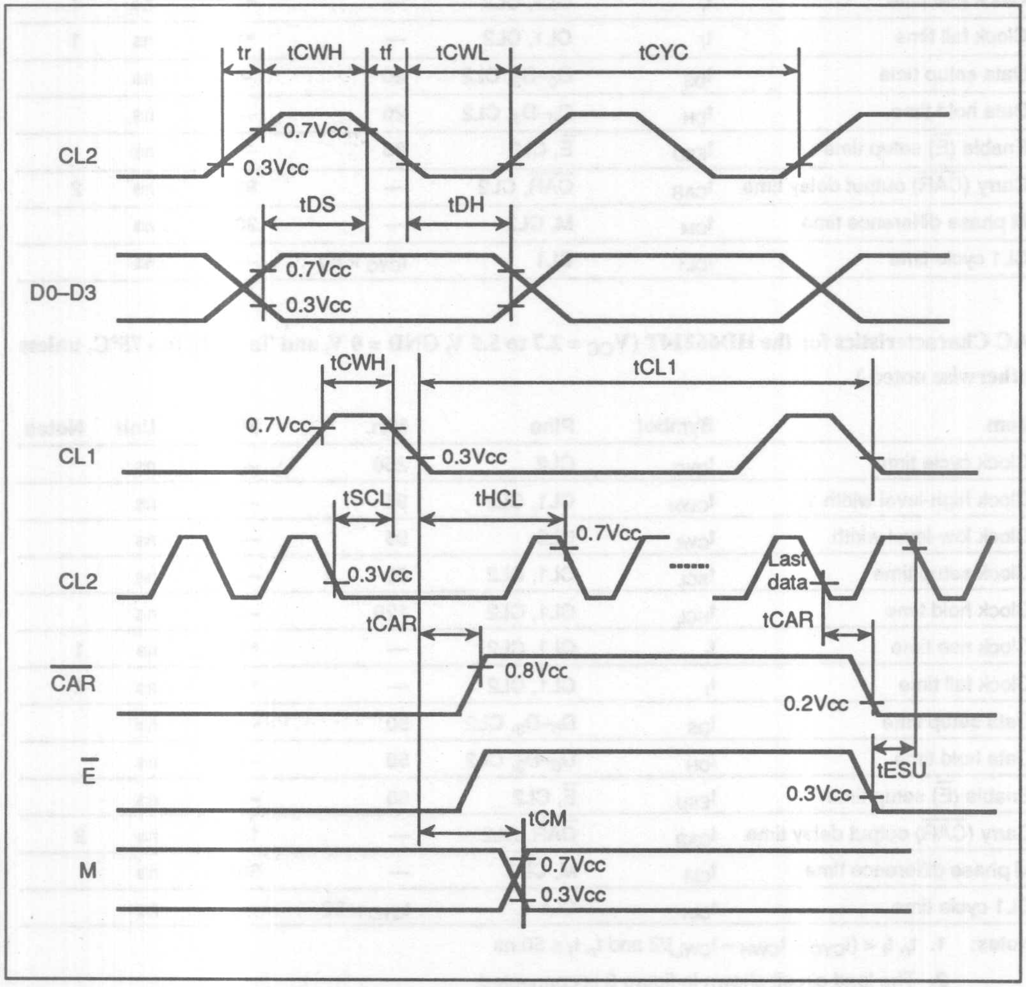


Figure 9 LCD Controller Interface Timing

HD66224T

(Dot Matrix Liquid Crystal Graphic Display Column Driver with 80-Channel Outputs)

Description

The HD66224T is a column driver for dot matrix liquid crystal graphic display ststem. It has 80 liquid crystal drive circuits and can drive large LCDs. The column driver latches parallel data for display (4/8 bit parallel) from the controller, then generates a drive signal and selects the proper LCD drive voltage. A built-in standby function that allows all internal drivers except one to be placed in standby mode (IST) lowers device power consumption. The column driver package is a 7.5-mm wide ultra-small tape carrier package (TCP), allowing designs using half the frame area of conventional displays.

The column driver can be used in a wide range of battery-powered designs because its logic power supply can operate with an input voltage ranging from 2.5 to 5.5 V.

Features

- Display duty cycle: 1/64 to 1/240
- Number of liquid crystal drive circuits: 80
- Parallel data transfer: 4/8 bits
- High voltage: Drive voltage 10–28 V (absolute maximum rating 30 V)
- High-speed operation: Maximum clock speed 8 MHz (for 5 V) or 6.5 MHz (for 2.5 V)
- Logic power supply voltage: 2.5–5.5 V
- Built-in display off function
- Built-in automatic generation function for chip-enable signal
- Built-in standby function
- 107-pin TCP

Ordering Information

Type No.	Data Input	Input Format	Outer Lead Pitch (μm)
HD66224TA1	4-bit input	Straight	210
HD66224TA2	4-bit input	Straight	200
HD66224TB0	8-bit input	Straight	200

Note: The details of TCP pattern are shown in "The Information of TCP."

Internal Block Diagram

Figure 1 is a block diagram of the HD66224T.

Liquid-Crystal Drive Circuit

The LCD drive circuit selects from four available voltage levels (V_1, V_3, V_4, and V_{EE}) based on the combination of the data of latch circuit 2 and input to pin M. The circuit outputs the selected voltage to the LCDs.

Level Shifter

The level shifter circuit raises the voltage of the logic power-supply voltage to the level used for driving the LCDs.

Latch Circuit 2

The 80-bit latch circuit 2 latches data from latch circuit 1 on the falling edge of clock CL1 and outputs the data to the level shifter circuit.

Latch Circuit 1

Latch circuit 1 consists of 4/8-bit parallel data latches that store input data D_0 to D_7 when signaled by the shift register.

Control Circuit

The control circuit generates signals that fetch the data for input to latch circuit 1.

Data Rearrange Circuit

The data rearrange circuit performs left to right (SHL) inversion on data D_0 to D_7.

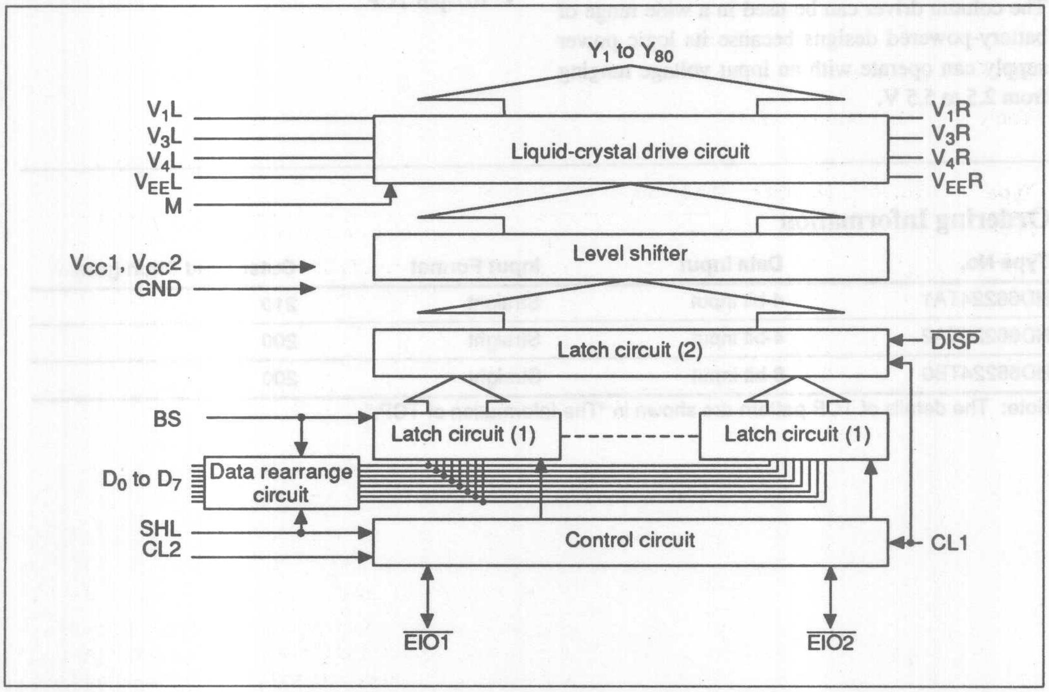
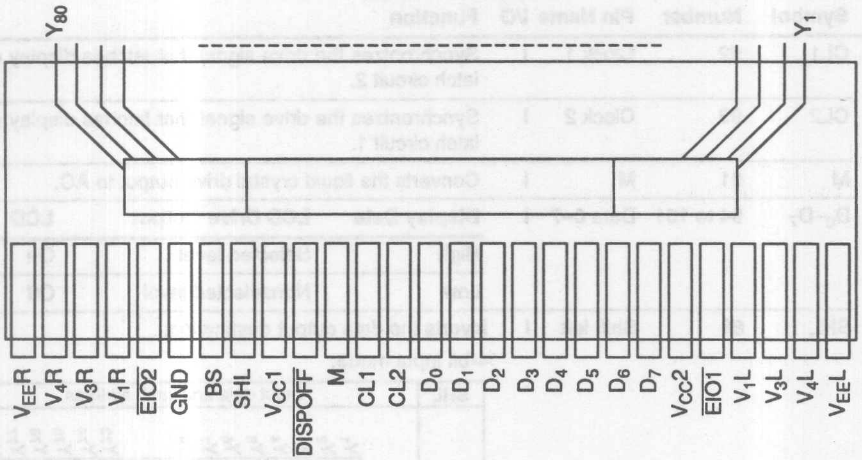


Figure 1 Block Diagram

Pin Arrangement



Note: This illustration does not correspond to the external shape of the TCP package.

Pin Description

Table 1 Pin Description

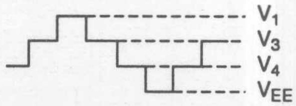
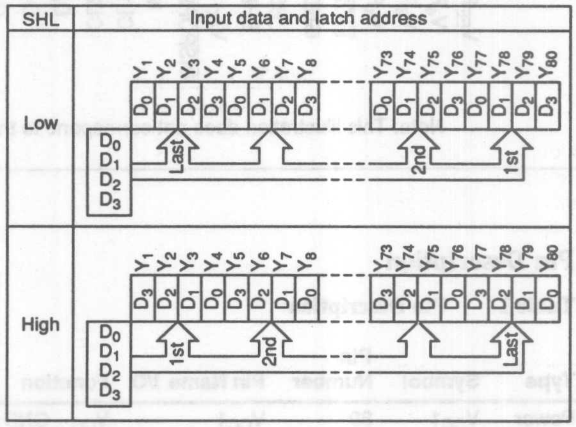
Type	Symbol	Pin Number	Pin Name	I/O	Function
Power supply	$V_{CC}1$	89	$V_{CC}1$	—	V_{CC} – GND: Connect to logic power supply.
	$V_{CC}2$	102	$V_{CC}2$		V_{CC} – V_{EE}: Connect to power supply for liquid-crystal drive circuit.
	GND	86	GND		
	$V_{EE}L$	107	$V_{EE}L$		
	$V_{EE}R$	81	$V_{EE}R$		
	V_1L	104	V_1L	I	Liquid crystal drive level power supply
	V_1R	84	V_1R		
	V_3L	105	V_3L		
	V_3R	83	V_3R		
	V_4L	106	V_4L		V_1, V_{EE}: selected level
	V_4R	82	V_4R		V_3, V_4: nonselected level
					The power supply should maintain the condition $Vcc \geq V_1 > V_3 > V_4 > V_{EE}$. The L and R sides of V_1, V_3, and V_4 are separated within the device, so the potentials externally supplied to them must be identical.

Table 1 Pin Description (cont)

Type	Symbol	Pin Number	Pin Name	I/O	Function
Control signal	CL1	92	Clock 1	I	Synchronizes the drive signal that latches display data into latch circuit 2.
	CL2	93	Clock 2	I	Synchronizes the drive signal that latches display data into latch circuit 1.
	M	91	M	I	Converts the liquid crystal drive output to AC.
	D_0–D_7	94 to 101	Data 0–7	I	**Display Data** / **LCD Drive Output** / **LCD** High / Selected level / On Low / Nonselected level / Off
	SHL	88	Shift left	I	Inverts the data output destination.

4-bit input mode:



8-bit input mode:

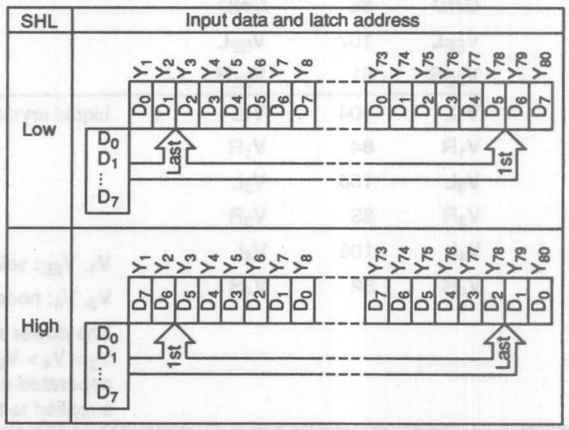
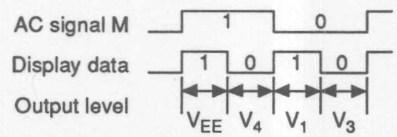


Table 1 Pin Description (cont)

Type	Symbol	Pin Number	Pin Name	I/O	Function
Control Signal (cont)	$\overline{\text{DISPOFF}}$	90	Display off	I	When the liquid crystal output nonselected level control input pin drives $\overline{\text{DISPOFF}}$ low, the liquid crystal drive output (Y_1 to Y_{80}) is set to the V1 level.
	$\overline{\text{EIO1}}$	103	Enable I/O 1	I/O	I/O pins for chip selection. Input/output is controlled by SHL input.
	$\overline{\text{EIO2}}$	85	Enable I/O 2		**SHL** / **Enable I/O 1** / **Enable I/O 2** 0 / Output / Input 1 / Input / Output When the enable input signal goes low, data fetch begins. When all data has been fetched, the enable output changes from high to low and the next stage IC starts up.
	BS	87	Bus select	I	Switches the number of input bits for the display data. When high, places the device in 8-bit input mode; when low, changes the device to the 4-bit input mode.
Liquid crystal drive output	Y_1 to Y_{80}	1 to 80	Y_1 to Y_{80}	O	Outputs one of the four voltage levels V_1, V_3, V_4, or V_{EE}, based on the combination of the M signal and the display data.



Note: 0 and low levels indicate ground level. High levels indicate V_{CC} level.

Sample Application

Figure 2 shows an example of an LCD panel comprised of 640 × 200 dots, using the HD66224T. The recommended common driver is HD66215. For 640 × 400 dots, extend the configuration shown to configure two screens.

R1 and R2 differ depending on the LCD panel used. For a 1/15 bias, for example, R1 = 3 kΩ and R2 = 33kΩ are used so that R1(4R1 + R2) = 1/15.

When designing a board locate bypass capacitors as close to each device as possible, to stabilize the power supply. We recommend that two capacitors (of about 0.1 pF) be used with each HD66224T. One capacitor should be connected between V_{CC} and GND, and one between V_{CC} and V_{EE}.

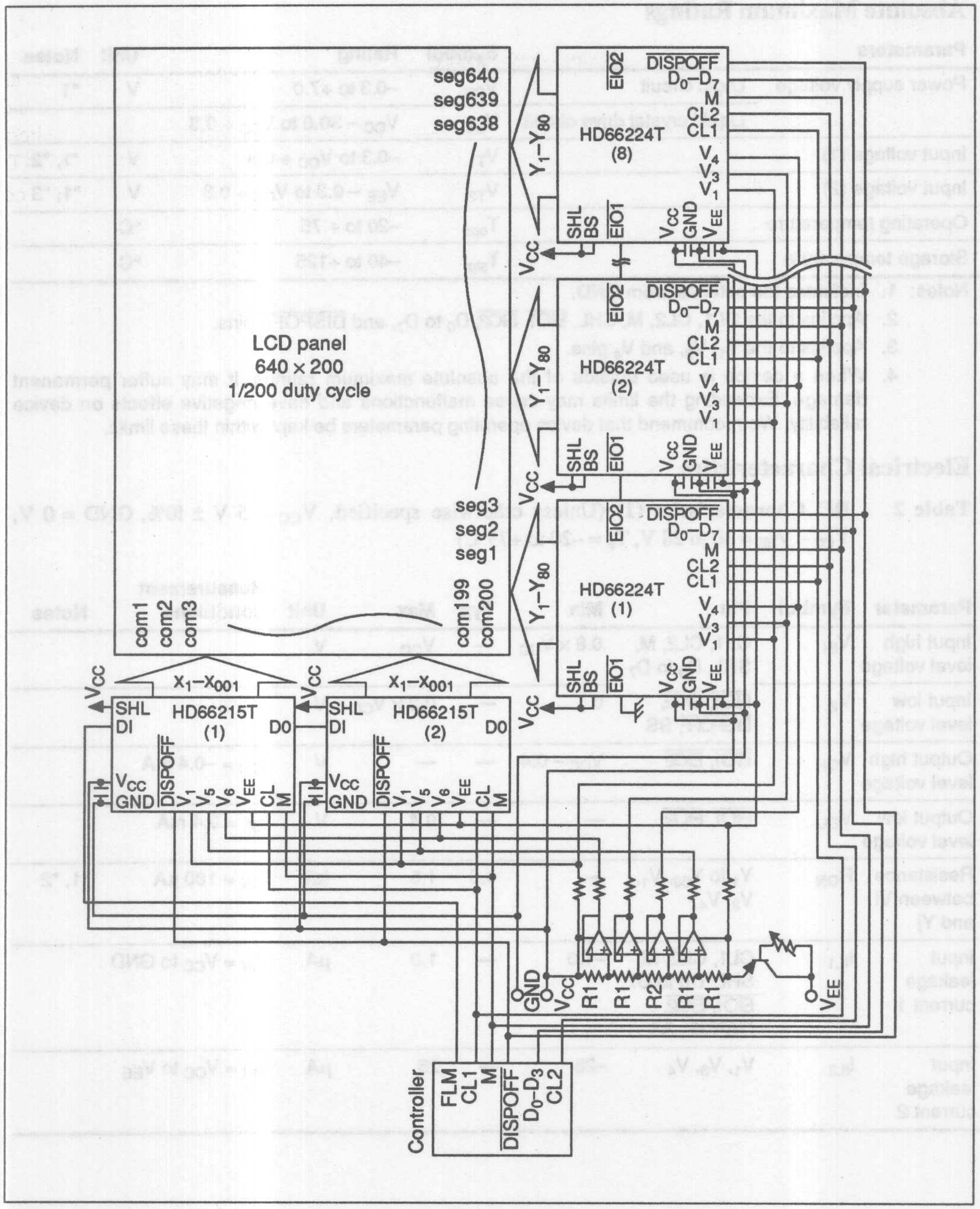


Figure 2 Application Example

Absolute Maximum Ratings

Parameters		Symbol	Rating	Unit	Notes
Power supply voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	*1
	Liquid crystal drive circuit	V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3		
Input voltage (1)		V_{T1}	–0.3 to V_{CC} + 0.3	V	*1, *2
Input voltage (2)		V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	*1, *3
Operating temperature		T_{opr}	–20 to + 75	°C	
Storage temperature		T_{stg}	–40 to +125	°C	

Notes: 1. Indicates the potential from GND.
2. Applies to the CL1, CL2, M, SHL, $\overline{EIO1}$, $\overline{EIO2}$, D_0 to D_7, and $\overline{DISPOFF}$ pins.
3. Applies to the V_1, V_3, and V_4 pins.
4. When a device is used outside of the absolute maximum ratings, it may suffer permanent damage. Exceeding the limits may cause malfunctions and have negative effects on device reliability. We recommend that device operating parameters be kept within these limits.

Electrical Characteristics

Table 2 **DC Characteristics (1)** (Unless otherwise specified, V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – V_{EE} = 10 to 28 V, T_a = –20 to +75°C)

Parameter	Symbol	Pin	Min	Typ	Max	Unit	Measurement Conditions	Notes
Input high level voltage	V_{IH}	CL1, CL2, M, SHL, D_0 to D_7	0.8 × V_{CC}	—	V_{CC}	V		
Input low level voltage	V_{IL}	$\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISPOFF}$, BS	0	—	0.2 × V_{CC}	V		
Output high level voltage	V_{OH}	$\overline{EIO1}$, $\overline{EIO2}$	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low level voltage	V_{OL}	$\overline{EIO1}$, $\overline{EIO2}$	—	—	0.4	V	I_{OL} = 0.4 mA	
Resistance between Vi and Yj	R_{ON}	Y_1 to Y_{80}, V_1, V_3, V_4	—	0.6	1.5	kΩ	I_{ON} = 100 µA	*1, *2
Input leakage current 1	I_{IL1}	CL1, CL2, M, SHL, D0 to D7, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISPOFF}$, BS	–1.0	—	1.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	V_1, V_3, V_4	–25	—	25	µA	V_{IN} = V_{CC} to V_{EE}	

Table 2 DC Characteristics (1) (cont)

Parameter	Symbol	Pin	Min	Typ	Max	Unit	Measurement Conditions	Notes
Current consumption 1	I_{GND}	—	—	—	3.0	mA	f_{CL2} = 8.0 MHz f_{CL1} = 20 kHz	*3
Current consumption 2	I_{EE}	—	—	150	500	µA	$V_{CC} - V_{EE}$ = 28 V	
Current consumption 3	I_{ST}	—	—	—	200	µA		*3, *4

Notes: 1. This is the resistance value between the Y pin and V pin (V_1, V_3, V_4, or V_{EE}) when a load current flows to one of the pins Y_1 to Y_{80}. Set with the following conditions:
$V_{CC} - V_{EE}$ = 28 V
V_1, $V_3 = V_{CC} - 2/10(V_{CC} - V_{EE})$
$V_4 = V_{EE} + 2/10(V_{CC} - V_{EE})$

2. Describes the voltage range for the liquid-crystal drive level power supply. A voltage near V_{CC} is supplied to V_1 and V_3. A voltage near V_{EE} is supplied to V4. Use within the range of ΔV for each. These ranges should be set so that the impedance ROM of the driver output obtained is stable. Note also that ΔV depends on the power supply voltage ($V_{CC} - V_{EE}$). See figure 3.
3. Excluding the current flowing to the input area and output area. When the driver uses an intermediate level for input, a through current flows to the input circuit and the power supply current increases, so be sure that $V_{IH} = V_{CC}$ and V_{IL} = GND.
4. Current during standby.

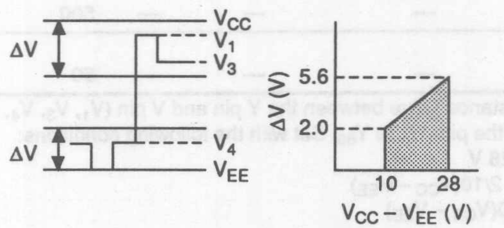


Figure 3 Relationship between Driver Output Waveform and Level Voltages

Table 3 DC Characteristics (2) (Unless otherwise specified, V_{CC} = 2.5 to 4.5 V ± 10%, GND = 0 V, V_{CC}–V_{EE} = 10–28 V, T_a = –20 to +75°C)

Parameter	Symbol	Pin	Min	Typ	Max	Unit	Measurement Conditions
Input high level voltage	V_{IH}	CL1, CL2, M, SHL, D_0 to D_7	$0.8 \times V_{CC}$	—	V_{CC}	V	—
Input low level voltage	V_{IL}	$\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISPOFF}$, BS	0	—	$0.2 \times V_{CC}$	V	—
Output high level voltage	V_{OH}	$\overline{EIO1}$, $\overline{EIO2}$	$V_{CC} - 0.4$	—	—	V	I_{OH} = –0.4 mA
Output low level voltage	V_{OL}	$\overline{EIO1}$, $\overline{EIO2}$	—	—	0.4	V	I_{OL} = 0.4 mA
Resistance between V_i and Y_j *1, *2	R_{ON}	Y_1 to Y_{80}, V_1, V_3, V_4	—	0.6	1.5	kΩ	I_{ON} = 100 µA
Input leakage current 1	I_{IL1}	CL1, CL2, M, SHL, D_0 to D_7, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISPOFF}$, BS	–1.0	—	1.0	µA	V_{IN} = V_{CC} to GND
Input leakage current 2	I_{IL2}	V_1, V_3, V_4	–25		25	µA	V_{IN} = V_{CC} to V_{EE}
Current consumption 1 *3	I_{GND}	—	—	—	1.5	mA	f_{CL2} = 6.5 MHz f_{CL1} = 16.8 kHz fm = 35 Hz V_{CC} = 3.0 V $V_{CC} - V_{EE}$ = 28 V
Current consumption 2	I_{EE}	—	—	—	500	µA	
Current consumption 3 *3, *4	I_{ST}	—	—	—	50	µA	

Notes: 1. This is the resistance value between the Y pin and V pin (V_1, V_3, V_4, or V_{EE}) when a load current flows to one of the pins Y_1 to Y_{80}. Set with the following conditions:
$V_{CC} - V_{EE}$ = 28 V
$V_1, V_3 = V_{CC} - 2/10(V_{CC} - V_{EE})$
$V_4 = V_{EE} + 2/10(V_{CC} - V_{EE})$

2. Describes the voltage range for the liquid-crystal drive level power supply. A voltage near V_{CC} is supplied to V_1 and V_3. A voltage near V_{EE} is supplied to V_4. Use within the range of ΔV for each. These ranges should be set so that the impedance ROM of the driver output obtained is stable. Note also that ΔV depends on the power supply voltage ($V_{CC} - V_{EE}$). See figure 3.
3. Excluding the current flowing to the input area and output area. When the driver uses an intermediate level for input, a through current flows to the input circuit and the power supply current increases, so be sure that V_{IH} = V_{CC} and V_{IL} = GND.
4. Current during standby.

Table 4 AC Characteristics (1) (Unless otherwise specified, V_{CC} = 5.0 V ±10%, GND = 0 V, T_a = –20 to +75 °C)

Parameter	Symbol	Pin	Min	Max	Unit
Clock cycle time	t_{CYC}	CL2	125	—	ns
Clock high level width 2	t_{CWH2}		45		
Clock low level width 2	t_{CWL2}				
Data setup time	t_{DS}	D_0 to D_7, CL2	30		
Data hold time	t_{DH}				
Clock high level width 1	t_{CWH1}	CL1	45		
CL2 rise to CL1 rise	t_{LD}	CL1, CL2	30		
CL2 fall to CL1 fall	t_{SCL}		45		
CL1 rise to CL2 rise	t_{LS}				
CL1 fall to CL2 fall	t_{HCL}				
Input signal rise time*1	t_r			50	
Input signal fall time*1	t_f				

Table 5 AC Characteristics (2) (Unless otherwise specified, V_{CC} = 2.5 V to 4.5 V, GND = 0 V, T_a = –20 to +75 °C)

Parameter	Symbol	Pin	Min	Max	Unit
Clock cycle time*2	t_{CYC}	CL2	152	—	ns
Clock high level width 2	t_{CWH2}		65		
Clock low level width 2	t_{CWL2}				
Data setup time	t_{DS}	D_0 to D_7, CL2	50		
Data hold time	t_{DH}		40		
Clock high level width 1	t_{CWH1}	CL1	65		
CL2 rise to CL1 rise	t_{LD}	CL1, CL2	20		
CL2 fall to CL1 fall	t_{SCL}		65		
CL1 rise to CL2 rise	t_{LS}				
CL1 fall to CL2 fall	t_{HCL}				
Input signal rise time*1	t_r			50	
Input signal fall time*1	t_f			50	

Notes (tables 4 and 5):

1. This is the resistance value between the Y pin and V pin (V_1, V_3, V_4, or V_{EE}) when a load current flows to one of the pins Y_1 to Y_{80}. Set with the following conditions:
   $V_{CC} - V_{EE}$ = 28 V
   $V_1, V_3 = V_{CC} - 2/10(V_{CC} - V_{EE})$
   $V_4 = V_{EE} + 2/10(V_{CC} - V_{EE})$
2. $t_r, t_f \leq 11$ ns

AC Characteristic Test Waveforms

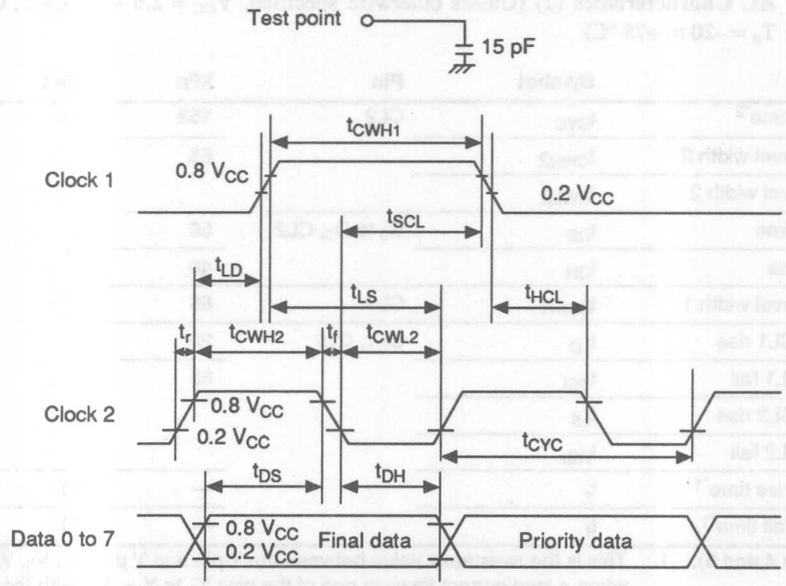
Figure 4 shows test point loading and test waveforms. Connect test points through a 15-pF capacitor to ground, as shown at the top of figure 4.

BS = GND (4-Bit Fetch Mode)

When the data fetch operation enable signal goes low (with SHL = GND and $\overline{EIO2}$ = GND), data standby is cleared. On the next rising edge of clock CL2, the standby is cleared. Figure 5 shows timing for 4-bit fetch mode operation. When CL2 falls, the first 4-bit data fetch is performed. The 4-bit fetches continue on each subsequent falling edge of CL2 until 76 bits have been fetched. The enable signal (when SHL = GND, $\overline{EIO1}$) then goes to GND level. When 80 bits have been fetched, fetch is automatically halted (standby). If the $\overline{EIO1}$ pin is connected to the $\overline{EIO2}$ pin of the next stage, the next device will begin 4-bit fetch operation.

The data output changes when CL1 falls. The output destination for the fetched data when SHL = GND is output pin Y_{80} for d_1, and Y_1 for d_{80}.

When SHL = V_{CC}, the destinations are reversed; d_{80} is output to Y_{80} and d_1 is output to Y_1. The output level (V_1 through V_4) is actually selected by the combination of the display data and AC signal M.



$$t_r, t_f < \frac{t_{CYC} - t_{CWH2} - t_{CWL2}}{2}$$

Figure 4 AC Characteristic Waveforms

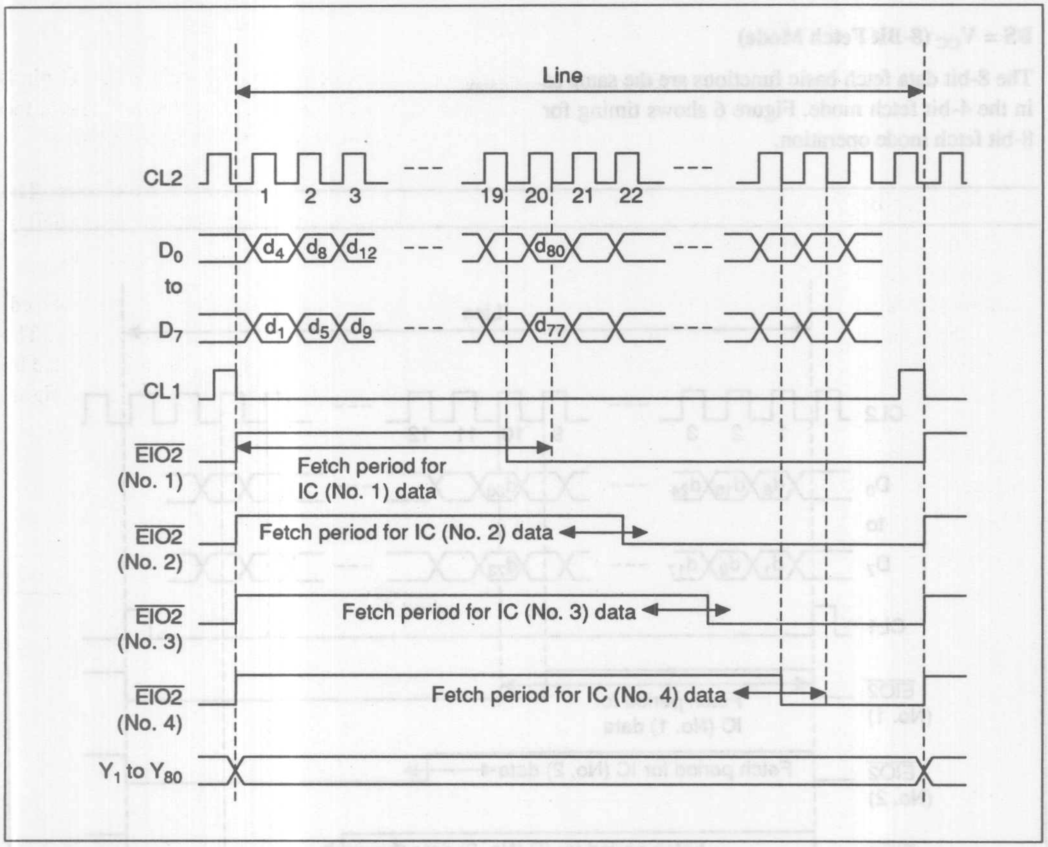


Figure 5 Operation Timing (4-Bit Fetch Mode)

BS = V_{CC} (8-Bit Fetch Mode)

The 8-bit data fetch basic functions are the same as in the 4-bit fetch mode. Figure 6 shows timing for 8-bit fetch mode operation.

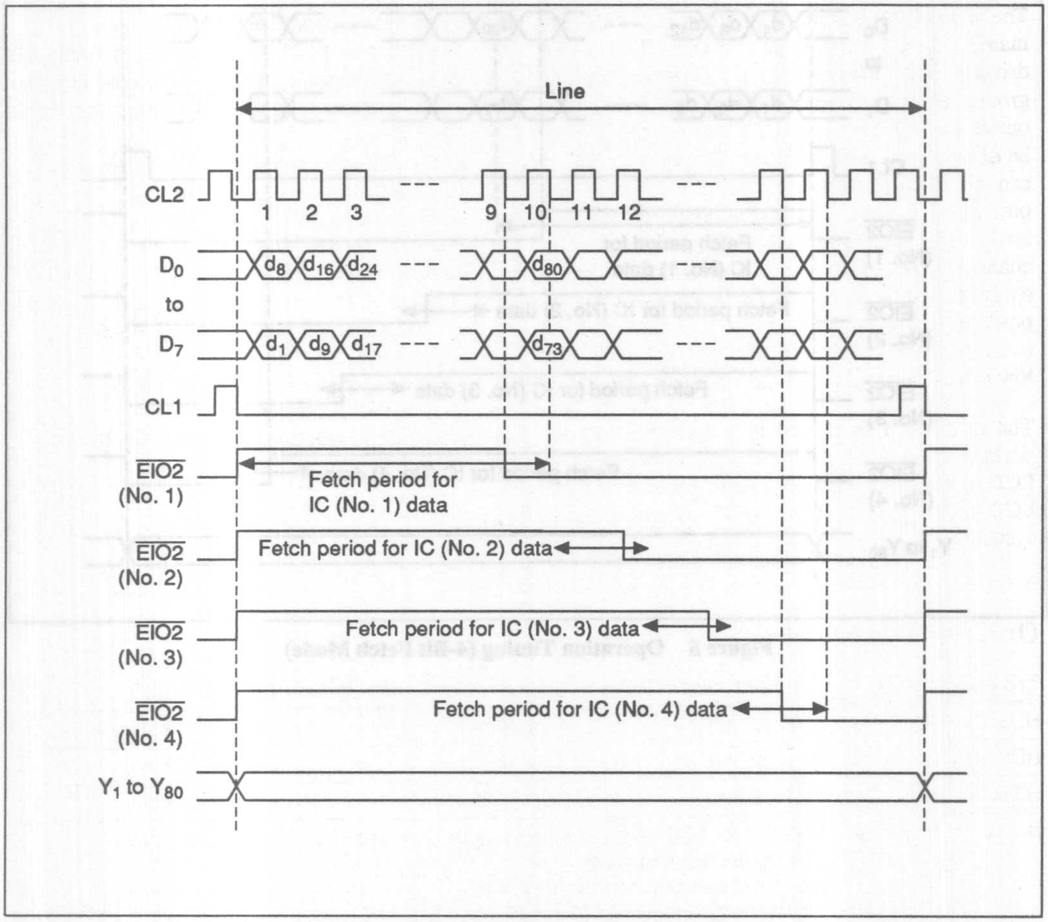


Figure 6 Operation Timing (8-Bit Fetch Mode)

HD66215T

(Common Driver for a Dot Matrix Liquid Crystal Graphic Display with 100-Channel Outputs)

Description

The HD66215T is a common driver for a large dot matrix liquid crystal graphic display (LCD). The driver's 100 channels can be divided into two groups of 50 channels by selecting data input/output pins. Outputs X_1 to X_{10} and X_{91} to X_{100} can be disabled by mode selection. Unused output pins can be equally distributed above and below the pins used for the LCD panel so that the panel can be neatly centered on the LCD board. A 101-channel output mode can also be selected for an application to various display panels. The driver is powered by about 3 V, making it suitable for battery-driven portable equipment featuring the low power dissipation of liquid crystal elements.

The HD66215T, packaged in a micro-tape carrier package (micro-TCP), allows design of a compact LCD system with a frame (an area peripheral to the LCD panel) about half the width of conventional systems.

Features

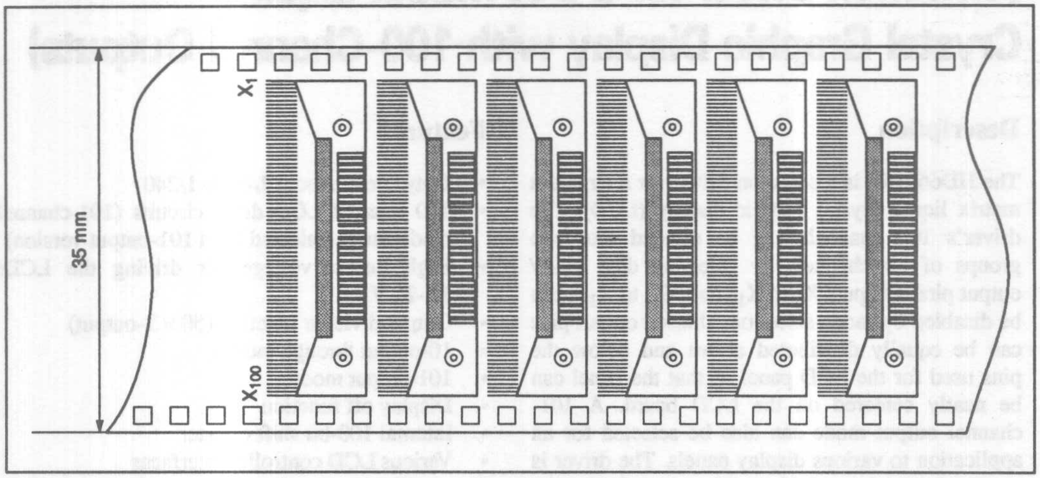
- Duty cycle: About 1/64 to 1/240
- 100 internal LCD drive circuits (101-channel mode can be selected for a 101-output version)
- High output voltage for driving the LCD: 10–28 V
- Output division function (50 × 2-output)
- 10-output through modes
- 101-output mode
- Display off function
- Internal 100-bit shift register
- Various LCD controller interfaces
  - — LCTC series: HD63645, HD64645, HD64646
  - — LVIC series: HD66840, HD66841
  - — CLINE: HD66850
- Micro-TCP with 3-sprocket-hole width
- Operating voltage: 2.5–5.5 V

Ordering Information

Type No.	Outer Lead Pitch 1	Outer Lead Pitch 2	Device Length
HD66215TA0	0.23 mm	1.20 mm	3 sprocket holes
HD66215TA1	0.22 mm	1.00 mm	3 sprocket holes
HD66215TA2	0.18 mm	0.85 mm	3 sprocket holes

Notes: 1. Outer lead pitch 1 is for LCD drive output pins, and outer lead pitch 2 for the other pins.
2. Device length includes test pad areas.
3. Spacing between two sprocket holes is 4.75 mm.
4. Tape film is Upirex (a trademark of Ube Industries, Ltd.).
5. 35-mm-wide tape is used.
6. Leads are plated with Sn.
7. The details of TCP pattern are shown in "The Information of TCP."

Tape Carrier Package



Pin Arrangement

1	V_1L
2	V_6L
3	V_5L
4	$V_{EE}L$
5	MODE1
6	DIO4
7	$\overline{\text{DISPOFF}}$
8	V_{CC}
9	SHL/R
10	DIO3
11	DIO2
12	GND
13	M
14	CL
15	DIO1
16	MODE2
17	$V_{EE}R$
18	V_5R
19	V_6R
20	V_1R

Pin Description

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{CC}	8	V_{CC}	—	Power supply
GND	12	GND		
V_1L, V_1R	1, 20	V_1L, V_1R	Input	
V_6L, V_6R	2, 19	V_6L, V_6R		
V_5L, V_5R	3, 18	V_5L, V_5R		
$V_{EE}L$, $V_{EE}R$	4, 17	$V_{EE}L$, $V_{EE}R$		
CL	14	Clock		Control signal
M	13	M		
SHL/R	9	Shift left/right		
DIO1	15	Data	Input/output	
DIO2	11			
DIO3	10			
DIO4	6			
$\overline{\text{DISPOFF}}$	7	Display off	Input	
MODE1, MODE2	5, 16	Mode1, Mode2		
X_1–X_{100}	21–120	X_1–X_{100}	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, GND: Supply power to the internal logic circuits.

V_1L, V_1R, V_5L, V_5R, V_6L, V_6R, $V_{EE}L$, $V_{EE}R$: Supply different levels of power to drive the LCD. V_1 and V_{EE} are selected levels, and V_5 and V_6 are non-selected levels. See figure 1.

Control Signals

CL: Inputs data shift clock pulses for the shift register. At the falling edge of each CL pulse, the shift register shifts data input via the DIO pins.

M: Changes LCD drive outputs to AC.

SHL/R: Selects the data shift direction for the shift register and the common signal scan direction (figure 2).

DIO1–DIO4: Input or output data. DIO1 and DIO2 are data input/output pins for X_1–X_{50}, and DIO3 and DIO4 are input/output pins for X_{51}–X_{100} (X_{101}) in 50 × 2-output modes. In a 100-output mode, DIO2 and DIO3 must be short-circuited, and DIO1 and DIO4 are used as data input/output pins.

$\overline{\text{DISPOFF}}$: Controls LCD output level. A low $\overline{\text{DISPOFF}}$ sets LCD drive outputs X_1–X_{100} (X_{101}) to V_1 level.

MODE1, MODE2: Select an LCD output mode (table 1). In 10-output through modes, ten unused output pins are made invalid. These ten pins must be open in these modes since they output M signals.

LCD Drive Outputs

X_1–X_{100}: Each X outputs one of the four voltage levels, V_1, V_5, V_6, or V_{EE}, depending on a combination of the M signal and data levels. See figure 3.

Table 1 Selection of LCD Output

MODE1	MODE2	Selected Mode	
0	0	Normal (100-output)	
0	1	10-output through	(X_1–X_{10})
1	0		(X_{91}–X_{100})
1	1	101-output	

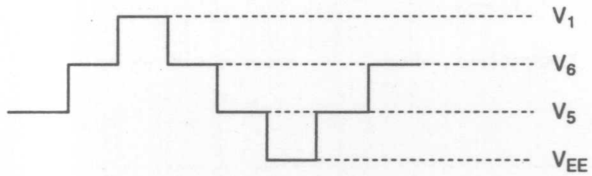


Figure 1 Different Power Supply Voltage Levels for LCD Drive Circuits

SHL/R	DIO1	DIO2	DIO3	DIO4	Data shift direction and common signal scan direction
	In 100 × 1-output mode				
Low	Input	Short-circuited		Output	$X_1 \rightarrow X_{100}$
	In 50 × 2-output mode				
Low	Input	Output	Input	Output	$X_1 \rightarrow X_{50}$ $X_{51} \rightarrow X_{100}$
	In 100 × 1-output mode				
High	Output	Short-circuited		Input	$X_{100} \rightarrow X_1$
	In 50 × 2-output mode				
High	Output	Input	Output	Input	$X_{50} \rightarrow X_1$ $X_{100} \rightarrow X_{51}$

For 10-output through modes and 101-output mode, see Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO Pins in Each Mode.

Figure 2 Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO Pins in Normal Mode (100-Output Mode)

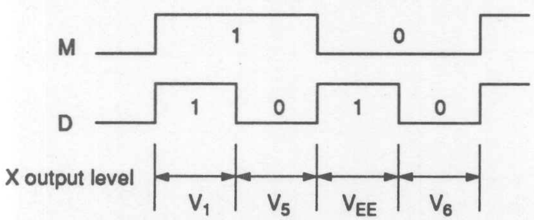
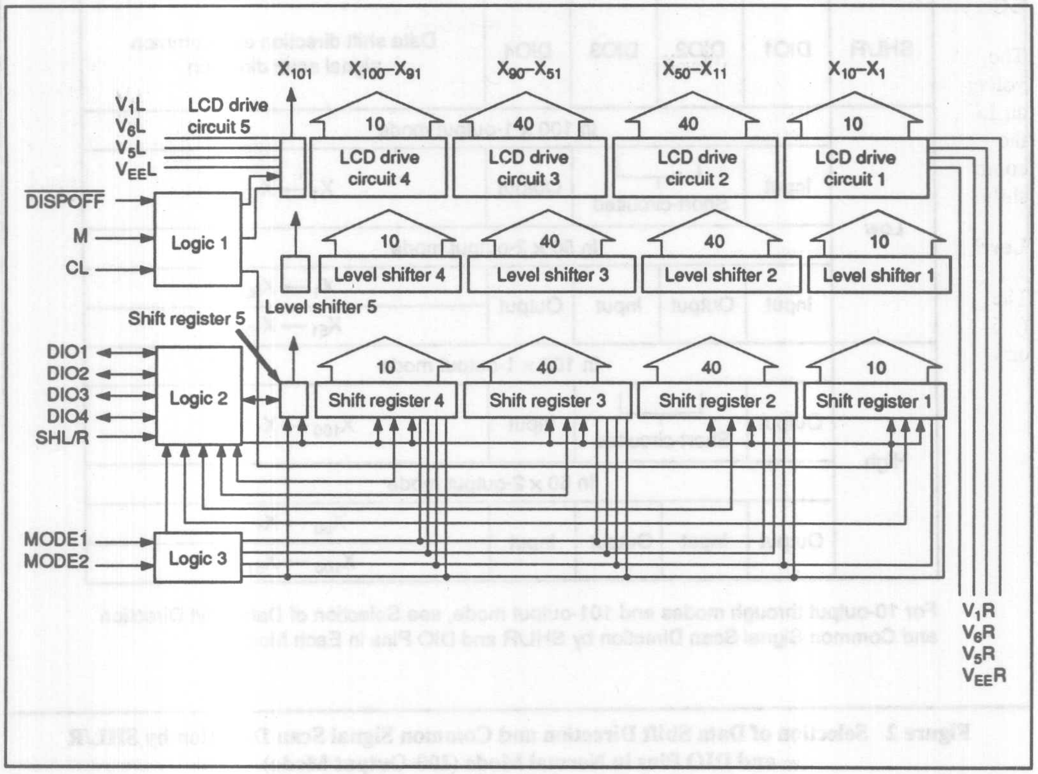


Figure 3 Selection of LCD Drive Output Level

Block Diagram



Block Functions

LCD Drive Circuits

The 100-bit LCD drive circuits generate four voltage levels, V_1, V_5, V_6, and V_{EE}, which drive an LCD panel. One of the four levels is output to the corresponding X pin, depending on a combination of the M signal and the data in the shift register.

Level Shifters

The level shifters change logic control signals (2.5–5.5 V) into high-voltage signals for the LCD drive circuit.

Shift Registers

The 100-bit shift registers shift data input via the DIO pin by one bit. The bit that is shifted out is output from the DIO pin to the next driver IC. Both shifting and output occur simultaneously at the falling edge of each shift clock (CL) pulse. The SHL/R pin selects the data shift direction.

Logic 3

Logic 3 selects which shift register operates depending on the settings of MODE1 and MODE2.

Data Shift and Common Signal Scan Direction

Figure 4–7 show the data shift direction and common signal scan direction selected by SHL/R and DIO pins in each mode.

SHL/R	DIO1	DIO2	DIO3	DIO4	Data shift direction and common signal scan direction
Low	In 100 × 1-output mode				
	Input	Short-circuited		Output	$X_1 \rightarrow X_{100}$
	In 50 × 2-output mode				
	Input	Output	Input	Output	$X_1 \rightarrow X_{50}$
					$X_{51} \rightarrow X_{100}$
High	In 100 × 1-output mode				
	Output	Short-circuited		Input	$X_{100} \rightarrow X_1$
	In 50 × 2-output mode				
	Output	Input	Output	Input	$X_{50} \rightarrow X_1$
					$X_{100} \rightarrow X_{51}$

Figure 4 Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO Pins in 100-Output Mode (MODE1 = 0 and MODE2 = 0)

SHL/R	DIO1	DIO2	DIO3	DIO4	Data shift direction and common signal scan direction
Low	In 90-output mode				
	Input	Short-circuited		Output	$X_{11} \rightarrow X_{100}$
	In 40- and 50-output mode				
	Input	Output	Input	Output	$X_{11} \rightarrow X_{50}$ $X_{51} \rightarrow X_{100}$
High	In 90-output mode				
	Output	Short-circuited		Input	$X_{100} \rightarrow X_{11}$
	In 40- and 50-output mode				
	Output	Input	Output	Input	$X_{50} \rightarrow X_{11}$ $X_{100} \rightarrow X_{51}$

Figure 5 Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO pins in 10-Output (X_1–X_{10}) Through Mode (MODE1 = 0 and MODE 2 = 1)

<table>
<tr><th>SHL/R</th><th>DIO1</th><th>DIO2</th><th>DIO3</th><th>DIO4</th><th>Data shift direction and common signal scan direction</th></tr>
<tr><td rowspan="4">Low</td><td colspan="5">In 90-output mode</td></tr>
<tr><td>Input</td><td colspan="2">Short-circuited</td><td>Output</td><td>$X_1 \rightarrow X_{90}$</td></tr>
<tr><td colspan="5">In 50- and 40-output mode</td></tr>
<tr><td>Input</td><td>Output</td><td>Input</td><td>Output</td><td>$X_1 \rightarrow X_{50}$
$X_{51} \rightarrow X_{90}$</td></tr>
<tr><td rowspan="4">High</td><td colspan="5">In 90-output mode</td></tr>
<tr><td>Output</td><td colspan="2">Short-circuited</td><td>Input</td><td>$X_{90} \rightarrow X_1$</td></tr>
<tr><td colspan="5">In 50- and 40-output mode</td></tr>
<tr><td>Output</td><td>Input</td><td>Output</td><td>Input</td><td>$X_{50} \rightarrow X_1$
$X_{90} \rightarrow X_{51}$</td></tr>
</table>

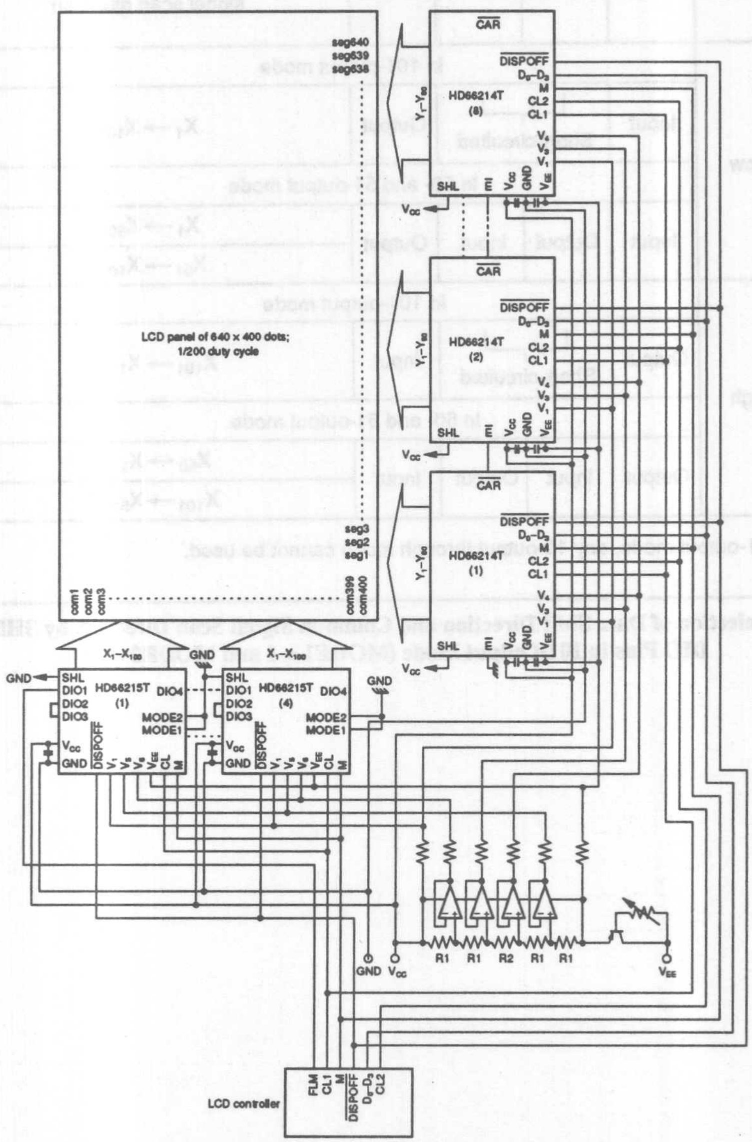
Figure 6 Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO Pins in 10-Output (X_{91}–X_{100}) Through Mode (MODE1 = 1 and MODE2 = 0)

SHL/R	DIO1	DIO2	DIO3	DIO4	Data shift direction and common signal scan direction
Low	In 101-output mode				
	Input	Short-circuited	Short-circuited	Output	$X_1 \rightarrow X_{101}$
	In 50- and 51-output mode				
	Input	Output	Input	Output	$X_1 \rightarrow X_{50}$
					$X_{51} \rightarrow X_{101}$
High	In 101-output mode				
	Output	Short-circuited	Short-circuited	Input	$X_{101} \rightarrow X_1$
	In 50- and 51-output mode				
	Output	Input	Output	Input	$X_{50} \rightarrow X_1$
					$X_{101} \rightarrow X_{51}$

In 101-output mode, any 10-output through mode cannot be used.

Figure 7 Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO Pins in 101-Output Mode (MODE1 = 1 and MODE2 = 1)

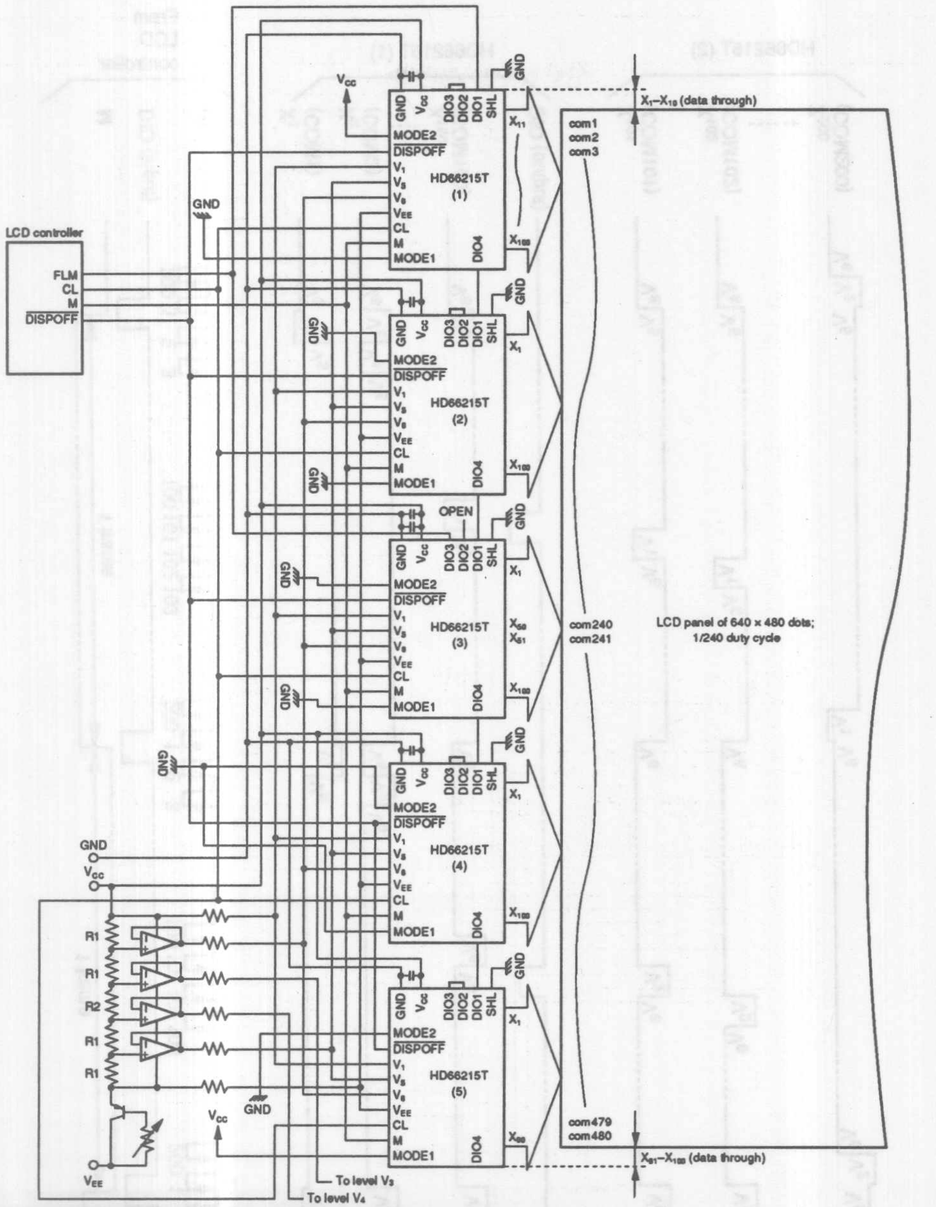
Application Examples



Notes: 1. The resistances of R1 and R2 depend on the type of LCD panel used. For example, for an LCD panel with a 1/15 bias, R1 and R2 must be 3 kΩ and 33 kΩ, respectively. That is, R1/(4·R1 + R2) should be 1/15.

2. To stabilize the power supply, place two 0.1-µF capacitors near each LCD driver: one between the V_{CC} and GND pins, and the other between the V_{CC} and V_{EE} pins.

Figure 8 LCD Panel of 640 × 400 Dots, 1/200 Duty Cycle



Notes: 1. The resistances of R1 and R2 depend on the type of LCD panel used. For example, for an LCD panel with a 1/15 bias, R1 and R2 must be 3 kΩ and 33 kΩ, respectively. That is, R1/(4·R1 + R2) should be 1/15.

2. To stabilize the power supply, place two 0.1-µF capacitors near each LCD driver: one between the V_{CC} and GND pins, and the other between the V_{CC} and V_{EE} pins.

Figure 9 LCD Panel of 640 × 480 Dots, 1/240 Duty Cycle

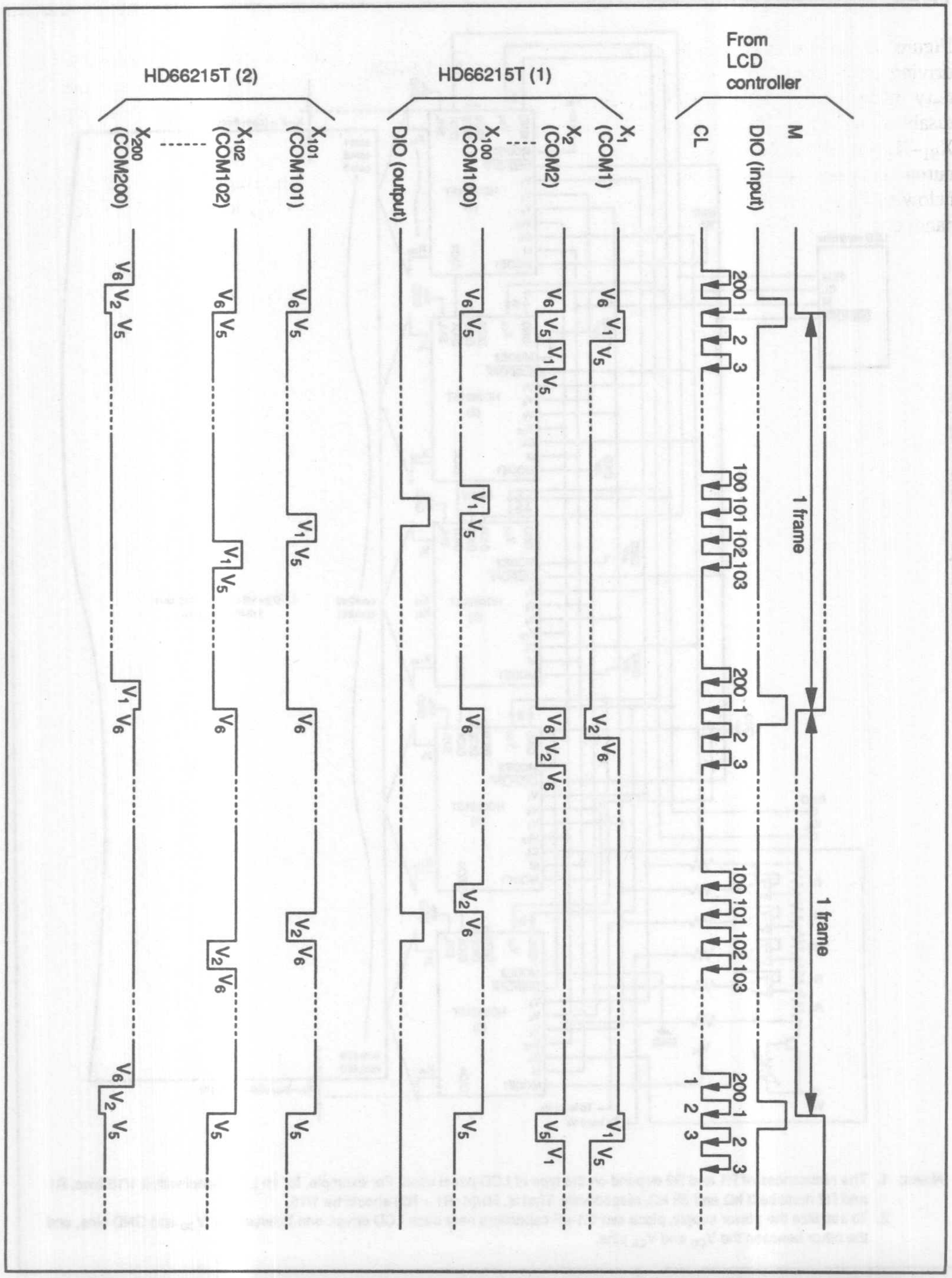


Figure 10 Operational Timing in Normal Mode (100-Output Mode, 1/200 Duty Cycle)

HD66215T Connection Examples

Figure 11 shows an example of an HD66215T driving a 480-line LCD panel with a 1/240 to 1/250 duty cycle. Here, selecting MODE1 and MODE2 disables outputs X_1–X_{10} of driver IC1 and outputs X_{91}–X_{100} of driver IC5. As a result, unused driver output pins can be equally distributed above and below the pins used for the LCD panel so that the panel can be neatly centered on the LCD board. In addition, since the 100 channels of the driver can be divided into two groups of 50 channels by selecting data input/output pins, data input is divided at the center of the panel (IC3).

Figure 12 shows an example of an HD66215T driving a 400-line LCD panel with a 1/200 to 1/210 duty cycle.

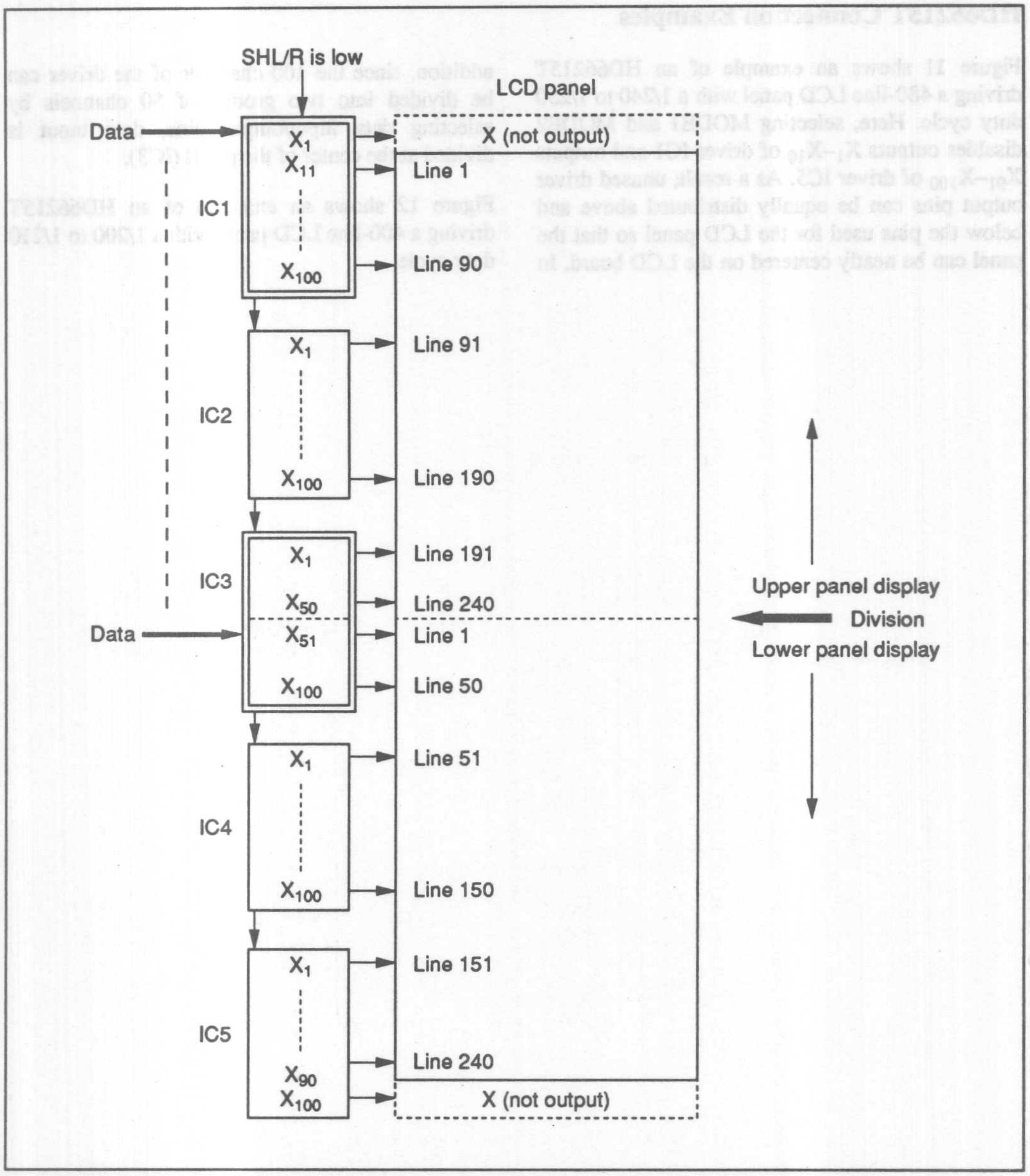


Figure 11 Connection Example for 480-Line LCD Panel with a 1/240–1/250 Duty Cycle

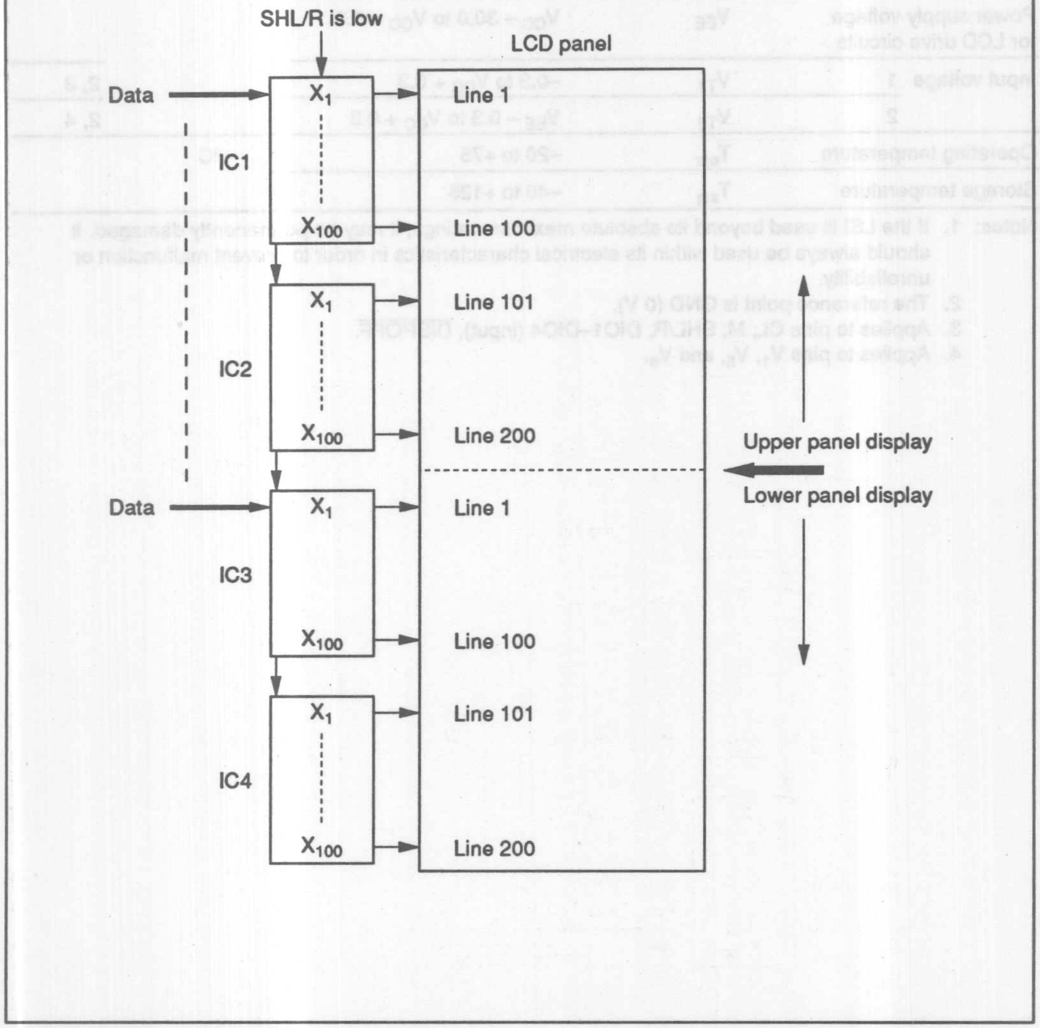


Figure 12 Connection Example for 400-Line LCD Panel with a 1/200–1/210 Duty Cycle

Absolute Maximum Ratings

Item		Symbol	Rating	Unit	Note
Power supply voltage for logic circuits		V_{CC}	–0.3 to +7.0	V	2
Power supply voltage for LCD drive circuits		V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3		
Input voltage	1	V_{T1}	–0.3 to V_{CC} + 0.3		2, 3
	2	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3		2, 4
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–40 to +125		

Notes: 1. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunction or unreliability.
2. The reference point is GND (0 V).
3. Applies to pins CL, M, SHL/R, DIO1–DIO4 (input), $\overline{\text{DISPOFF}}$.
4. Applies to pins V_1, V_5, and V_6.

Electrical Characteristics

DC Characteristics (V_{CC} = 2.5 to 5.5 V, GND = 0 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Condition	Note
Input high voltage	V_{IH}	1	$0.7 \times V_{CC}$	—	V_{CC}	V		
Input low voltage	V_{IL}	1	0	—	$0.3 \times V_{CC}$			
Output high voltage	V_{OH}	2	$V_{CC} - 0.4$	—	—		$I_{OH} = -0.4$ mA	
Output low voltage	V_{OL}	2	—	—	0.4		$I_{OL} = 0.4$ mA	
Vi–Xj on resistance	R_{ON}	3	—	0.5	1.0	kΩ	$I_{ON} = 100\ \mu A$	1
Input leakage current 1	I_{IL1}	4	–1.0	—	1.0	μA	$V_{IN} = V_{CC}$ to GND	
2	I_{IL2}	5	–25	—	25		$V_{IN} = V_{CC}$ to V_{EE}	
3	I_{IL3}	2	–5.0	—	5.0		$V_{IN} = V_{CC}$ to GND	
Current consumption (5 V)	I_{GND}	—	—	—	100		f_{CL} = 19.2 kHz	2
	I_{EE}	—	—	—	250		$V_{CC} - V_{EE}$ = 28 V	
							f_{FLM} = 80 Hz	
							V_{CC} – GND = 5 V	
(3 V)	I_{GND}	—	—	—	50		f_{CL} = 19.2 kHz	2
	I_{EE}	—	—	—	250		$V_{CC} - V_{EE}$ = 28 V	
							f_{FLM} = 80 Hz	
							V_{CC} – GND = 3 V	

Pins:
1. CL, M, SHL/R, $\overline{\text{DISPOFF}}$, DIO1–DIO4 (input)
2. DIO1–DIO4 (input)
3. X_1–X_{100}, V_1, V_5, V_6
4. CL, M, SHL/R, MODE1, MODE2, $\overline{\text{DISPOFF}}$
5. V_1, V_5, V_6

Notes:
1. Indicates the resistance between one pin from X_1–X_{100} and another pin from V_1, V_5, V_6, and V_{EE}, when load current is applied to the X pin. Defined under the following conditions:

   $V_{CC} - V_{EE} = 28$ V
   $V_1, V_6 = V_{CC} - \{1/10\ (V_{CC} - V_{EE})\}$
   $V_5 = V_{EE} + \{1/10\ (V_{CC} - V_{EE})\}$

   V_1 and V_6 should be near V_{CC} level, and V_5 should be near V_{EE} level (figure 4). All voltage must be within Δ V. Δ V is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that Δ V depends on power supply voltages $V_{CC} - V_{EE}$ (figure 5).

2. Excludes input and output current. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.

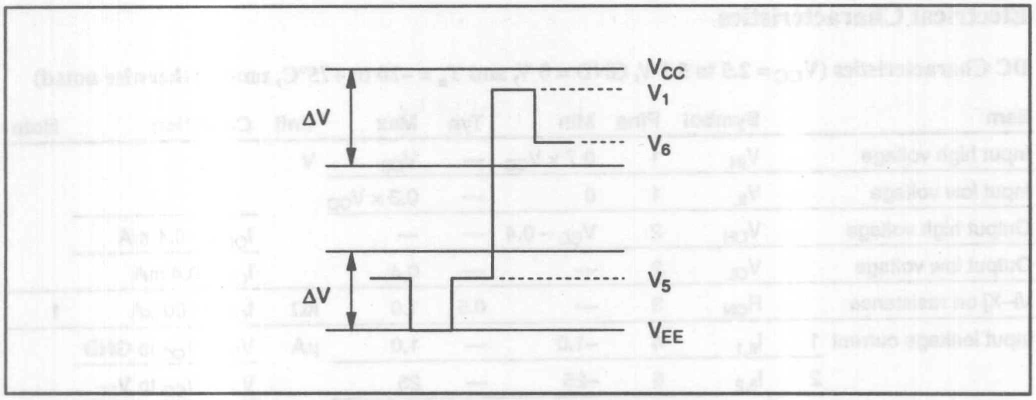


Figure 13 Relation between Driver Output Waveform and Level Voltages

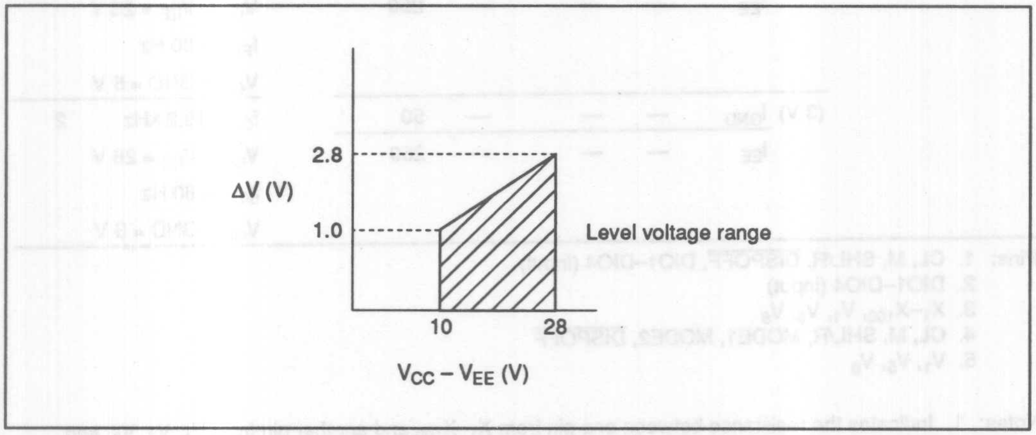


Figure 14 Relation between $V_{CC} - V_{EE}$ and ΔV

AC Characteristics (V_{CC} = 2.5 to 5.5 V, GND = 0 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit
Clock cycle time	t_{CYC}	CL	10	—	µs
Clock high-level width	t_{CWH}		65	—	ns
Clock low-level width	t_{CWL}		1.0	—	µs
Clock rise time	t_r			50	ns
Clock fall time	t_f				
Data setup time	t_{DS}	DIO1–DIO4, CL	100	—	ns
Data hold time	t_{DH}				
Data output delay time*	t_{DD}		—	7.0	µs
Data output hold time	t_{DHW}		100	—	ns

Note: * The load circuit is shown in figure 15 is connected.

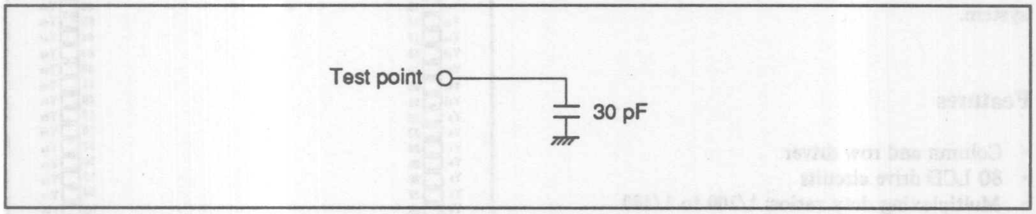


Figure 15 Load Circuit

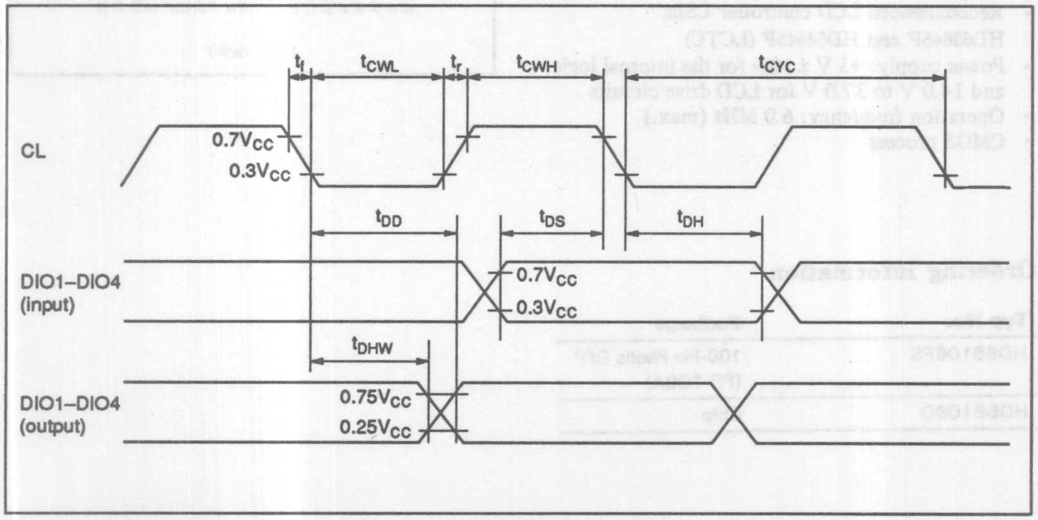


Figure 16 LCD Controller Interface Timing

HD66106F
(LCD Driver for High Voltage)

Description

The HD66106F LCD driver has a high duty ratio and many outputs for driving a large capacity dot matrix LCD panel.

It includes 80 LCD drive circuits and can drive at up to 1/480 duty cycle. For example, only 14 drivers are enough to drive an LCD panel of 640 × 480 dots. It also easily interfaces with various LCD controllers because of its internal automatic chip enable signal generator.

Using this LSI sharply lowers the cost of an LCD system.

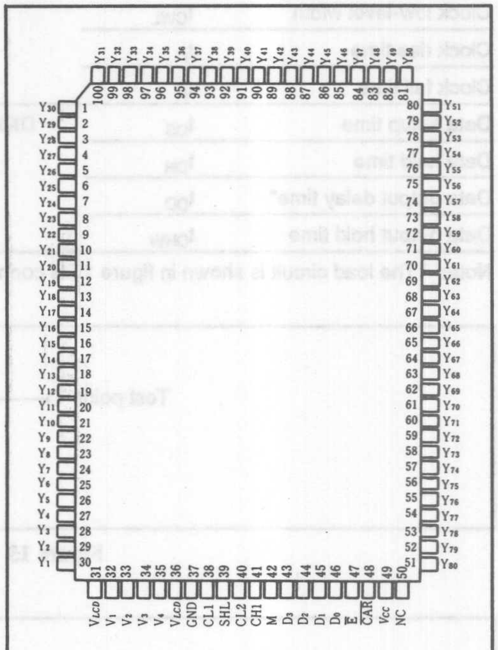
Features

- Column and row driver
- 80 LCD drive circuits
- Multiplexing duty ratios: 1/100 to 1/480
- 4-bit parallel data transfer
- Internal automatic chip enable signal generator
- Internal standby function
- Recommended LCD controller LSIs: HD63645F and HD64645F (LCTC)
- Power supply: +5 V ± 10% for the internal logic, and 14.0 V to 37.0 V for LCD drive circuits
- Operation frequency: 6.0 MHz (max.)
- CMOS process

Ordering Iuformation

Typ No.	Package
HD66106FS	100-Pin Plastic QFP (FP-100A)
HD66106D	Chip

Pin Arrangement



(Top view)

Pin Description

Power supply

V_{CC}, GND: V_{CC} supplies power to the internal logic circuit. GND is the logic and drive ground.

V_{LCD}: V_{LCD} supplies power to the LCD drive circuit.

V_1, V_2, V_3, and V_4: V_1-V_4 supply power for driving LCD (figure 1).

Control signals

CL1: The LSI latches data at the negative edge of CL1 when the LSI is used as a column driver. Fix to GND when the LSI is used as a row driver.

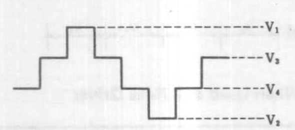
CL2: The LSI latches display data at the negative edge of CL2 when the LSI is used as a column driver, and shifts line select data at the negative edge when it is used as a row driver.

M: M changes LCD drive outputs to AC.

D_0-D_3: D_0-D_3 input display data for the column driver (table 2).

Table 1 Pin Function

Symbol	Pin No.	Pin Name	I/O
V_{CC}	49	V_{CC}	I
GND	37	Ground	I
V_{LCD}	31, 36	V_{LCD}	I
V_1	32	LCD voltage 1	I
V_2	33	V_2 LCD voltage 2	I
V_3	34	V_3 LCD voltage 3	I
V_4	35	V_4 LCD voltage 4	I
CL1	38	Clock 1	I
CL2	40	Clock 2	I
M	42	M	I
D_0-D_3	46-43	Data 0 to data 3	I
SHL	39	Shift left	I
$\overline{E}$	47	Enable	I
$\overline{CAR}$	48	Carry	O
CH1	41	Channel 1	I
Y_1-Y_{80}	30-1, 100-51	Drive outputs 1-80	O
NC	50	No connection	—



V_1, V_2: Selected level
V_3, V_4: Nonselected level

Figure 1 Power Supply for Driving LCD

Table 2 Relation between Display Data and LCD State

Display Data	LCD Outputs	LCD
1 (= high level)	Selected level	On
0 (= low level)	Nonselected level	Off

SHL: SHL controls the shift direction of display data and line select data (figure 2, table 3).

$\overline{E}$: $\overline{E}$ inputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}). The LSI is disabled when $\overline{E}$ is high and enabled when low. $\overline{E}$ inputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66106Fs are connected in cascade, E connects with $\overline{CAR}$ of the preceding LSI.

$\overline{CAR}$: $\overline{CAR}$ outputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}). $\overline{CAR}$ outputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66106Fs are connected in cascade, $\overline{CAR}$ connects with $\overline{E}$ of the next LSI.

CH1: CH1 selects the driver function. The chip drives columns when CH1 = V_{CC}, and rows when CH1 = GND.

Y_1-Y_{80}: Each Y outputs one of the four voltage levels—V_1, V_2, V_3, or V_4—according to the combination of M and display data (figure 3).

NC: NC is not used. Do not connect any wire.

Table 3 Relation between SHL and Scan Direction of Selected Line (When LSI is Used as a Row Driver)

SHL	Shift Direction of Shift Register	Scan Direction of Selected Line
V_{CC}	$\overline{E}$ → 1 → 2 → 3 ---------------→ 80	Y_1 → Y_2 → Y_3 ------------------→ Y_{80}
GND	$\overline{E}$ → 80 → 79 → 78 ---------------→ 1	Y_{80} → Y_{79} → Y_{78} ------------------→ Y_1

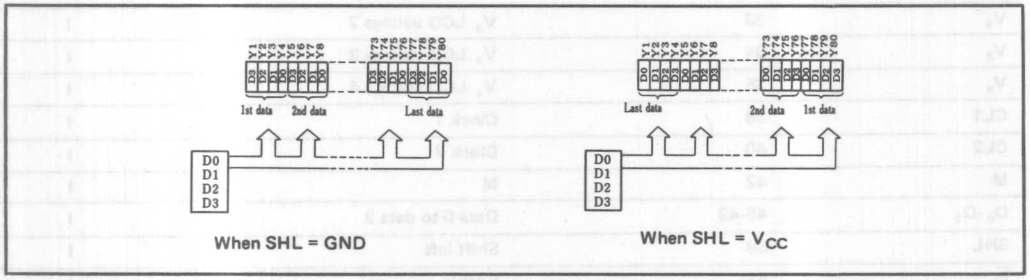


Figure 2 Relation between SHL and Data Output (When LSI is Used as a Column Driver)

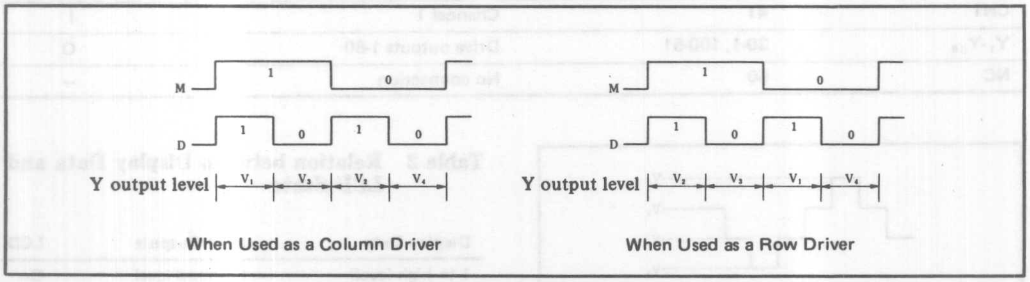


Figure 3 Selection of LCD Drive Output Level

Internal Block Diagram

LCD Drive Circuits

The HD66106F (figure 4) begins latching data when $\overline{E}$ goes low, which enables the data latching operation. It latches 4 bits of data simultaneously at the fall of CL2 and stops automatically (= standby state) when it has latched 80 bits.

Latch Circuit 2

When the LSI is used as a column driver, latch circuit 2 functions as an 80-bit latch circuit. It latches the data sent from latch circuit 1 at the fall of CL1 and transfers its outputs to the LCD drive circuits.

When the LSI is used as a row driver, this circuit functions as an 80-bit bidirectional shift register. The data sent from the $\overline{E}$ pin shifts at the fall of CL2. When SHL = V_{CC}, the data shifts from bit 1 to bit 80 in order of entry. When SHL = GND, the data shifts from bit 80 to bit 1.

Latch Circuit 1

Latch circuit 1 is composed of twenty 4-bit parallel data latches. It latches the display data D_0-D_3 at the fall of CL2 when the LSI is used as a column driver. The signals sent from the selector determine which 4-bit latch should latch the data.

Selector

The selector is composed of a 5-bit up and down counter and a decoder. When the LSI is used as a column driver, it generates the latch signal to be sent to latch circuit 1, incrementing the counter at the negative edge of CL2.

Controller

The controller operates when the LSI is used as a column driver. It stops data latching when twenty pulses of CL2 have been input (= power-down function) and automatically generates the chip enable signal announcing the start of data latching into the next LSI.

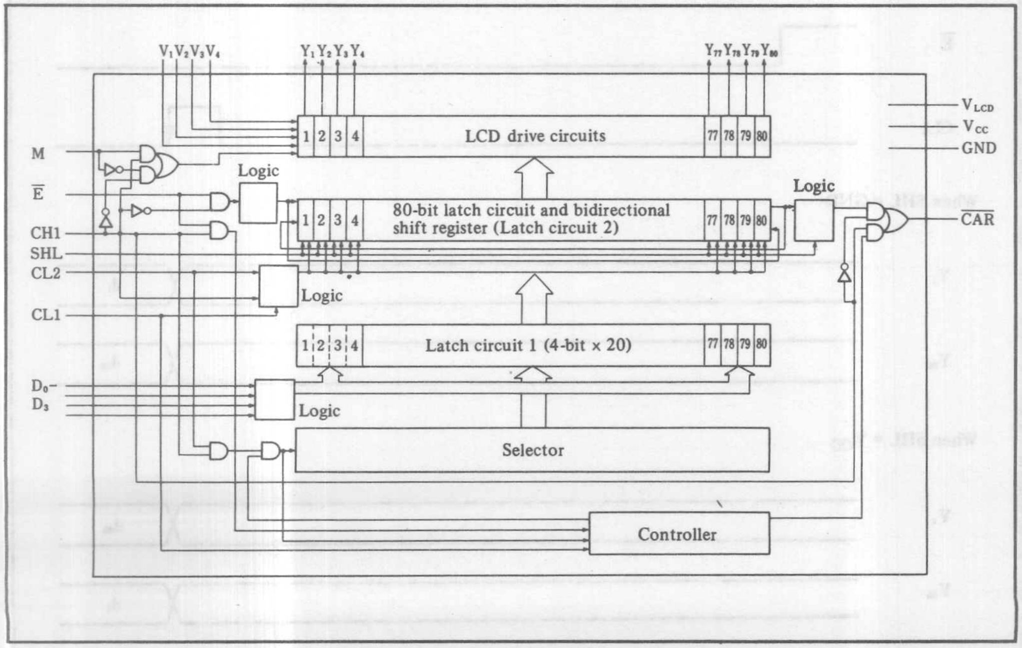


Figure 4 Block Diagram

Functional Description

When Used as a Column Driver

The HD66106F begins latching data when $\overline{E}$ goes low, which enables the data latching operation. It latches 4 bits of data simultaneously at the fall of CL2 and stops automatically (= standby state) when it has latched 80 bits.

Data outputs change at the fall of CL1. Latched data d_1 is transferred to the output pin Y_1 and d_{80} to Y_{80} when SHL = GND. Conversely, d_{80} is transferred to Y_1 and d_1 to Y_{80} when SHL = V_{CC}. The output level is selected out of V_1-V_4 according to the combination of display data and the alternating signal M (figure 5).

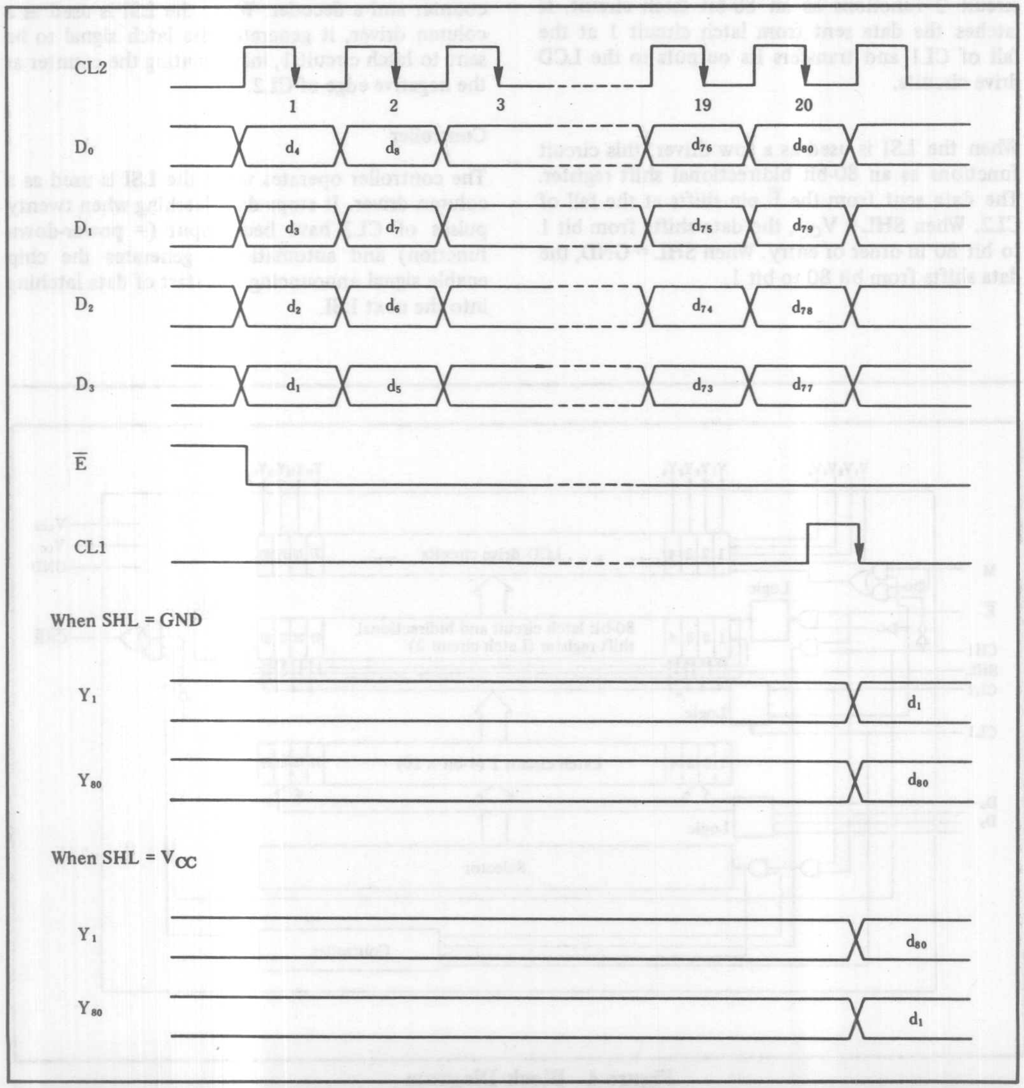


Figure 5 Column Driver Timing Chart

When Used as a Row Driver

The HD66106F shifts the line scan data sent from the pin $\overline{E}$ in order at the fall of CL2. When SHL = V_{CC}, data is shifted from Y_1 to Y_{80} and Y_{80} to Y_1 when SHL = GND.

In both cases, the data delayed for 80 bits by the shift register is output from the $\overline{CAR}$ pin to become the line scan data for the next LSI (figure 6).

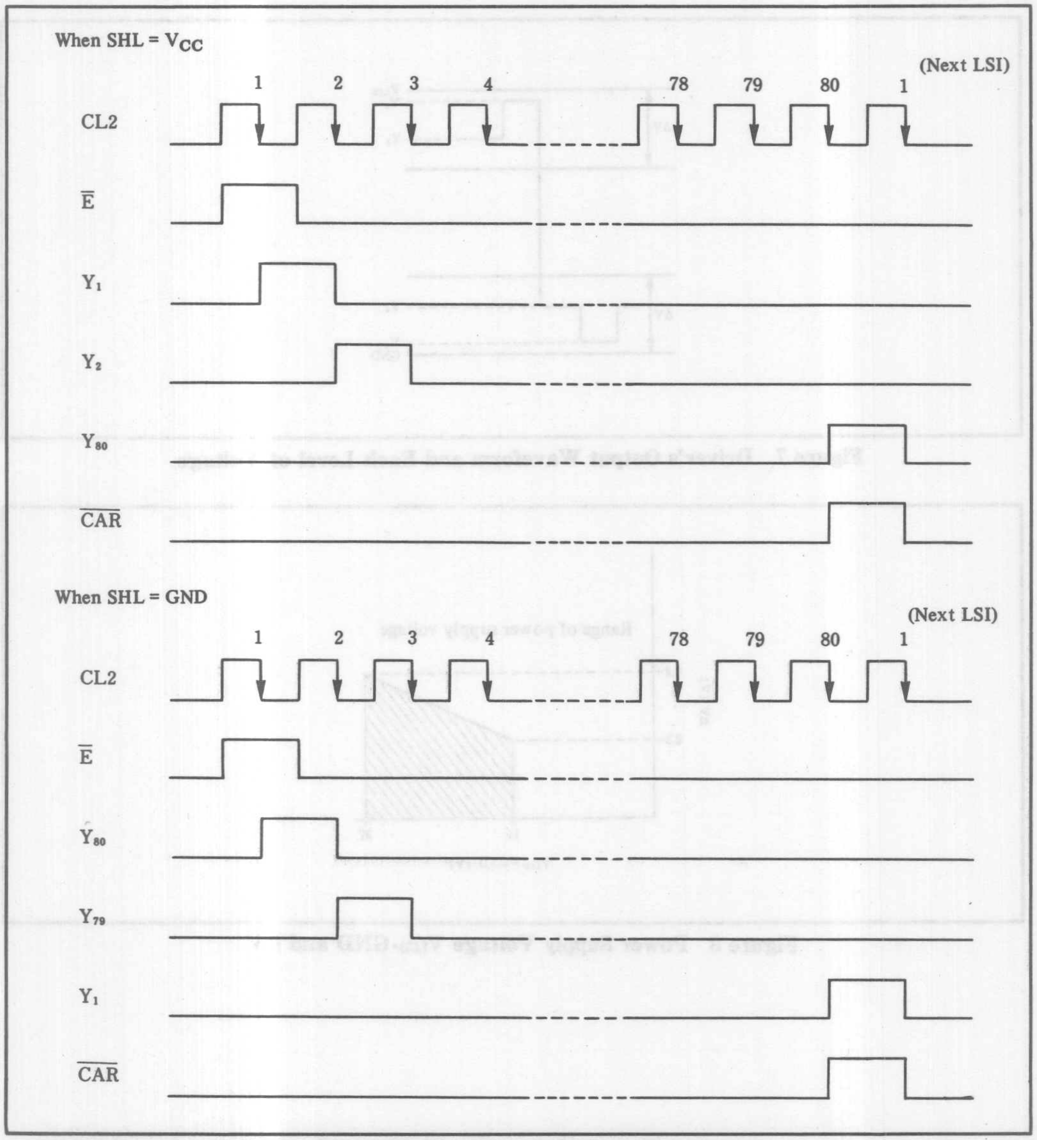


Figure 6 Row Driver Timing Chart

LCD Power Supply

This section explains the range of power supply voltage for driving LCD. V_1 and V_3 voltages should be near V_{LCD}, and V_2 and V_4 should be near GND (figure 7). Each voltage must be within ΔV. ΔV determines the range within which R_{ON}, impedance of driver's output, is stable. Note that ΔV depends on power supply voltage V_{LCD}-GND (figure 8).

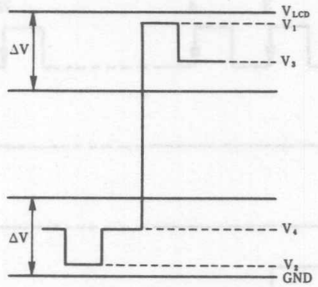


Figure 7 Driver's Output Waveform and Each Level of Voltage

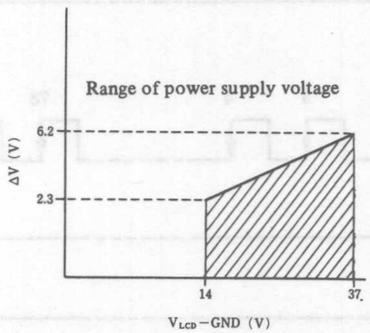
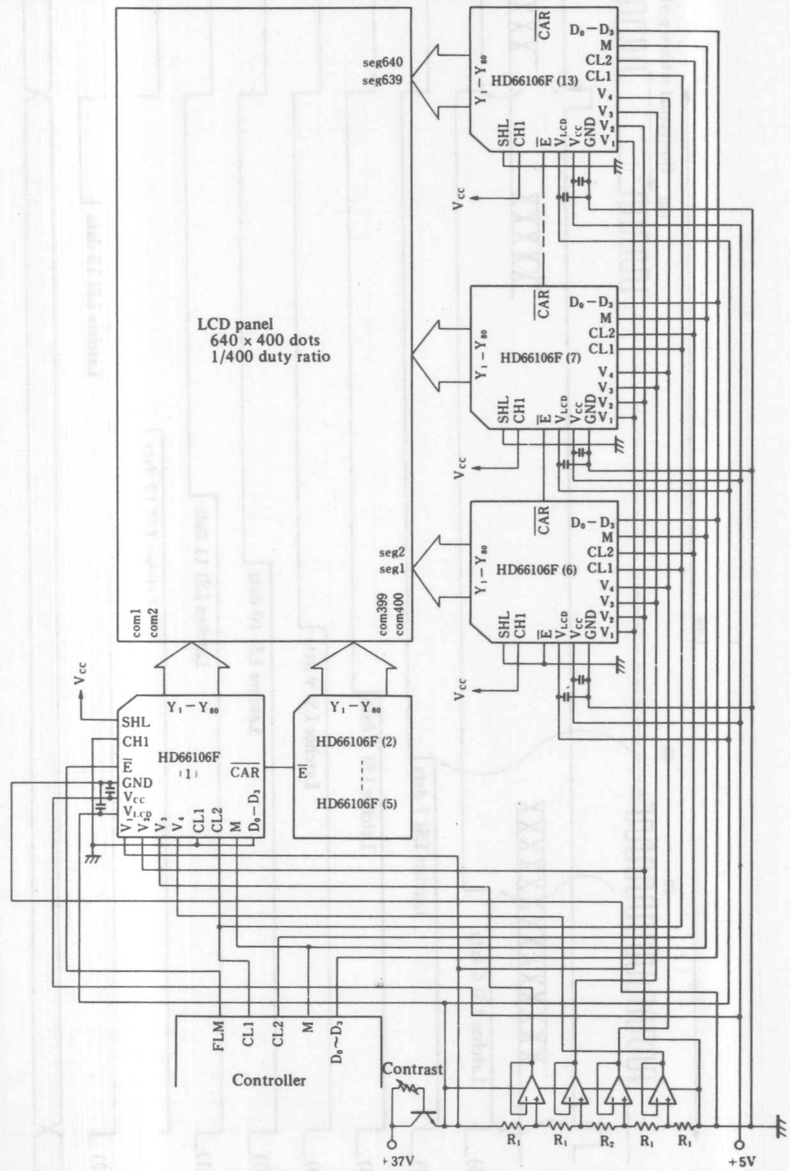


Figure 8 Power Supply Voltage V_{LCD}-GND and ΔV

Application Example

Application Diagram

Figure 9 shows an example of an LCD panel of 640 x 400 dots driven by HD66106Fs.



Notes: 1. R_1 and R_2 depend on the LCD panel in use. When using an LCD panel with 1/20 bias, $R_1/(4R_1+R_2)$ should be 1/20. For example, $R_1 = 3k\Omega$ and $R_2 = 48k\Omega$.
2. Use bypass capacitors to stabilize power supply when designing a board. It is desirable to use two capacitors with some 0.1 µF per LSI, putting one between V_{LCD} and GND, and the other between V_{CC} and GND.

Figure 9 Application Example

Timing waveform example

Figures 10 and 11 show the timing waveforms of the application example shown in figure 9.

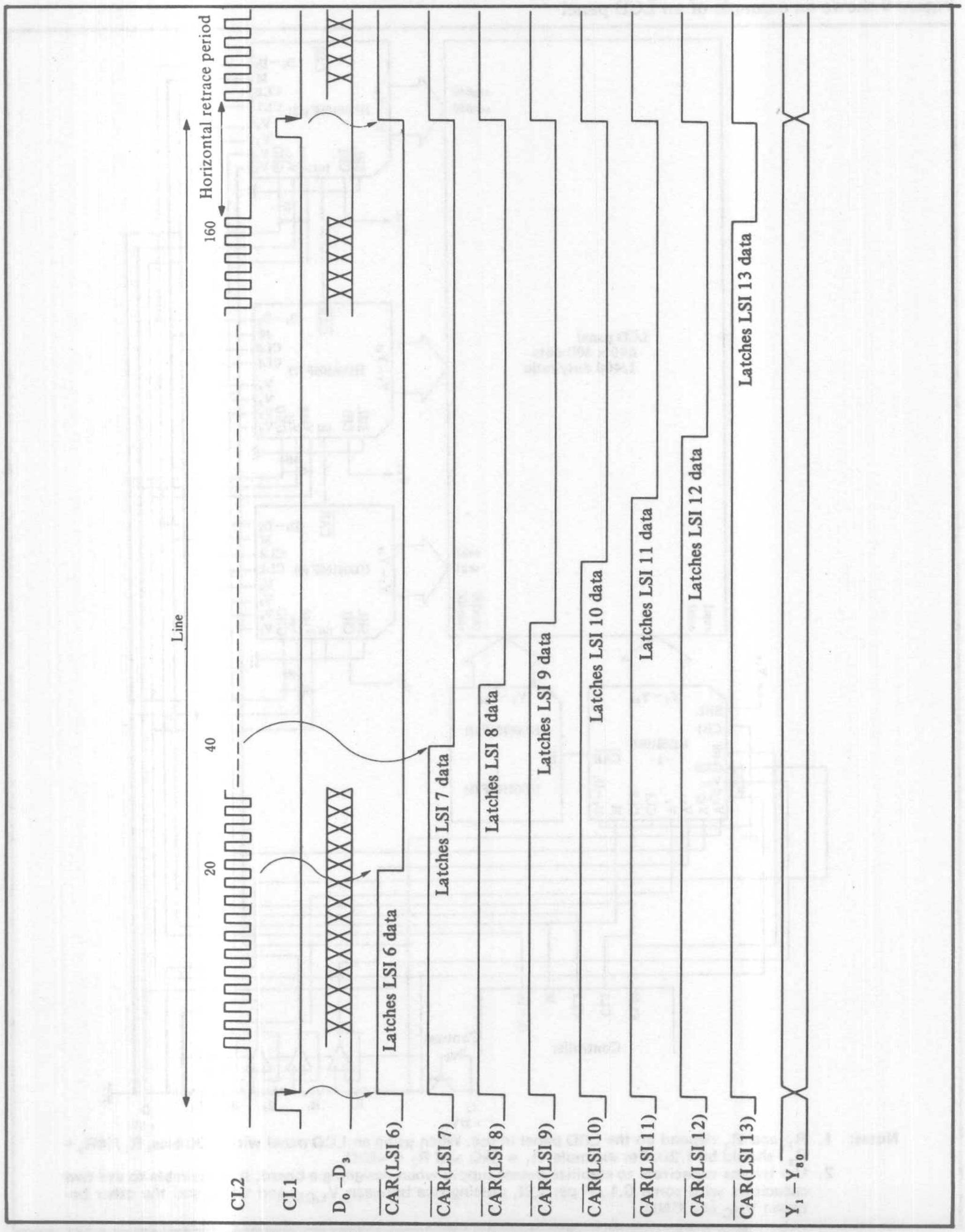


Figure 10 Timing Waveform for Column Drivers (LSI 6-LSI 13)

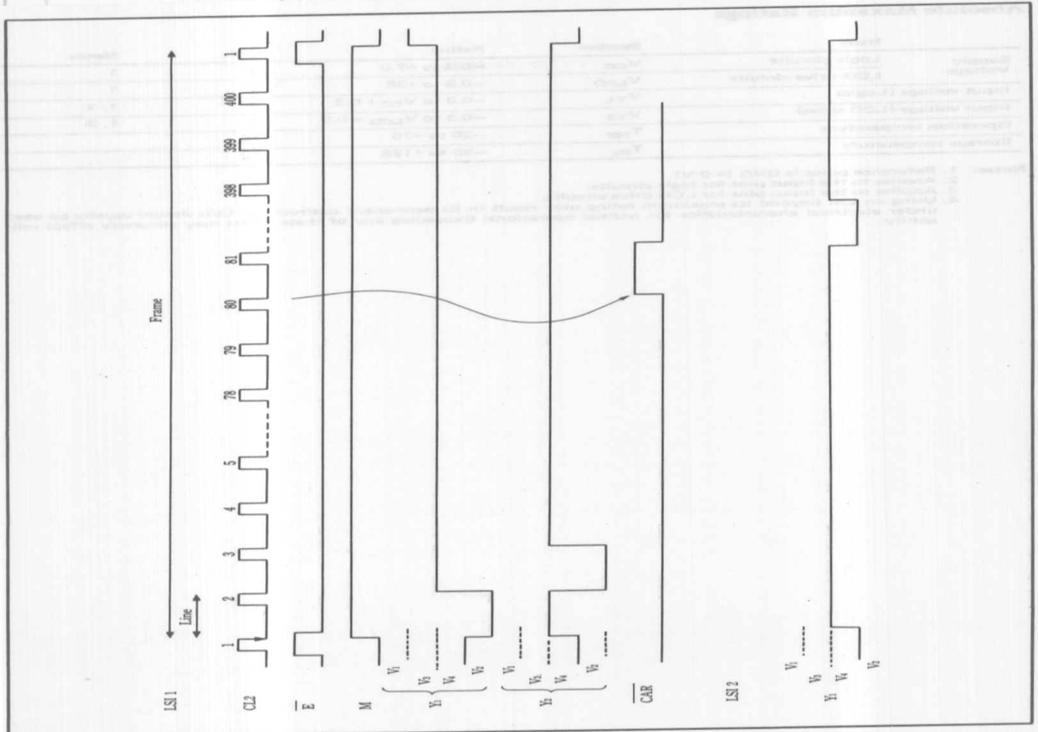


Figure 11 Timing Waveform for Row Drivers (LSI 1-LSI 5)

Absolute Maximum Ratings

Item		Symbol	Rating	Unit	Notes
Supply Voltage	Logic circuits	V_{CC}	–0.3 to +7.0	V	1
	LCD drive circuits	V_{LCD}	–0.3 to +38	V	1
Input voltage (Logic)		V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (LCD drive)		V_{T2}	–0.3 to V_{LCD} + 0.3	V	1, 3
Operation temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–55 to +125	°C	

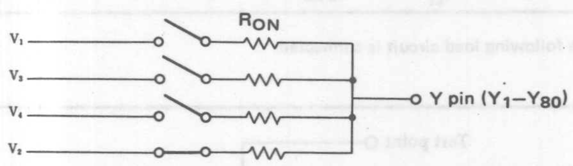
Notes: 1. Reference point is GND (= 0 V).
2. Applies to the input pins for logic circuits.
3. Applies to the input pins for LCD drive circuits.
4. Using an LSI beyond its maximum rating may result in its permanent destruction. LSIs should usually be used under electrical characteristics for normal operations. Exceeding any of these limits may adversely affect reliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ± 10 %, V_{LCD} = 14 V to 37 V, Ta = –20°C to 75°C unless otherwise noted)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	CL1, CL2, M, SHL,	0.8 x Vcc	–	Vcc	V		
Input low voltage	V_{IL}	D_0–D_3, $\overline{E}$, CH1	0	–	0.2 x V_{CC}	V		
Output high voltage	V_{OH}	$\overline{CAR}$	V_{CC} – 0.4	–	–	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}		–	–	0.4	V	I_{OL} = 0.4 mA	
Vi-Yj on resistance	R_{ON}	Y_1–Y_{80}, V_1–V_4	–	–	3.0	kΩ	I_{ON} = 100 µA	4
Input leakage current (1)	I_{IL1}	CL1, CL2, M, SHL, D_0–D_3, $\overline{E}$, CH1	–5.0	–	5.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current (2)	I_{IL2}	V_1–V_4	–50.0	–	50.0	µA	V_{IN} = V_{LCD} to GND	
Current consumption (1)	I_{CC1}		–	–	3.0	mA	f_{CL2} = 6 MHz,	
(2)	I_{LCD1}		–	–	0.5	mA	f_{CL1} = 28 kHz	1
(3)	I_{ST}		–	–	0.2	mA	At the standby state f_{CL2} = 6 MHz, f_{CL1} = 28 kHz	2
(4)	I_{CC2}		–	–	0.2	mA	f_{CL1} = 28 kHz,	1
(5)	I_{LCD2}		–	–	0.1	mA	f_m = 35 Hz	3

Notes: 1. Input and output current is excluded. When the input is at the intermediate level in CMOS, excessive current flows from the power supply through the input circuit. V_{IH} and V_{IL} must be fixed at V_{CC} and GND respectively to avoid it.
2. Applies when the LSI is used as a column driver.
3. Applies when the LSI is used as a row driver.
4. Indicates the resistance between Y pin and V pin (one of V_1, V_2, V_3, and V_4) when it supplies load current to one of Y_1–Y_{80} pins.
Conditions: V_{LCD} – GND = 37 V
V_1, V_3 = V_{LCD} – 2/20 (V_{LCD} – GND)
V_2, V_4 = GND + 2/20 (V_{LCD} – GND)



AC Characteristics (V_{CC} = 5 V ± 10 %, V_{LCD} = 14 V to 37 V, Ta = –20°C to +75°C unless otherwise noted)

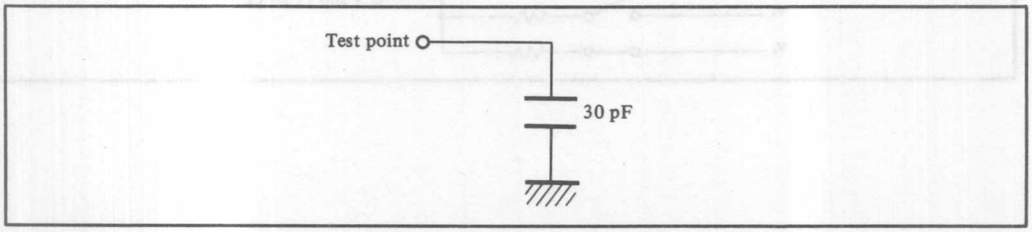
Column Driver

Item	Symbol	Pin	Min	Typ	Max	Unit	Notes
Clock cycle time	t_{cyc}	CL2	166	–	–	ns	
Clock high level width	t_{CWH}	CL2	50	–	–	ns	
Clock low level width	t_{CWL}	CL2	50	–	–	ns	
Clock setup time	t_{SCL}	CL2	200	–	–	ns	
Clock hold time	t_{HCL}	CL2	200	–	–	ns	
Clock rise/fall time	t_{ct}	CL1, CL2	–	–	30	ns	
Data setup time	t_{DSU}	D_0–D_3	30	–	–	ns	
Data hold time	t_{DH}	D_0–D_3	30	–	–	ns	
$\overline{E}$ setup time	t_{ESU}	$\overline{E}$	50	–	–	ns	
Output delay time	t_{DCAR}	$\overline{CAR}$	–	–	80	ns	1
M phase difference	t_{CM}	M, CL1	–	–	300	ns	

Row Driver

Item	Symbol	Pin	Min	Typ	Max	Unit	Notes
Clock low level width	t_{WL1}	CL2	5	–	–	µs	
Clock high level width	t_{WH1}	CL2	125	–	–	ns	
Data setup time	t_{DS}	$\overline{E}$	100	–	–	ns	
Data hold time	t_{DH}	$\overline{E}$	30	–	–	ns	
Data output delay time	t_{DD}	$\overline{CAR}$	–	–	3	µs	1
Data output hold time	t_{DHW}	$\overline{CAR}$	30	–	–	ns	1
Clock rise/fall time	t_{ct}	CL2	–	–	30	ns	

Note: 1. Values when the following load circuit is connected:



Column Driver

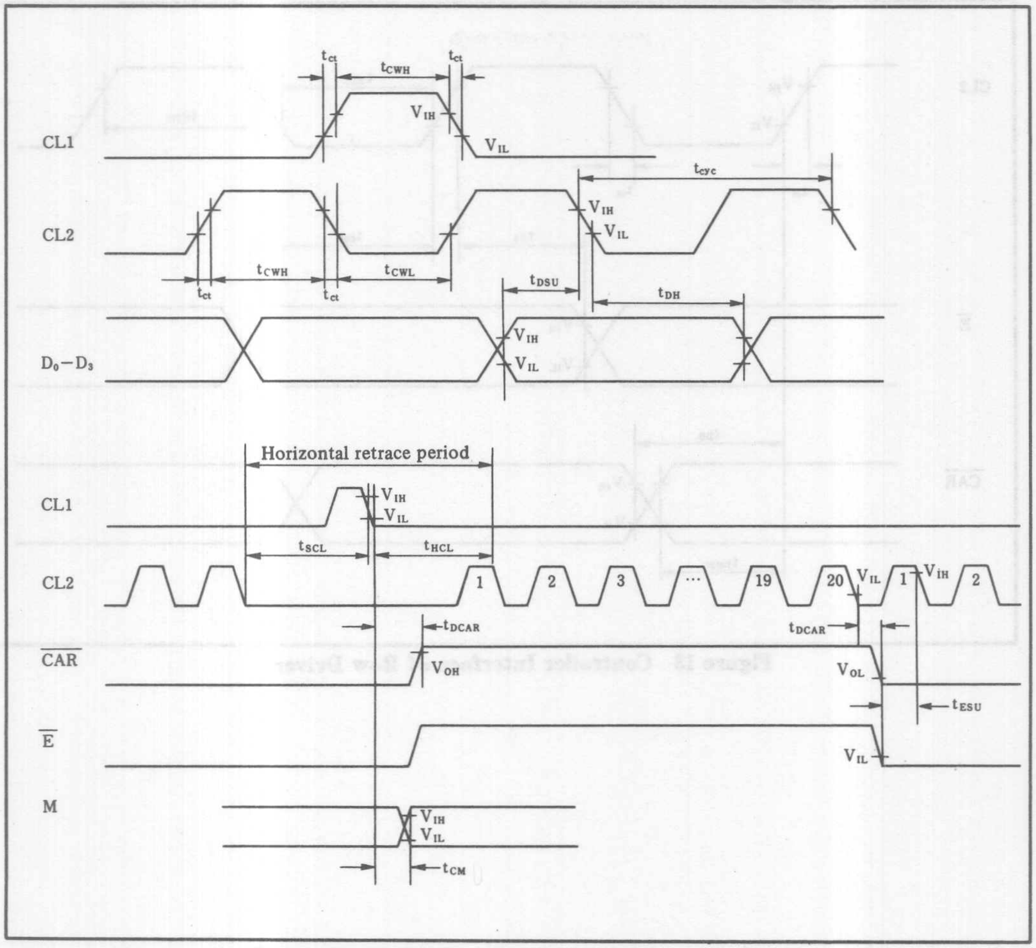


Figure 12 Controller Interface of Column Driver

Row Driver

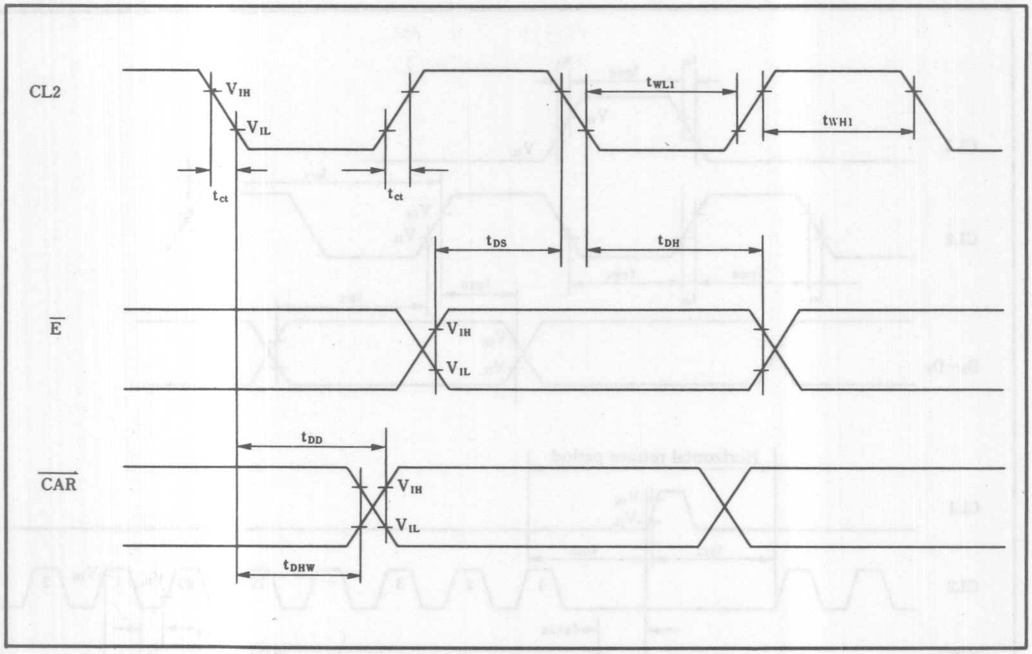


Figure 13 Controller Interface of Row Driver

HD66107T
(LCD Driver for High Voltage)

Description

The HD66107T is a multi-output, high duty ratio LCD driver used for large capacity dot matrix LCD panels. It consists of 160 LCD drive circuits with a display duty ratio up to 1/480: the seven HD66107Ts can drive a 640× 480 dots LCD panel. Moreover, the LCD driver enables interfaces with various LCD controllers due to a built-in automatic generator of chip enable signals. Use of the HD66107T can help reduce the cost of an LCD-panel configuration, since it reduces the number of LCD drivers, compared with use of the HD61104 and HD61105.

Features

- Column and row driver
- 160 LCD drive circuits
- Multiplexing duty ratios: 1/100 to 1/480
- 4-bit and 8-bit parallel data transfer
- Internal automatic chip enable signal generator
- Internal standby mode
- Recommended LCD controller LSIs:
  HD63645F, HD64645F, and HD64646FS (LCTC), HD66840/HD66841 (LVIC), HD66850 (CLINE)
- Power supply voltage
  —internal logic: +5 V ± 10%
  —LCD drive circuit : 14.0 to 37.0 V
- Operation frequency: 8.0 MHz (max.)
- CMOS Process
- 192-pin TCP

Ordering Information

Type No.	Number of outputs	Outer lead pitch (μm)	Material of tape*2	Note
HD66107T11	160	180	Kapton	
HD66107T24	160	180	Upilex	
HD66107T12	160	250	Kapton	
HD66107T00	160	280	Kapton	
HD66107T01	80	280	Kapton	12 perforated holes
HD66107T25	80	280	Kapton	8 perforated holes

Note: *1"Kapton" is a trademark of Dupont, Ltd.
"Upilex" is a trademark of Ube Industries, Ltd.
*2The details of TCP pattern are shown in "The Information of TCP".

Pin Description

Power Supply

V_{CC}, GND: V_{CC} supplies power to the internal logic circuits. GND is the logic and drive ground.

V_{LCD}: V_{LCD} supplies power to the LCD drive circuit.

V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, V_{4R}: V_1 to V_4 supply power for driving an LCD (figure 1).

Control Signal

CL1: The LSI latches data at the negative edge of CL1 when the LSI is used as a column driver. Fix to GND when the LSI is used as a row driver.

CL2: The LSI latches display data at the negative edge of CL2 when the LSI is used as a column driver, and shifts line select data at the negative edge when it is used as a row driver.

Table 1 Pin Function

Symbol	Pin No.	Pin name	Input/output
V_{CC}	167	V_{CC}	
GND	161, 186, 187	Ground	
V_{LCD}	166, 192	V_{LCD}	
V1L, R V2L, R V3L, R V4L, R	191, 165 188, 162 190, 164 189, 163	V1L, V1R V2L, V2R V3L, V3R V4L, V4R	
CL1	183	Clock 1	Input
CL2	184	Clock 2	Input
M	182	M	Input
D_0-D_7	174-181	DATA0-DATA7	Input
SHL	172	Shift left	Input
CH2	171	Channel 2	Input
BS	173	Bus Select	Input
TEST	185	TEST	Input
Y1-Y160	1-160	Y1-Y160	Output
$\overline{E}$	169	Enable	Input
$\overline{CAR}$	168	Carry	Output
CH1	170	Channel 1	Input

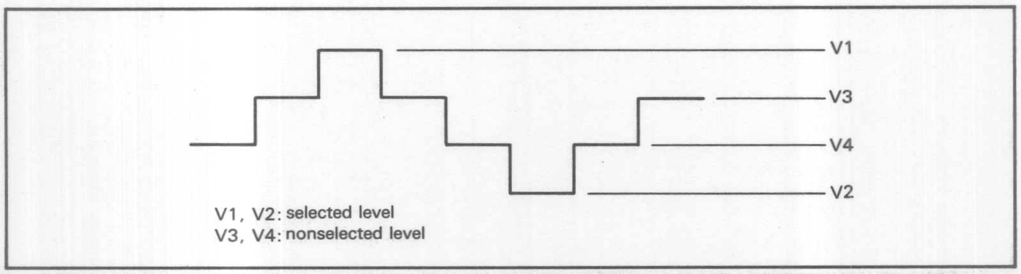


Figure 1 Power Supply for Driving an LCD

M: M changes LCD drive outputs to AC.

D_0-D_7: D_0-D_7 input display data for the column driver (table 2).

SHL: SHL controls the shift direction of display data and line select data (figure 2, table 3).

$\overline{E}$: $\overline{E}$ inputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}).

The LSI is disabled when $\overline{E}$ is high and enabled when low. $\overline{E}$ inputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66107Ts are connected in cascade, $\overline{E}$ connects with $\overline{CAR}$ of the preceding LSI.

$\overline{CAR}$: $\overline{CAR}$ outputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}).

$\overline{CAR}$ outputs scan data when the LSI is used as a row driver (CH1=GND). When HD66107Ts are connected in cascade, $\overline{CAR}$ connects with $\overline{E}$ of the next LSI.

CH1: CH1 selects the driver function. The chip devices are columns when CH1 = V_{CC}, and rows when CH1 = GND.

CH2: CH2 selects the number of output data bits. The number of output data bits is 160 when CH2 = GND, and 80 when CH2 = V_{CC}.

BS: BS selects the number of input data bits. When BS = V_{CC}, the chip latches 8-bits data. When BS = GND, the chip latches 4-bits data via D_0 to D_3. Fix D_4 through D_7 to GND.

TEST: Used for testing. Fixed to GND, other wise.

Table 2 Relation between Display data and LCD state

Display Data	LCD Output	LCD
1 (=high level)	V1L, R/V2L, R	On
0 (=low level)	Nonselected level	Off

Table 3 Relation between SHL and Scan Direction of Selected Line (When LSI is Used as Row Driver)

SHL	Shift Direction of Shift Register	Scan Direction of Selected Line
V_{CC}	E→ 1→ 2→ 3→ 4––––––→160	Y1→ Y2→ Y3→ Y4––––––→Y160
GND	E→ 160→ 159→ 158→ 157––––––→1	Y160→ Y159→ Y158→ Y157––––––→Y1

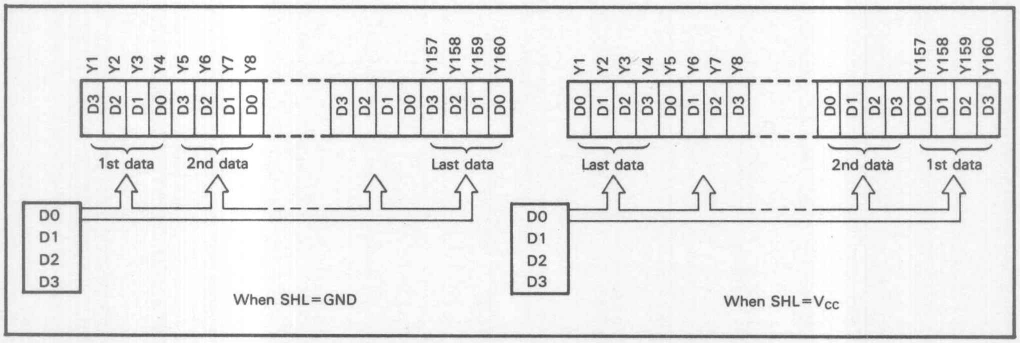


Figure 2 Relation between SHL and Data Output

LCD Drive Interface

Y1-Y160: Each Y outputs one of the four voltage levels-V_1, V_2, V_3, V_4-according to the combination of M and display data (figure 3).

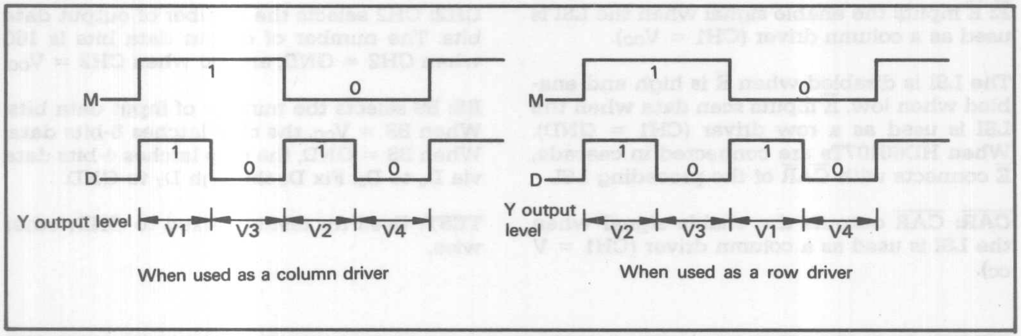
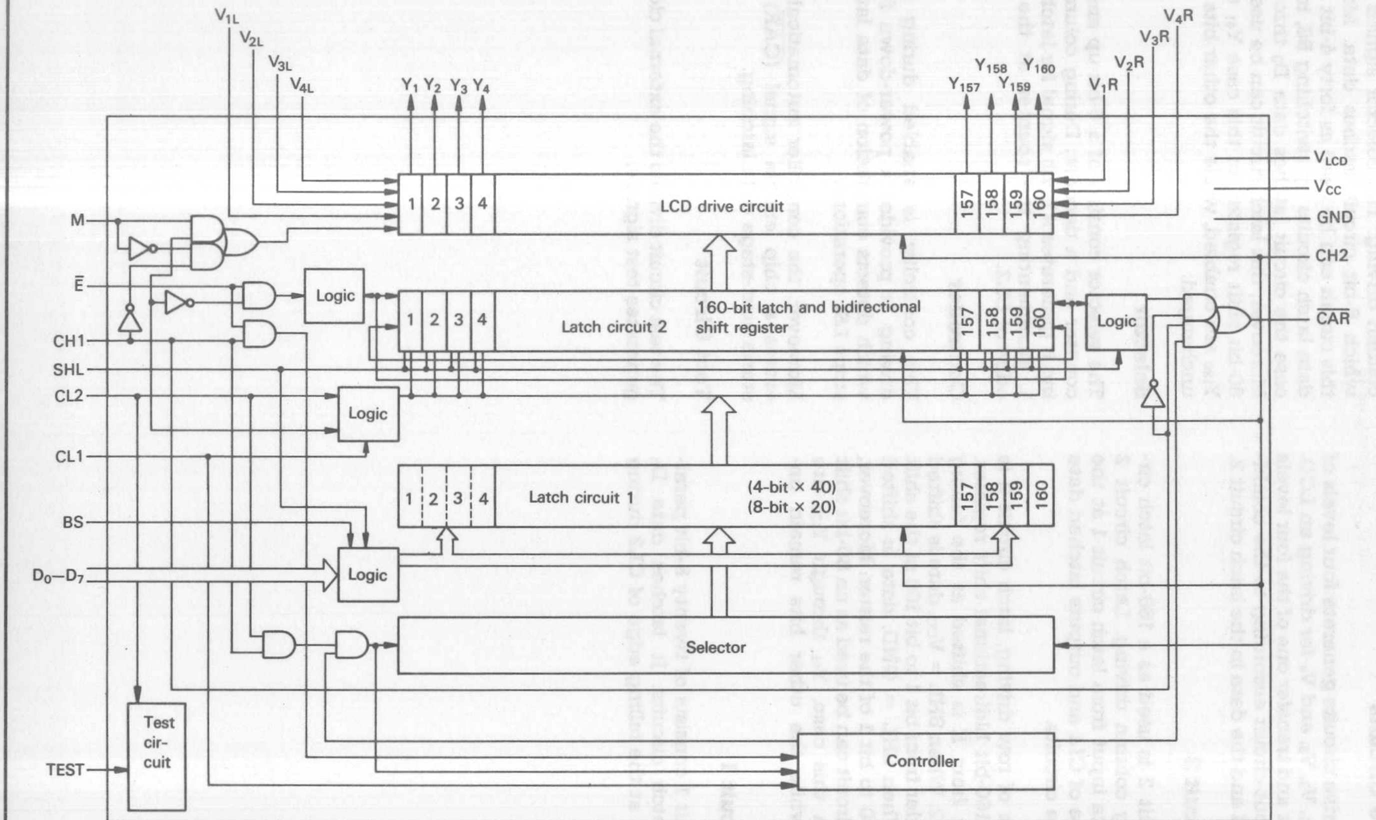


Figure 3 Selection of LCD Driver Output Level

Block Diagram



Function

LCD Drive Circuits

The LCD drive circuits generate four levels of voltages-V_1, V_2, V_3, and V_4-for driving an LCD. They select and transfer one of the four levels to the output circuit according to the combination of M and the data in the latch circuit 2.

Latch Circuit 2

Latch circuit 2 is used as a 160-bit latch circuit during column driving. Latch circuit 2 latches data input from latch circuit 1 at the falling edge of CL1 and outputs latched data to the drive circuits.

In the case of row driving, latch circuit 2 is used as a 160-bit bidirectional shift register. Data input from $\overline{E}$ is shifted at the falling edge of CL2. When SHL = V_{CC}, data is shifted in input order from bit 1 to bit 160 of the shift register. When SHL = GND, data is shifted from bit 160 to bit 1 of the reister. Moreover, this latch circuit can be used as an 80-bit shift register. In this case, Y_{41} through Y_{120} are enabled, while the other bits remain unchanged.

Latch Circuit 1

Latch circuit 1 consists of twenty 8-bit parallel data latch circuits. It latches data D_0 through D_7 at the falling edge of CL2 during column driving. The selector signals specify which 8-bit circuit latches data. Moreover, this circuit can be used as forty 4-bit parallel data latch circuits by switching BS, in which case the circuit latches data D_0 through D_3. Moreover, this latch circuit can be used as an 80-bit shift register. In this case Y_{41} through Y_{120} are enabled, while the other bits remain unchanged.

Selector

The selector consists of a 6-bit up and down counter and a decoder. During column driving it generates a latch signal for latch circuit 1, incrementing the counter at the falling edge of CL2.

Controller

This controller is enabled during column driving. It provides a power-down function which detects completion of data latch and stops LSI operations.

Moreover, the controller automatically generates a chip enable signal ($\overline{CAR}$) which starts next-stage data latching.

Test Circuit

The test circuit divides the external clock and generates test signals.

Fundamental Operations

Column Driving (1)

- CH2 = GND (160-bit data output mode)
- BS = V_{CC} (8-bit data latch mode)

The HD66107T starts data latch when $\overline{E}$ is at low level. In this case, 8-bit parallel data is latched at the falling edge of CL2. When 160-bit data latch is completed, the HD66107T automatically stops and enters standby mode and $\overline{CAR}$ is goes to low level. If $\overline{CAR}$ is connected with $\overline{E}$ of the next-stage LSI, this next-stage LSI is activated when $\overline{CAR}$ of the previous LSI goes low.

Data is output at the falling edge of CL1. When SHL = GND, data d_1 is output to pin Y1 and d_{160} to Y_{160}. On the other hand, when SHL = V_{CC}, data d_{160} is output to pin Y1 and d1 to Y_{160}. The output level is selected from among V_1-V_4 according to the combination of display data and alternating signal M. See figure 4.

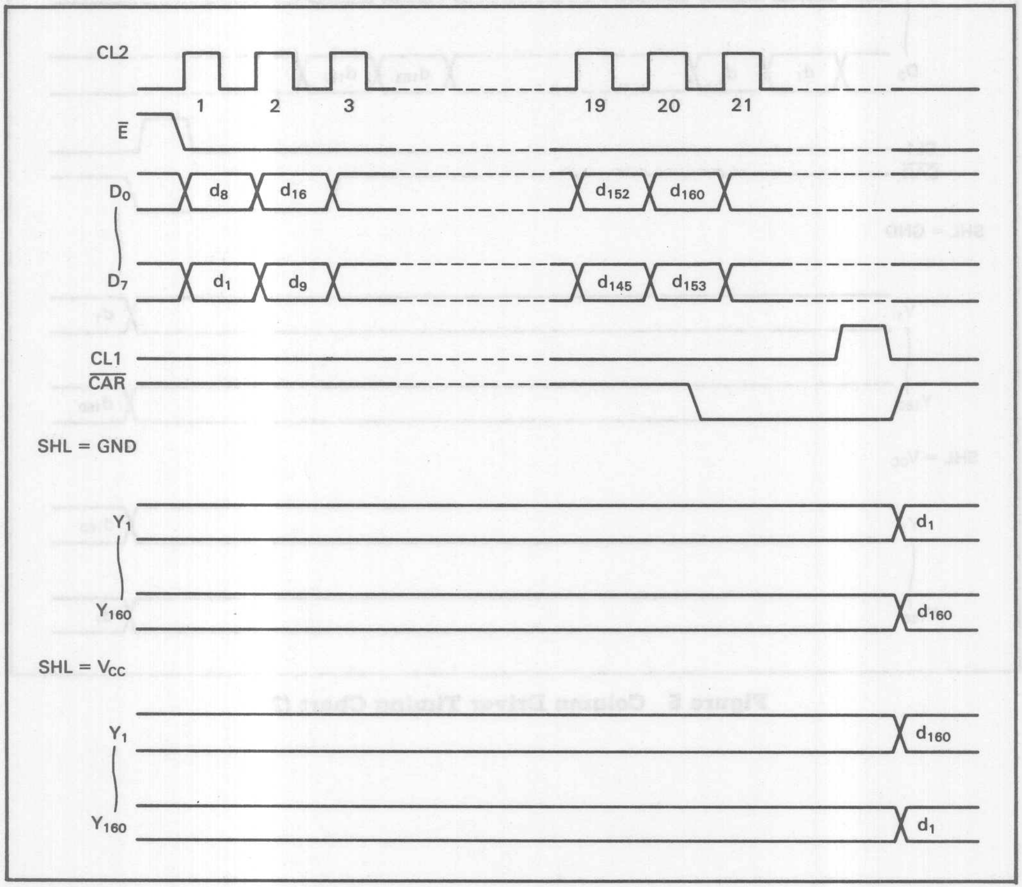


Figure 4 Column Driver Timing Chart (1)

Column Driving (2)

- CH2 = GND (160-bit data output mode)
- BS = GND (4-bit data latch mode)

4-bit display data (D_0-D_3) is latched at the falling edge of CL2. Other operations are performed in the same way as described in "Column Driving (1)". See figure 5.

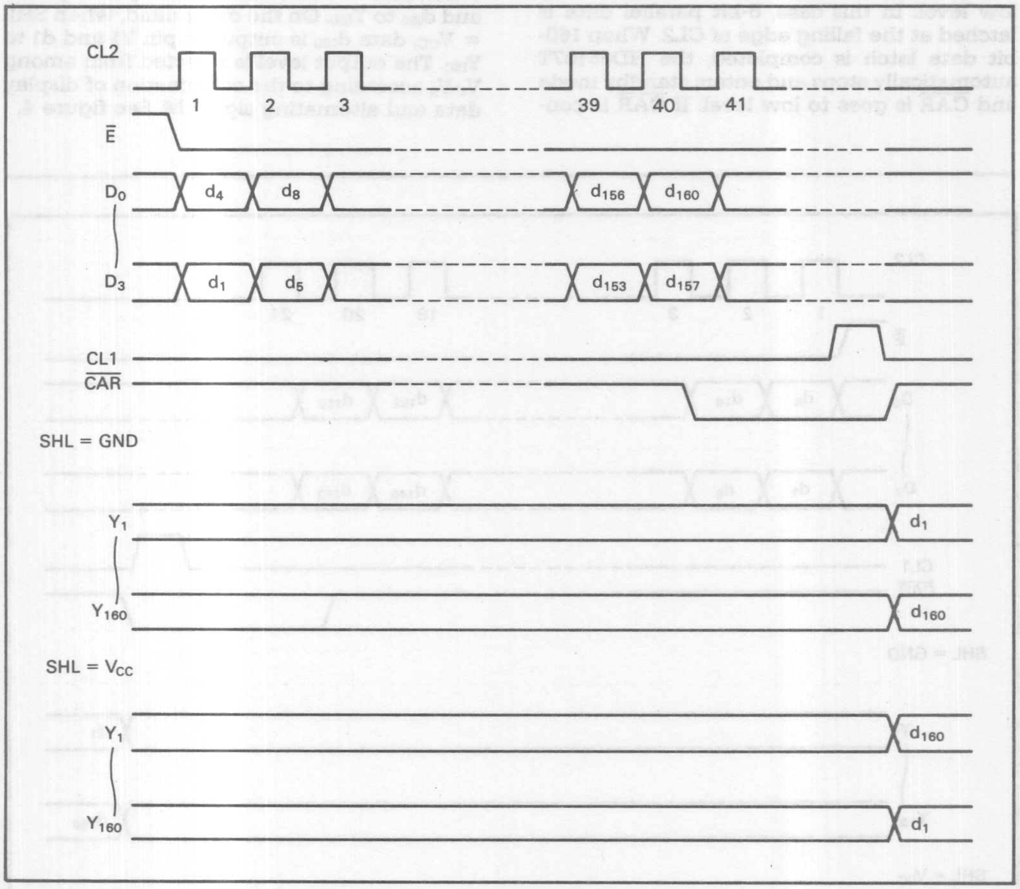


Figure 5 Column Driver Timing Chart (2)

Column Driving (3)

- CH2 = V_{CC} (80-bit data output mode)
- BS = V_{CC} (8-bit data latch mode)

When CH2 is high (V_{CC}), the HD66107T can be used as an 80-bit column driver. In this case, Y_{41} through Y_{120} are enabled, the states of Y_1 through Y_{40} and Y_{121} through Y_{160} remain unchanged.

When SHL = GND, data d1 is output to pin Y_{41} and d_{80} is output to Y_{120}. Conversely, when SHL = V_{CC}, data d_{80} is output to Y_{41} and d_1 is output to Y_{120}. See figure 6.

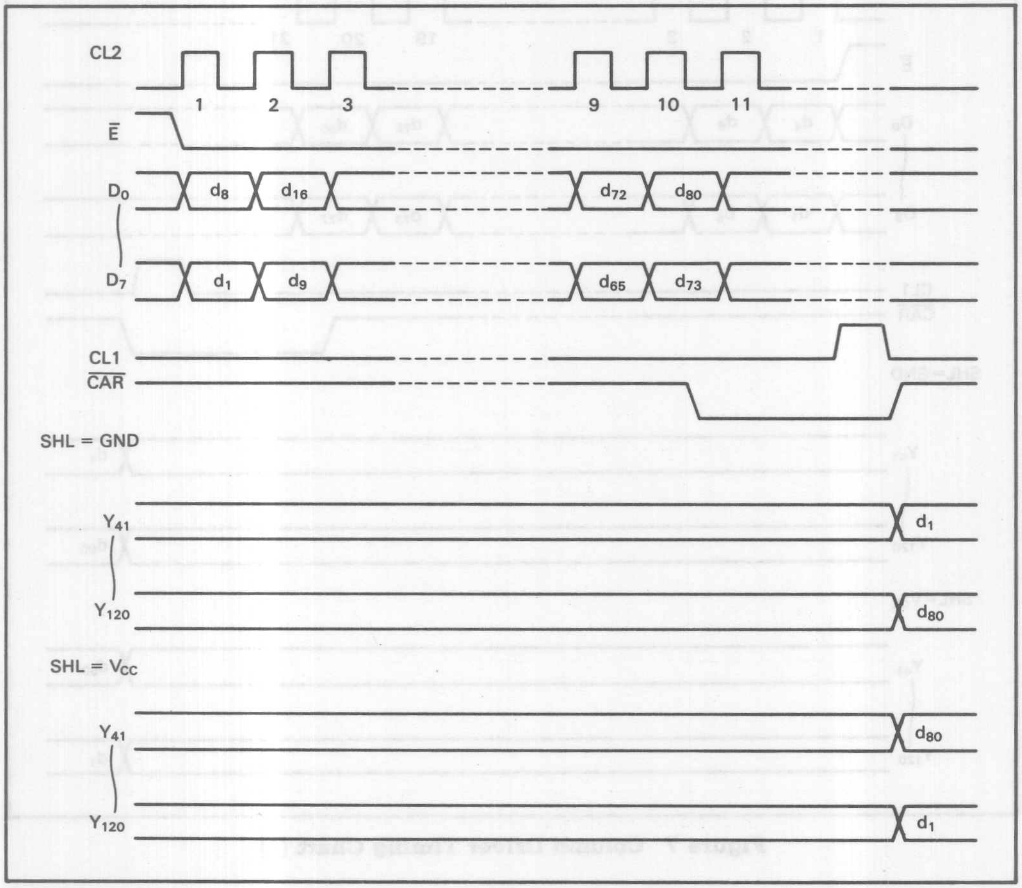


Figure 6 Column Driver Timing Chart (3)

Column Driving (4)

- CH2 = V_{CC} (80-bit data output mode)
- BS = GND (4-bit data latch mode)

When CH2 = V_{CC} and BS = GND, 4-bit parallel data is latched, while 80-bit data is output. The output of latched data is performed in described in "Column Driving (3)". See figure 7.

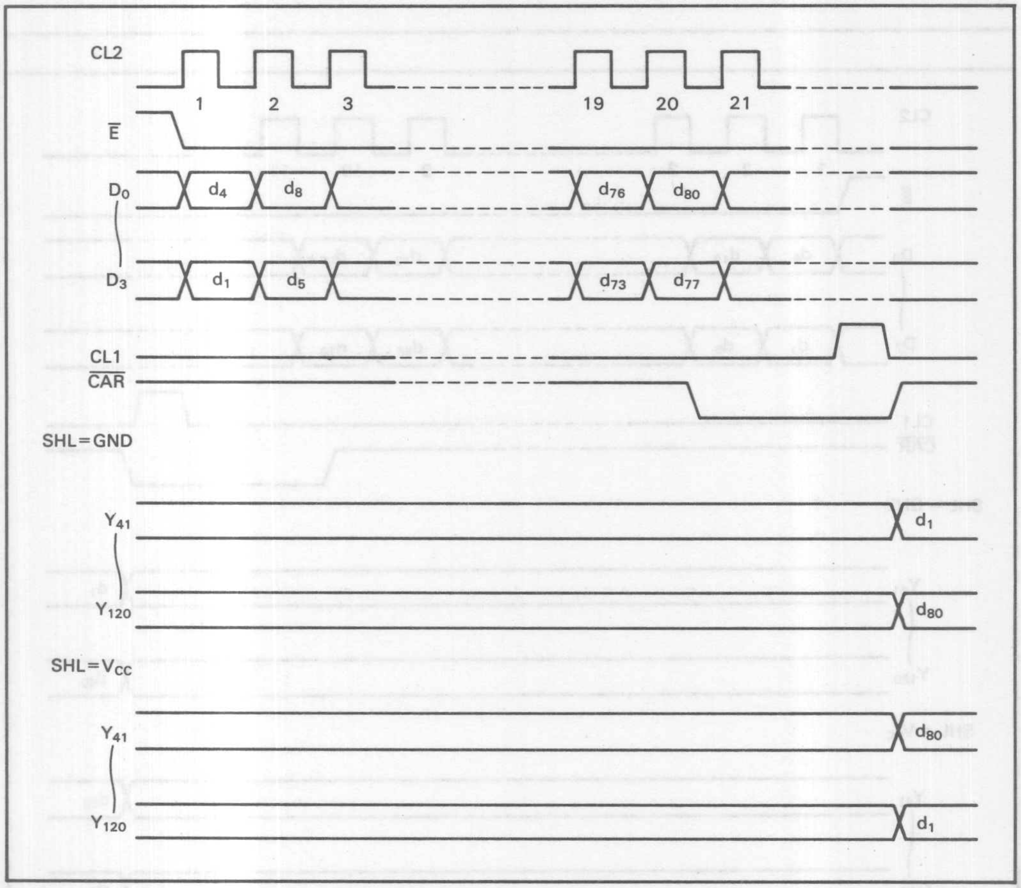


Figure 7 Column Driver Timing Chart (4)

Row Driving (1)

· CH2 = GND (160-bit data output mode)

The HD66107T shifts line scan data input through $\overline{E}$ at the falling edge of CL2.

When SHL = V_{CC}, 160-bit data is shifted from Y_1 to Y_{160}, whereas when SHL = GND, data is shifted from Y_{160} to Y_1. In both cases the HD66107T outputs the data delayed for 160 bits by the shift register through $\overline{CAR}$, becoming line scan data for the next IC driver. See figure 8.

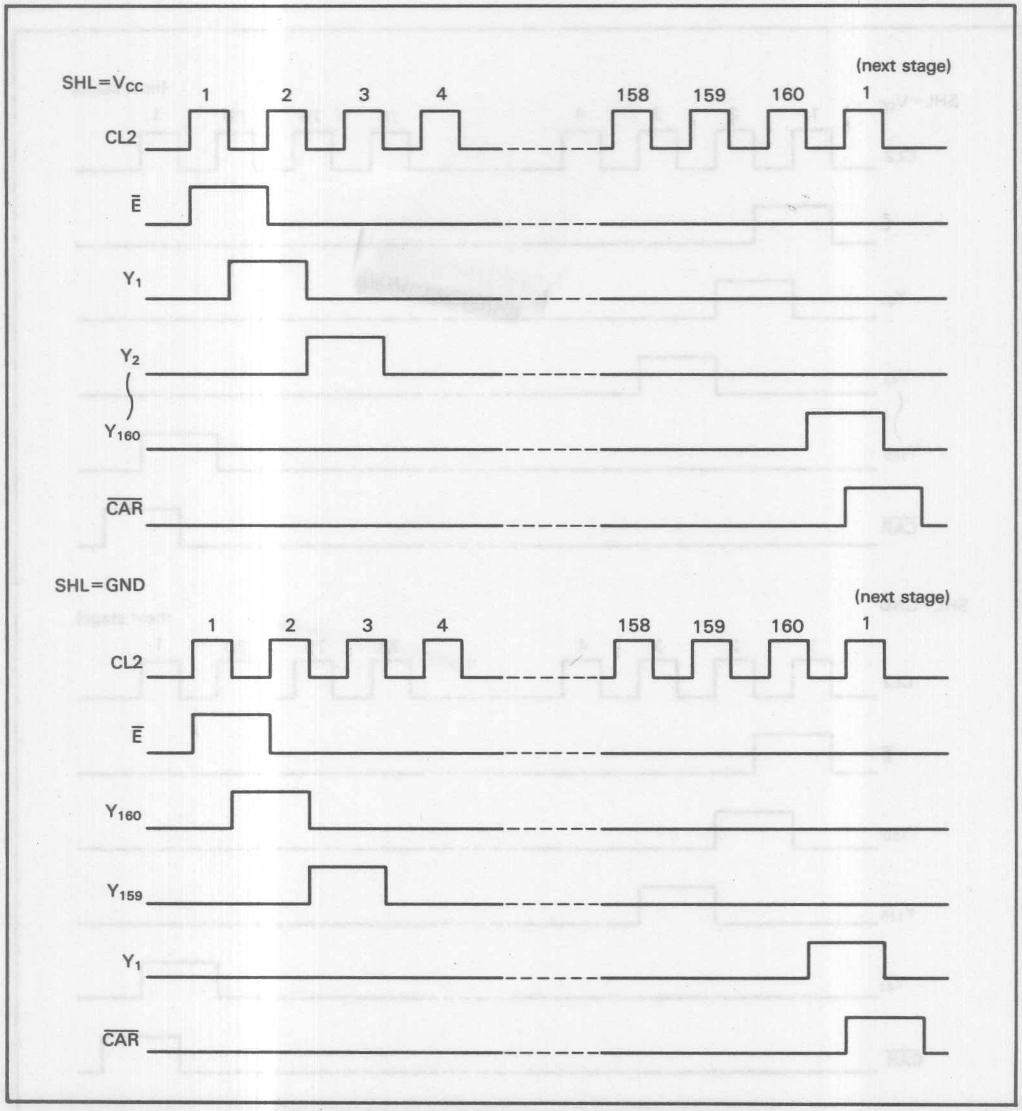


Figure 8 Row Driver Timing Chart (1)

Row Driving (2)

· CH2 = V_{CC} (80-bit data output mode)

When CH2 is high, the HD66107T can be used as an 80-bit row driver. In this case, Y_{41} to Y_{120} are enabled, while the other bits remain unchanged.

Line scan data input through $\overline{E}$ is shifted at the falling edge of CL2. When SHL = V_{CC}, data is shifted from Y_{41} to Y_{120}. Conversely, when SHL = GND, data is shifted from Y_{120} to Y_{41}. In both cases the HD66107T outputs the data delayed for 80 bits by the shift register through $\overline{CAR}$, becoming line scan data for the next LSI. See figure 9.

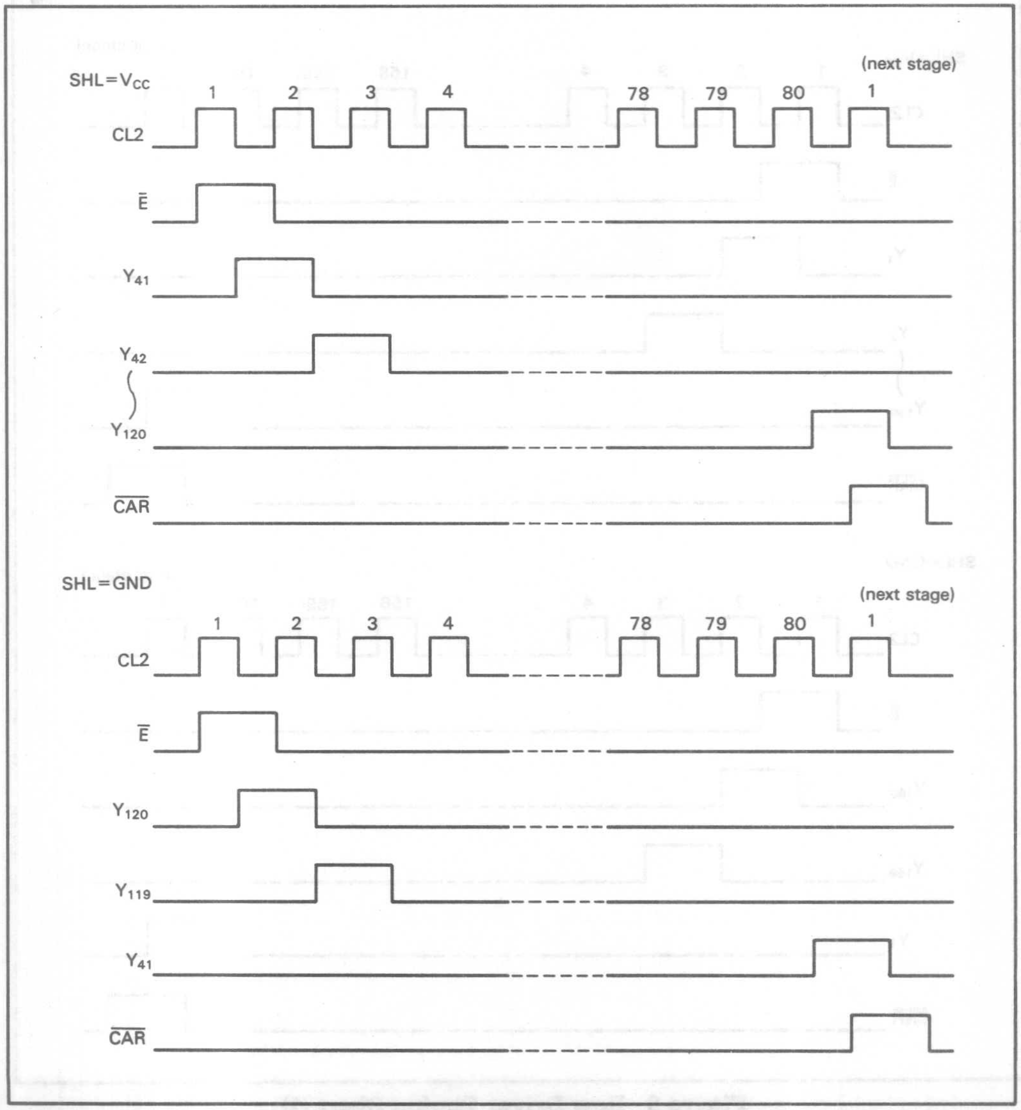
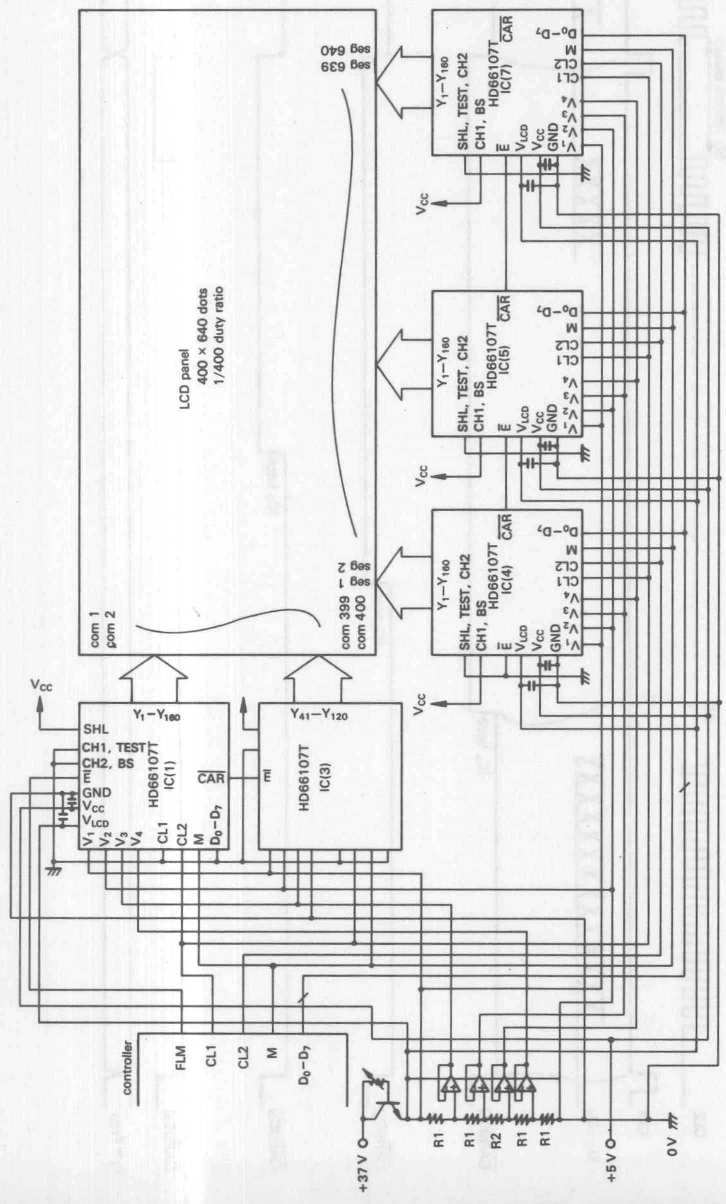


Figure 9 Row Driver Timing Chart (2)

Application

The following example shows a system configuration for driving a 640×400-dot LCD panel using the HD66107T.



Notes 1. R1 and R2 are specified depending on the type of LCD panel. When using an LCD panel with 1/20 bias, R1/(4R1 + R2) must be 1/20, i.e., R1 = 3kΩ and R2 = 48kΩ.

Notes 2. When designing a board, place capacitors close to each LSI in order to stabilize power supply. It is recommended to use two 0.1 μF capacitors per LSI; one is connected between V_{CC} and GND, and the other between V_{LCD} and GND.

Figure 10 Application Example

Waveform Examples

Column Driving

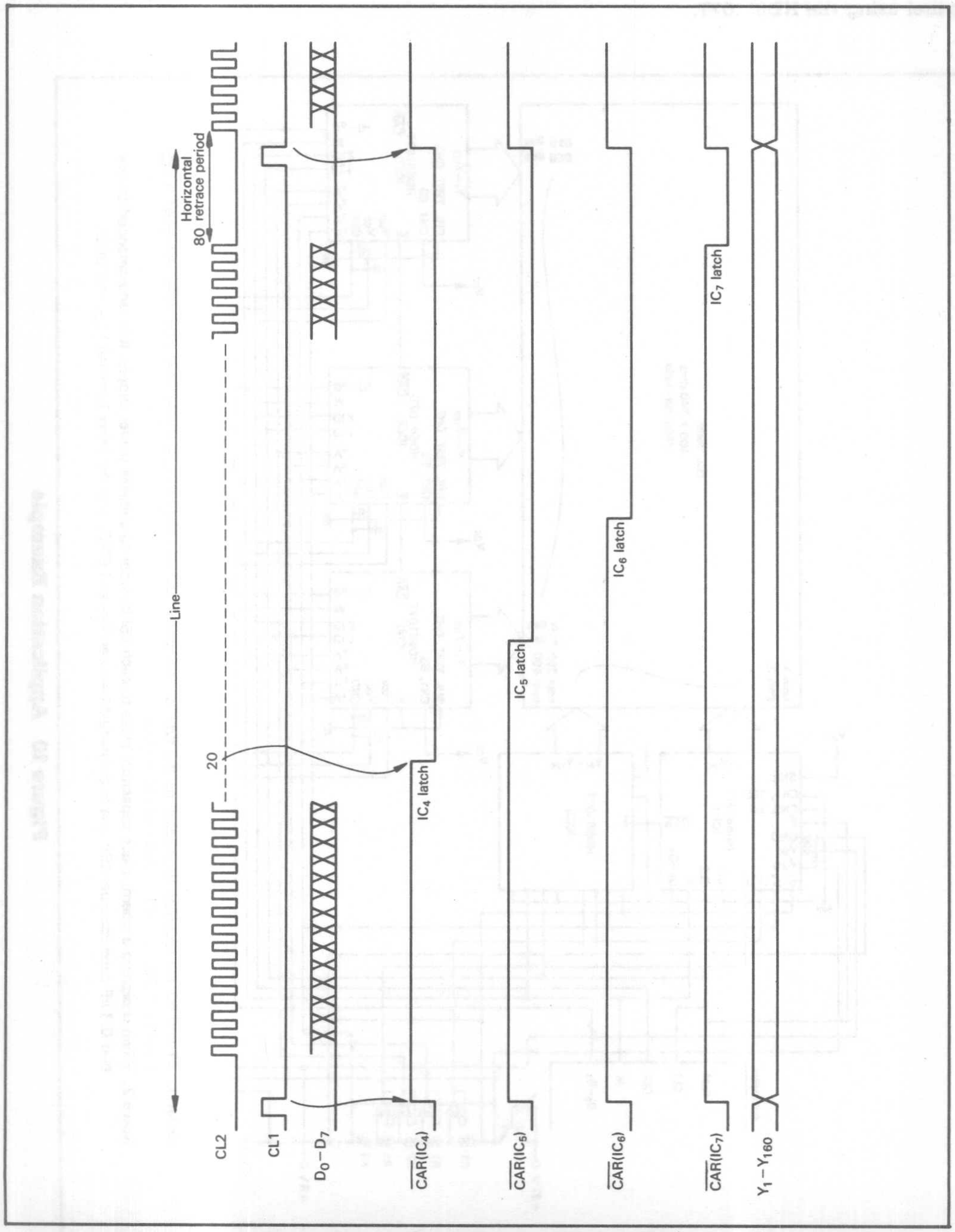


Figure 11 Column Driver Timing Chart

Row Driving

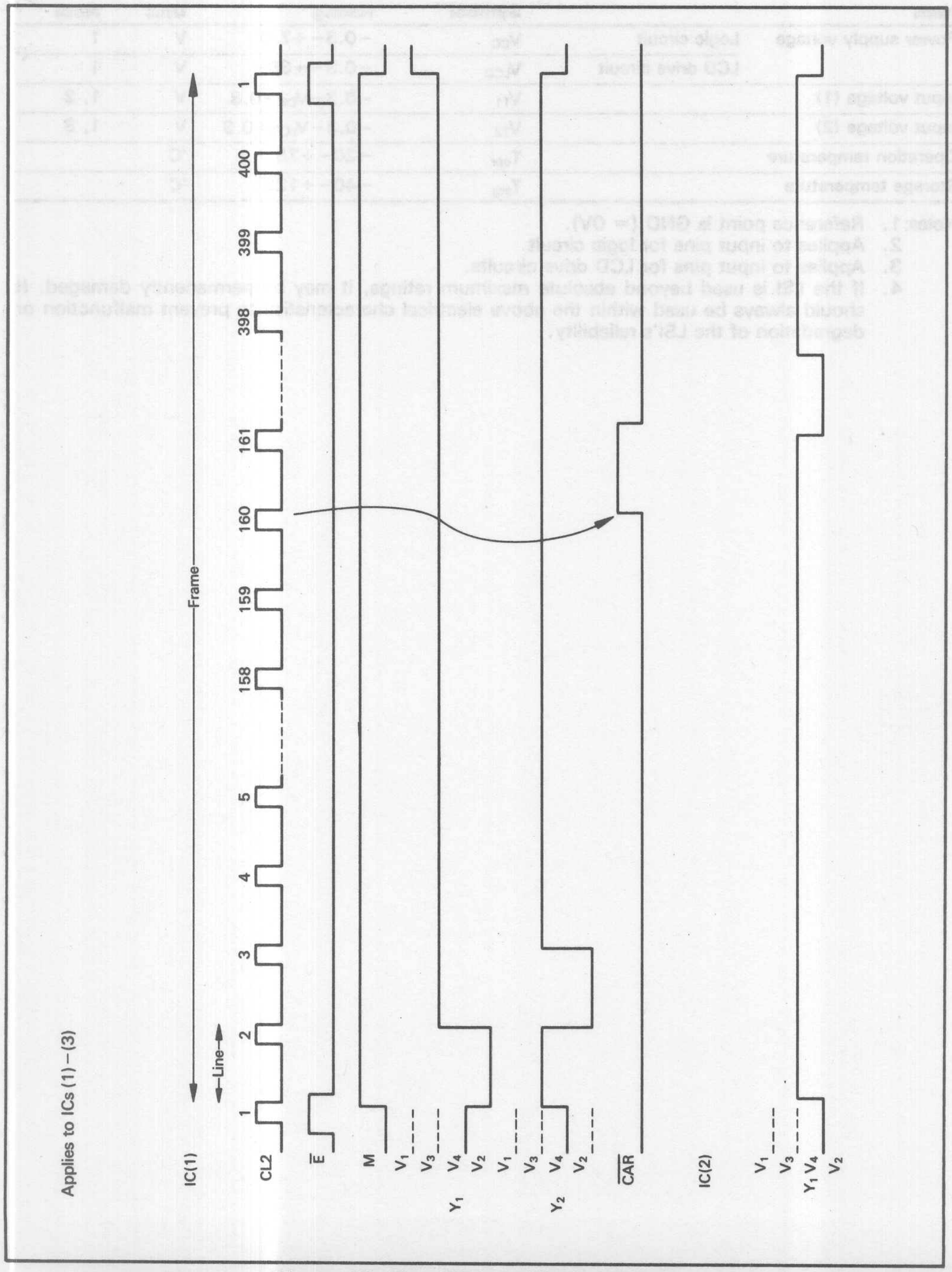


Figure 12 Row Driver Timing Chart

Absolute Maximum Rating

Item		Symbol	Rating	Unit	Note
Power supply voltage	Logic circuit	V_{CC}	−0.3− +7.0	V	1
	LCD drive circuit	V_{LCD}	−0.3− +38	V	1
Input voltage (1)		V_{T1}	−0.3−V_{CC}+0.3	V	1, 2
Input voltage (2)		V_{T2}	−0.3−V_{LCD}+0.3	V	1, 3
Operation temperature		T_{opr}	−20− +75	°C	
Storage temperature		T_{stg}	−40− +125	°C	

Notes:
1. Reference point is GND (= 0V).
2. Applies to input pins for logic circuit.
3. Applies to input pins for LCD drive circuits.
4. If the LSI is used beyond absolute maximum ratings, it may be permanently damaged. It should always be used within the above electrical characteristics to prevent malfunction or degradation of the LSI's reliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ± 10%, V_{LCD} = 14 to 37 V, Ta = −20 to 75°C)

Item	Symbol	Pins	Min.	Max.	Unit	Condition	Note
Input high voltage	V_{IH}	CL1, CL2, M SHL, BS, CH2,	0.8 × V_{CC}	V_{CC}	V		
Input low voltage	V_{IL}	TEST, D_0-D_7, $\overline{E}$, CH1	0	0.2 × V_{CC}	V		
Output high voltage	V_{OH}	$\overline{CAR}$	V_{CC}−0.4	–	V	I_{OH}=−0.4 mA	
Output low voltage	V_{OL}		–	0.4	V	I_{OL}=0.4 mA	
Vi−Yj on resistance	R_{ON}	Y1−Y160, V1−V4	–	3.0	kΩ	I_{ON}=150 μA	4
Input leak current (1)	I_{IL1}	CL1, CL2, M SHL, BS, CH2, TEST, D_0−D_7, $\overline{E}$, CH1	−5.0	5.0	μA	V_{IN}=V_{CC}−GND	
Input leak current (2)	I_{IL2}	V1−V4	−100	100	μA	V_{IN}=V_{LCD}−GND	
Power dissipation (1)	I_{CC1}		–	5.0	mA	f_{CL2}=8 MHz	1
Power dissipation (2)	I_{LCD1}		–	2.0	mA	f_{CL1}=28 kHz	2
Power dissipation (3)	I_{ST}		–	0.5	mA	In standby mode: f_{CL2}=8 MHz, f_{CL1}=28 kHz	1 2
Power dissipation (4)	I_{CC2}		–	1.0	mA	f_{fcL1}=28 kHz	1
Power dissipation (5)	I_{LCD2}		–	0.5	mA	fm=35 Hz	3

Notes: 1. Input and output current is excluded. When an input is at the intermediate level is CMOS, excessive current flows from the power supply though the input circuit. To avoid it, V_{IH} and V_{IL} must be fixed to V_{CC} and GND respectively.
2. Applies to column driving.
3. Applies to row driving.
4. Indicates the resistance between one pin from Y 1-Y160 and another pin from V1-V4 when load current is applied to the Y Pin; defined under the following conditions.
V_{LCD}−GND=370
V1, V3=V_{LCD}− {2/20(V_{LCD}-GND)}
V2, V4=V_{LCD}+ {2/20(V_{LCD}-GND)}
This section explains the range of power supply voltage for driving LCD. V 1 and V3 voltage should be near V_{LCD}, and V2 and V4 should be near GND (figure 13).
Each voltage must be within ΔV. ΔV determines the range within which R_{ON}, impedance of driver's output, is stable. Note thatΔV depends on power supply voltage V_{LCD}-GND (figure 14).

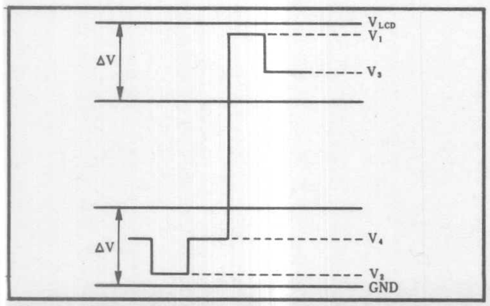


Figure 13 Driver's Output Waveform and Each Level of Voltage

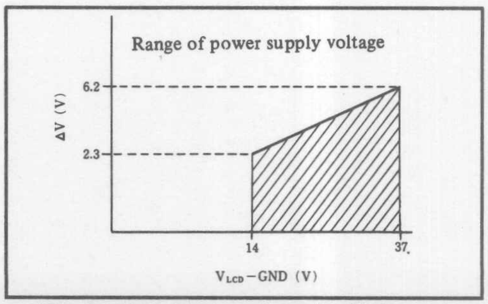


Figure 14 Power Supply Voltage V_{LCD}-GND and ΔV

AC Characteristics (V_{CC} = 5 V ± 10%, V_{LCD} = 14 to 37 V, Ta = −20 to 75°C)

Column Driving

Item	Symbol	Pin name	Min.	Max.	Unit	Note
Clock cycle time	t_{cyc}	CL2	125	–	ns	
Clock high-level width (1)	t_{CWH1}	CL2	30	–	ns	
Clock high-level width (2)	t_{CWH2}	CL1	60	–	ns	
Clock low-level width	t_{CWL}	CL2	30	–	ns	
Clock setup time	t_{SCL}	CL2	200	–	ns	
Clock hold time	t_{HCL}	CL2	200	–	ns	
Clock rising/falling time	tct	CL1, CL2	–	30	ns	
Data setup time	t_{DSU}	D_0–D_7	30	–	ns	
Data hold time	t_{DH}	D_0–D_7	30	–	ns	
$\overline{E}$ setup time	t_{ESU}	$\overline{E}$	25	–	ns	
Output delay time (1)	t_{DCAR1}	$\overline{CAR}$	–	70	ns	1
Output delay time (2)	t_{DCAR2}	$\overline{CAR}$	–	200	ns	1
M phase difference	t_{CM}	M, CL1	–	300	ns	

Notes: 1. Specified when connecting the load circuit shown in figure 15.

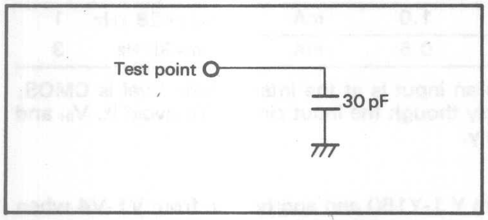


Figure 15 Test Circuit

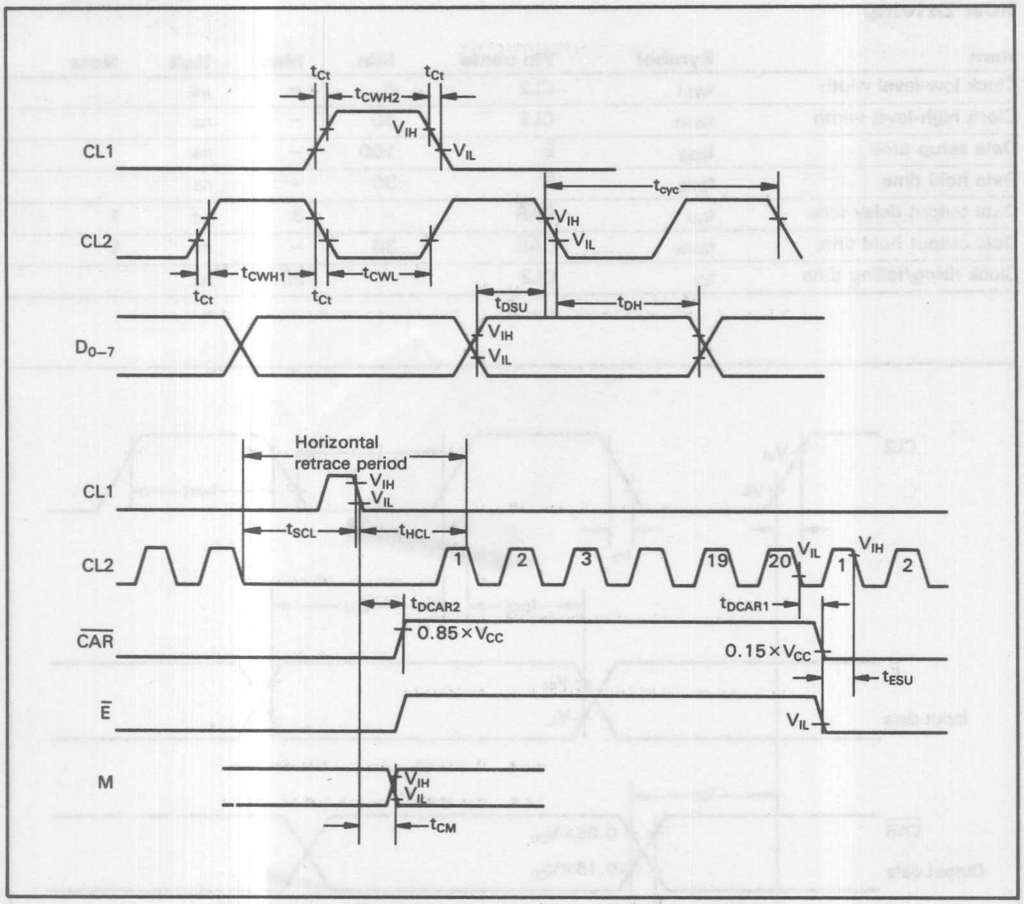


Figure 16 Controller Interface of Column Driver

Row Driving

Item	Symbol	Pin name	Min.	Max.	Unit	Note
Clock low-level width	t_{WL1}	CL2	5	–	μs	
Clock high-level width	t_{WH1}	CL2	60	–	ns	
Data setup time	t_{DS2}	$\overline{E}$	100	–	ns	
Data hold time	t_{DH2}	$\overline{E}$	30	–	ns	
Data output delay time	t_{DD}	$\overline{CAR}$	–	3	μs	1
Data output hold time	t_{DHW}	$\overline{CAR}$	30	–	ns	1
Clock rising/falling time	t_{Ct}	CL2	–	30	ns	

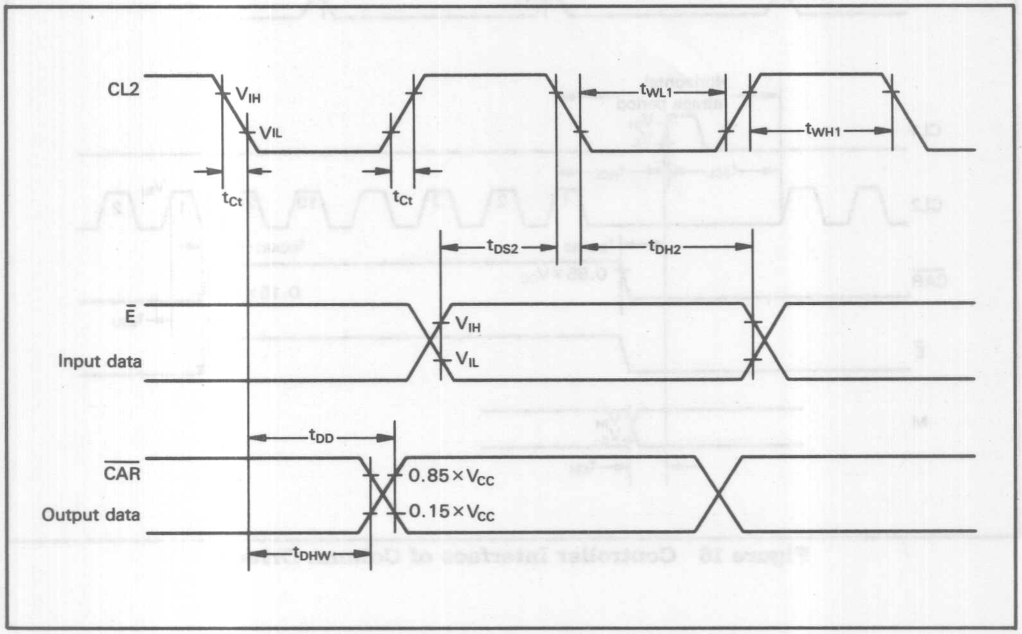


Figure 17 Controller Interface of Row Driver

HD66110RT
(Column Driver)

Description

The HD66110RT, the column driver for a large liquid crystal display (LCD) panel, features as many as 160 LCD outputs powered by 160 internal LCD drive circuits, and a high duty cycle. This device can interface to various LCD controllers by using an internal automatic chip enable signal generator. Its strip shape enables a slim tape carrier package (TCP).

Features

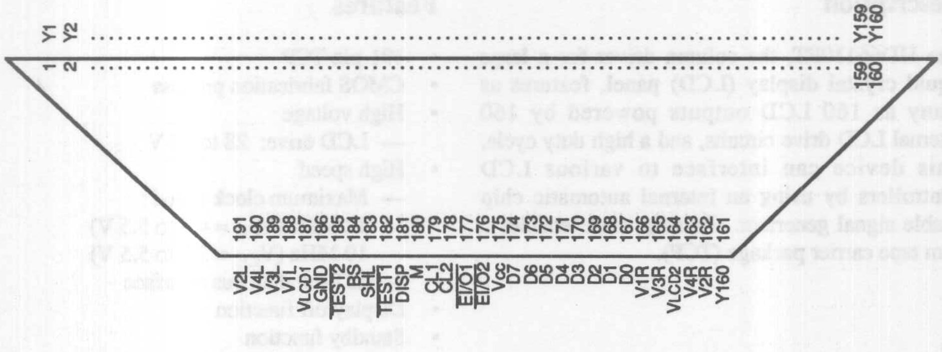
- 191-pin TCP
- CMOS fabrication process
- High voltage
  - — LCD drive: 28 to 40 V
- High speed
  - — Maximum clock speed :
    12 MHz (V_{CC} = 4.5 to 5.5 V)
    10 MHz (V_{CC} = 2.7 to 5.5 V)
- 4- and 8-bit data bus interface
- Display off function
- Standby function
- Various LCD controller interfaces
  - — LCTC series: HD63645, HD64645, HD64646
  - — LVIC series: HD66840, HD66841
  - — CLINE: HD66850

Ordering Information

Type No.	Outer lead pitch(μm)	User Area (mm)
HD66110RTA8	140	10.85
HD66110RTB0	92	11.9
HD66110RTB1	92	9.0
HD66110TA4	80	9.66

Note : The details of TCP pattern are shown in " The Information of TCP. "

Pin Arrangement



Note: This is just an example of TCP; other TCP shapes are also possible.

Pin Description

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{CC}	175	V_{CC}	—	Power supply
GND	186	GND	—	Power supply
V_{LCD1}	187	V_{LCD1}	Input	Power supply
V_{LCD2}	164	V_{LCD2}	—	Power supply
V1R	166	V1R	Input	Power supply
V2R	162	V2R	Input	Power supply
V3R	165	V3R	Input	Power supply
V4R	163	V4R	Input	Power supply
V1L	188	V1L	Input	Power supply
V2L	191	V2L	Input	Power supply
V3L	189	V3L	Input	Power supply
V4L	190	V4L	Input	Power supply
CL1	179	Clock 1	Input	Control signal
CL2	178	Clock 2	Input	Control signal
M	180	M	Input	Control signal
D_0–D_7	167–174	Data 0–data 7	Input	Control signal
SHL	183	Shift left	Input	Control signal
EI/O1, $\overline{\text{EI/O2}}$	177, 176	Enable IO 1, enable IO 2	Input/output	Control signal
$\overline{\text{DISP}}$	181	Display off	Input	Control signal
BS	184	Bus select	Input	Control signal
$\overline{\text{TEST1}}$, $\overline{\text{TEST2}}$	182, 185	Test 1, test 2	Input	Control signal
Y_1–Y_{160}	1–160	Y_1–Y_{160}	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, V_{LCD1}, V_{LCD2}, GND: V_{CC} – GND supplies power to the internal logic circuits. V_{LCD} – GND supplies power to the LCD drive circuits. See figure 1.

V1R, V1L, V2R, V2L, V3R, V3L, V4R, V4L: Supply different levels of power to drive the LCD. V1 and V2 are selected levels, and V3 and V4 are non-selected levels.

Control Signals

CL1: Inputs display data latch pulses for latch circuit 2. Latch circuit 2 latches display data input from latch circuit 1, and outputs LCD drive signals corresponding to the latched data, both at the falling edge of each CL1 pulse.

CL2: Inputs display data latch pulses for latch circuit 1. Latch circuit 1 latches display data input via D_0–D_7 at the falling edge of each CL2 pulse.

M: Changes LCD drive outputs to AC.

D_0–D_7: Input display data. High-voltage level (V_{CC} level) of data corresponds to a selected level and turns an LCD pixel on, and low-voltage level (GND level) data corresponds to a non-selected level and turns an LCD pixel off.

SHL: Shifts the destinations of display data output, and determines which chip enable pin ($\overline{\text{EI/O1}}$ or $\overline{\text{EI/O2}}$) is an input and which is an output. See figure 2.

$\overline{\text{EI/O1}}$, $\overline{\text{EI/O2}}$: If SHL is GND level, $\overline{\text{EI/O1}}$ inputs the chip enable signal, and $\overline{\text{EI/O2}}$ outputs the signal. If SHL is Vcc level, $\overline{\text{EI/O1}}$ outputs the chip enable signal, and $\overline{\text{EI/O2}}$ inputs the signal. The chip enable input pin of the first HD66110RT must be grounded, and those of the other HD66110RTs must be connected to the chip enable output pin of the previous HD66110RT. The chip enable output pin of the last HD66110RT must be open.

$\overline{\text{DISP}}$: A low $\overline{\text{DISP}}$ sets LCD drive outputs Y_1–Y_{160} to V2 level.

BS: Selects either the 4-bit or 8-bit display data bus interface. If BS is V_{CC} level, the 8-bit bus is selected, and if BS is GND level, the 4-bit bus is selected. In 4-bit bus mode, data is latched via D_0–D_3; D_4–D_7 must be grounded.

$\overline{\text{TEST1}}$, $\overline{\text{TEST2}}$: Used to test the LSI, and must be connected to V_{CC} level.

LCD Drive Output

Y_1–Y_{160}: Each Y outputs one of the four voltage levels V1, V2, V3, or V4, depending on a combination of the M signal and display data levels. See figure 3.

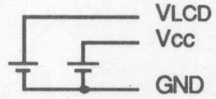


Figure 1 Power Supply for Logic and LCD Drive Circuits

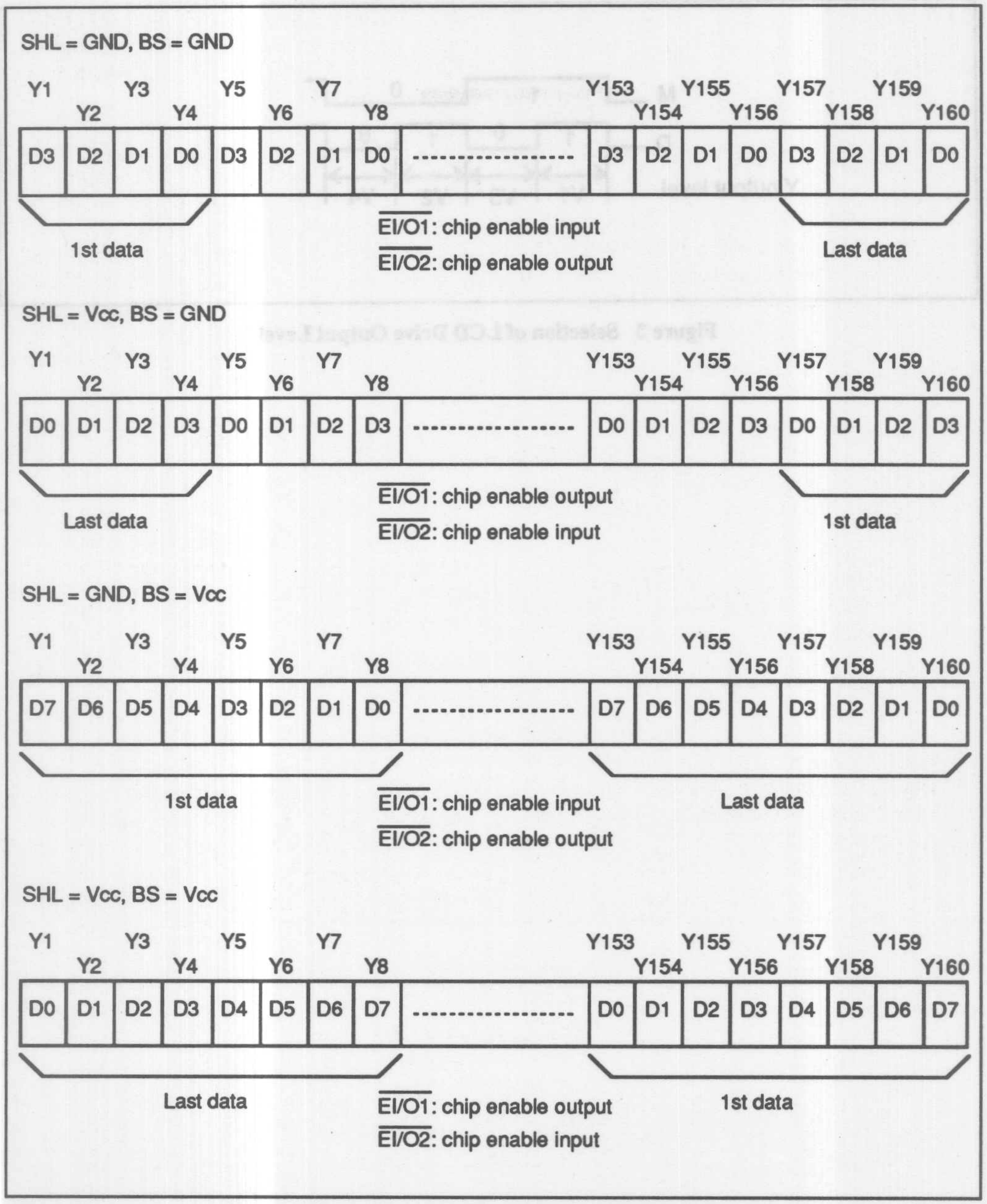


Figure 2 Selection of Destinations of Display Data Output

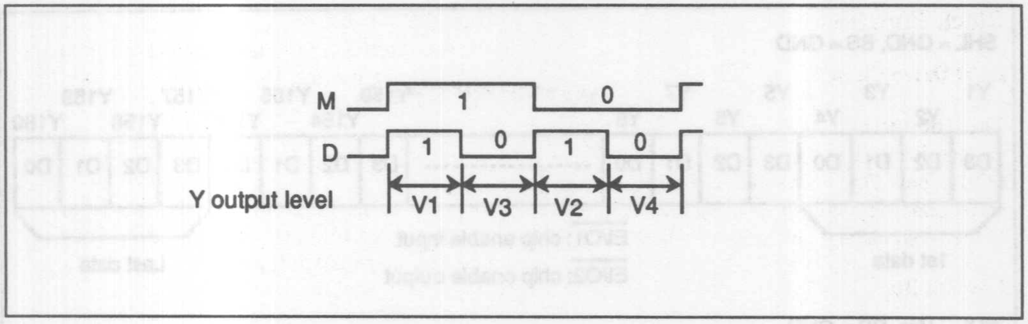


Figure 3 Selection of LCD Drive Output Level

Block Functions

LCD Drive Circuit

The 160-bit LCD drive circuit generates four voltage levels V1, V2, V3, and V4, for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on a combination of the M signal and the data in the latch circuit 2.

Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

Latch Circuit 2

160-bit latch circuit 2 latches data input from latch circuit 1, and outputs the latched data to the level shifter, both at the falling edge of each clock 1 (CL1) pulse.

Latch Circuit 1

160-bit latch circuit 1 latches 4-bit or 8-bit parallel data input via the D_0 to D_7 pins at the timing generated by the shift register.

Shift Register

The 40-bit shift register generates and outputs data latch signals for latch circuit 1 at the falling edge of each clock 2 (CL2) pulse.

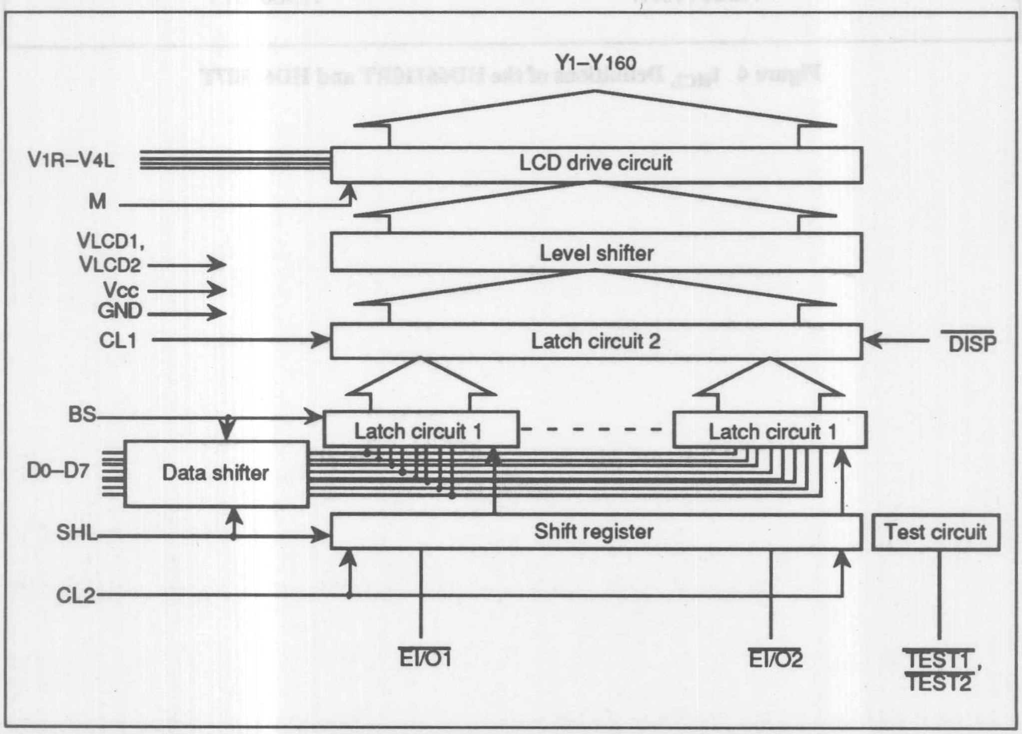
Data Shifter

The data shifter shifts the destinations of display data output, when necessary.

Test Circuit

The test circuit divides the external clock pulses and generates test signals ($\overline{\text{TEST1}}$ and $\overline{\text{TEST2}}$).

Block Diagram



Comparison of the HD66110RT with the HD66107T

Item		HD66110RT	HD66107T
Common LCD drive circuits		Not provided	160
Column LCD drive circuits		160	160 or 80
LCD drive voltage range		28 to 40 V	14 to 37 V
Speed	V_{CC} = 4.5 to 5.5 V	12 MHz	8 MHz
	V_{CC} = 2.7 to 4.5 V	10 MHz	—
Clock hold time (t_{HCL}) definition		From the falling edge of CL1 to the rising edge of CL2 (figure 1)	From the falling edge of CL1 to the falling edge of CL2 (figure 1)
Test pin level at normal operation		V_{CC}	GND
Display off function		Provided	Not provided
TCP shape		Can be thin	Cannot be thin

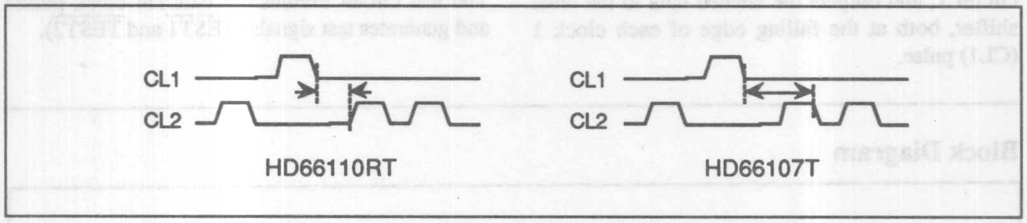


Figure 4 t_{HCL} Definitions of the HD66110RT and HD66107T

Operation Timing

4-Bit Bus Mode (BS = GND)

Figure 5 shows 4-bit data latch timing when SHL = GND, that is, the $\overline{\text{EI/O1}}$ pin is a chip enable input and $\overline{\text{EI/O2}}$ pin is a chip enable output. When SHL = V_{CC}, the $\overline{\text{EI/O1}}$ pin is a chip enable output and $\overline{\text{EI/O2}}$ pin is a chip enable input.

When a low chip enable signal is input via the $\overline{\text{EI/O1}}$ pin, the HD66110RT is first released from data standby state, and, at the falling edge of the following CL2 pulse, it is released entirely from standby state and starts latching data.

It simultaneously latches 4 bits of data at the falling edge of each CL2 pulse. When it has latched 156 bits of data, it sets the $\overline{\text{EI/O2}}$ signal low. When it has latched 160 bits of data, it automatically stops and enters standby state, initiating the next HD66110RT, as long as its $\overline{\text{EI/O2}}$ pin is connected to the $\overline{\text{EI/O1}}$ pin of the next HD66110RT.

The HD66110RTs output one line of data from the Y_1–Y_{160} pins at the falling edge of each CL1 pulse. Data d_1 is output from Y_1, and d_{160} from Y_{160} when SHL = GND, and d_1 is output from Y_{160}, and d_{160} from Y_1 when SHL = V_{CC}.

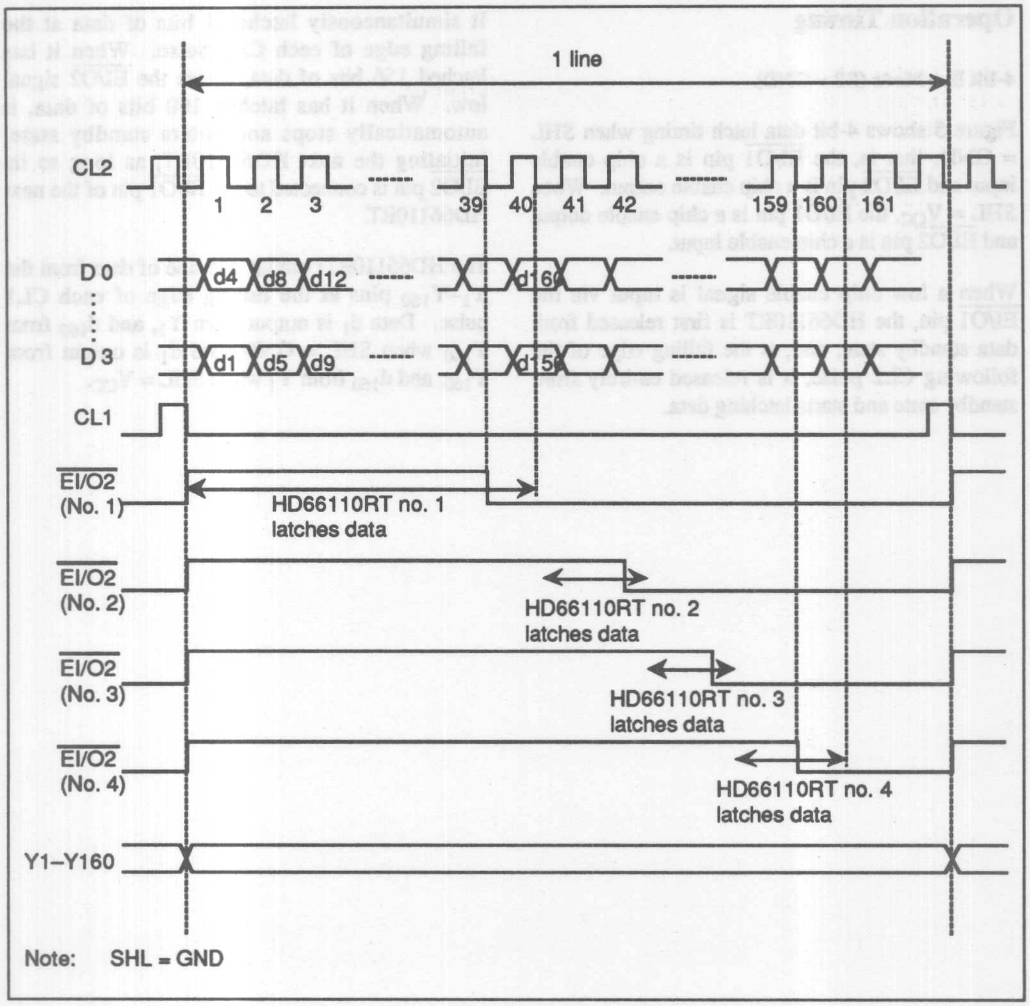


Figure 5 4-Bit Data Latch Timing (SHL = GND)

8-Bit Bus Mode (BS = V_{CC})

Figure 6 shows 8-bit data latch timing when SHL = GND, that is, the $\overline{EI/O1}$ pin is a chip enable input and $\overline{EI/O2}$ pin is a chip enable output.

When SHL = V_{CC}, the $\overline{EI/O1}$ pin is a chip enable output and $\overline{EI/O2}$ pin is a chip enable input.

The operation is the same as that in 4-bit bus mode except that 8 bits of data are latched simultaneously.

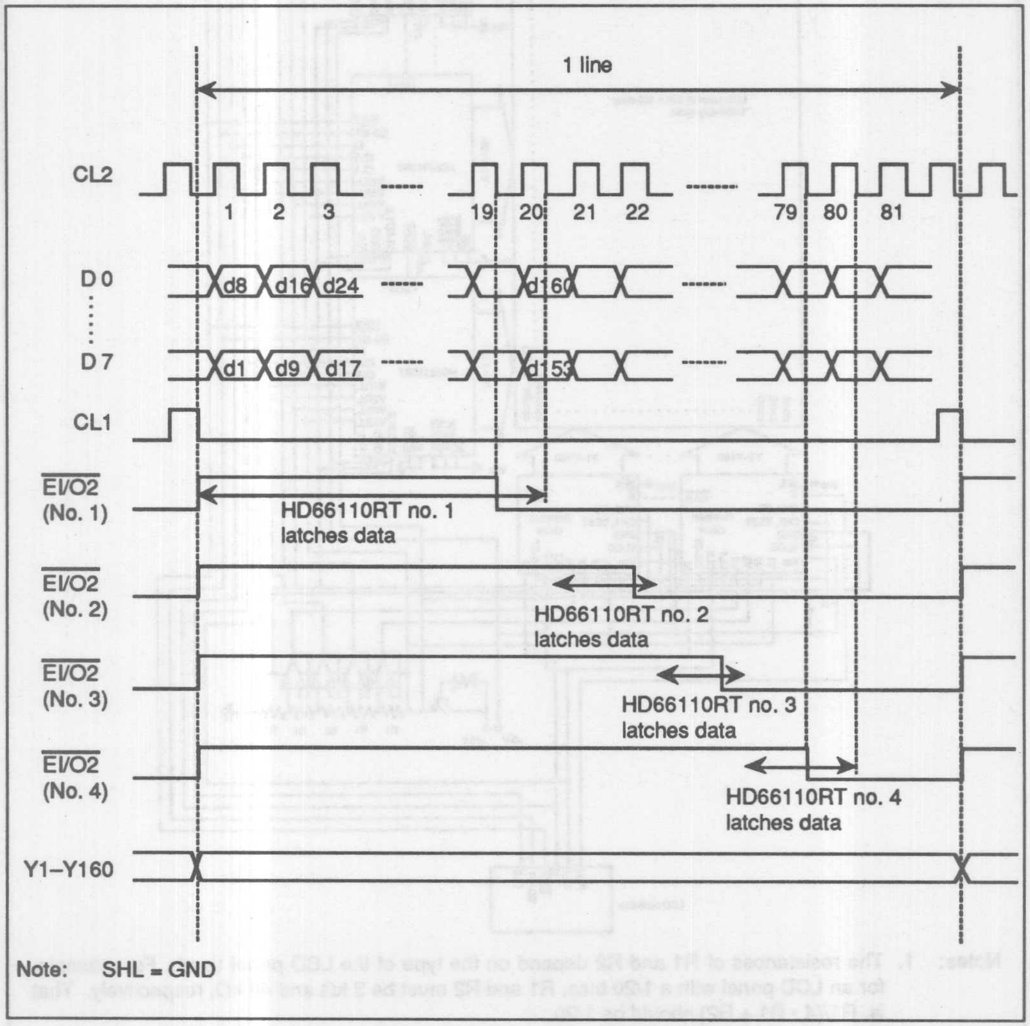
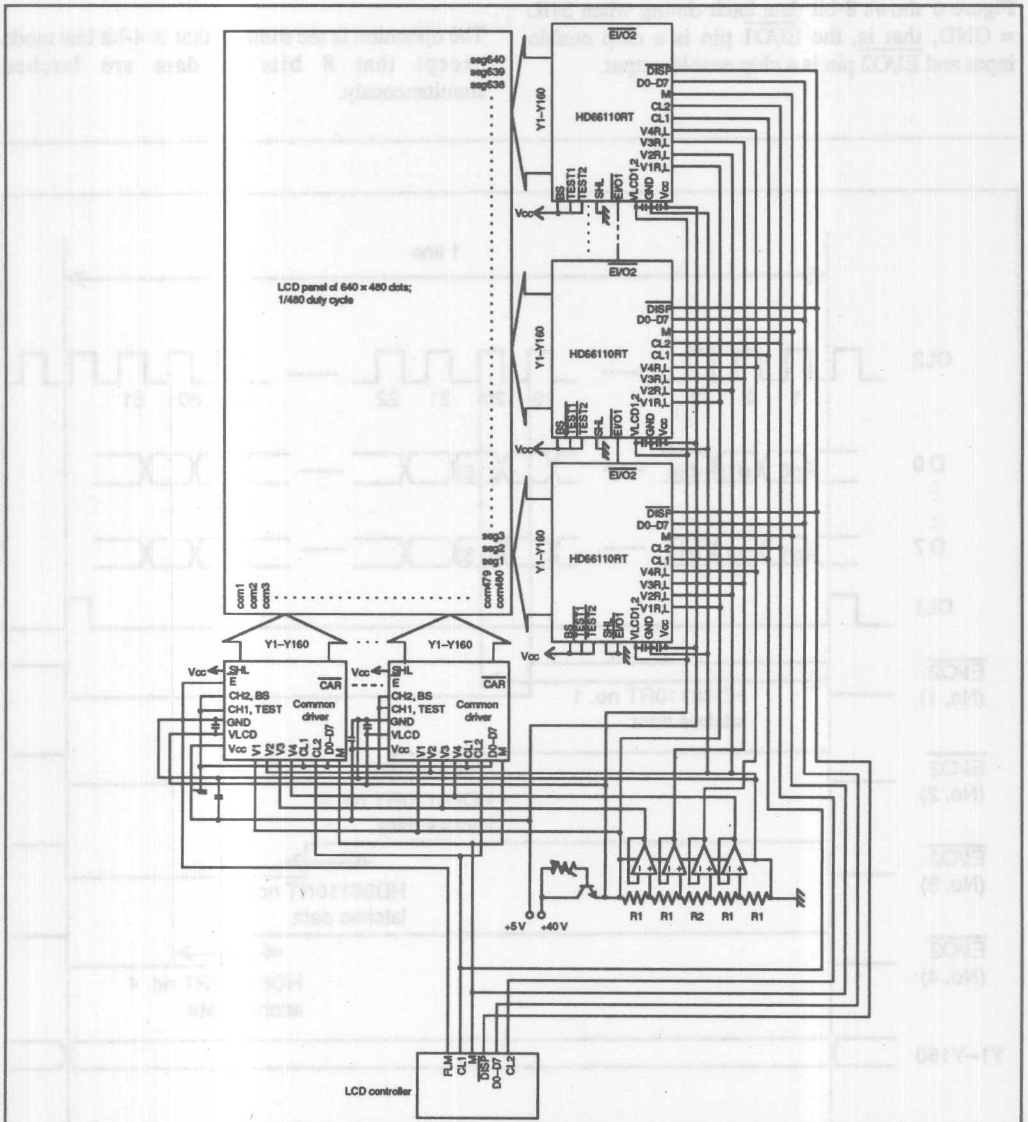


Figure 6 8-Bit Data Latch Timing (SHL = GND)

Application Example



Notes: 1. The resistances of R1 and R2 depend on the type of the LCD panel used. For example, for an LCD panel with a 1/20 bias, R1 and R2 must be 3 kΩ and 48 kΩ, respectively. That is, R1/(4 • R1 + R2) should be 1/20.

2. To stabilize the power supply, place two 0.1-µF capacitors near each LCD driver: one between the Vcc and GND pins, and the other between the V_{LCD} and GND pins.

3. The load must be less than 30 pF between the $\overline{\text{EI/O2}}$ and $\overline{\text{EI/O1}}$ connections of HD66110RTs.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1, 5
Power supply voltage for LCD drive circuits	V_{LCD}	–0.3 to +42	V	1, 2, 5
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 3
Input voltage 2	V_{T2}	–0.3 to V_{LCD} + 0.3	V	1, 4
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

Notes: 1. The reference point is GND (0 V).
2. Indicates the voltage between GND and V_{LCD}.
3. Applies to input pins for logic circuits, that is, control signaı pins.
4. Applies to input pins for LCD drive level voltages, that is, V1–V4 pins.
5. Power should be applied to V_{CC}-GND first, and then V_{LCD}-GND. It should be disconnected in the reverse order.
6. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

Electrical Characteristics

DC Characteristics1 (V_{CC} = 2.7 to 4.5V, V_{LCD} – GND = 28 to 40 V, and T_a = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Condition	Notes
Input high voltage	V_{IH}	1	0.8 × V_{CC}	V_{CC}	V		
Input low voltage	V_{IL}	1	0	0.2 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	3.0	kΩ	I_{ON} = 150 µA	1
Input leakage current 1	I_{IL1}	1	–5.0	5.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–100	100	µA	V_{IN} = V_{LCD} to GND	
Current consumption 1	I_{CC}	—	—	2.2	mA	f_{CL2} = 10 MHz f_{CL1} = 28 kHz V_{CC}=3.0V	2
Current consumption 2	I_{LCD}	—	—	3.0	mA	Same as above	2
Current consumption 3	I_{ST}	—	—	0.3	mA	Same as above	2, 3

Pins and notes on next page.

DC Characteristics2 (V_{CC} = 5 V ± 10%, V_{LCD} – GND = 28 to 40 V, and T_a = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Condition	Notes
Input high voltage	V_{IH}	1	$0.8 \times V_{CC}$	V_{CC}	V		
Input low voltage	V_{IL}	1	0	$0.2 \times V_{CC}$	V		
Output high voltage	V_{OH}	2	$V_{CC} - 0.4$	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	3.0	kΩ	I_{ON} = 150 µA	1
Input leakage current 1	I_{IL1}	1	–5.0	5.0	µA	$V_{IN} = V_{CC}$ to GND	
Input leakage current 2	I_{IL2}	4	–100	100	µA	$V_{IN} = V_{LCD}$ to GND	
Current consumption 1	I_{CC}	—	—	5.0	mA	f_{CL2} = 12 MHz f_{CL1} = 28 kHz	2
Current consumption 2	I_{LCD}	—	—	3.0	mA	Same as above	2
Current consumption 3	I_{ST}	—	—	0.7	mA	Same as above	2, 3

Pins:
1. CL1, CL2, M, SHL, BS, $\overline{EI/O1}$, $\overline{EI/O2}$, $\overline{DISP}$, $\overline{TEST1}$, $\overline{TEST2}$, D_0–D_7
2. $\overline{EI/O1}$, $\overline{EI/O2}$
3. Y_1–Y_{160}, V1–V4
4. V1–V4

Notes:
1. Indicates the resistance between one pin from Y_1–Y_{160} and another pin from V1–V4 when load current is applied to the Y pin; defined under the following conditions.

   V_{LCD} – GND = 40 V

   V1, V3 = V_{LCD} – {1/20(V_{LCD} – GND)}

   V2, V4 = V_{LCD} + {1/20(V_{LCD} – GND)}

   V1 and V3 should be near V_{LCD} level, and V2 and V4 should be near GND level (figure 7). All voltage must be within ΔV. ΔV is the range within which RON, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage V_{LCD} – GND (figure 8).
2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.
3. Applies to standby mode.

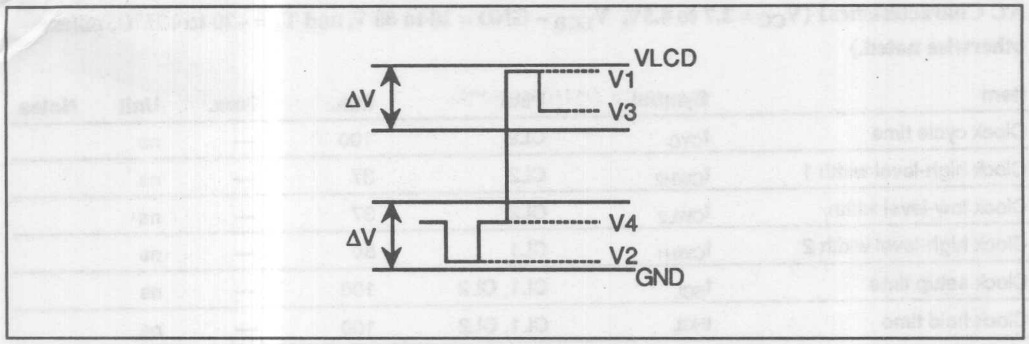


Figure 7 Relation between Driver Output Waveform and Level Voltages

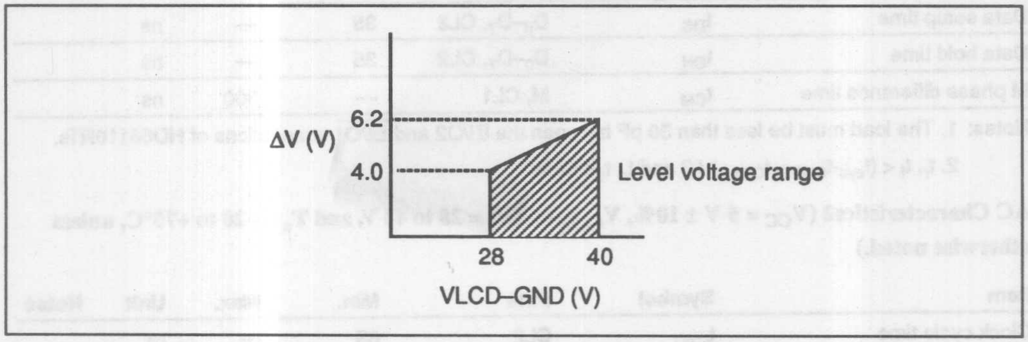


Figure 8 Relation between V_{LCD} – GND and ΔV

AC Characteristics1 (V_{CC} = 2.7 to 4.5V, V_{LCD} – GND = 28 to 40 V, and T_a = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Notes
Clock cycle time	t_{CYC}	CL2	100	—	ns	
Clock high-level width 1	t_{CWH2}	CL2	37	—	ns	
Clock low-level width	t_{CWL2}	CL2	37	—	ns	
Clock high-level width 2	t_{CWH1}	CL1	50	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	100	—	ns	
Clock hold time	tHCL	CL1, CL2	100	—	ns	
Clock rise time	t_r	CL1, CL2	—	50	ns	2
Clock fall time	t_f	CL1, CL2	—	50	ns	2
Data setup time	t_{DS}	D_0–D_7, CL2	35	—	ns	
Data hold time	t_{DH}	D_0–D_7, CL2	35	—	ns	
M phase difference time	t_{CM}	M, CL1	—	300	ns	

Notes: 1. The load must be less than 30 pF between the $\overline{EI/O2}$ and $\overline{EI/O1}$ connections of HD66110RTs.

2. t_r, t_f < (t_{cyc}-t_{CWH2}-t_{CWL2}) / 2 and t_r, $t_f \leq$ 50ns

AC Characteristics2 (V_{CC} = 5 V ± 10%, V_{LCD} – GND = 28 to 40 V, and T_a = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Notes
Clock cycle time	t_{CYC}	CL2	83	—	ns	
Clock high-level width 1	t_{CWH2}	CL2	20	—	ns	
Clock low-level width	t_{CWL2}	CL2	20	—	ns	
Clock high-level width 2	t_{CWH1}	CL1	50	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	100	—	ns	
Clock hold time	tHCL	CL1, CL2	100	—	ns	
Clock rise time	t_r	CL1, CL2	—	50	ns	2
Clock fall time	t_f	CL1, CL2	—	50	ns	2
Data setup time	t_{DS}	D_0–D_7, CL2	10	—	ns	
Data hold time	t_{DH}	D_0–D_7, CL2	10	—	ns	
M phase difference time	t_{CM}	M, CL1	—	300	ns	

Notes: 1. The load must be less than 30 pF between the $\overline{EI/O2}$ and $\overline{EI/O1}$ connections of HD66110RTs.

2. t_r, t_f < (t_{cyc}-t_{CWH2}-t_{CWL2}) / 2 and t_r, $t_f \leq$ 50ns

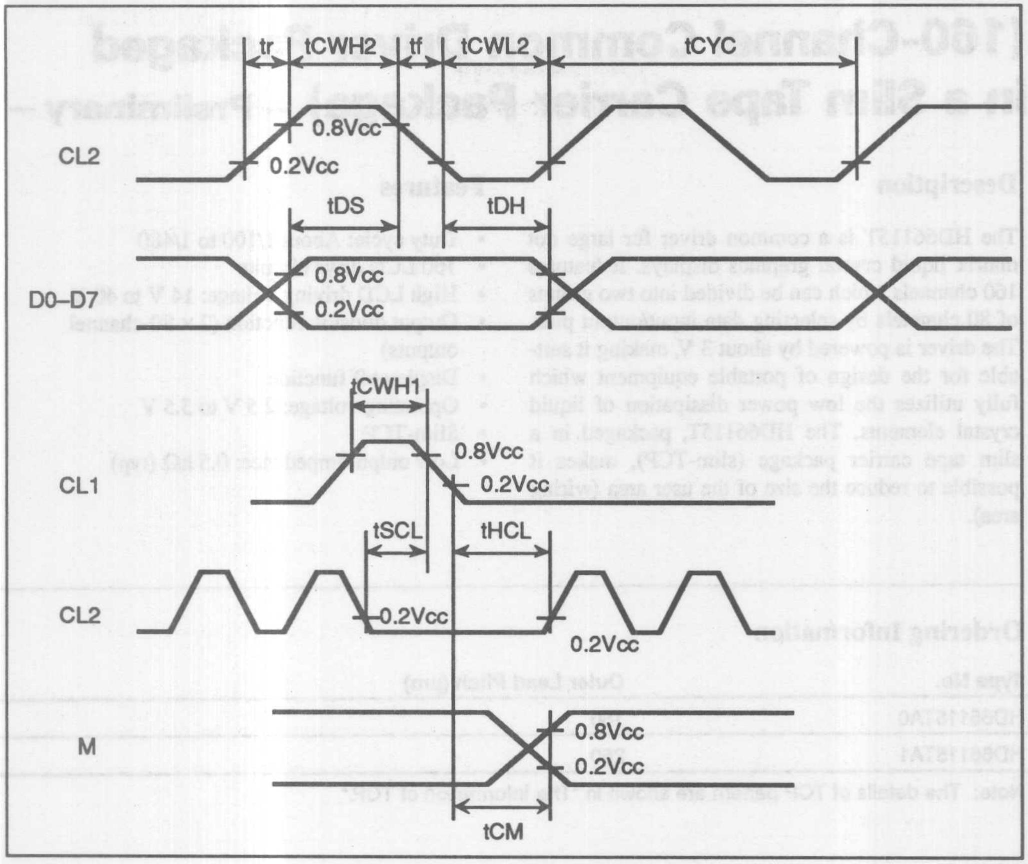


Figure 9 LCD Controller Interface Timing

HD66115T

(160-Channel Common Driver Packaged in a Slim Tape Carrier Package) – Preliminary –

Description

The HD66115T is a common driver for large dot matrix liquid crystal graphics displays. It features 160 channels which can be divided into two groups of 80 channels by selecting data input/output pins. The driver is powered by about 3 V, making it suitable for the design of portable equipment which fully utilizes the low power dissipation of liquid crystal elements. The HD66115T, packaged in a slim tape carrier package (slim-TCP), makes it possible to reduce the size of the user area (wiring area).

Features

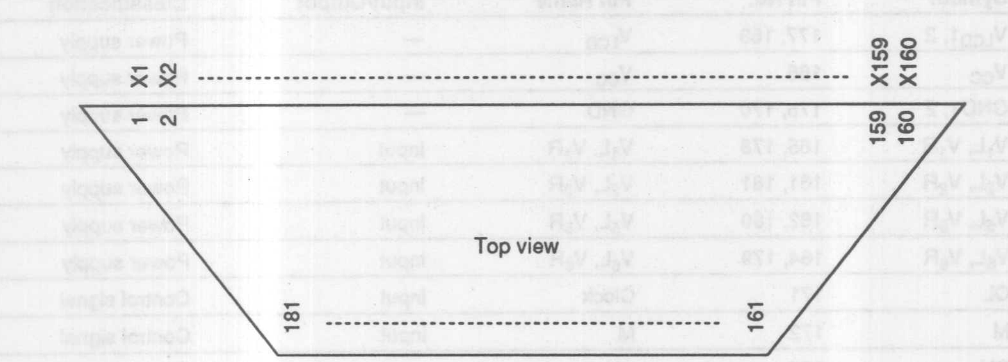
- Duty cycle: About 1/100 to 1/480
- 160 LCD drive circuits
- High LCD driving voltage: 14 V to 40 V
- Output division function (2 × 80-channel outputs)
- Display off function
- Operating voltage: 2.5 V to 5.5 V
- Slim-TCP
- Low output impedance: 0.5 kΩ (typ)

Ordering Information

Type No.	Outer Lead Pitch (μm)
HD66115TA0	180
HD66115TA1	250

Note: The details of TCP pattern are shown in "The Information of TCP."

Pin Arrangement



Note: This figure does not specify the tape carrier package dimensions.

Pin Assignments

V2L	V5L	V6L	V1L	$V_{LCD}1$	GND1	CH	SHL	$\overline{Dispoff}$	M	CL	GND2	DIO1	DI	DIO2	V_{CC}	V1R	V6R	$V_{LCD}2$	V5R	V2R
181	180	179	178	177	176	175	174	173	172	171	170	169	168	167	166	165	164	163	162	161

Pin Descriptions

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{LCD}1, 2	177, 163	V_{LCD}	—	Power supply
V_{CC}	166	V_{CC}	—	Power supply
GND1, 2	176, 170	GND	—	Power supply
V_1L, V_1R	165, 178	V_1L, V_1R	Input	Power supply
V_2L, V_2R	161, 181	V_2L, V_2R	Input	Power supply
V_5L, V_5R	162, 180	V_5L, V_5R	Input	Power supply
V_6L, V_6R	164, 179	V_6L, V_6R	Input	Power supply
CL	171	Clock	Input	Control signal
M	172	M	Input	Control signal
CH	175	CH	Input	Control signal
SHL	174	Shift left	Input	Control signal
DIO1	169	Data	Input/output	Control signal
DIO2	167	Data	Input/output	Control signal
DI	168	Data	Input	Control signal
$\overline{\text{Dispoff}}$	173	Display off	Input	Control signal
X1–X160	1–160	X1–X160	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, GND: Supply power to the internal logic circuits.

V_{LCD}, GND: Supply power to the LCD drive circuits (figure 1).

V_1L, V_1R, V_2L, V_2R, V_5L, V_5R, V_6L, V_6R: Supply different power levels to drive the LCD. V_1 and V_2 are selected levels, and V_5 and V_6 are non-selected levels.

Control Signals

CL: Inputs data shift clock pulses for the shift register. At the falling edge of each CL pulse, the shift register shifts data input via the DIO pins.

M: Changes the LCD drive outputs to AC.

CH: Selects the data shift mode. (CH = high: 2 × 80-output mode, CH = low: 160-output mode)

SHL: Selects the data shift direction for the shift register and the common signal scan direction (figure 2).

DIO1, DIO2: Input or output data. DIO1 is input and DIO2 is output when SHL is high. DIO1 is output and DIO2 is input when SHL is low.

DI: Input data. DI is input to X81–X160 when CH and SHL are high, and to X81–X1 when SHL is low.

$\overline{\text{Dispoff}}$: Controls LCD output level. A low $\overline{\text{Dispoff}}$ sets the LCD drive outputs X1–X160 to the V_2 level. A high $\overline{\text{Dispoff}}$ is normally used.

LCD Drive Outputs

X1–X160: Each X outputs one of four voltage levels V_1, V_2, V_5, or V_6, depending on the combination of the M signal and the data level (figure 3).

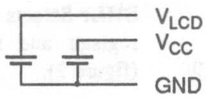


Figure 1 Power Supply for LCD Driver

SHL	Data shift direction
High	Shift to right DIO1 → SR1 → SR2 → SR3 • • • → SR160 → DIO2
Low	Shift to left DIO2 → SR160 → SR159 • • • → SR1 → DIO1

Note: SR1 to SR160 correspond to the outputs of X1 to X160, respectively.

Figure 2 Selection of Data Shift Direction and Common Signal Scan Direction by SHL

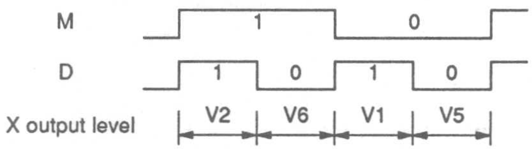
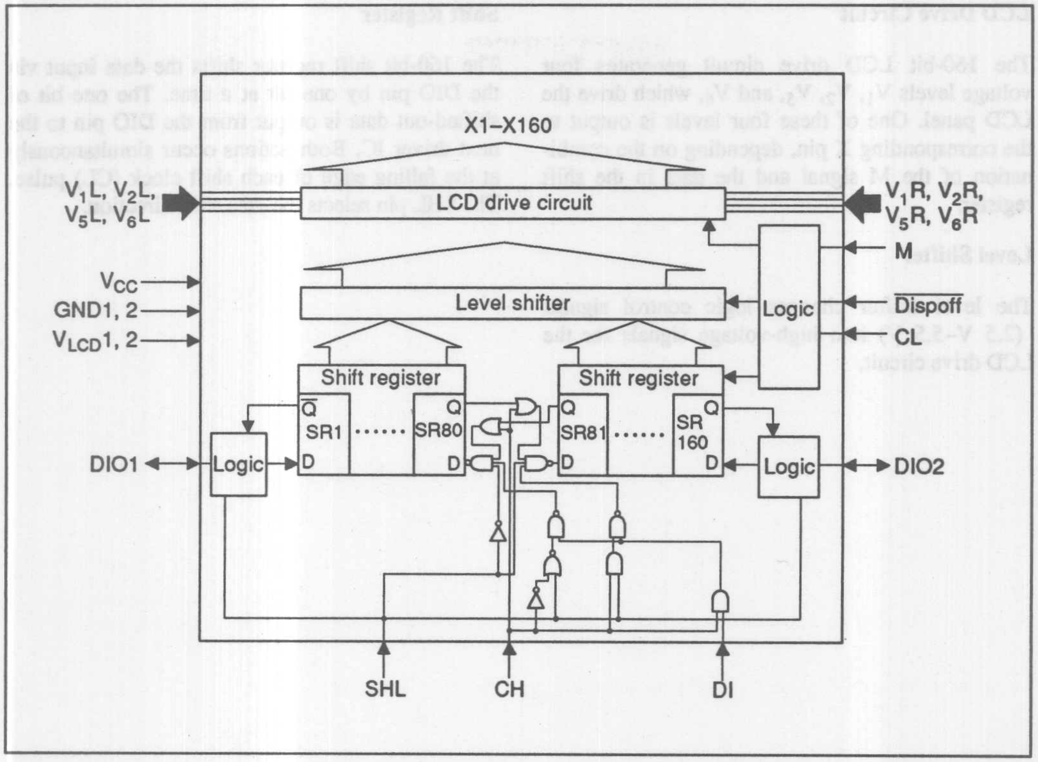


Figure 3 Selection of LCD Drive Output Level

Block Diagram



Block Functions

LCD Drive Circuit

The 160-bit LCD drive circuit generates four voltage levels V_1, V_2, V_5, and V_6, which drive the LCD panel. One of these four levels is output to the corresponding X pin, depending on the combination of the M signal and the data in the shift register.

Level Shifter

The level shifter changes logic control signals (2.5 V–5.5 V) into high-voltage signals for the LCD drive circuit.

Shift Register

The 160-bit shift register shifts the data input via the DIO pin by one bit at a time. The one bit of shifted-out data is output from the DIO pin to the next driver IC. Both actions occur simultaneously at the falling edge of each shift clock (CL) pulse. The SHL pin selects the data shift direction.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1, 5
Power supply voltage for LCD drive circuits	V_{LCD}	–0.3 to +42	V	1, 5
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	V_{T2}	–0.3 to V_{LCD} + 0.3	V	1, 3
Input voltage 3	V_{T3}	–0.3 to +7.0	V	1, 4
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

Notes: 1. The reference point is GND (0 V).
2. Applies to pins CL, M, SHL, DI, $\overline{\text{Dispoff}}$, and CH.
3. Applies to pins V_1 and V_6.
4. Applies to pins V_2 and V_5.
5. Power should be applied to V_{CC}–GND first, and then V_{LCD}–GND. It should be disconnected in the reverse order.
6. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its specified operating range in order to prevent malfunctions or loss of reliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 2.5 V to 5.5 V, GND = 0 V, and T_a = –20°C to +75°C, unless otherwise stated)

Item	Symbol	Pins	Min.	Typ.	Max.	Unit	Test Condition	Notes
Input high voltage	V_{IH}	1	$0.8 \times V_{CC}$	—	V_{CC}	V		
Input low voltage	V_{IL}	1	0	—	$0.2 \times V_{CC}$	V		
Output high voltage	V_{OH}	2	$V_{CC} - 0.4$	—	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Xj on resistance	R_{ON}	3	—	0.5	1.0	kΩ	I_{ON} = 150 µA	1
Input leakage current 1	I_{IL1}	1	–5	—	5	µA	$V_{IN} = V_{CC}$ to GND	
Input leakage current 2	I_{IL2}	4	–25	—	25	µA	$V_{IN} = V_{LCD}$ to GND	
Current consumption 1	I_{GND}	—	—	—	T.B.D	µA		2
Current consumption 2	I_{LCD}	—	—	—	T.B.D	µA		
Current consumption 3	I_{GND}	—	—	—	T.B.D	µA		2
Current consumption 4	I_{LCD}	—	—	—	T.B.D	µA		

Note: Pins:
1. CL, M, SHL, CH, DI, DIO1, DIO2, $\overline{\text{Dispoff}}$
2. DIO1, DIO2
3. X1–X160, V
4. V_1, V_2, V_5, V_6

Notes: 1. Indicates the resistance between one of the pins X1–X160 and one of the voltage supply pins V_1, V_2, V_5, or V_6, when load current is applied to the X pin; defined under the following conditions:

V_{LCD}–GND = 40 V
$V_1, V_6 = V_{CC} - \{1/20\ (V_{LCD}\text{–GND})\}$
$V_5, V_2 = \text{GND} + \{1/20\ (V_{LCD}\text{–GND})\}$

All voltages must be within ΔV, $V_{LCD} \geq V_1 \geq V_6 \geq V_{LCD} - 7.0$ V, and $7.0\ V \geq V_5 \geq V_2 \geq$ GND. Note that ΔV depends on the power supply voltage V_{LCD}–GND (figure 5).

2. Input and output currents are excluded. When a CMOS input is left floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held at V_{CC} and GND, respectively.

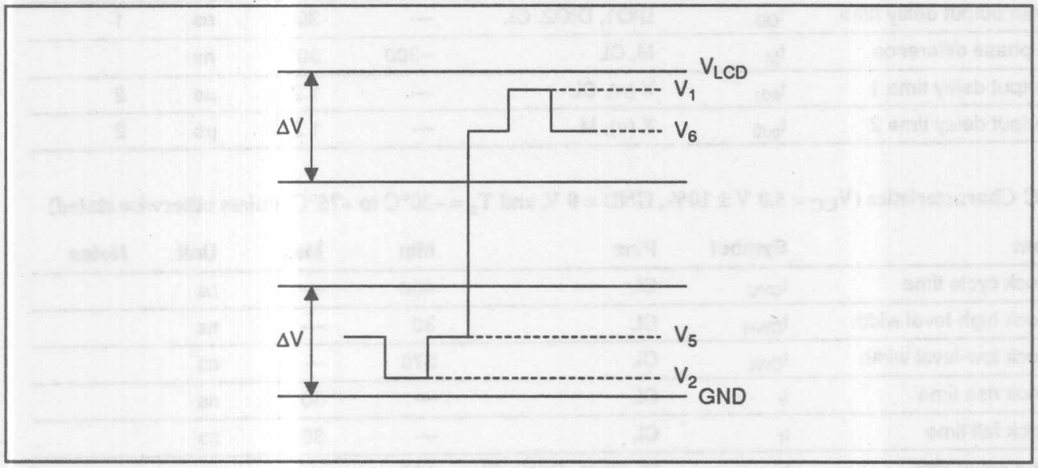


Figure 4 Relation between Driver Output Waveform and Voltage Levels

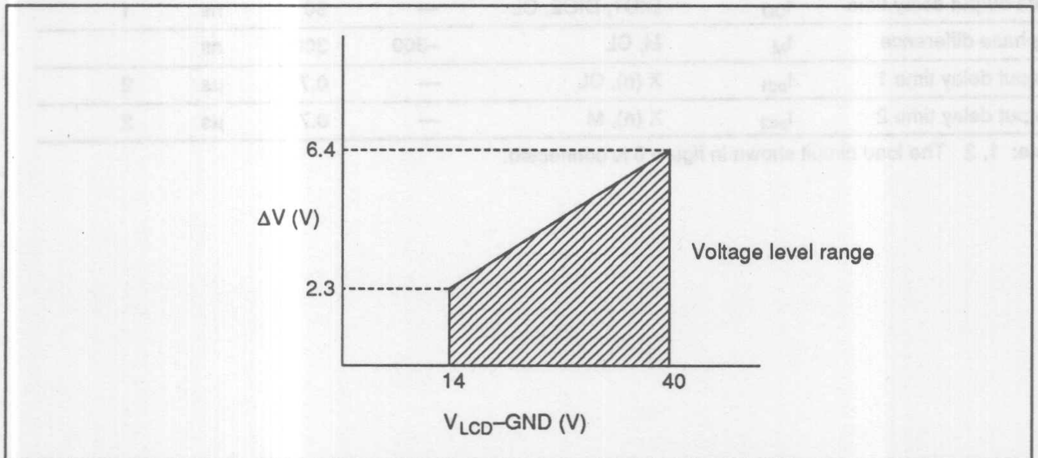


Figure 5 Relation between V_{LCD}–GND and ΔV

AC Characteristics (V_{CC} = 2.5 V to 5.5 V, GND = 0 V, and T_a = –20°C to +75°C, unless otherwise stated)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL	400	—	ns	
Clock high-level width	t_{CWH}	CL	30	—	ns	
Clock low-level width	t_{CWL}	CL	370	—	ns	
Clock rise time	t_r	CL	—	30	ns	
Clock fall time	t_f	CL	—	30	ns	
Data setup time	t_{DS}	DI, DIO1, DIO2, CL	100	—	ns	
Data hold time	t_{DH}	DI, DIO1, DIO2, CL	30	—	ns	
Data output delay time	t_{DD}	DIO1, DIO2, CL	—	350	ns	1
M phase difference	t_M	M, CL	–300	300	ns	
Output delay time 1	t_{pd1}	X (n), CL	—	1.2	µs	2
Output delay time 2	t_{pd2}	X (n), M	—	1.2	µs	2

AC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, and T_a = –20°C to +75°C, unless otherwise stated)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL	400	—	ns	
Clock high-level width	t_{CWH}	CL	30	—	ns	
Clock low-level width	t_{CWL}	CL	370	—	ns	
Clock rise time	t_r	CL	—	30	ns	
Clock fall time	t_f	CL	—	30	ns	
Data setup time	t_{DS}	DI, DIO1, DIO2, CL	100	—	ns	
Data hold time	t_{DH}	DI, DIO1, DIO2, CL	30	—	ns	
Data output delay time	t_{DD}	DIO1, DIO2, CL	—	90	ns	1
M phase difference	t_M	M, CL	–300	300	ns	
Output delay time 1	t_{pd1}	X (n), CL	—	0.7	µs	2
Output delay time 2	t_{pd2}	X (n), M	—	0.7	µs	2

Note: 1, 2 The load circuit shown in figure 6 is connected.

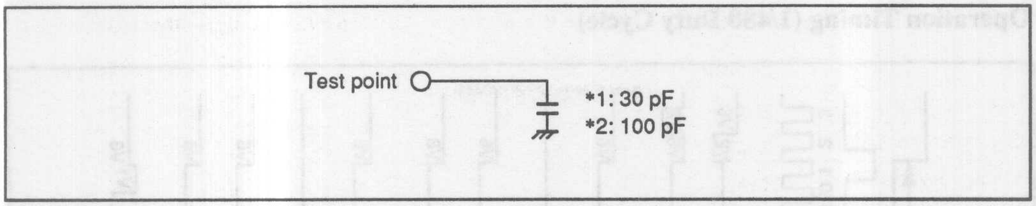


Figure 6 Load Circuit

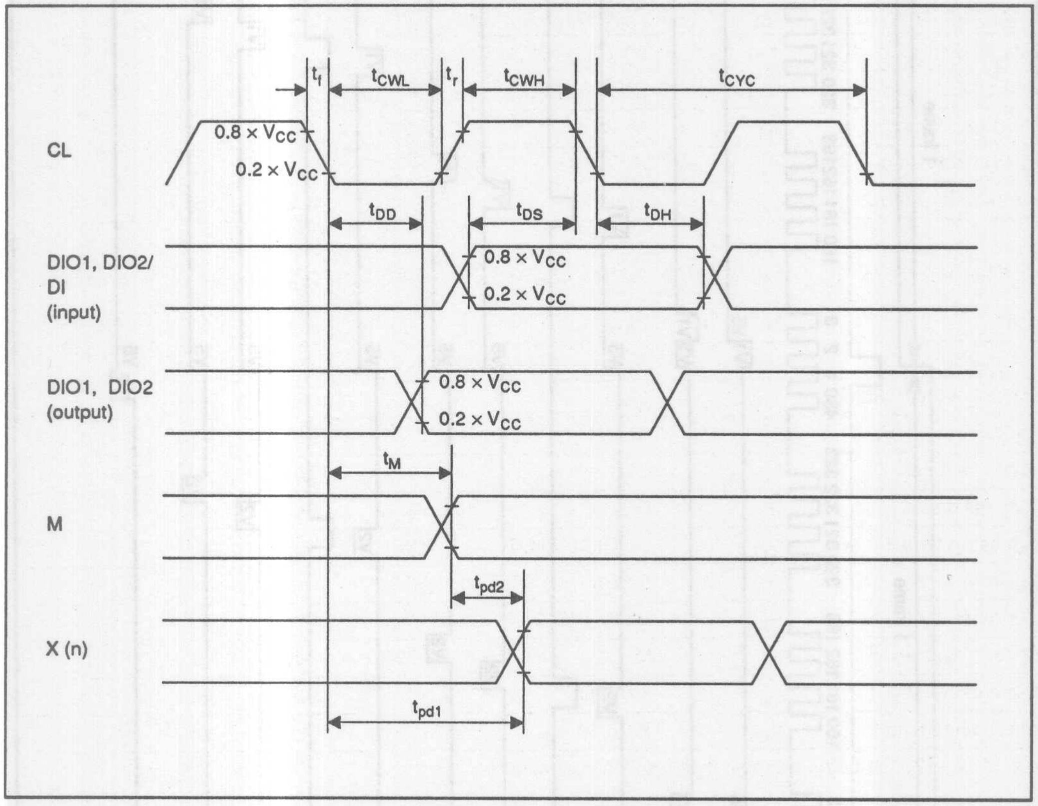
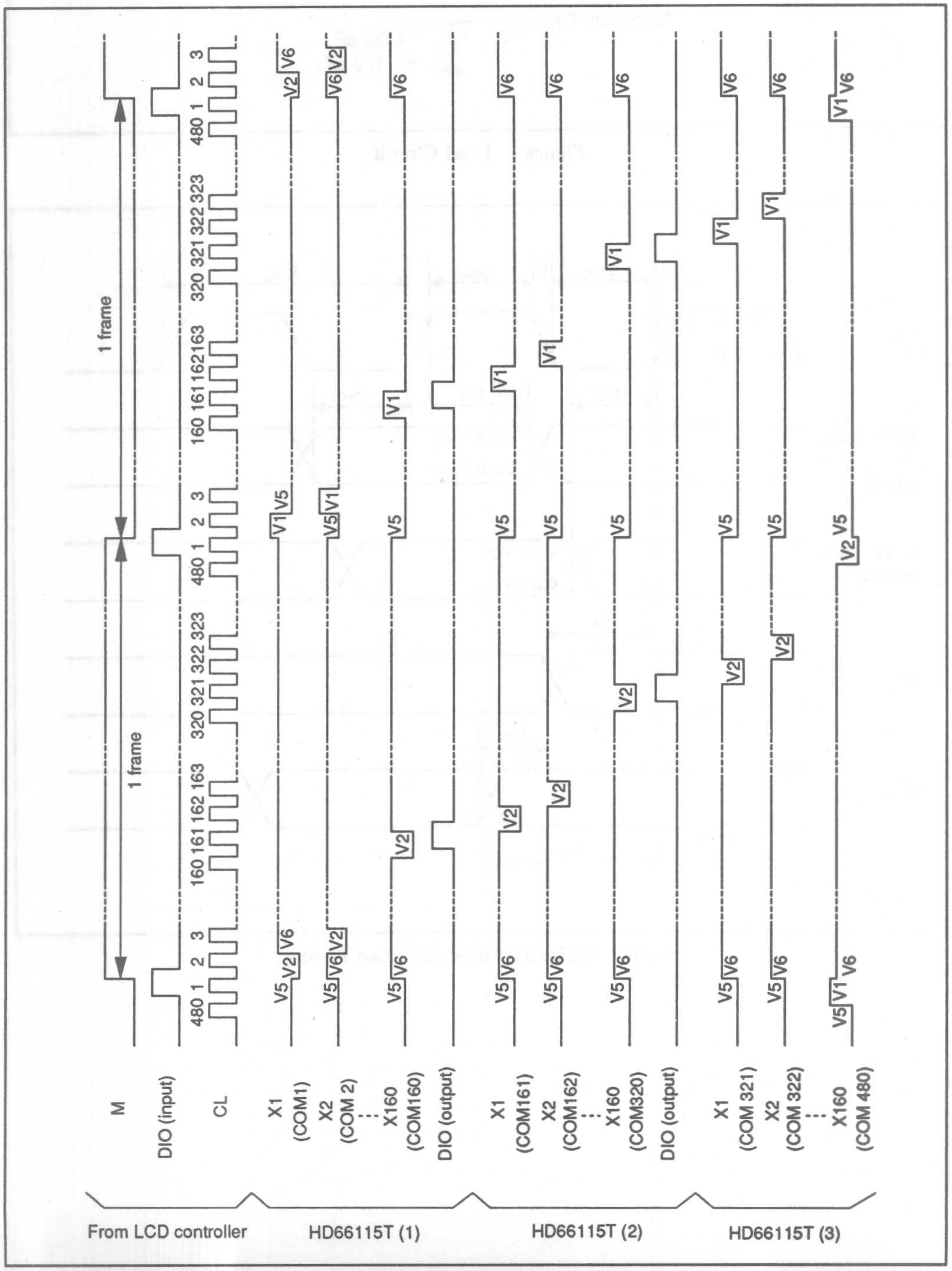


Figure 7 LCD Controller Interface Timing

Operation Timing (1/480 Duty Cycle)



Connection Examples

Figures 8 and 9 show examples of how HD66115Ts can be configured to drive a 480-line LCD panel with a 1/240 duty cycle. Figures 10 and 11 show examples of how HD66115Ts can be configured to drive a 480-line LCD panel with a 1/480 duty cycle. The HD66115T's 160 channels can be divided into two groups of 80 channels, and its data shift direction can be changed by selecting the data output mode pin (CH) and data shift pin (SHL), respectively.

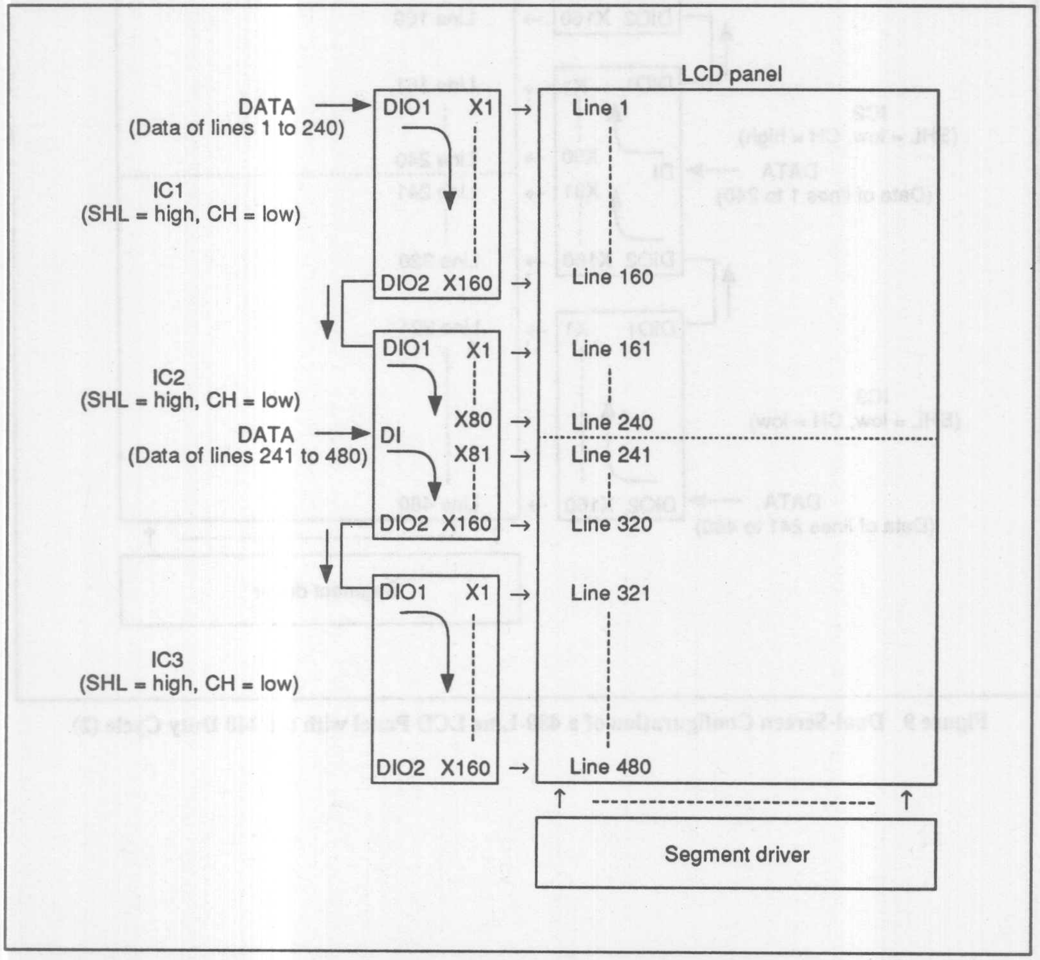


Figure 8 Dual-Screen Configuration of a 480-Line LCD Panel with a 1/240 Duty Cycle (1)

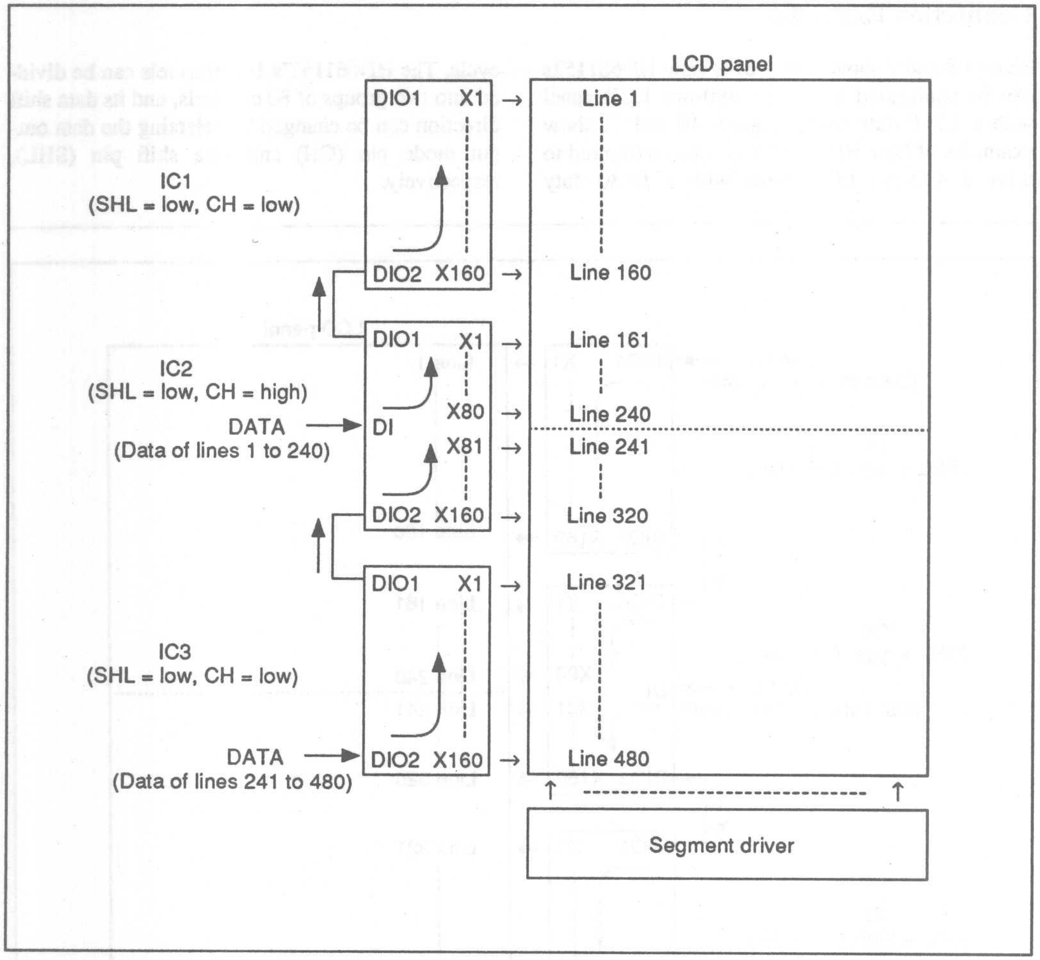


Figure 9 Dual-Screen Configuration of a 480-Line LCD Panel with a 1/240 Duty Cycle (2)

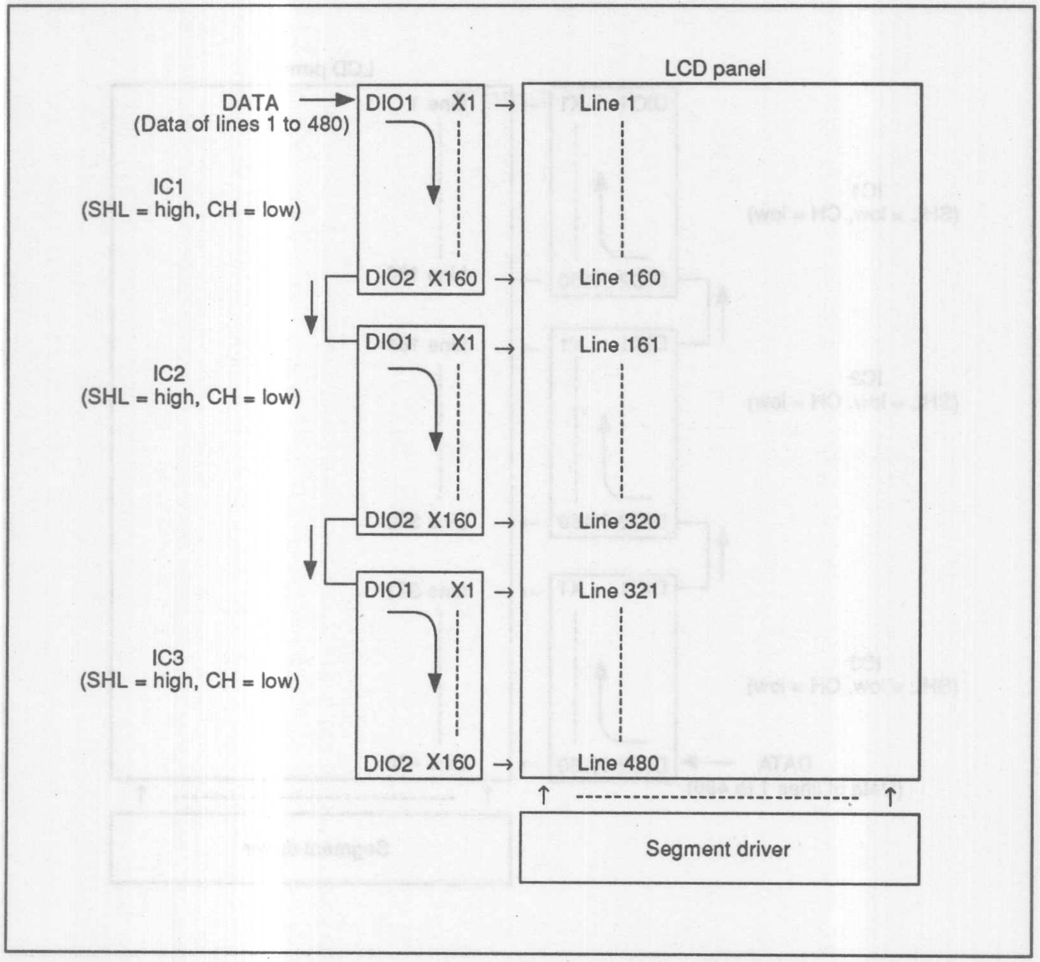


Figure 10 Single-Screen Configuration of a 480-Line LCD Panel with a 1/480 Duty Cycle (1)

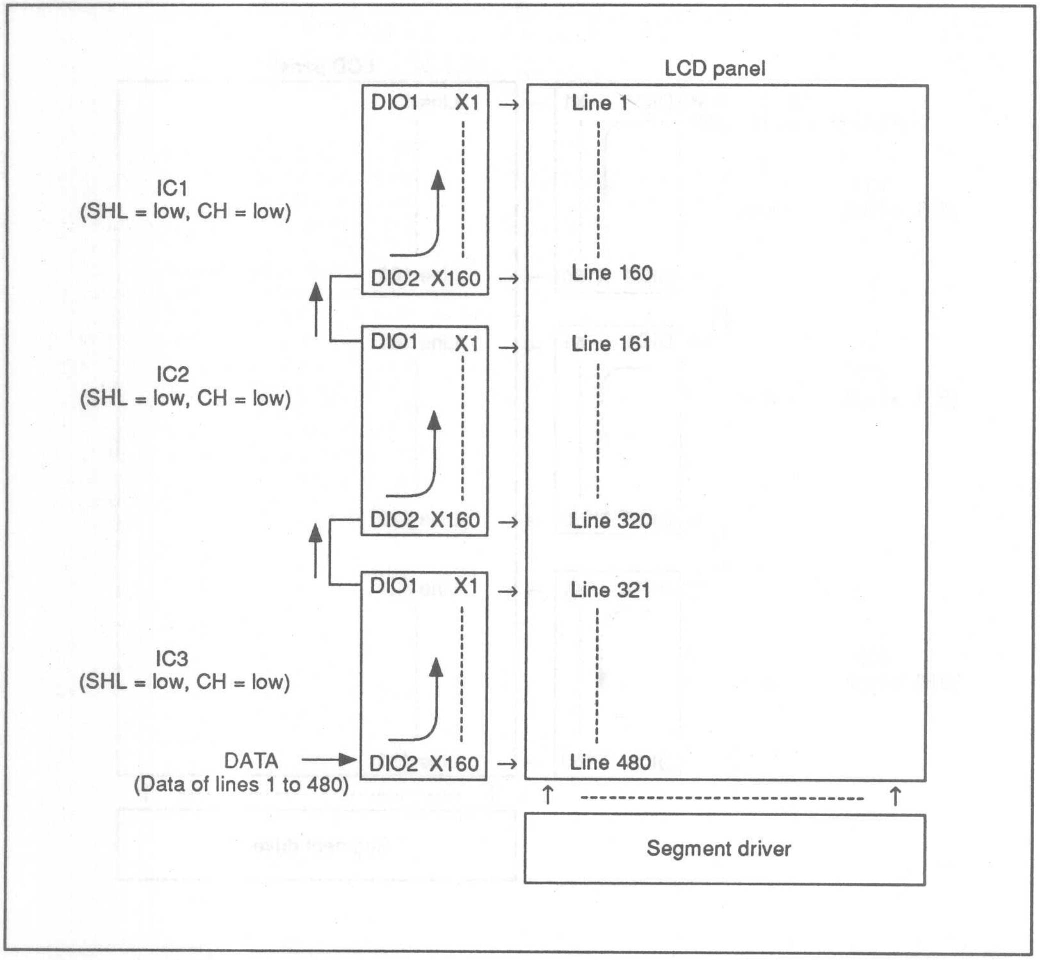


Figure 11 Single-Screen Configuration of a 480-Line LCD Panel with a 1/480 Duty Cycle (2)

HD61602/HD61603
(Segment Type LCD Driver)

Descripition

The HD61602 and the HD61603 are liquid crystal display driver LSIs with a TTL and CMOS compatible interface. Each of the LSIs can be connected to various microprocessors such as the HMCS6800 series.

The HD61602 incorporates the power supply circuit for the liquid crystal display driver. Using the software-controlled liquid crystal driving method, several types of liquid crystals can be connected according to the applications.

The HD61603 is a liquid crystal display driver LSI only for static drive and has 64 segment outputs that can display 8 digits per chip.

Features

- Wide-range operating voltage
  —Operates in a wide range of supply voltage: 2.2 V to 5.5 V
  —Compatible with TTL interface at 4.5 V to 5.5 V
- Low current consumption
  —Can run from a battery power supply (100 μA max. at 5 V)
  —Standby input enables standby operation at lower current consumption (5 μA max. on 5 V)
- Internal power supply circuit for liquid crystal display driver (HD61602)
  —Internal power supply circuit for liquid crystal display driver facilitates the connection to a microprocessor system

Versatile segment driving capacity

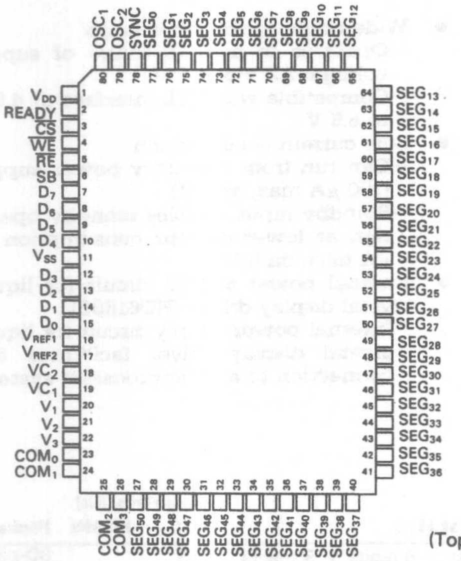
Type No.	Driving Method		Display Segments	Example of Use	Frame Freq. (Hz) at f_{osc} = 100 kHz	Package
HD61602	Static		51	8 segments × 6 digits + 3 marks	33	80-pin Plastic QFP (FP-80, FP-80A, TFP-80)
	1/2 bias	1/2 duty	102	8 segments × 12 digits + 6 marks	65	
	1/3 bias	1/3 duty	153	9 segments × 17 digits	208	
		1/4 duty	204	8 segments × 25 digits + 4 marks	223	
HD61603	Static		64	8 segments × 8 digits	33	80-pin Plastic QFP (FP-80)

Ordering Information

Type No.	Package
HD61602R	80-pin plastic QFP(FP-80)
HD61602RH	80-pin plastic QFP(FP-80A)
HD61603R	80-pin plastic QFP(FP-80)

Pin Arrangement (Top View)

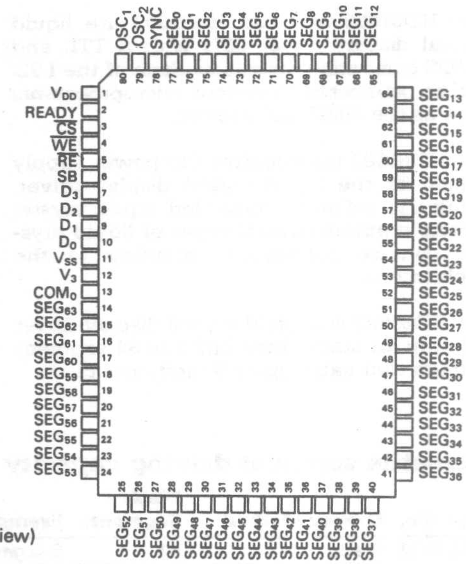
HD61602R



(FP-80)

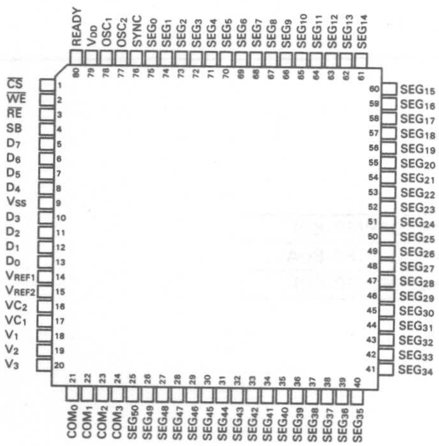
(Top View)

HD61603R



(FP-80)

HD61602RH

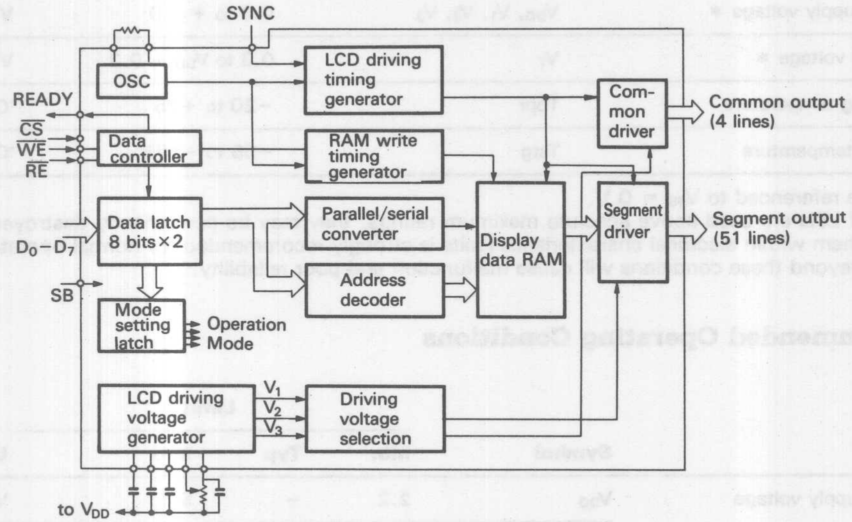


(FP-80A)

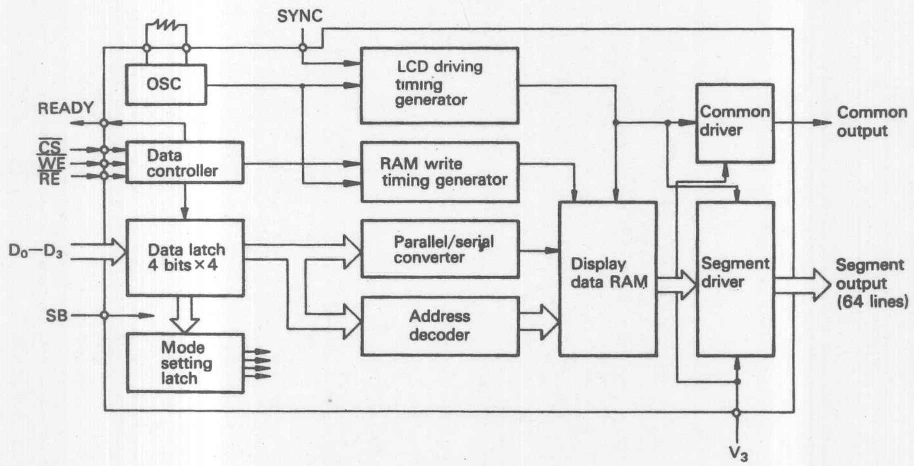
(Top View)

Block Diagram

HD61602



HD61603



Absolute Maximum Ratings

Item	Symbol	Limit	Unit
Power supply voltage *	V_{DD}, V_1, V_2, V_3	0.3 to + 7.0	V
Terminal voltage *	V_T	0.3 to V_{DD} − 0.3	V
Operating temperature	Topr	−20 to +75	°C
Storage temperature	Tstg	−55 to +125	°C

* Value referenced to V_{SS} = 0 V.

Note: If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Recommended Operating Conditions

Item	Symbol	Limit Min	Limit Typ	Limit Max	Unit
Power supply voltage	V_{DD}	2.2	–	5.5	V
	V_1, V_2, V_3	0	–	V_{DD}	V
Terminal voltage *	V_T	0	–	V_{DD}	V
Operating temperature	Topr	−20	–	75	°C

* Value referenced to V_{SS} = 0 V.

Electrical Characteristics

DC Characteristics (1)

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Ta = −20 to +75°C, unless otherwise noted)

Item		Symbol	Limit			Unit	Test Condition
			Min	Typ	Max		
Input high voltage	OSC_1	V_{IH1}	$0.8V_{DD}$	–	V_{DD}	V	
	Others	V_{IH2}	2.0	–	V_{DD}	V	
Input low voltage	OSC_1	V_{IL1}	0	–	$0.2V_{DD}$	V	
	Others	V_{IL2}	0	–	0.8	V	
Output leakage current	READY	I_{OH}	–	–	5	μA	$V_O = V_{DD}$
Output low voltage	READY	V_{OL}	–	–	0.4	V	I_{OL} = 0.4 mA
Input leakage current *1	Input terminal	I_{IL1}	−1.0	–	1.0	μA	$V_{IN} = 0-V_{DD}$
	V_1	I_{IL2}	−20	–	20	μA	$V_{IN} = 0-V_3$
	V_2, V_3	I_{IL3}	−5.0	–	5.0	μA	
LCD driver voltage drop	COM_0-COM_3	V_{d1}	–	–	0.3	V	±Id = 3 μA for each COM, $V_3 = V_{DD}-3$ V
	SEG_0-SEG_{50}	V_{d2}	–	–	0.6	V	±Id = 3 μA for each SEG, $V_3 = V_{DD}-3$ V
Power supply current		I_{DD}	–	–	100	μA	During display* R_{OSC} = 360 kΩ
		I_{DD}	–	–	5	μA	At standby
Internal driving voltage drop	V_1, V_2, V_3	V_{TR}	–	–	0.4	V	$V_{REF2} = V_{DD}-1$ V, C_1-C_4 = 0.3 μF, RL = 3 MΩ

* Except the transfer operation of display data and bit data.
*1 V_1, V_2: apply only to HD61602.

DC Characteristics (2)

(V_{SS} = 0 V, V_{DD} = 2.2 to 3.8 V, Ta = −20 to +75°C, unless otherwise noted)

Item		Symbol	Limit Min	Limit Typ	Limit Max	Unit	Test Condition
Input high voltage		V_{IH}	$0.8V_{DD}$	–	V_{DD}	V	
Input low voltage		V_{IL}	0	–	$0.1V_{DD}$	V	
Output leakage current	READY	I_{OH}	–	–	5	μA	$V_{IN} = V_{DD}$
Output low voltage	READY	V_{OL}	–	–	$0.1V_{DD}$	V	I_{OL} = 0.04 mA
Input leakage current *1	Input terminal	I_{IL1}	−1.0	0	1.0	μA	$V_{IN} = 0-V_{DD}$
	V_1	I_{IL2}	−20	–	20	μA	$V_{IN} = 0-V_3$
	V_2, V_3	I_{IL3}	−5.0	–	5.0	μA	
LCD driver voltage drop	COM_0-COM_3	V_{d1}	–	–	0.3	V	±Id = 3 μA for each COM, $V_3 = V_{DD}-3$ V
	SEG_0-SEG_{50}	V_{d2}	–	–	0.6	V	±Id = 3 μA for each SEG, $V_3 = V_{DD}-3$ V
Power supply current		I_{SS}	–	–	50	μA	During display* R_{OSC} = 330 kΩ
		I_{SS}	–	–	5	μA	At standby
Internal driving voltage drop	V_1, V_2, V_3	V_{TR}	–	–	0.4	V	$V_{REF2} = V_{DD}-1$ V, C_1-C_4 = 0.3 μF RL = 3 MΩ, V_{DD} = 3−3.8 V

* Except the transfer operation of display data and bit data.
*1 V_1, V_2: apply only to HD61602.

AC Characteristics (1)

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Ta = −20 to +75°C, unless otherwise noted)

Item		Symbol	Limit Min	Typ	Max	Unit	Test Condition
Oscillation frequency	OSC_2	f_{osc}	70	100	130	kHz	R_{osc}=360 kΩ
External clock frequency	OSC_1	f_{osc}	70	100	130	kHz	
External clock duty	OSC_1	Duty	40	50	60	%	
I/O signal timing		t_S	400	–	–	ns	
		t_H	10	–	–	ns	
		t_{WH}	300	–	–	ns	
		t_{WL}	400	–	–	ns	
		t_{WR}	400	–	–	ns	
		t_{DL}	–	–	1.0	μs	Figure 5
		t_{EN}	400	–	–	ns	
		t_{OP1}	9.5	–	10.5	Clock	For display data transfer
		t_{OP2}	2.5	–	3.5	Clock	For bit and mode data transfer
Input signal rise time and fall time		t_r, t_f	–	–	25	ns	

AC Characteristics (2)

(V_{SS} = 0 V, V_{DD} = 2.2 to 3.8 V, Ta = −20 to +75°C, unless otherwise noted)

Item		Symbol	Limit Min	Typ	Max	Unit	Test Condition
Oscillation frequency	OSC_2	f_{osc}	70	100	130	kHz	R_{osc}=330 kΩ
External clock frequency	OSC_1	f_{osc}	70	100	130	kHz	
External clock duty	OSC_1	Duty	40	50	60	%	
I/O signal timing (V_{DD} = 3.0−3.8 V)		t_S	1.5	–	–	μs	
		t_H	1.0	–	–	μs	
		t_{WH}	1.5	–	–	μs	
		t_{WL}	1.5	–	–	μs	
		t_{DL}	–	–	2.0	μs	Figure 6
		t_{WR}	1.5	–	–	μs	
		t_{EN}	2.0	–	–	μs	
		t_{OP1}	9.5	–	10.5	Clock	For display data transfer
		t_{OP2}	2.5	–	3.5	Clock	For bit and mode data transfer
Input signal rise time and fall time		t_r, t_f	–	–	25	ns	

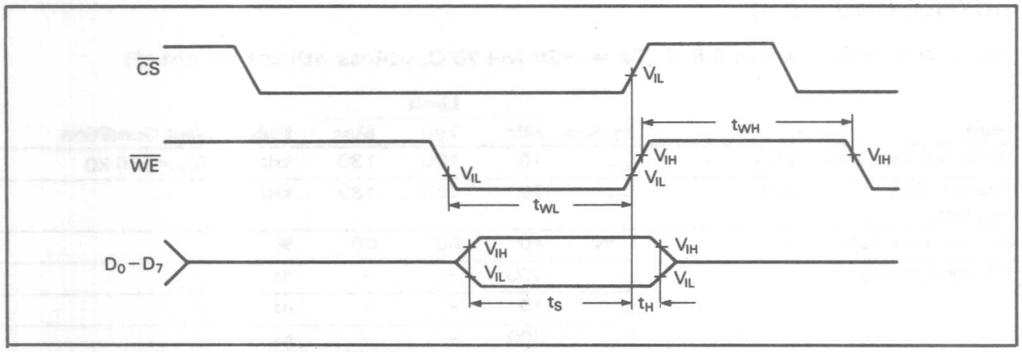


Figure 1 Write Timing
(RE is fixed at high level, and SYNC at low level)

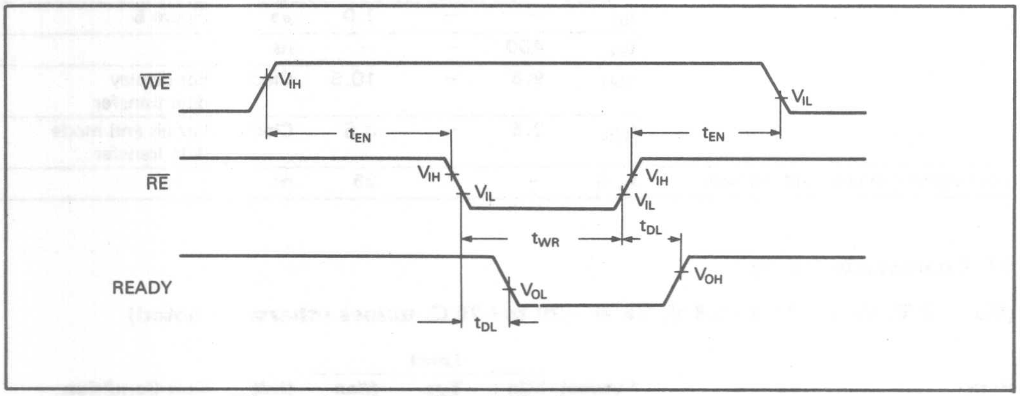


Figure 2 Reset/Read Timing
(CS and SYNC are fixed at low level)

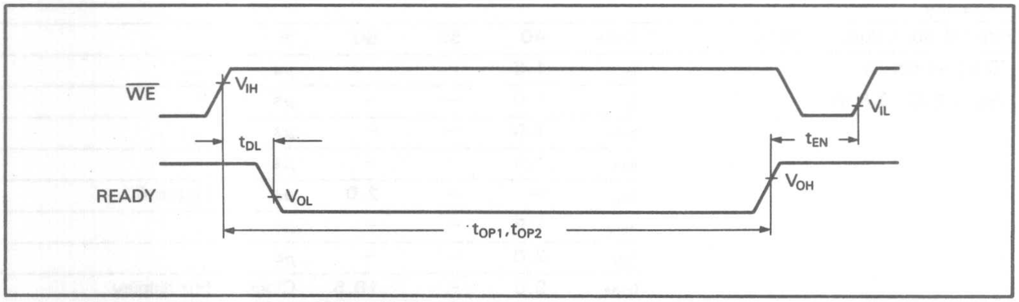


Figure 3 READY Timing
(When the READY output is always available)

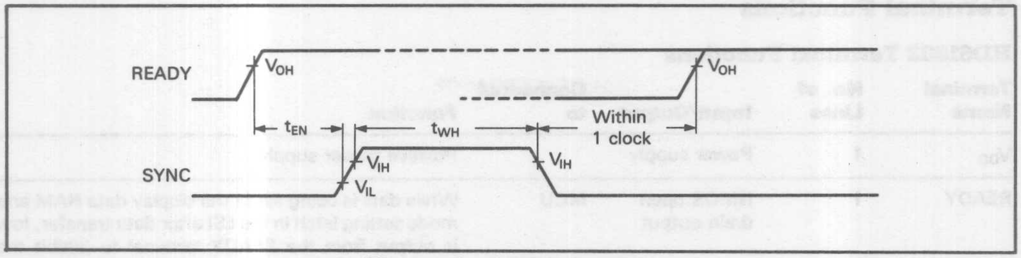


Figure 4 SYNC Timing

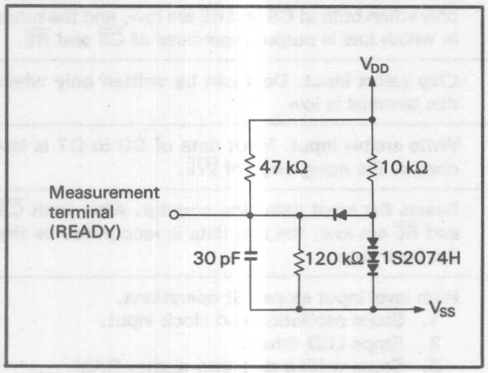


Figure 5 Bus Timing Load Circuit (LS-TTL Load)

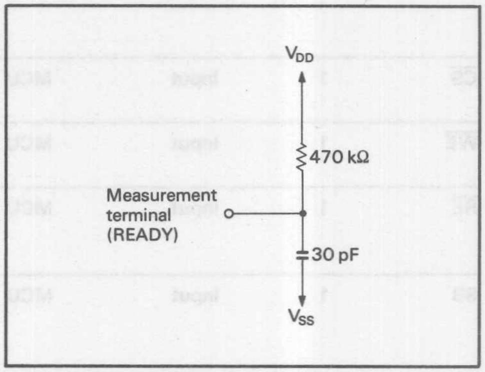


Figure 6 Bus Timing Load Circuit (CMOS Load)

Terminal Functions

HD61602 Terminal Functions

Terminal Name	No. of Lines	Input/Output	Connected to	Function
V_{DD}	1	Power supply		Positive power supply.
READY	1	NMOS open drain output	MCU	While data is being set in the display data RAM and mode setting latch in the LSI after data transfer, low is output from the READY terminal to inhibit the next data input. There are two modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.
$\overline{CS}$	1	Input	MCU	Chip select input. Data can be written only when this terminal is low.
$\overline{WE}$	1	Input	MCU	Write enable input. Input data of D0 to D7 is latched at the rising edge of $\overline{WE}$.
$\overline{RE}$	1	Input	MCU	Resets the input data byte counter. After both $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the 1st byte data.
SB	1	Input	MCU	High level input stops LSI operations. 1. Stops oscillation and clock input. 2. Stops LCD driver. 3. Stops writing data into display RAM.
D_0-D_7	8	Input	MCU	Data input terminal for 8-bit × 2-byte data.
V_{SS}	1	Power supply		Negative power supply.
V_{REF1}	1	Output	External R	Reference voltage output. Generates LCD driving voltage.
V_{REF2}	1	Input	External R	Divides the reference voltage of V_{REF1} with external R to determine LCD driving voltage. $V_{REF2} \fallingdotseq V_1$.
V_{C1}, V_{C2}	2	Output	External C	Connection terminals for boosting C of LCD driving voltage generator. An external C is connected between V_{C1} and V_{C2}.
V_1, V_2, V_3	3	Output (Input)	External C	LCD driving voltage outputs. An external C is connected to each terminal.
COM_0-COM_3	4	Output	LCD	LCD common (backplate) driving output.
SEG_0-SEG_{50}	51	Output	LCD	LCD segment driving output.
SYNC	1	Input	MCU	Synchronous input for 2 or more chips applications. LCD driver timing circuit is reset by high input. LCD is off.
OSC_1 OSC_2	2	Input Output	External R	Attach external R to these terminals for oscillation. An external clock (100 kHz) can be input to OSC1.

Note: Logic polarity is positive. 1 = high = active.

HD61603 Terminal Functions

Terminal Name	No. of Lines	Input/Output	Connected to	Function
V_{DD}	1	Power supply		Positive power supply.
READY	1	NMOS open drain output	MCU	While data is being set in the display data RAM and mode setting latch in the LSI after data transfer, low is output from the READY terminal to inhibit the next data input. There are two modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.
$\overline{CS}$	1	Input	MCU	Chip select input. Data can be written only when this terminal is low.
$\overline{WE}$	1	Input	MCU	Write enable input. Input data of D_0 to D_3 is latched at the rising edge of $\overline{WE}$.
$\overline{RE}$	1	Input	MCU	Reset the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the 1st byte data.
SB	1	Input	MCU	High level input stops the LSI operations. 1. Stops oscillation and clock input. 2. Stops LCD driver. 3. Stops writing data into display RAM.
D_0-D_3	4	Input	MCU	Data input terminal from where 4-bit × 4 data are input.
V_{SS}	1	Power supply		Negative power supply.
V_3	1	Input	Power supply	Power supply input for LCD drive. Voltage between V_{DD} and V_3 is used as driving voltage.
COM_0	1	Output	LCD	LCD common (backplate) driving output.
SEG_0-SEG_{63}	64	Output	LCD	LCD segment driving output.
SYNC	1	Input	MCU	Synchronous input for 2 or more chips applications. LCD driver timing circuit is reset by high input. LCD is off.
OSC_1 OSC_2	2	Input Output	External R	Attach external R to these terminals for oscillation. An external clock (100 kHz) can be input to OSC_1.

Note: Logic polarity is positive. 1 = high = active.

Display RAM

HD61602 Display RAM

The HD61602 has an internal display RAM shown in figure 7. Display data is stored in the RAM, or is read according to the LCD driving timing to display on the LCD. One bit of the RAM corresponds to 1 segment of the LCD. Note that some bits of the RAM cannot be displayed depending on LCD driving mode.

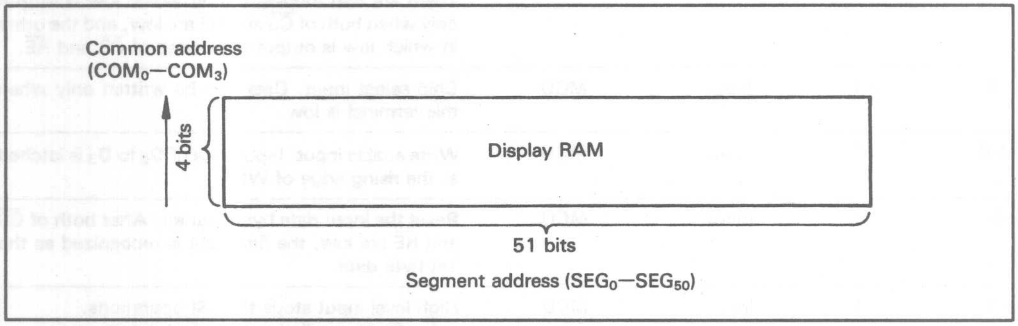


Figure 7 Display RAM

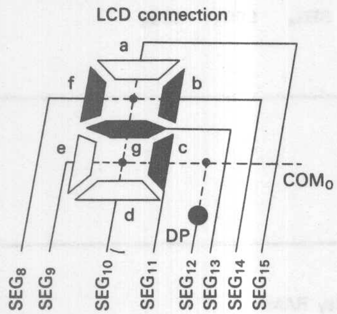
Reading Data from Display RAM: A display RAM segment address corresponds to a segment output. The data at segment address SEGn is output to segment output SEGn terminal.

A common address corresponds to the output timing of a common output and a segment output. The same common address data is simultaneously read. The data of display RAM is reproduced on the LCD panel.

When a 7-segment type LCD driver is connected, for example, the correspondence between the display RAM and the display pattern in each mode is as follows:

1. Static drive
   In the static drive, only the column of COM_0 of display RAM is output. COM_1 to COM_3 are not displayed.

LCD connection



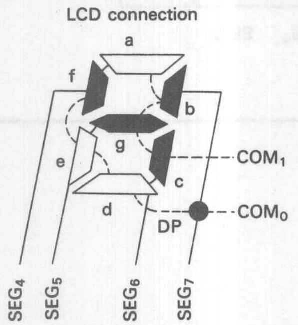
Display RAM

COM_3									
COM_2									
COM_1									
COM_0	f	e	d	c	DP	g	b	a	
	SEG_8	SEG_9	SEG_{10}	SEG_{11}	SEG_{12}	SEG_{13}	SEG_{14}	SEG_{15}	

2. 1/2 duty cycle drive

   In the 1/2 duty cycle drive, the columns of COM_0 and COM_1 of display RAM are output in time sharing. The columns of COM_2 and COM_3 are not displayed.

LCD connection



Display RAM

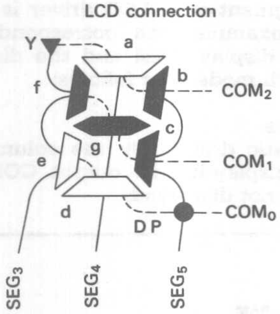
COM_3							
COM_2							
COM_1	a	g	c	b			
COM_0	f	e	d	DP			
	SEG_4	SEG_5	SEG_6	SEG_7	SEG_8	SEG_9	

3. 1/3 duty cycle drive

   In the 1/3 duty cycle drive, the columns of COM_0 to COM_2 are output in time sharing. No column of COM_3 is displayed.

"Y" cannot be rewritten by display data (input on an 8-segment basis). Please use bit manipulation to turn on/off the display of "Y".

LCD connection



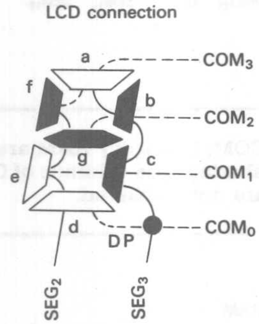
Display RAM

COM_3					
COM_2	Y	a	b		
COM_1	f	g	c		
COM_0	e	d	DP		
	SEG_3	SEG_4	SEG_5	SEG_6	

4. 1/4 duty cycle drive

In the 1/4 duty cycle drive, all the columns of COM_0 to COM_3 are displayed.

LCD connection



Display RAM

COM_3	f	a		
COM_2	g	b		
COM_1	e	c		
COM_0	d	DP		
	SEG_2	SEG_3	SEG_4	

Writing Data into Display RAM: Data is written into the display RAM in the following five methods:

1. Bit manipulation
   Data is written into any bit of RAM on a bit basis.
2. Static display mode
   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.
3. 1/2 duty cycle display mode
   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/2 duty cycle drive.
4. 1/3 duty cycle display mode
   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/3 duty cycle drive.
5. 1/4 duty cycle display mode
   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/4 duty cycle drive.

The RAM area and the allocation of the segment data for 1-digit display depend on the driving methods as described in "Reading Data from Display RAM".

8-bit data is written on a digit basis corresponding to the above duty cycle driving methods. The digits are allocated as shown figure 8 (allocation of digits). As the data can be transferred on a digit basis from a microprocessor, transfer efficiency is improved by allocating the LCD pattern according to the allocation of each bit data of the digit in the data RAM.
Figure 8 shows the digit address (displayed

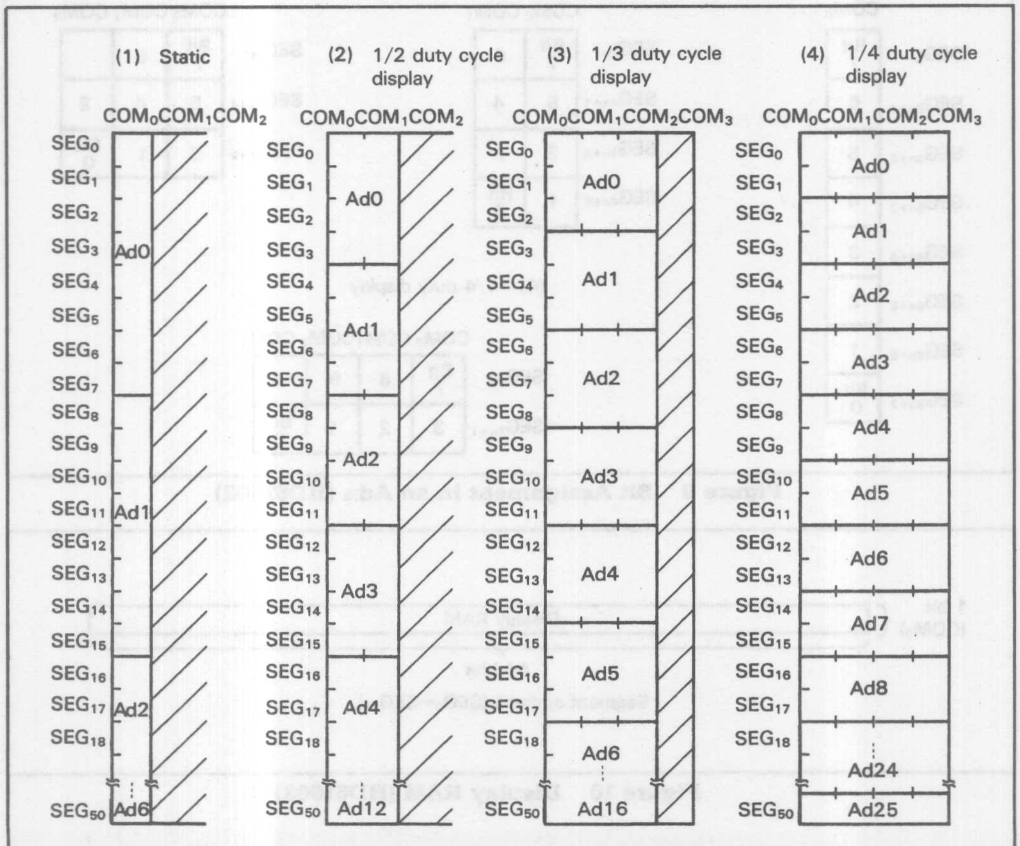


Figure 8 Allocation of Digit (HD61602)

as Adn) to specify the store address of the transferred 8-bit data on a digit basis.
Figure 9 shows the correspondence between each segment in an Adn and the 8-bit input data.
When data is transferred on a digit basis, 8-bit display data and digit address should be specified as described above.

However, when the digit address is Ad6 for static, Ad12 for 1/2 duty cycle, or Ad25 for 1/4 duty cycle, display RAM does not have enough bits for the data.

Thus the extra bits of the input 8-bit data are ignored.

In bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data, a segment address (6 bits) and a common address (2 bits) should be specified.

HD61603 Display RAM

The HD61603 has an internal display RAM an shown in figure 10. Display data is stored in the RAM and output to the segment output terminal.

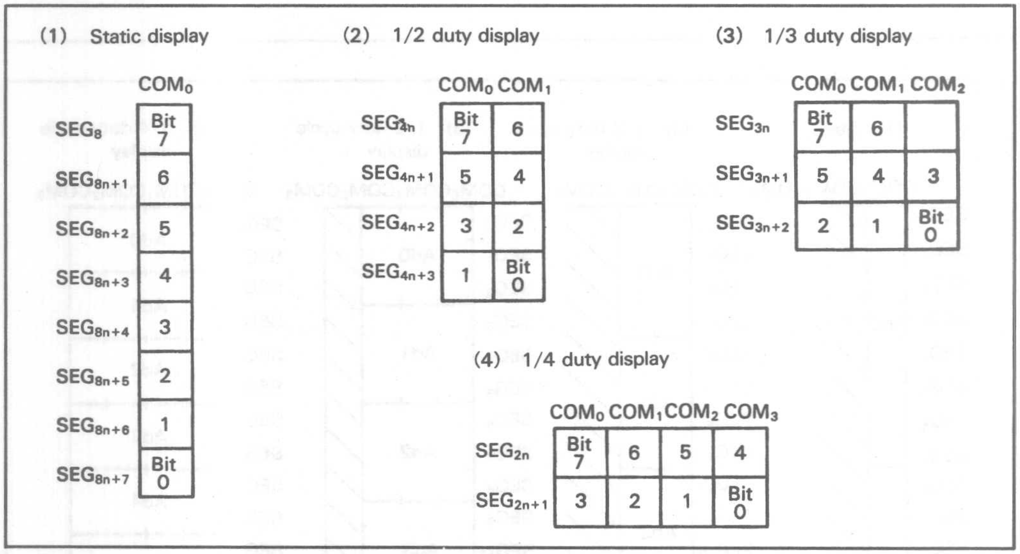


Figure 9 Bit Assignment in an Adn (HD61602)

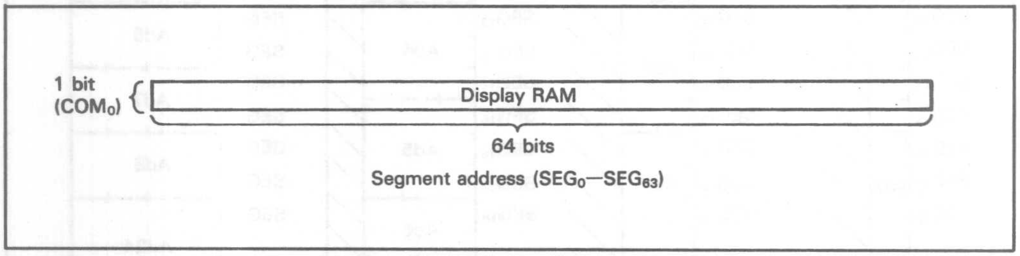


Figure 10 Display RAM (HD61603)

Reading Data from Display RAM: Each bit of the display RAM corresponds to an LCD segment. The data at segment address SEGn is output to segment output SEGn terminal. Figure 11 shows an example of the correspondence between the display RAM bit and the display pattern when a 7-segment type LCD is connected.

Writing Data into Display RAM: Data is written into the display RAM in the following two methods:

1. Bit manipulation
   Data is written into any bit of RAM on a bit basis.
2. Static display mode
   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

The 8-bit data is written on a digit basis into the digit address (displayed as Adn) shown in figure 12. When data is transferred from a microprocessor, four 4-bit data are needed to specify the digit address and an 8-bit display data. Figure 13 shows the correspondence between each segment in an Adn and the transferred 8-bit data.

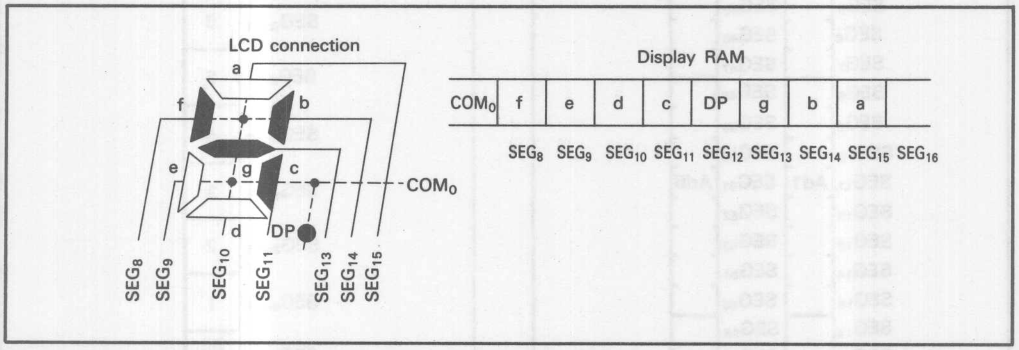


Figure 11 Example of Correspondence between Display RAM Bit and Display Pattern (HD61603)

In bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data and a segment address (6 bits) should be specified.

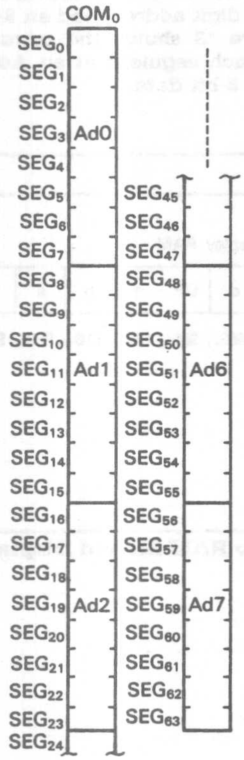


Figure 12 Allocation of Digits (HD61603)

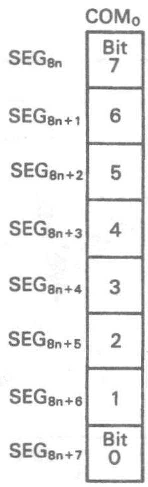


Figure 13 Bit Assignment in an Adn (HD61603)

OPERATING MODES

HD61602 Operating Modes

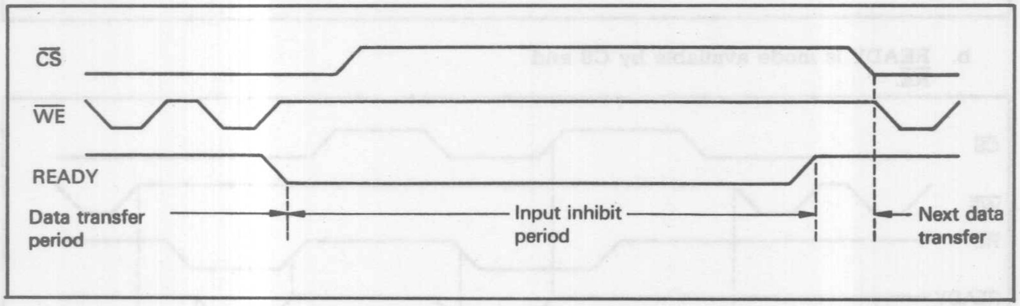
The HD61602 has the following operating modes:

1. LCD drive mode
   Determines the LCD driving method.
   a. Static drive mode
      LCD is driven statically.
   b. 1/2 duty cycle drive mode
      LCD is driven at 1/2 duty cycle and 1/2 bias.
   c. 1/3 duty cycle drive mode
      LCD is driven at 1/3 duty cycle and 1/3 bias.
   d. 1/4 duty cycle drive mode
      LCD is driven at 1/4 duty cycle and 1/3 bias.

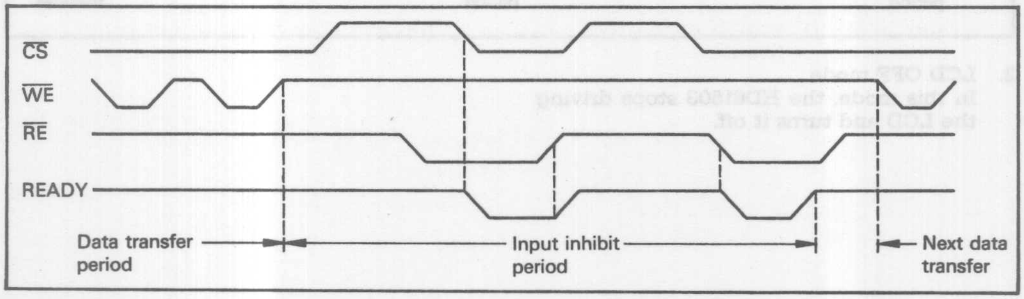
2. Data display mode
   Determines how to write display data into the data RAM.
   a. Static display mode
      8-bit data is written into the display RAM according to the digit in static drive.
   b. 1/2 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/2 duty cycle drive.
   c. 1/3 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/3 duty cycle drive.
   d. 1/4 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/4 duty cycle drive.

3. READY output mode
   Determines the READY output timing. After a data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when the READY is output can be selected from the following two modes:

a. READY is mode always available.



b. READY is mode available by $\overline{CS}$ and $\overline{RE}$.



4. LCD OFF mode
   In this mode, the HD61602 stops driving LCD and turns it off.

5. External driving voltage mode
   A mode for using external driving voltage (V_1, V_2, and V_3).

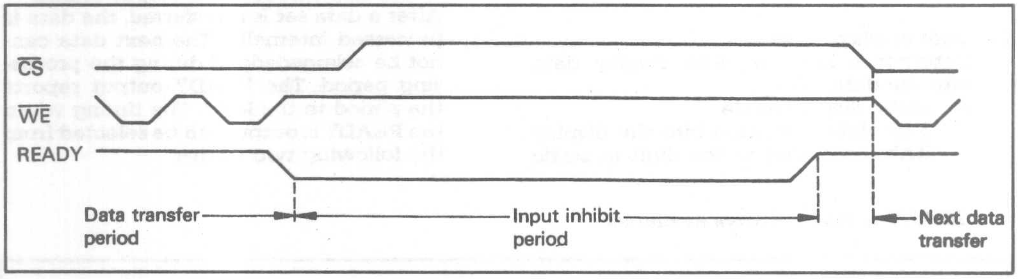
The above 5 modes are specified by mode setting data. The modes are independent of each other and can be used in any combination. Bit manipulation is independent of data display mode and can be used regardless of it.

HD61603 Operating Modes

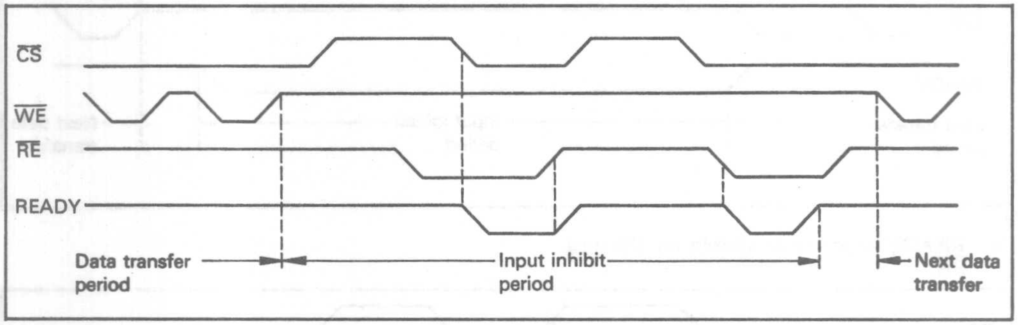
The HD61603 has the following modes:

1. READY output mode
   Determines the READY output timing. After a data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

   a. READY is always available.



   b. READY is mode available by $\overline{CS}$ and $\overline{RE}$.



2. LCD OFF mode
   In this mode, the HD61603 stops driving the LCD and turns it off.

INPUT DATA FORMATS

HD61602 Input Data Formats

Input data is composed of 8 bits × 2. Input them as 2-byte data after READY output changes from low to high or low pulse is entered into $\overline{RE}$ terminal.

1. Display data (Updates display on an 8-segment basis)

1st byte

7	6	5	4	3	2	1	0
0	0	×	Display address (Digit address Adn)				

2nd byte

7	6	5	4	3	2	1	0
Display data							

a. Display address: Digit address Adn in accordance with display mode

b. Display data: Pattern data that is written into the display RAM according to display mode and the address

2. Bit manipulation data (Updates display on a segment basis)

1st byte

7	6	5	4	3	2	1	0
0	1	Display data	×	×	×	COM address	

2nd byte

7	6	5	4	3	2	1	0
×	×	SEG address					

a. Display data: Data that is written into 1 bit of the specified display RAM

b. COM address: Common address of display RAM

c. SEG address: Segment address of display RAM

3. Mode setting data

1st byte

7	6	5	4	3	2	1	0
1	0	×	0	External power supply	READY bit	Drive mode bits	

2nd byte

7	6	5	4	3	2	1	0
×	×	×	×	×	OFF/ON bit	Display mode bits	

a. Display mode bits:
   - 00: Static display mode
   - 01: 1/2 duty cycle display mode
   - 10: 1/3 duty cycle display mode
   - 11: 1/4 duty cycle display mode

b. OFF/ON bit:
   - 1: LCD off (set to 1 when SYNC is entered.)
   - 0: LCD on

c. Drive mode bits:
   - 00: Static drive
   - 01: 1/2 duty cycle drive
   - 10: 1/3 duty cycle drive
   - 11: 1/4 duty cycle drive

d. READY bit:
   - 0: READY bus mode; $\overline{READY}$ outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0. (reset to 0 when SYNC is entered.)
   - 1: READY port mode; $\overline{READY}$ outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$.

e. External power supply bit:
   - 0: Driving voltage is generated internally.
   - 1: Driving voltage is supplied externally. (set to 1 when SYNC is entered.)

4. 1-byte instruction

1st byte

7	6	5	4	3	2	1	0
1	1	×	×	×	×	×	×

The first data (first byte) is ignored when bit 6 and bit 7 in the byte are 1.

HD61603 Input Data Formats

Input data is composed of 4 bits × 4. Input them as four 4-bit data after READY output changes from low to high or low pulse is entered into $\overline{RE}$ terminal.

1. Display data (Updates display on an 8-segment basis.)

1st byte

3	2	1	0
0	0	×	×

2nd byte

3	2	1	0
×	Display address (Digit address Adn)		

3rd byte

3	2	1	0
Display data Bit 7	6	5	4

4th byte

3	2	1	0
Display data Bit3	2	1	0

a. Display address: Digit address Adn shown in figure 12.

b. Display data: Pattern data that is written into the display RAM as shown in figure 13.

2. Bit manipulation data (Updates display on a segment basis.)

1st byte

3	2	1	0
0	1	Display data	×

2nd byte

3	2	1	0
×	×	0	0

3rd byte

3	2	1	0
×	×	SEG address Bit 5	4

4th byte

3	2	1	0
SEG address Bit 3	2	1	0

a. Display data: Data that is written into 1 bit of the specified display RAM.

b. SEG address: Segment address of display RAM (segment output).

3. Mode setting data

1st byte

3	2	1	0
1	0	×	0

2nd byte

3	2	1	0
×	READY bit	×	×

3rd byte

3	2	1	0
×	×	×	×

4th byte

3	2	1	0
×	OFF/ON bit	0	0

a. OFF/ON bit:
   1: LCD off (set to 1 when SYNC is entered.)
   0: LCD on

b. READY bits:
   0: READY bus mode; $\overline{READY}$ outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0. (reset to 0 when SYNC is entered.)
   1: READY port mode; $\overline{READY}$ outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$.

4. 1-byte instruction

1st byte

3	2	1	0
1	1	×	×

The first data (4 bits) is ignored when bit 3 and 2 in the data are 1.

How To Input Data

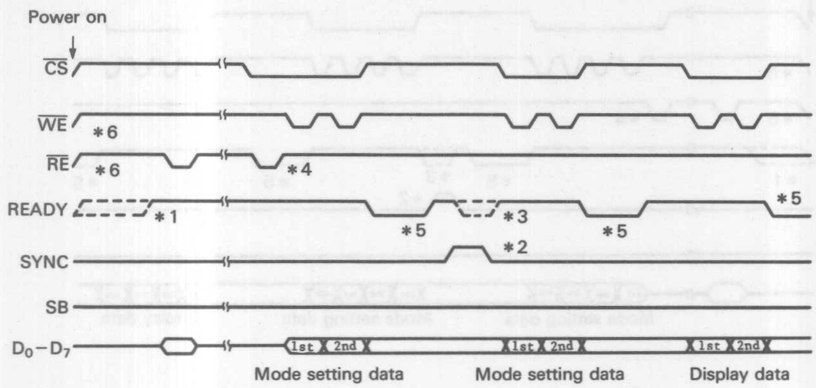
How to Input HD61602 Data

Input data is composed of 8 bits × 2. Take care that the data transfer is not interrupted, because the first 8-bit data is distinguished from the second one by the sequence only.

If data transfer is interrupted, or at power on, the following two methods can be used to reset the count of the number of bytes (count of the first and second bytes):

1. Set $\overline{CS}$ and $\overline{RE}$ inputs low (no display data changes).
2. Input 2 or more "1-byte instruction" data in which bit 7 and 6 are 1 (display data may change).

The data input method via data input terminals ($\overline{CS}$, $\overline{WE}$, D_0 to D_7) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microprocessor are used for an access, refer to the timing specifications and figure 14.



*1: READY output is indefinite during 12 clocks after the oscillation start at power on (clock: OSC_2 clock).
*2: High pulse should be applied to SYNC terminal when using two or more chips synchronously.
*3: In the mode in which READY is always available, READY output is in definite while SYNC is high.
*4: Reset the byte counter after power on.
*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
*6: Connect a pull-up resister if $\overline{WE}$ or $\overline{RE}$ may be floating.
*7: It is not always necessary to follow this example.

Figure 14 Example of Data Transfer Sequence

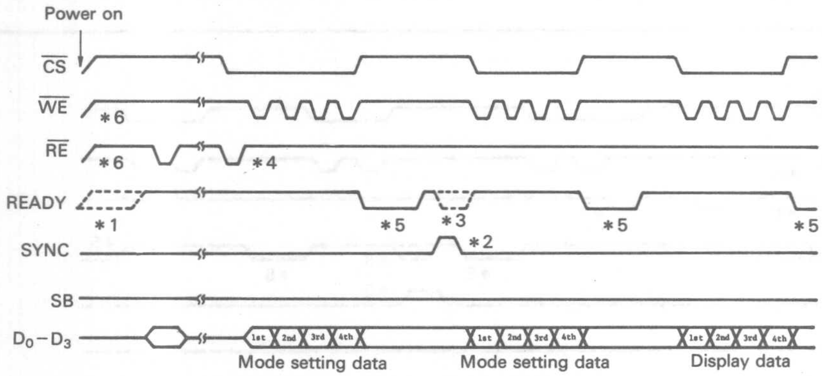
How to Input HD61603 Data

Input data is composed of 4 bits × 4. Take care that data transfer is not interrupted, because the first 4-bit data to the fourth 4-bit data are distinguished from each other by the sequence only.

If data transfer is interrupted, or at power on, the following two methods can be used to reset the count of the number of data (count of the first 4-bit data to the fourth 4-bit data):

1. Set $\overline{CS}$ and $\overline{RE}$ low.
2. Input 4 or more "1-byte instruction" data (4-bit data) in which bit 3 and 2 are 1 (display data may change).

The data input method via data input terminals ($\overline{CS}$, $\overline{WE}$, DO to D3) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microprocessor are used for an access, refer to the timing specifications and figure 15.



*1: READY output is indefinite during 12 clocks after the oscillation start at power on (clock: OSC_2 clock).
*2: High pulse should be applied to SYNC terminal when using two or more chips synchronously.
*3: In the mode in which READY is always available, READY output is indefinite while SYNC is high.
*4: Reset the 4-bit data counter after power on.
*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
*6: Connect a pull-up resister if $\overline{WE}$ or $\overline{RE}$ may be floating.
*7: It is not always necessary to follow this example.

Figure 15 Example of Data Transfer Sequence

Notes on READY Output

Note that the READY output will be unsettled during 1.5 clocks (max) after inputting the first 2-byte data for setting the mode after turning the power on. This is because the READY bit data of mode setting latches and the mode of READY pin (READY bus or port mode) are unsettled until the completion of mode setting.

There are two kinds of the READY output waveforms depending of the modes:

1. READY bus mode (READY bit = 0)
2. READY port mode (READY bit = 1)

However, if you input SYNC before mode setting, waveform will be determined; when you choose READY bus mode, (1) a in figure 16 will be output, and when you choose READY port mode, (2) a will be output. The figures can be applied both to HD61602 and HD61603.

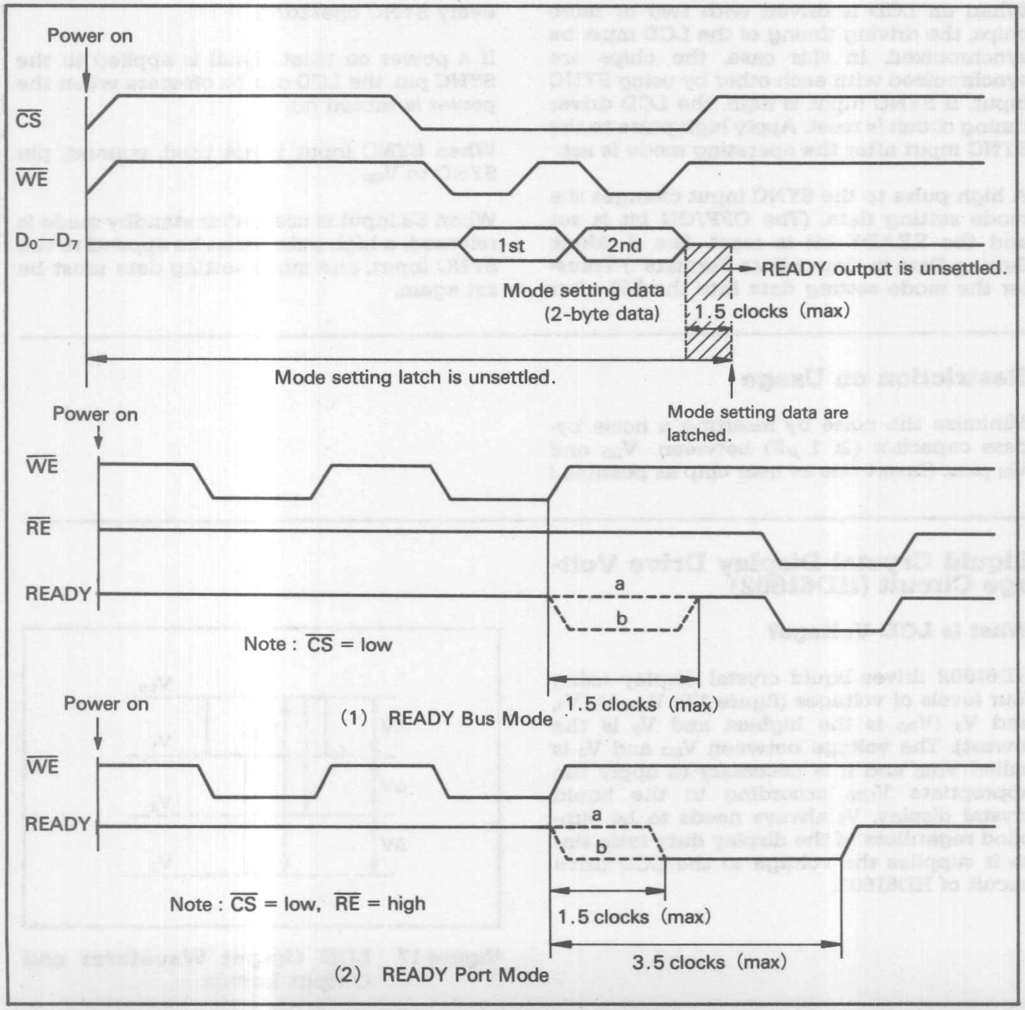


Figure 16 READY Output According to Modes

Standby Operation

Standby operation with low power consumption can be activated when pin SB is used. Normal operation of the LSI is activated when pin SB is low level, and the LSI goes into the standby state when pin SB is high level. The standby state of the LSI is as follows:

1. LCD driver is stopped (LCD is off).
2. Display data and operating mode are held.
3. The operation is suspended while display changes (while READY is outputting low.) In this case, READY outputs high within 10.5 clocks or 3.5 clocks after release from the standby mode.
4. Oscillation is stopped.

When this mode is not used, connect pin SB to V_{SS}.

Multichip Operation

When an LCD is driven with two or more chips, the driving timing of the LCD must be synchronized. In this case, the chips are synchronized with each other by using SYNC input. If SYNC input is high, the LCD driver timing circuit is reset. Apply high pulse to the SYNC input after the operating mode is set.

A high pulse to the SYNC input changes the mode setting data. (The OFF/ON bit is set and the READY bit is reset. See 3. Mode Setting Data in "Input Data Formats".) Transfer the mode setting data into the LSI after every SYNC operation.

If a power on reset signal is applied to the SYNC pin, the LCD can be off-state when the power is turned on.

When SYNC input is not used, connect pin SYNC to V_{SS}.

When SB input is used, after standby mode is released, a high pulse must be applied to the SYNC input, and mode setting data must be set again.

Restriction on Usage

Minimize the noise by inserting a noise bypass capacitor ($\geqq$ 1 μF) between V_{DD} and V_{SS} pins. (Insert one as near chip as possible.)

Liquid Crystal Display Drive Voltage Circuit (HD61602)

What is LCD Voltage?

HD61602 drives liquid crystal display using four levels of voltages (figure 17); V_{DD}, V_1, V_2, and V_3 (V_{DD} is the highest and V_3 is the lowest). The voltage between V_{DD} and V_3 is called V_{LCD} and it is necessary to apply the appropriate V_{LCD} according to the liquid crystal display. V_3 always needs to be supplied regardless of the display duty ratio since it supplies the voltage to the LCD drive circuit of HD61602.

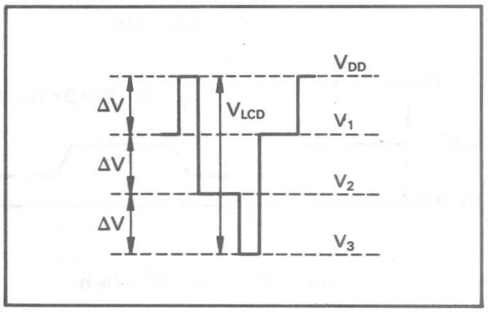


Figure 17 LCD Output Waveform and Output Levels

When Internal Drive Power Supply is Used

When the internal drive power supply is used, attach C_1-C_4 for charge pump circuits and variable resistance R_1 for deciding display drive voltage to HD61602 as shown in figure 18.

Internal voltage is available by setting external voltage switching bits of mode setting data 0.

Figure 19 shows voltage characteristics between V_{DD} and V_{REF1}. Voltage is divided at R_1, and then input into V_{REF2}. Voltage between V_{DD} and V_{REF2} is equivalent to ΔV in figure 19, and so V_{LCD} can be changed by regulating the voltage.

V_{REF2} is usually regulated by variable resistance, but when replacing R_1 with two nonvariable resistances take V_{REF1} between max and min into consideration as shown in figure 19.

Internal drive power supply is generated by using capacitance, and so large current cannot flow. When large liquid crystal display panel is used, examine the external drive power supply.

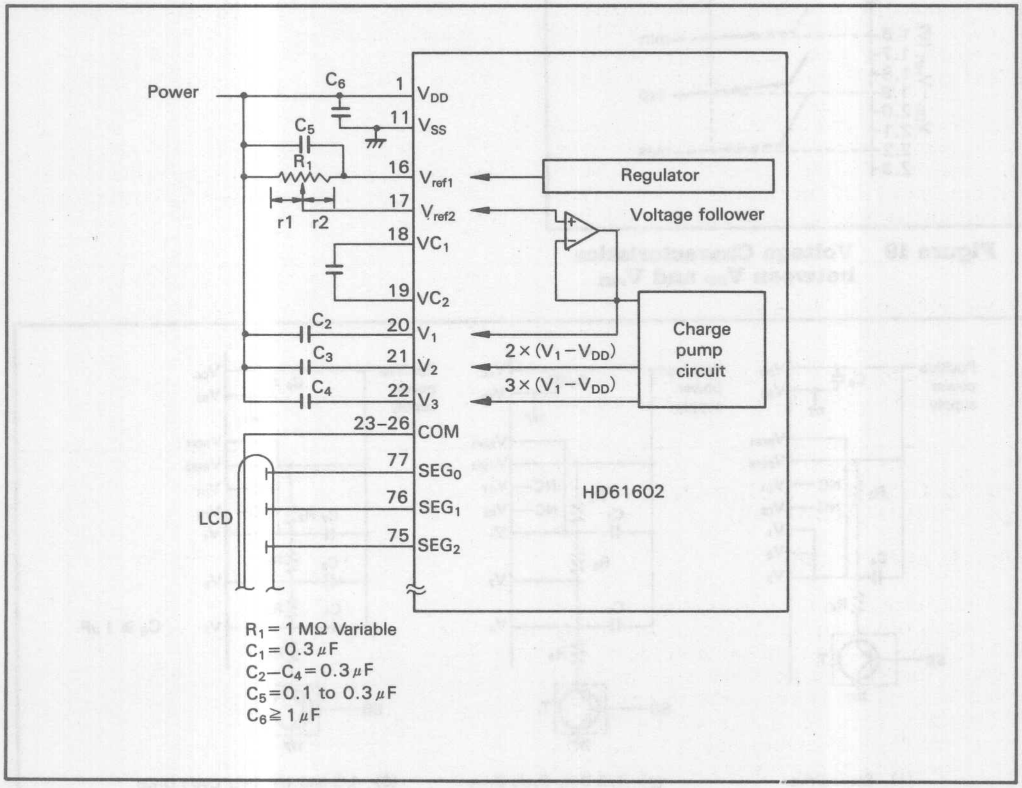


Figure 18 Example

When External Drive Power Supply is Used

An external power supply can be used by setting external voltage switching bits of mode setting data to 1. When a large liquid crystal display panel is used, in multichip designs, which need accurate liquid crystal drive voltage, use the external power supply. See figure 20.

R_2-R_5 is connected in series between V_{DD} and V_{SS}, and by these resistance ratio each voltage of ΔV and V_{LCD} is generated and then supplied to V_1, V_2, and V_3. C_2-C_4 are smoothing capacitors.

When regulating brightness, change the resistance value by setting R_5 variable resistance.

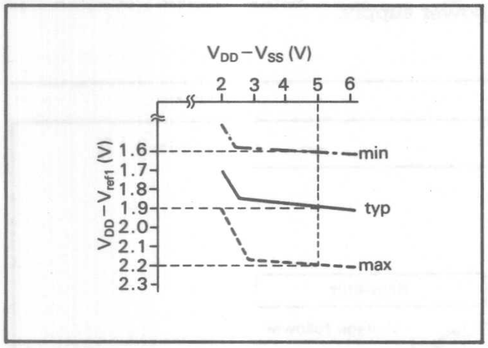
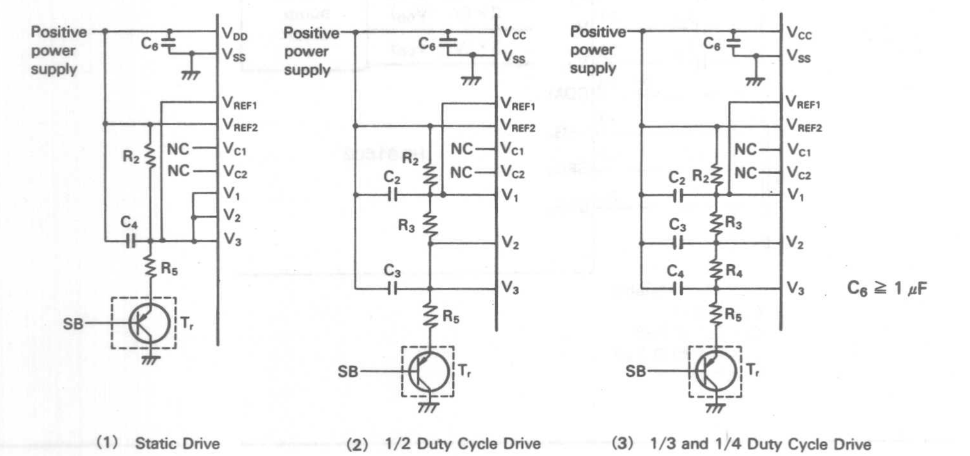


Figure 19 Voltage Characteristics between V_{DD} and V_{ref1}



Note: 1. When standby mode is used, a transistor is required.
2. R_2-R_5 should be some kΩ-some tens of kΩ, and C_2-C_4 should be 0.1 μF−0.3 μF.

Figure 20 Example when External Drive Voltage is Used

Liquid Crystal Display Drive Voltage (HD61603)

As shown in figure 21, apply LCD drive voltage from the external power supply.

Oscillation Circuit

When Internal Oscillation Circuit is Used

When the internal oscillation circuit is used, attach an external resister R_{OSC} as shown in figure 22. (Insert R_{OSC} as near chip as possible, and make the OSC1 side shorter.)

When External Clock is Used

When an external clock of 100 kHz with CMOS level is provided, pin OSC_1 can be used for the input pin. In this case, open pin OSC_2.

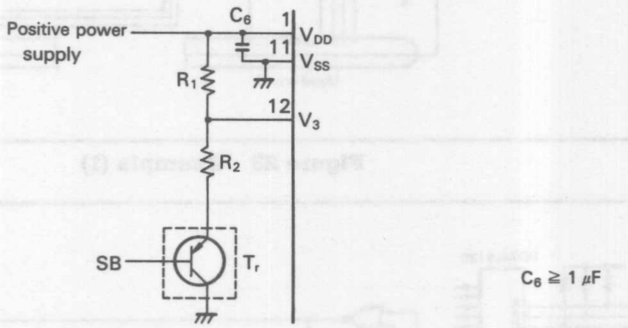


Figure 21 Example of Drive Voltage Generator

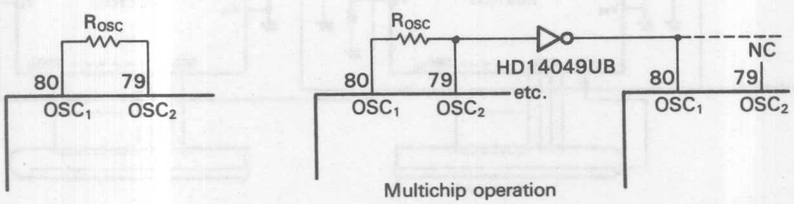


Figure 22 Example of Oscillation Circuit

Applications

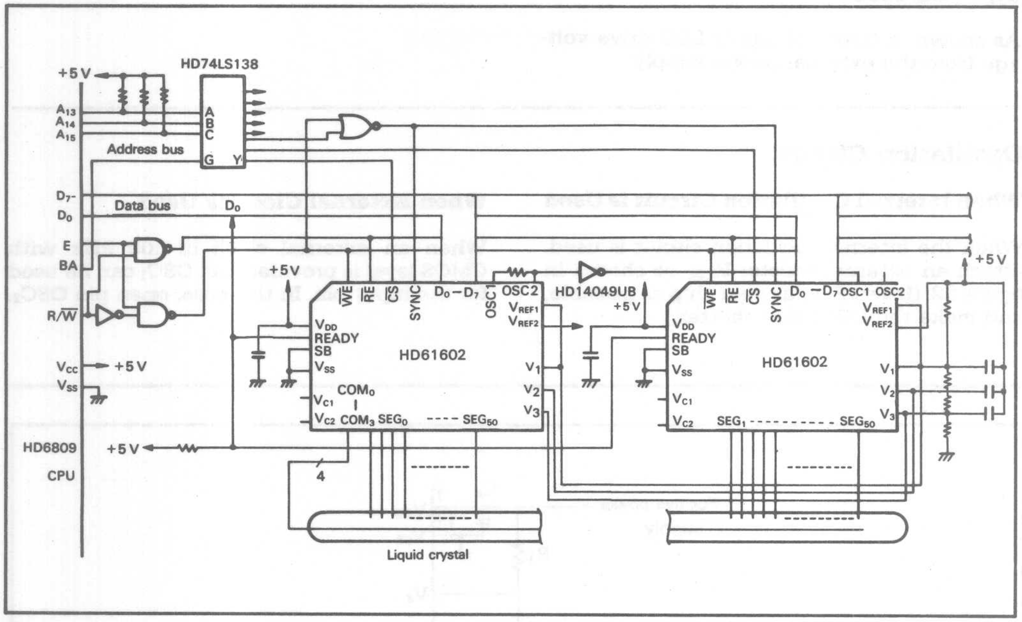


Figure 23 Example (1)

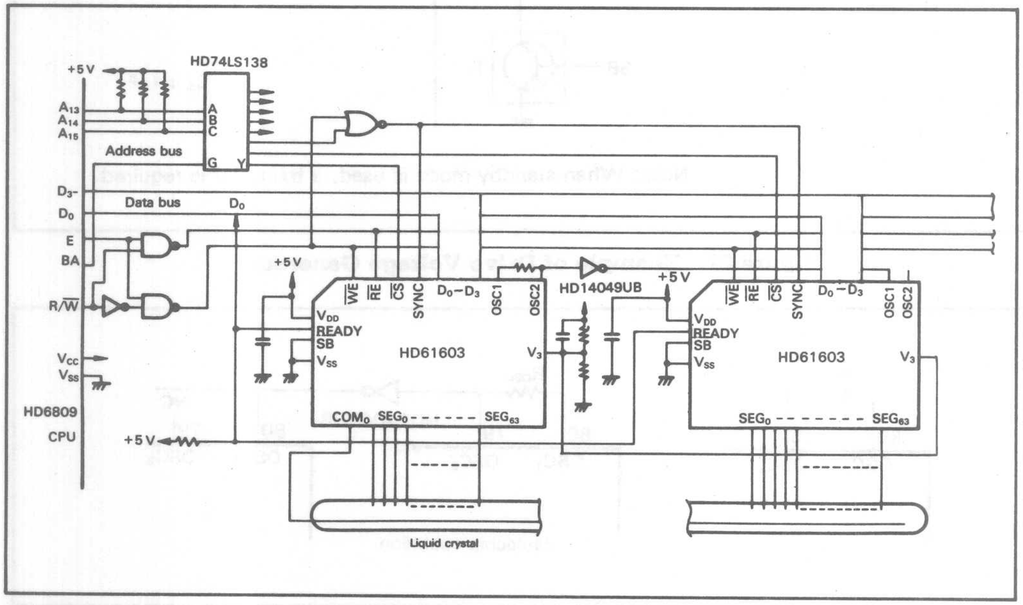


Figure 24 Example (2)

HD61604/HD61605

(Segment Type LCD Driver)

Description

The HD61604 and the HD61605 are liquid crystal display driver LSIs with TTL and CMOS compatible interface. Each of the LSIs can be connected to various microprocessors such as the HMCS6800 series.

Several types of liquid crystal displays can be connected to the HD61604 according to the applications because of the software-controlled liquid crystal dispay drive method.

The HD61605 is a liquid crystal display driver LSI only for static drive and has 64 segment outputs that can display 8 digits per chip.

Features

- Low current consumption
  —Can drive from a battery power supply (100 μA max on 5 V).
  —Standby input enables a standby operation at lower current consumption (5 μA max on 5 V).

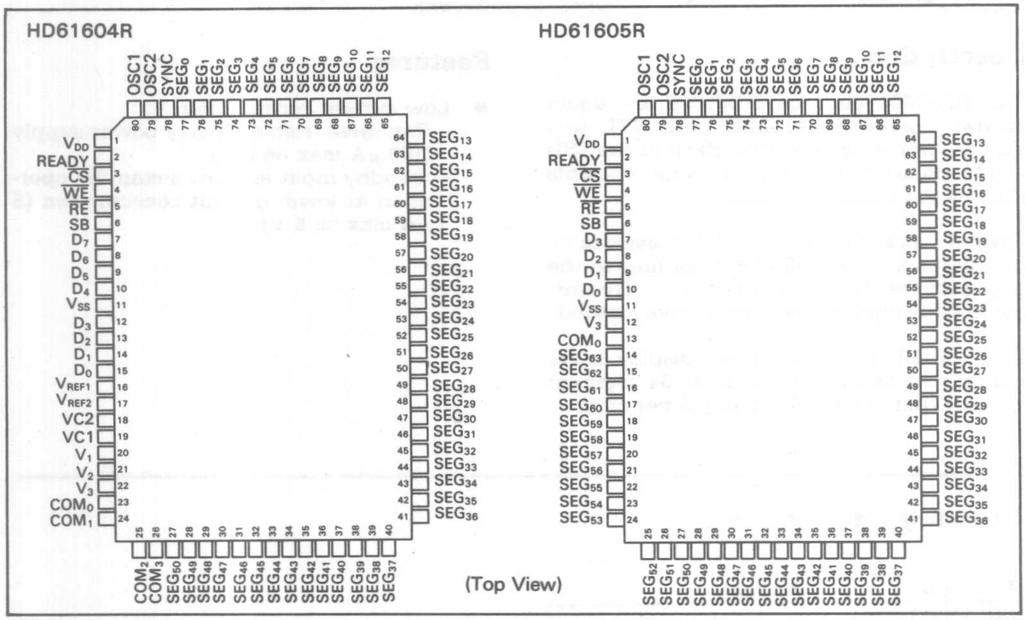
Ordering Information

Type No.	Package
HD61604R	80-pin plastic QFP(FP-80)
HD61605R	

Versatile Segment Driving Capacity

Type No.	Drive Method	Display Segments	Example of Use	Frame Freq (Hz) at fosc=100 kHz
HD61604R	Static	51	8 segments × 6 digits + 3 marks	98
	1/2 bias 1/2 duty cycle	102	8 segments × 12 digits + 6 marks	195
	1/3 bias 1/3 duty cycle	153	9 segments × 17 digits	521
	1/4 duty cycle	204	8 segments × 25 digits + 4 marks	781
HD61605R	Static	64	8 segments × 8 digits	98

Pin Arrangement



Block Diagram

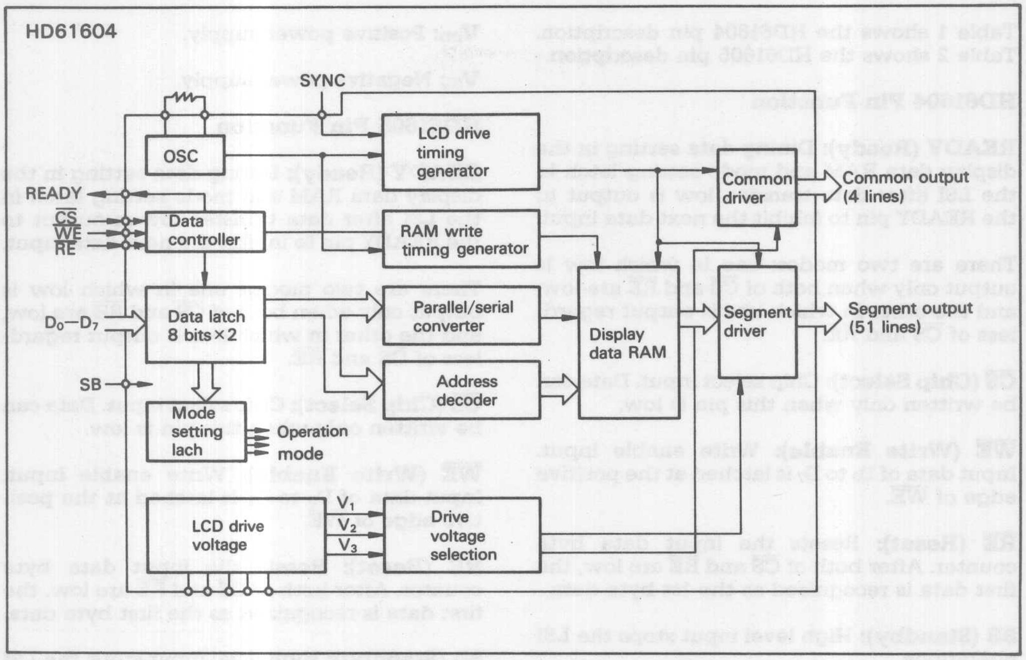


Figure 1 HD61604 Block Diagram

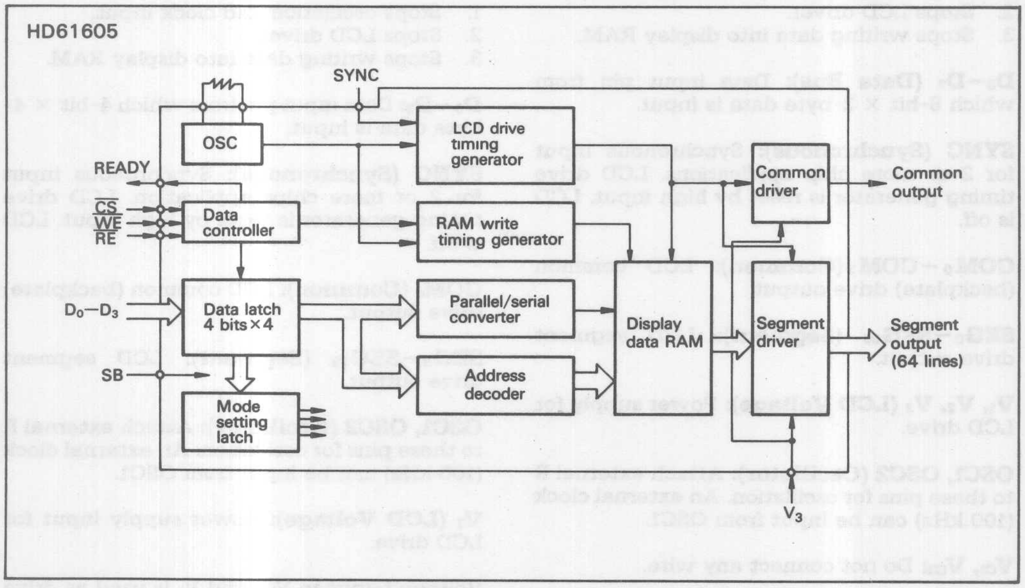


Figure 2 HD61605 Block Diagram

Pin Functions

Table 1 shows the HD61604 pin description. Table 2 shows the HD61605 pin description.

HD61604 Pin Function

READY (Ready): During data setting in the display data RAM and mode setting latch in the LSI after data transfer, low is output to the READY pin to inhibit the next data input.

There are two modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.

$\overline{CS}$ (Chip Select): Chip select input. Data can be written only when this pin is low.

$\overline{WE}$ (Write Enable): Write enable input. Input data of D_0 to D_7 is latched at the positive edge of $\overline{WE}$.

$\overline{RE}$ (Reset): Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the 1st byte data.

SB (Standby): High level input stops the LSI operations.

1. Stops oscillation and clock input.
2. Stops LCD driver.
3. Stops writing data into display RAM.

D_0-D_7 (Data Bus): Data input pin from which 8-bit × 2-byte data is input.

SYNC (Synchronous): Synchronous input for 2 or more chip applications. LCD drive timing generator is reset by high input. LCD is off.

COM_0-COM_3 (Common): LCD common (backplate) drive output.

SEG_0-SEG_{50} (Segment): LCD segment drive output.

V_1, V_2, V_3 (LCD Voltage): Power supply for LCD drive.

OSC1, OSC2 (Oscillator): Attach external R to these pins for oscillation. An external clock (100 kHz) can be input from OSC1.

V_{C1}, V_{C2}: Do not connect any wire.

V_{REF1}: Connect this pin to V1 pin.

V_{REF2}: Hold at V_{DD} level.

V_{DD}: Positive power supply.

V_{SS}: Negative power supply.

HD61605 Pin Function

READY (Ready): During data setting in the display data RAM and mode setting latch in the LSI after data transfer, low is output to the READY pin to inhibit the next data input.

There are two modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.

$\overline{CS}$ (Chip Select): Chip select input. Data can be written only when this pin is low.

$\overline{WE}$ (Write Enable): Write enable input. Input data of D_0 to D_3 is latched at the positive edge of $\overline{WE}$.

$\overline{RE}$ (Reset): Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the first byte data.

SB (Standby): High level input stops the LSI operations.

1. Stops oscillation and clock input.
2. Stops LCD driver.
3. Stops writing data into display RAM.

D_0-D_3: Data input pin from which 4-bit × 4-byte data is input.

SYNC (Synchronous): Synchronous input for 2 or more chips application. LCD drive timing generator is reset by high input. LCD is off.

COM_0 (Common): LCD common (backplate) drive output.

SEG_0-SEG_{63} (Segment): LCD segment drive output.

OSC1, OSC2 (Oscillator): Attach external R to these pins for oscillation. An external clock (100 kHz) can be input from OSC1.

V_3 (LCD Voltage): Power supply input for LCD drive.

Voltage between V_{DD} and V_3 is used as drive voltage.

V_{SS}: Negative power supply.

V_{DD}: Positive power supply.

Table 1 HD61604 Pin Description

Pin Name	No.of Lines	Input/Output	Connected to
READY	1	NMOS open drain output	MCU
$\overline{CS}$	1	Input	MCU
$\overline{WE}$	1	Input	MCU
$\overline{RE}$	1	Input	MCU
SB	1	Input	MCU
D_0-D_7	8	Input	MCU
SYNC	1	Input	MCU
COM_0-COM_3	4	Output	LCD
SEG_0-SEG_{50}	51	Output	LCD
V_1, V_2, V_3	3	Power supply	External R
OSC1, OSC2	2	Input, output	External R
V_{C1}, V_{C2}	2	Output	
V_{REF1}	1	Input	V_1
V_{REF2}	1	Input	V_{DD}
V_{DD}	1	Power supply	
V_{SS}	1	Power supply	

Note: Logic polarity is positive.
1 = high = active.

Table 2 HD61605 Pin Description

Pin Name	No.of Lines	Input/Output	Connected to
READY	1	NMOS open drain output	MCU
$\overline{CS}$	1	Input	MCU
$\overline{WE}$	1	Input	MCU
$\overline{RE}$	1	Input	MCU
SB	1	Input	MCU
D_0-D_3	4	Input	MCU
SYNC	1	Input	MCU
COM_0	1	Output	LCD
SEG_0-SEG_{63}	64	Output	LCD
OSC1, OSC2	2	Input, output	External R
V_3	1	Input	Power supply
V_{SS}	1	Power supply	
V_{DD}	1	Power supply	

Note: Logic polarity is positive.
1 = high = active.

Display RAM

HD61604 Display RAM

The HD61604 has an internal display RAM shown in figure 3. Display data is stored in the RAM, or is read according to the LCD drive timing to display on the LCD. One bit of the RAM corresponds to 1 segment of LCD. Note that some bits of the RAM cannot be displayed depending on LCD drive modes.

Reading Data from HD61604 Display RAM

A display RAM segment address corresponds to a segment output. The data at segment address SEGn is output to segment output SEGn pin.

A common address corresponds to the output timings of a common output and a segment output. The same common address data is simultaneously read. The data of display RAM is reproduced on the LCD panel.

The following shows the correspondence between the 7-segment type LCD connection and the display RAM in each mode.

1. **Static Drive:** In static drive, only the column of COM_0 of display RAM is output. COM_1 to COM_3 are not displayed (figure 4).

2. **1/2 Duty Cycle Drive:** In the 1/2 duty cycle drive, the columns of COM_0 and COM_1 of display RAM are output in time sharing. The columns of COM_2 and COM_3 are not displayed (figure 5).

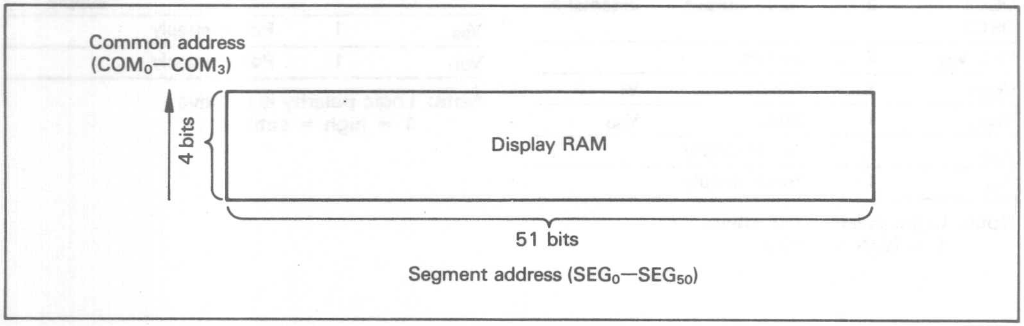
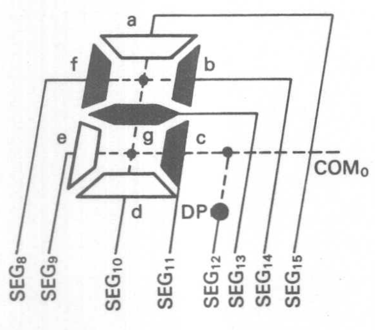


Figure 3 Display RAM (HD61604)

LCD connection



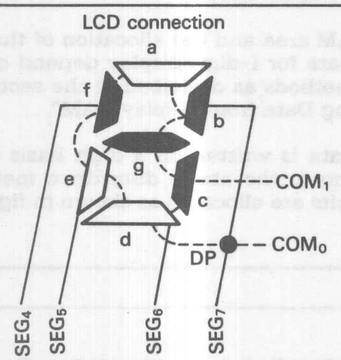
Display RAM

COM_3								
COM_2								
COM_1								
COM_0	f	e	d	c	DP	g	b	a
	SEG_8	SEG_9	SEG_{10}	SEG_{11}	SEG_{12}	SEG_{13}	SEG_{14}	SEG_{15}

Figure 4 Example of Correspondence between LCD Connection and Display RAM (Static Drive, HD61604)

3. **1/3 Duty Cycle Drive:** In the 1/3 duty cycle drive, the columns of COM_0 to COM_2 are output in time sharing. No column of COM_3 is displayed. "y" cannot be rewritten by display data (input on an 8-segment basis). Please use bit manipulation in turning on/off the display of "y" cycle (figure 6).

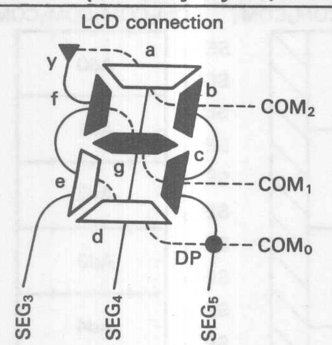
4. **1/4 Duty Cycle Drive:** In the 1/4 duty cycle drive, all the columns of COM_0 to COM_3 are displayed (figure 7).



Display RAM

COM_3				
COM_2				
COM_1	a	g	c	b
COM_0	f	e	d	DP
	SEG_4	SEG_5	SEG_6	SEG_7

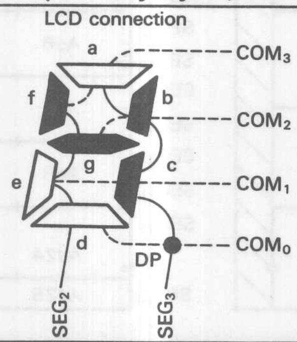
Figure 5 Example of Correspondence between LCD Connection and Display RAM (1/2 Duty Cycle, HD61604)



Display RAM

COM_3			
COM_2	y	a	b
COM_1	f	g	c
COM_0	e	d	DP
	SEG_3	SEG_4	SEG_5

Figure 6 Example of Correspondence between LCD Connection and Display RAM (1/3 Duty Cycle, HD61604)



Display RAM

COM_3	f	a
COM_2	g	b
COM_1	e	c
COM_0	d	DP
	SEG_2	SEG_3

Figure 7 Example of Correspondence between LCD Connection and Display RAM (1/4 Duty Cycle, HD61604)

Writing Data into HD61604 Display RAM

Data is written into the display RAM in the following five methods:

1. **Bit Manipulation:** Data is written into any bit of RAM on a bit basis.
2. **Static Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.
3. **1/2 Duty Cycle Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/2 duty cycle drive.
4. **1/3 Duty Cycle Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/3 duty cycle drive.
5. **1/4 Duty Cycle Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/4 duty cycle drive.

The RAM area and the allocation of the segment data for 1-digit display depend on the drive methods as described in the section of "Reading Data from Display RAM".

8-bit data is written on a digit basis corresponding to the above duty drive methods. The digits are allocated as shown in figure 8.

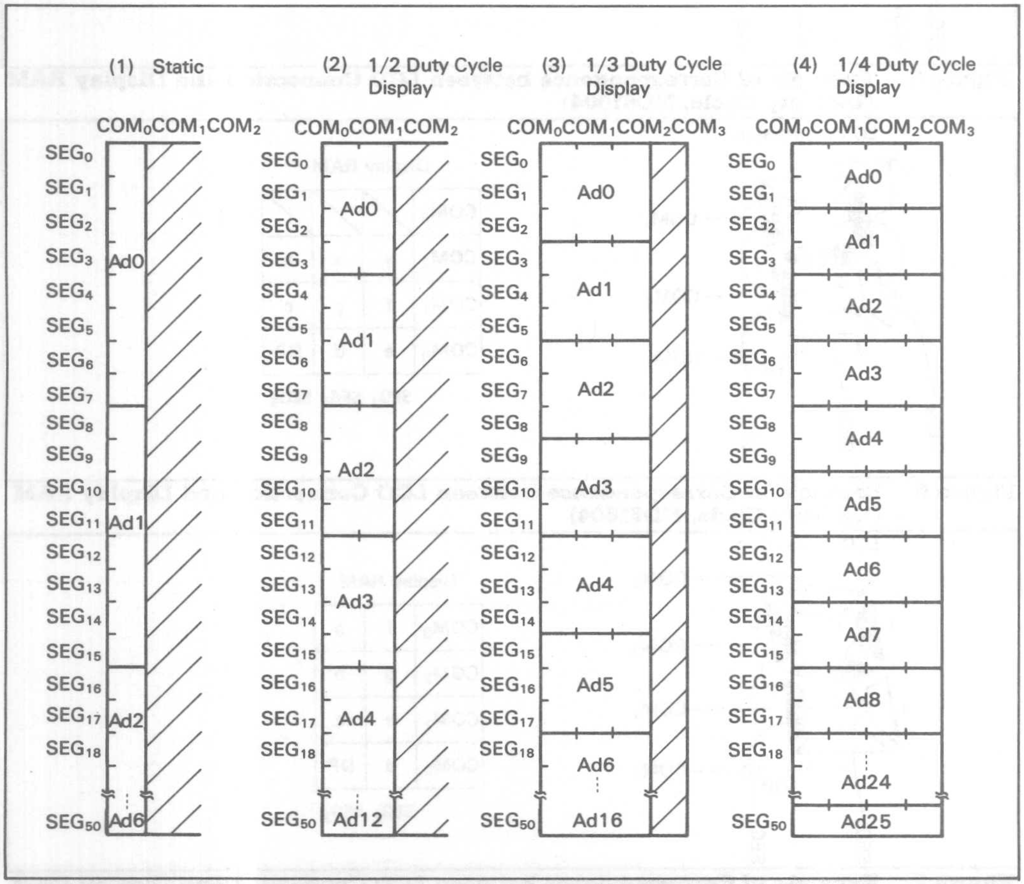


Figure 8 Allocation of Digits (HD61604)

As the data can be transferred on a digit basis from a microprocessor, transfer efficiency is improved by allocating the LCD pattern according to the allocation of each bit data of the digit in the data RAM.

Figure 8 shows the digit address (displayed as Adn) to specify the store address of the transferred 8-bit data on a digit basis.

Figure 9 shows the correspondence between each segment in an Adn and the 8-bit input data.

When data is transferred on a digit basis, 8-bit display data and digit address should be specified as described above.

However, when the digit address is Ad6 of static, Ad12 of 1/2 duty cycle, or Ad25 of 1/4 duty cycle, display RAM does not have enough bits for the data. Thus the extra bits of the input 8-bit data are ignored.

In bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data, a segment address (6 bits)s and a common address (2 bits) should be specified.

HD61605 Display RAM

The HD61605 has an internal display RAM as shown in figure 10. Display data is stored in the RAM and output to the segment output pin.

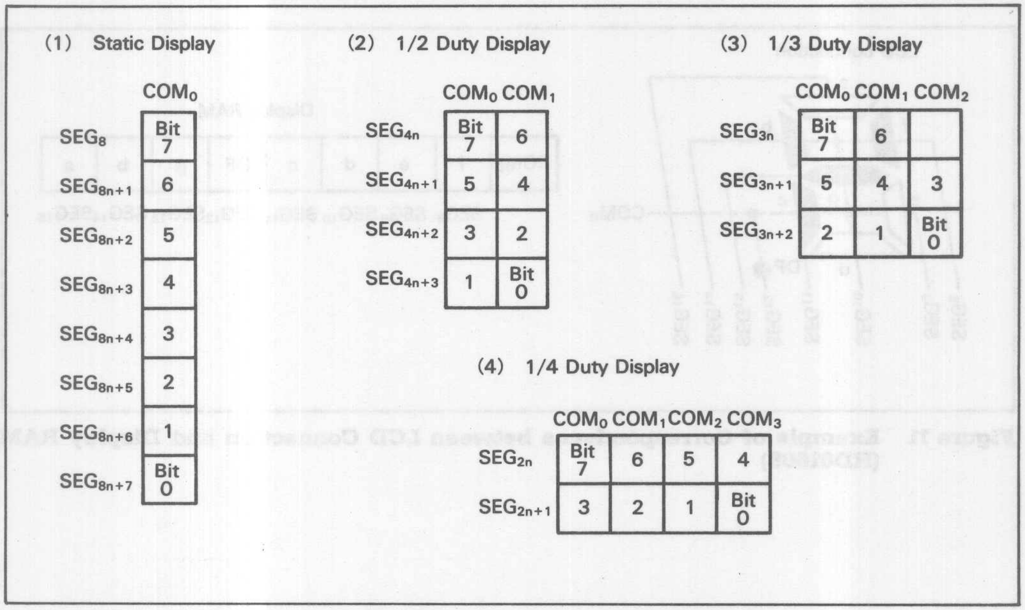


Figure 9 Bit Assignment in an Adn (HD61604)

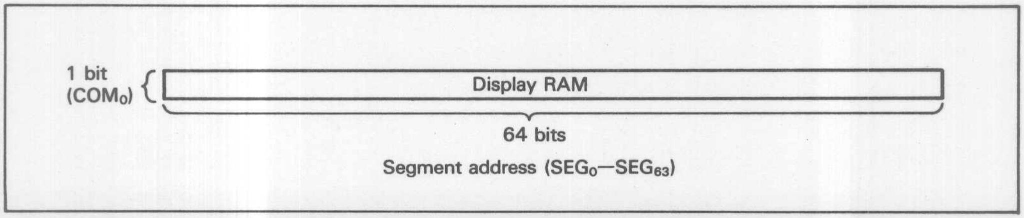


Figure 10 Display RAM (HD61605)

Reading Data from HD61605 Display RAM

Each bit of the display RAM corresponds to an LCD segment. The data at segment address SEGn is output to segment output SEGn pin. Figure 11 shows the correspondence between the 7-segment type LCD connection and the display RAM .

Writing Data into HD61605 Display RAM

Data is written into the display RAM in the following two methods:

1. **Bit Manipulation:** Data is written into any bit of RAM on a bit basis.
2. **Static Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

The 8-bit data is written on a digit basis into the digit address (displayed as Adn) shown in figure 12. When data is transferred from a microprocessor, four 4-bit data are needed to specify the digit address and an 8-bit display data. Figure 13 shows the correspondence between each segment in an Adn and the transferred 8-bit data.

In bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data and a segment address (6 bits) should be specified.

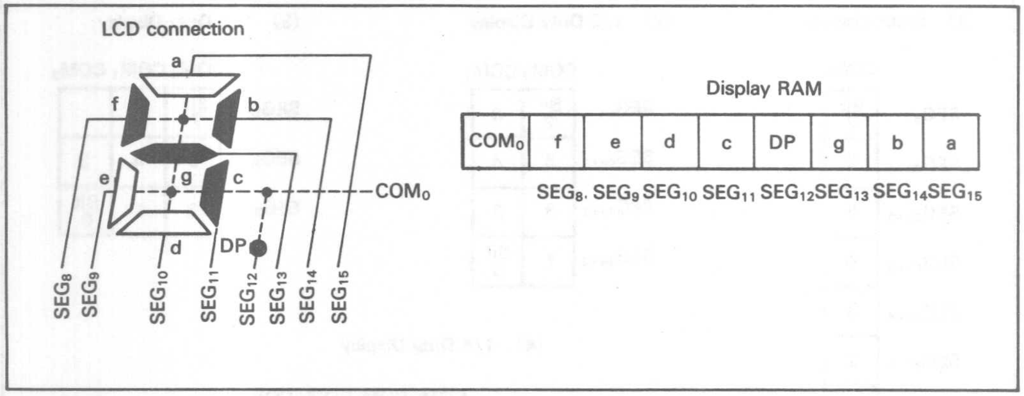


Figure 11 Example of Correspondence between LCD Connection and Display RAM (HD61605)

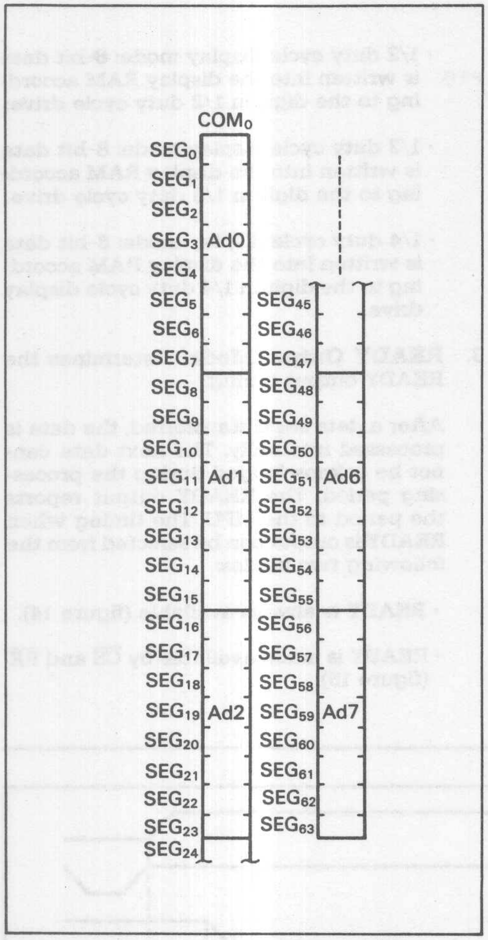


Figure 12 Allocation of Digits (HD61605)

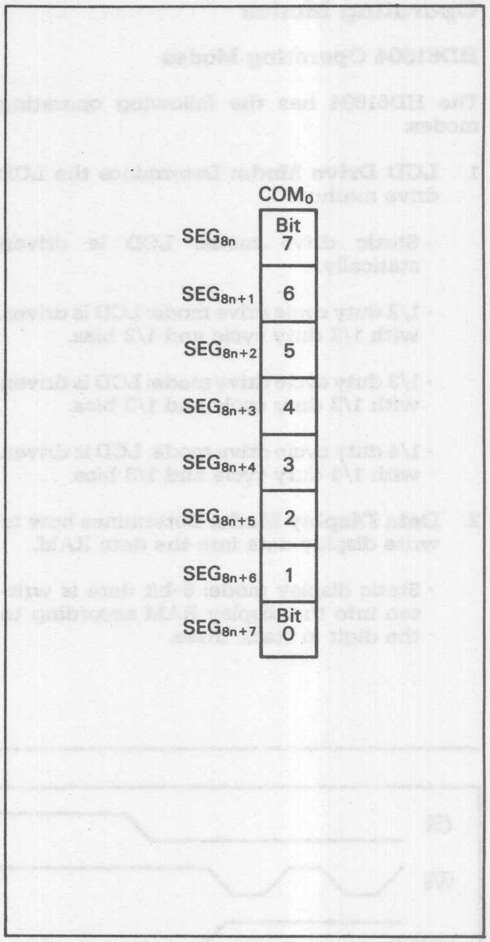


Figure 13 Bit Assignment in an Adn (HD 61605)

Operating Modes

HD61604 Operating Modes

The HD61604 has the following operating modes:

1. **LCD Drive Mode:** Determines the LCD drive method.

   · Static drive mode: LCD is driven statically.

   · 1/2 duty cycle drive mode: LCD is driven with 1/2 duty cycle and 1/2 bias.

   · 1/3 duty cycle drive mode: LCD is driven with 1/3 duty cycle and 1/3 bias.

   · 1/4 duty cycle drive mode: LCD is driven with 1/4 duty cycle and 1/3 bias.

2. **Data Display Mode:** Determines how to write display data into the data RAM.

   · Static display mode: 8-bit data is written into the display RAM according to the digit in static drive.

   · 1/2 duty cycle display mode: 8-bit data is written into the display RAM according to the digit in 1/2 duty cycle drive.

   · 1/3 duty cycle display mode: 8-bit data is written into the display RAM according to the digit in 1/3 duty cycle drive.

   · 1/4 duty cycle display mode: 8-bit data is written into the display RAM according to the digit in 1/4 duty cycle display drive.

3. **READY Output Mode:** Determines the READY output timing.

   After a data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

   · READY is always available (figure 14).

   · READY is made available by $\overline{CS}$ and $\overline{RE}$ (figure 15).

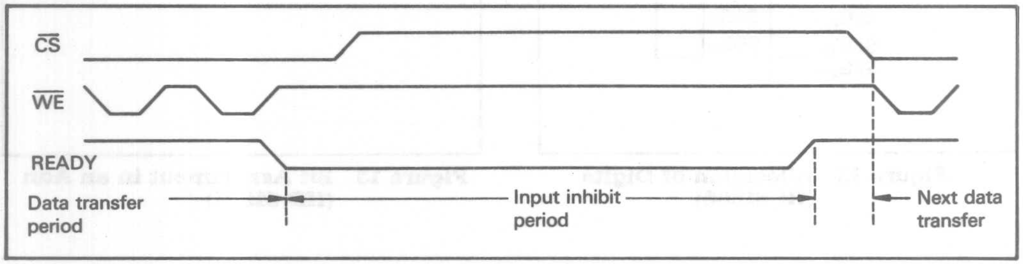


Figure 14 READY Output Timing (When It is Always Available)

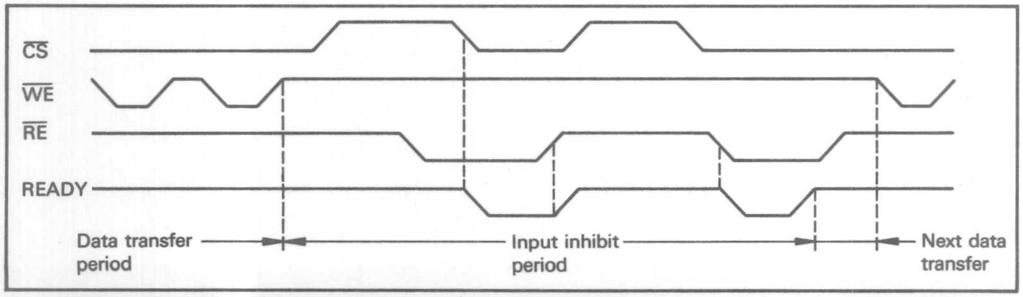


Figure 15 READY Output Timing (When It is Made Available by $\overline{CS}$ and $\overline{RE}$)

4. **LCD Off Mode:** In this mode, the HD61604 stops driving the LCD and turns it off.

The above 4 modes are specified by mode setting data. The modes are independent of each other and can be used in any combination. The bit manipulation is independent of data display mode and can be used regardless of it.

HD61605 Operating Modes

The HD61605 has the following operating modes:

1. **READY Output Mode:** Determines the READY output timing.

After a data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

- READY is always available (figure 16).
- READY is made available by $\overline{CS}$ and $\overline{RE}$ (figure 17).

2. **LCD Off Mode:** In this mode, the HD61605 stops driving the LCD and turns it off.

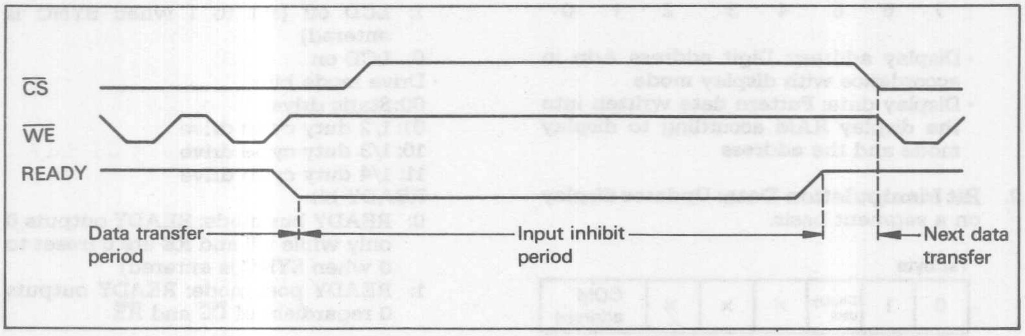


Figure 16 READY Output Timing (When It is Always Available)

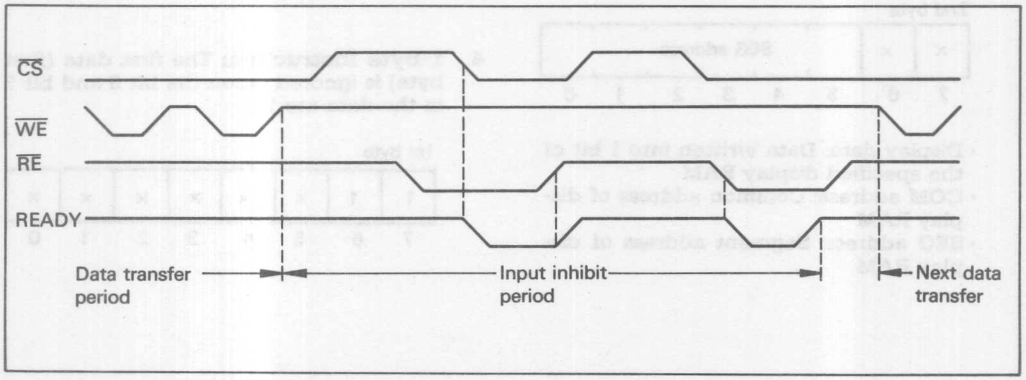


Figure 17 READY Output Timing (When It is Made Available by $\overline{CS}$ and $\overline{RE}$.)

Input Data Formats

HD61604 Input Data Formats

Input data is composed of 8 bits × 2 bytes. Input them as 2-byte data after READY output changes from low to high or low pulse enters into $\overline{RE}$ pin.

1. **Display Data:** Updates display on an 8-segment basis.

1st byte

7	6	5	4	3	2	1	0
0	0	×	Display address (Digit address Adn)				

2nd byte

7	6	5	4	3	2	1	0
Display data							

- Display address: Digit address Adn in accordance with display mode
- Display data: Pattern data written into the display RAM according to display mode and the address

2. **Bit Manipulation Data:** Updates display on a segment basis.

1st byte

7	6	5	4	3	2	1	0
0	1	Display data	×	×	×	COM address	

2nd byte

7	6	5	4	3	2	1	0
×	×	SEG address					

- Display data: Data written into 1 bit of the specified display RAM
- COM address: Common address of display RAM
- SEG address: Segment address of display RAM

3. **Mode Setting Data:**

1st byte

7	6	5	4	3	2	1	0
1	0	×	0	1	READY bit	Drive mode bits	

2nd byte

7	6	5	4	3	2	1	0
×	×	×	×	×	OFF/ON bit	Display mode bits	

- Display mode bits:
  00: Static display mode
  01: 1/2 duty cycle display mode
  10: 1/3 duty cycle display mode
  11: 1/4 duty cycle display mode
- OFF/ON bit:
  1: LCD off (set to 1 when SYNC is entered)
  0: LCD on
- Drive mode bits:
  00: Static drive
  01: 1/2 duty cycle drive
  10: 1/3 duty cycle drive
  11: 1/4 duty cycle drive
- READY bit:
  0: READY bus mode: $\overline{READY}$ outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0 (reset to 0 when SYNC is entered)
  1: READY port mode: $\overline{READY}$ outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$

Note: Input the same data to display mode bits and drive mode bits.

4. **1-Byte Instruction:** The first data (first byte) is ignored when the bit 6 and bit 7 in the data are 1.

1st byte

7	6	5	4	3	2	1	0
1	1	×	×	×	×	×	×

HD61605 Input Data Formats

Input data is composed of 4 bits × 4 bytes. Input them as four 4-bit data after READY output changes from low to high or low pulse enters into $\overline{RE}$ pin.

1. **Display Data:** Updates display on an 8-segment basis.

1st byte

3	2	1	0
0	0	×	×

2nd byte

3	2	1	0
×	Display address (Digit address Adn)		

3rd byte

3	2	1	0
Display data			
Bit7	6	5	4

4th byte

3	2	1	0
Display data			
Bit3	2	1	0

· Display address: Digit address Adn shown in figure 12.
· Display data: Pattern data written into the display RAM as shown in figure 13.

2. **Bit Manipulation Data:** Updates display on a segment basis.

1st byte

3	2	1	0
0	1	Display data	×

2nd byte

3	2	1	0
×	×	0	0

3rd byte

3	2	1	0
×	×	SEG address	
		Bit 5	4

4th byte

3	2	1	0
SEG address			
Bit 3	2	1	0

· Display data: Data written into the 1 bit of the specified display RAM.
· SEG address: Segment address of display RAM (segment output).

3. **Mode Setting Data:**

1st byte

3	2	1	0
1	0	×	0

2nd byte

3	2	1	0
×	READY bit	×	×

3rd byte

3	2	1	0
×	×	×	×

4th byte

3	2	1	0
×	OFF/ON bit	0	0

· OFF/ON bit:
1: LCD off (It is set to 1 when SYNC is entered)
0: LCD on
· READY bit:
0: READY bus mode: READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0 (reset to 0 when SYNC is entered)
1: READY port mode: READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$

4. **1-Byte Instruction:** The first data (4 bits) is ignored when the bit 3 and bit 2 in the data are 1.

1st byte

3	2	1	0
1	1	×	×

How to Input Data

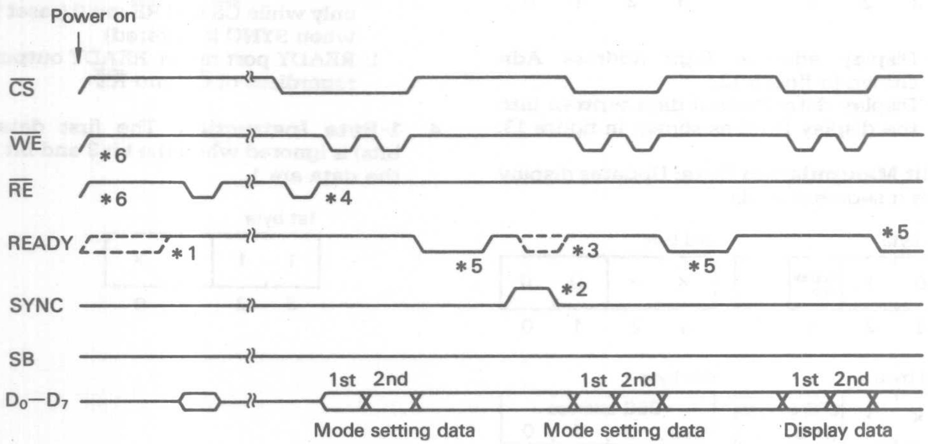
How to Input Data into HD61604

Input data is composed of 8 bits × 2 bytes. Take care that the data transfer is not interrupted because the first 8-bit data is distinguished from the second one by the sequence only.

When data transfer is interrupted, or at power on, the following two methods can be used to reset the count of the number of bytes (count of the first and second bytes):

1. Set $\overline{CS}$ and $\overline{RE}$ to low (no display data changes).
2. Input 2 or more 1-byte instruction data whose bit 7 and 6 are high (display data may change).

The data input method via data input pins ($\overline{CS}$, $\overline{WE}$, D_0 to D_7) is similar to that of static RAM such as HM6116. Access to the LSI can be made through the same bus line as ROM and RAM. When output ports of a microprocessor are used for access, refer to the timing specifications and figure 18.



∗1: READY output is indefinite during 12 clocks after the oscillation starts at power on (clock: OSC2 clock).
∗2: High pulse should be applied to SYNC pin when using two or more chips simultaneously.
∗3: In the mode in which READY is always available, READY output is indefinite while high is being applied to SYNC.
∗4: Reset the byte counter after power on.
∗5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
∗6: Connect a pull-up resistor if $\overline{WE}$ or $\overline{RE}$ is floating.
∗7: It is not always necessary to follow this example.

Figure 18 Example of Data Transfer Sequence

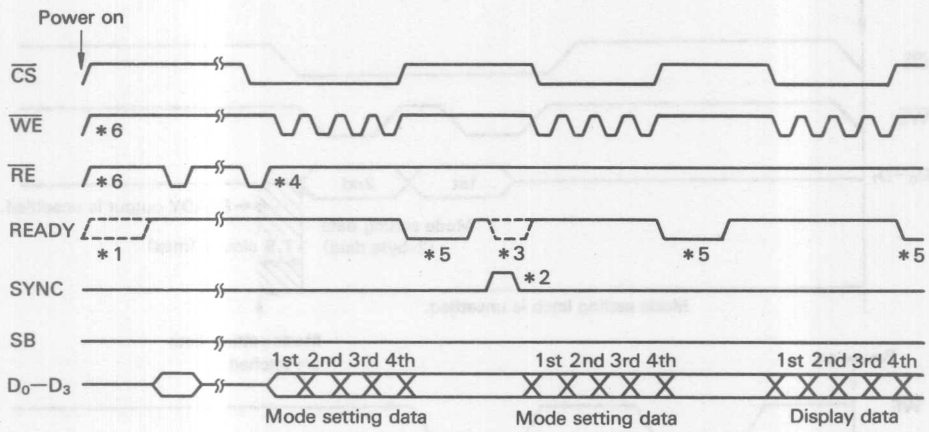
How to Input Data into HD61605

Input data is composed of 4 bits × 4 bytes. Take care that the data transfer is not interrupted because the first 4-bit data to the fourth 4-bit data are distinguished from each other by the sequence only.

When data transfer is interrupted, or at power on, the following two methods can be used to reset the count of the number of data (count of the first 4-bit data to the fourth 4-bit data):

1. Set $\overline{CS}$ and $\overline{RE}$ to low (no display data changes.)
2. Input 4 or more 1-byte instruction data (4-bit data) whose bit 3 and 2 are high (display data may change).

The data input method via data input pins ($\overline{CS}$, $\overline{WE}$ D_0 to D_3) is similar to that of static RAM such as HM6116. Access to the LSI can be made through the same bus line as ROM and RAM. When output ports of a microprocessor are used for access, refer to the timing specifications and figure 19.



*1: READY output is indefinite during 12 clocks after the oscillation starts at power on (clock: OSC2 clock).
*2: High pulse should be applied to SYNC pin when using two or more chips simultaneously.
*3: In the mode in which READY is always available, READY output is indefinite while high is being applied to SYNC.
*4: Reset the 4-bit data counter after power on.
*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
*6: Connect a pull-up resistor if $\overline{WE}$ or $\overline{RE}$ is floating.
*7: It is not always necessary to follow this example.

Figure 19 Example of Data Transfer Sequence

Notes on READY Output

Note that the READY output will be unsettled during 1.5 clocks (max) after inputting the first 2-byte data for setting the mode after turning the power on. This is because the READY bit data of mode setting latches and the mode of READY pin (READY bus or port mode) are unsettled untill the completion of mode setting.

There are two kinds of the READY output waveforms depending on the modes.

1. READY bus mode (READY bit = 0)
2. READY port mode (READY bit = 1)

However, if you input SYNC before mode setting, waveform will be determined; when you choose READY bus mode, (1) a in figure 20 will be output, and when you choose READY port mode, (2) a will be output. The figures can be applied both to HD61604 and HD61605.

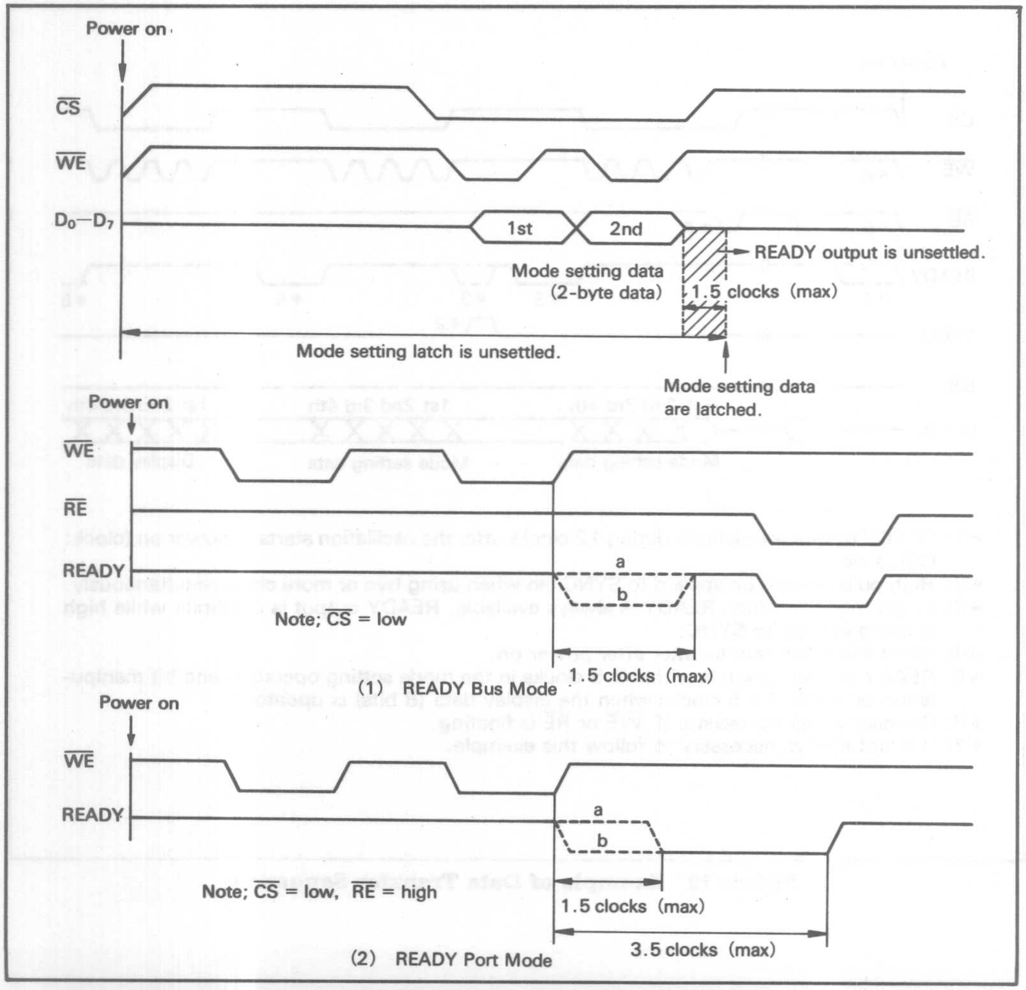


Figure 20 READY Output According to Modes

Standby Operation

Standby operation with low power consumption can be activated when pin SB is used. Normal operation of the LSI is activated when pin SB is low level, and the LSI goes into the standby state when pin SB is high level. The standby state of the LSI is as follows:

1. LCD driver is stopped (LCD is off).
2. Display data and operating mode are held.
3. The operation is suspended while display changes (while READY is outputting low.) In this case, READY outputs high within 10.5 clocks or 3.5 clocks after release from the standby mode.
4. Oscillation is stopped.

When this mode is not used, connect pin SB to V_{SS}.

Multi Chip Operation

When an LCD is driven with the two or more chips, the driving timing of LCD must be synchronized. In this case, the chips are synchronized with each other by using SYNC input. If SYNC input is high, the LCD driver timing circuit is reset. Apply high pulse to the SYNC input after the operating mode is set.

A high pulse to the SYNC input changes the mode setting data. (The OFF/ON bit is set and the READY bit is reset. See (3) Mode Setting Data in "Input Data Formats".) Transfer the mode setting data into the LSI after every SYNC operation.

If a power on reset signal is applied to the SYNC pin, the LCD can be off-state when the power is turned on.

When SYNC input is not used, connect pin SYNC to V_{SS}.

When SB input is used, after standby mode is released, high pulse must be applied to the SYNC input, and mode setting data must be set again.

Restriction on Usage

Minimize the noise by inserting a noise bypass capacitor ($\geqq$ 1 μF) between V_{DD} and V_{SS} pins. (Insert one as near chip as possible.)

Liquid Crystal Display Drive Voltage Circuit (HD61604)

What is LCD Voltage?

HD61604 drives liquid crystal display using four levels of voltages (figure 21); V_{DD}, V_1, V_2, and V_3 (V_{DD} is the highest and V_3 is the lowest). The voltage between V_{DD} and V_3 is called V_{LCD} and it is necessary to apply the appropriate V_{LCD} according to the liquid crystal display. V_3 always needs to be supplied regardless of the display duty ratio since it supplies the voltage to the LCD drive circuit of HD61604.

Connecting R2−R5 in series between V_{DD} and V_{SS} (figure 22) generates ΔV or V_{LCD} by using the resistance ratio to supply these voltage to pins V_1, V_2, V_3. C2−C4 are the smoothing capacitors. Connect a trimmer potentiometer for R5 and change its resistance value to control the contrast.

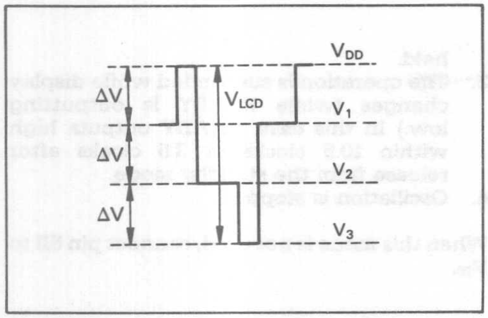
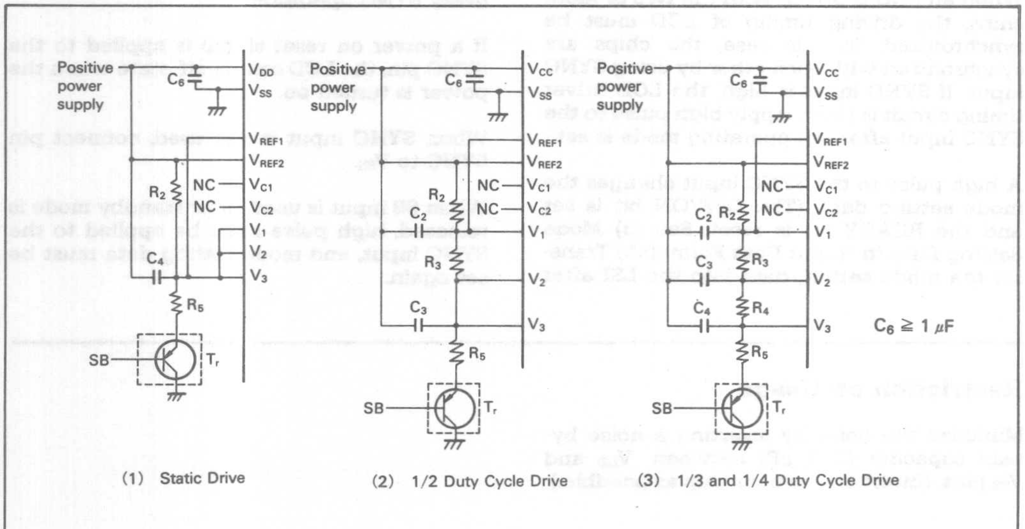


Figure 21 LCD Output Waveform and Output Levels (1/3 Duty Cycle, 1/3 Bias)



Note: 1 When standby mode is used, a transistor is required.
2 R2 − R5 should be some kΩ − some tens of kΩ, and C2 − C4 should be 0.1 μF − 0.3 μF.

Figure 22 Example when External Drive Voltage is Used

Liquid Crystal Display Drive Voltage (HD61605)

As shown in figure 23, apply LCD drive voltage from the external power supply.

Oscillation Circuit

When Internal Oscillation Circuit is Used

When the internal oscillation circuit is used, attach an external resistor R_{OSC} as shown in figure 24. (Insert R_{OSC} as near chip as possible, and make the OSC1 side shorter.)

When External Clock is Used

When an external clock of 100 kHz with CMOS level is provided, pin OSC1 can be used for the input pin. In this case, open pin OSC2.

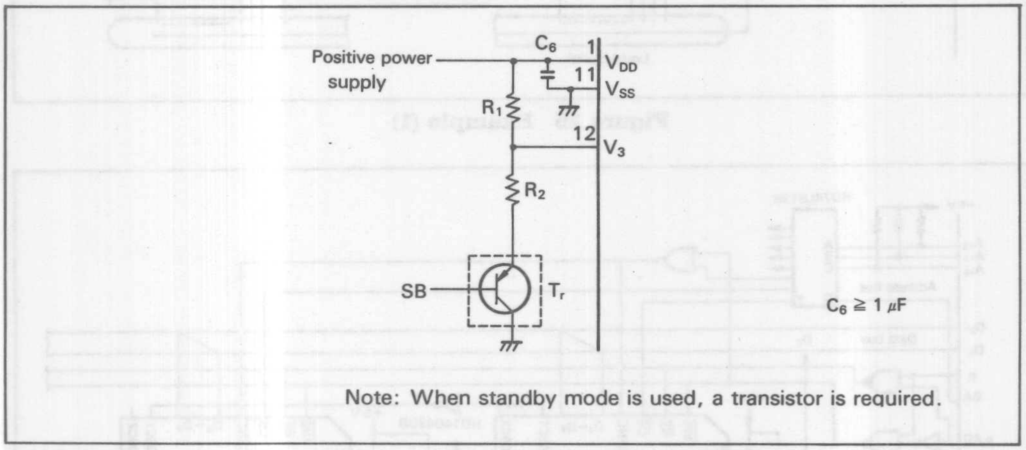


Figure 23 Example of Drive Voltage Generator

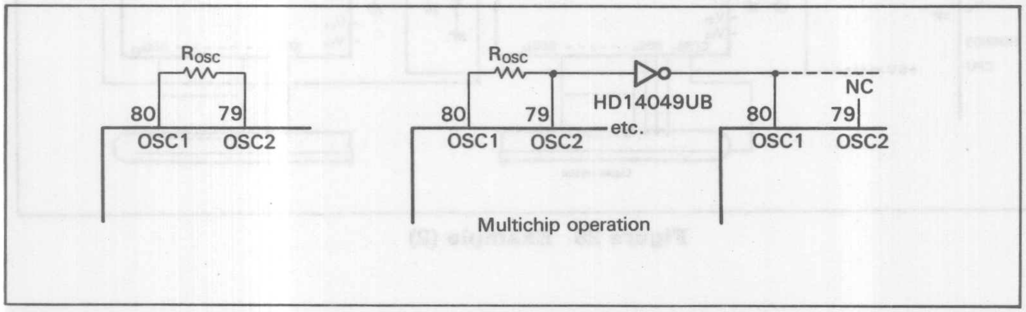


Figure 24 Example of Oscillation Circuit

Applications

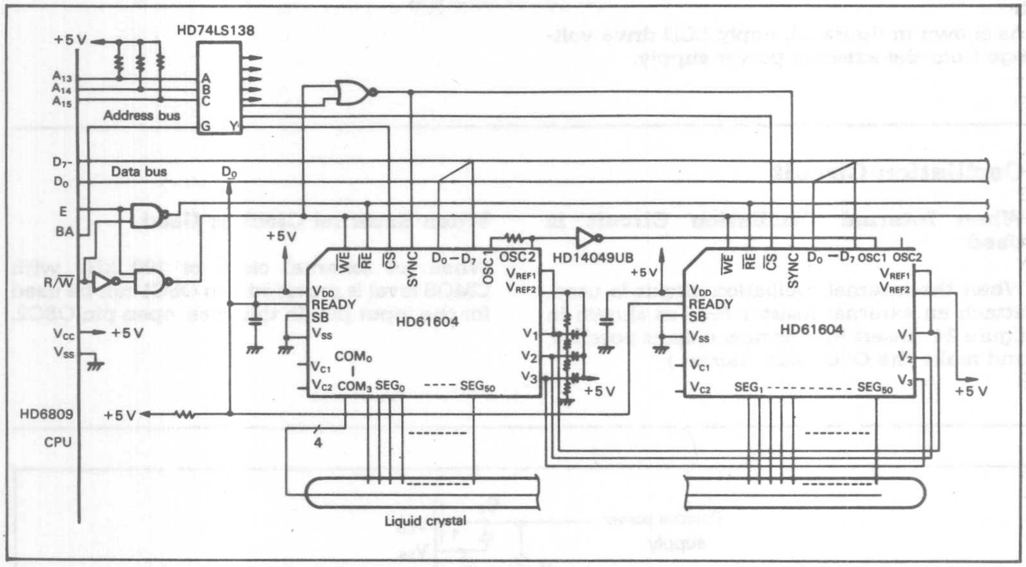


Figure 25 Example (1)

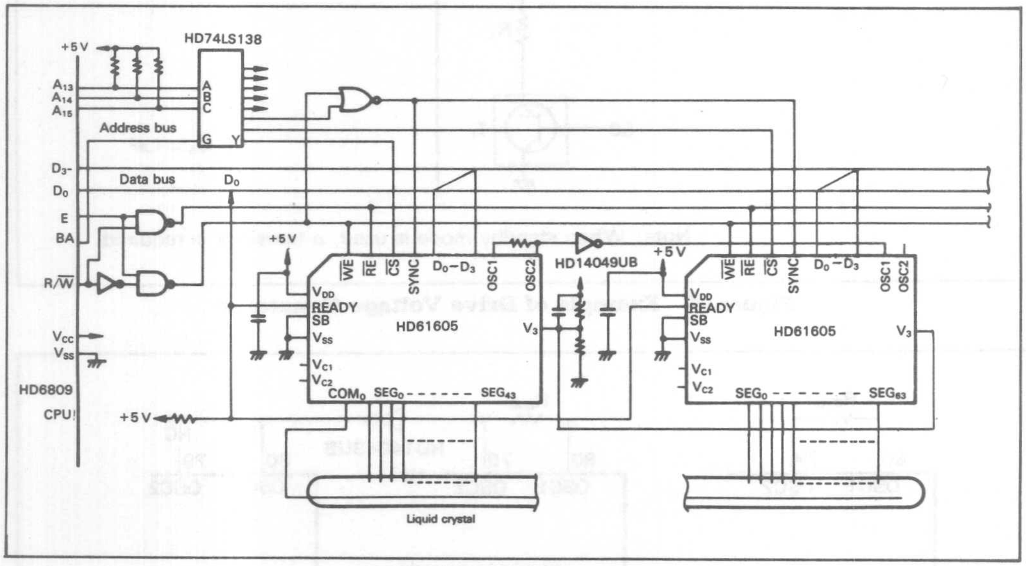


Figure 26 Example (2)

Absolute Maximum Ratings

Item	Symbol	Limit	Unit
Power supply voltage *	V_{DD}, V_1, V_2, V_3	−0.3 to + 7.0	V
Pin voltage *	V_T	−0.3 to V_{DD} + 0.3	V
Operating temperature	Topr	−20 to +75	°C
Storage temperature	Tstg	−55 to +125	°C

* Value referenced to V_{SS} = 0 V.

Note: If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Recommended Operating Conditions

Item	Symbol	Limit Min	Limit Typ	Limit Max	Unit
Power supply voltage *	V_{DD}	4.5	−	5.5	V
	V_1, V_2, V_3	0	−	V_{DD}	V
Pin voltage *	V_T	0	−	V_{DD}	V
Operating temperature	Topr	−20	−	+75	°C

* Value referenced to V_{SS} = 0 V.

Electrical Characteristics

DC Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 V to 5.5 V, Ta= −20 °C to +75 °C, unless otherwise noted)

Item		Symbol	Limit Min	Typ	Max	Unit	Test Condition
Input high voltage	OSC1	V_{IH1}	$0.8V_{DD}$	–	V_{DD}	V	
	Others	V_{IH2}	2.0	–	V_{DD}	V	
Input low voltage	OSC1	V_{IL1}	0	–	$0.2V_{DD}$	V	
	Others	V_{IL2}	0	–	0.8	V	
Output leakage current	READY	I_{OH}			5	μA	Pull up the pin to V_{DD}
Output low voltage	READY	V_{OL}	–	–	0.4	V	I_{OL}=0.4 mA
Input leakage current *1	Input pin	I_{IL1}	−1.0		1.0	μA	V_{IN}=0 to V_{DD}
	V_1	I_{IL2}	−20	–	20	μA	V_{IN}=V_{DD} to V_3
	V_2, V_3	I_{IL3}	−5.0	–	5.0	μA	
LCD driver voltage drop	COM_0−COM_3	V_{d1}	–	–	0.3	V	±Id=3 μA for each COM, V_3=V_{DD} to 3 V
	SEG_0−SEG_{50}	V_{d2}	–	–	0.6	V	±Id=3 μA for each SEG, V_3=V_{DD} to 3 V
Current consumption *2		I_{DD}	–	–	100	μA	During display * R_{OSC}=360 kΩ
		I_{DD}	–	–	5	μA	At standby

* Except the transfer operation of display data and bit data.
*1 V_1, V_2: applied only to HD61604.
*2 Do not connect any wire to the output pins and connect the input pins to V_{DD} or V_{SS}.

AC Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 V to 5.5 V, Ta = −20 °C to +75 °C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
			Limit				
Oscillation frequency	OSC2	f_{OSC}	70	100	130	kHz	R_{OSC}=360 kΩ
External clock frequency	OSC1	f_{OSC}	70	100	130	kHz	
External clock duty	OSC1	Duty	40	50	60	%	
I/O signal timing		t_S	400	–	–	ns	
		t_H	10	–	–	ns	
		t_{WH}	300	–	–	ns	
		t_{WL}	400	–	–	ns	
		t_{WR}	400	–	–	ns	
		t_{DL}	–	–	1.0	μs	Figure 31
		t_{EN}	400	–	–	ns	
		t_{OP1}	9.5	–	10.5	Clock	For display data transfer
		t_{OP2}	2.5	–	3.5	Clock	For bit and mode data transfer
Input signal rise time and fall time		t_r, t_f	–	–	25	ns	

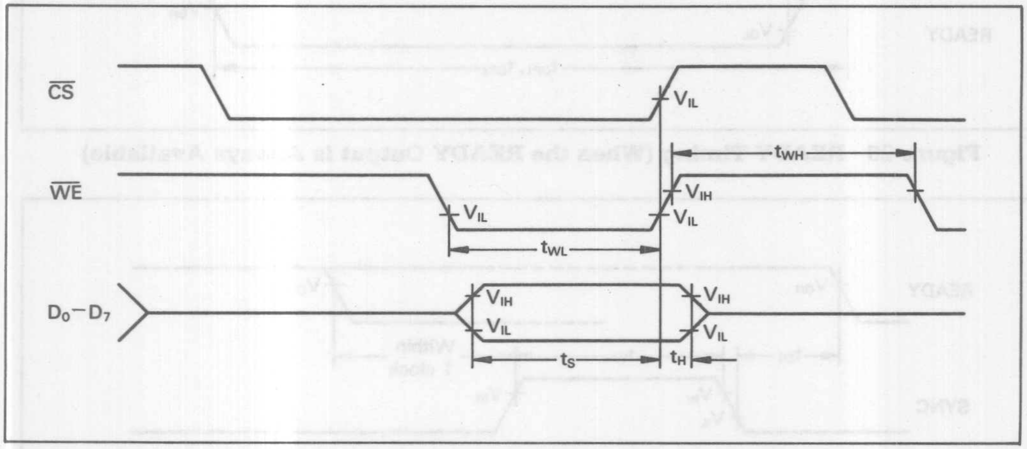


Figure 27 Write Timing ($\overline{RE}$ is fixed high and SYNC low)

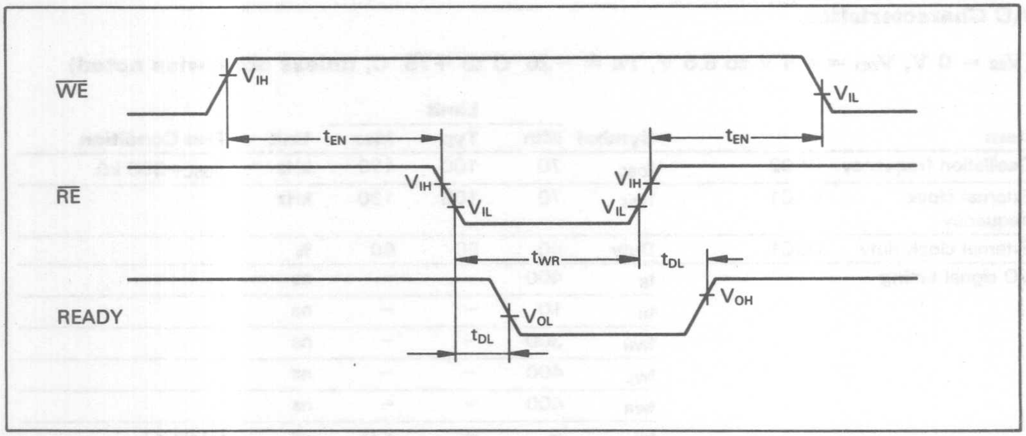


Figure 28 Reset/Read Timing ($\overline{CS}$ and SYNC are fixed low)

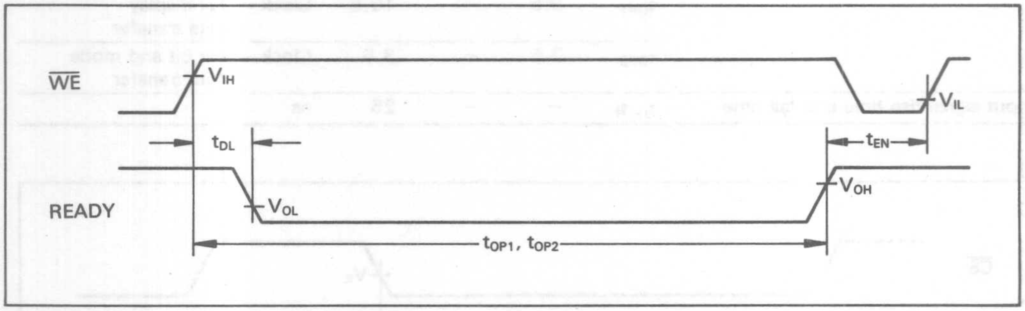


Figure 29 READY Timing (When the READY Output is Always Available)

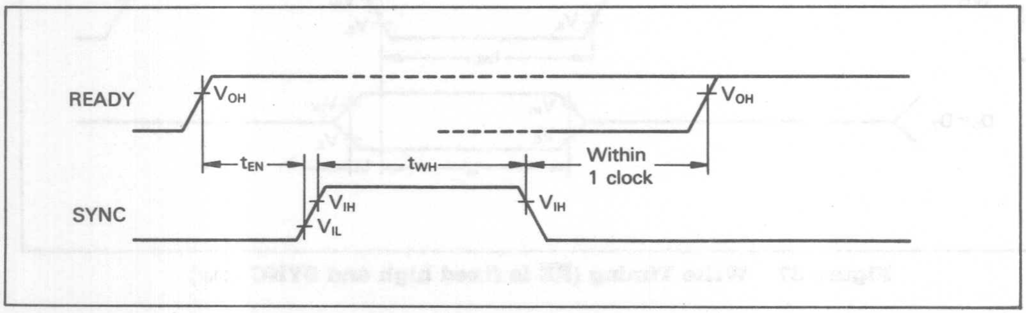


Figure 30 SYNC Timing

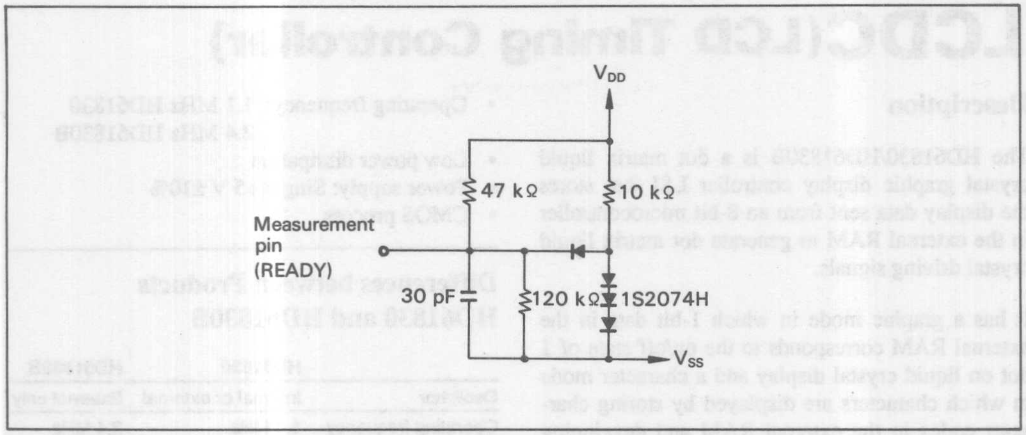


Figure 31 Bus Timing Load Circuit (LS-TTL Load)

HD61830/HD61830B
LCDC(LCD Timing Controller)

Description

The HD61830/HD61830B is a dot matrix liquid crystal graphic display controller LSI that stores the display data sent from an 8-bit microcontroller in the external RAM to generate dot matrix liquid crystal driving signals.

It has a graphic mode in which 1-bit data in the external RAM corresponds to the on/off state of 1 dot on liquid crystal display and a character mode in which characters are displayed by storing character codes in the external RAM and developing them into the dot patterns with the internal character generator ROM. Both modes can be provided for various applications.

The HD61830/HD61830B is produced by the CMOS process. Thus, combined with a CMOS microcontroller it can complete a liquid crystal display device with lower power dissipation.

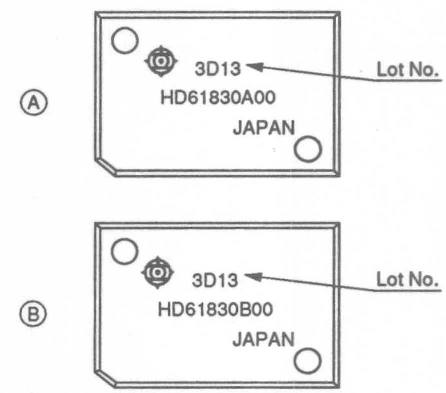
Features

- Dot matrix liquid crystal graphic display controller
- Display control capacity
  - —Graphic mode: 512k dots (2^{16} bytes)
  - —Character mode: 4096 characters (2^{12} characters)
- Internal character generator ROM: 7360 bits
  - —160 types of 5 × 7 dot characters
  - —32 types of 5 × 11 dot characters
    Total 192 characters
  - —Can be extended to 256 characters (4 kbytes max.) by external ROM
- Interfaces to 8-bit MPU
- Display duty cycle (can be selected by a program) Static to 1/128 duty cycle
- Various instruction functions
  - —Scroll, cursor on/off/blink, character blink, bit manipulation
- Display method: Selectable A or B types
- Internal oscillator (with external resistor and capacitor) HD61830
- Operating frequency: 1.1 MHz HD61830
  2.4 MHz HD61830B
- Low power dissipation
- Power supply: Single +5 V ±10%
- CMOS process

Differences between Products HD61830 and HD61830B

	HD61830	HD61830B
Oscillator	Internal or external	External only
Operating frequency	1.1 MHz	2.4 MHz
Pin arrangement and signal name	Pin 6: C Pin 7: R Pin 9: CPO	Pin 6: $\overline{CE}$ Pin 7: $\overline{OE}$ Pin 9: NC
Package marking to see figure	Ⓐ	Ⓑ

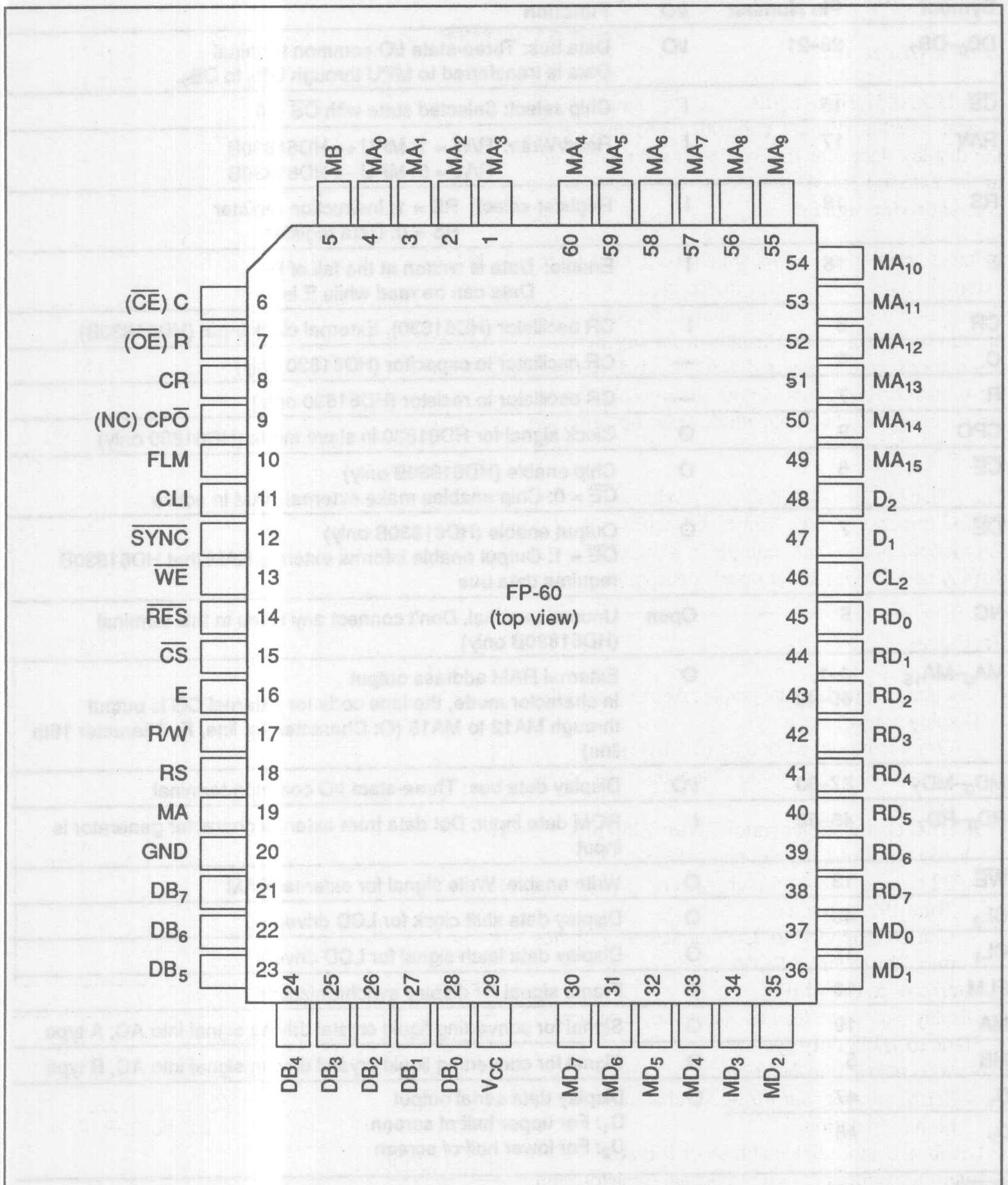
Package Marking



Ordering Information

Type No.	Package
HD61830A00H	60-pin plastic QFP (FP-60)
HD61830B00H	

Pin Arrangement

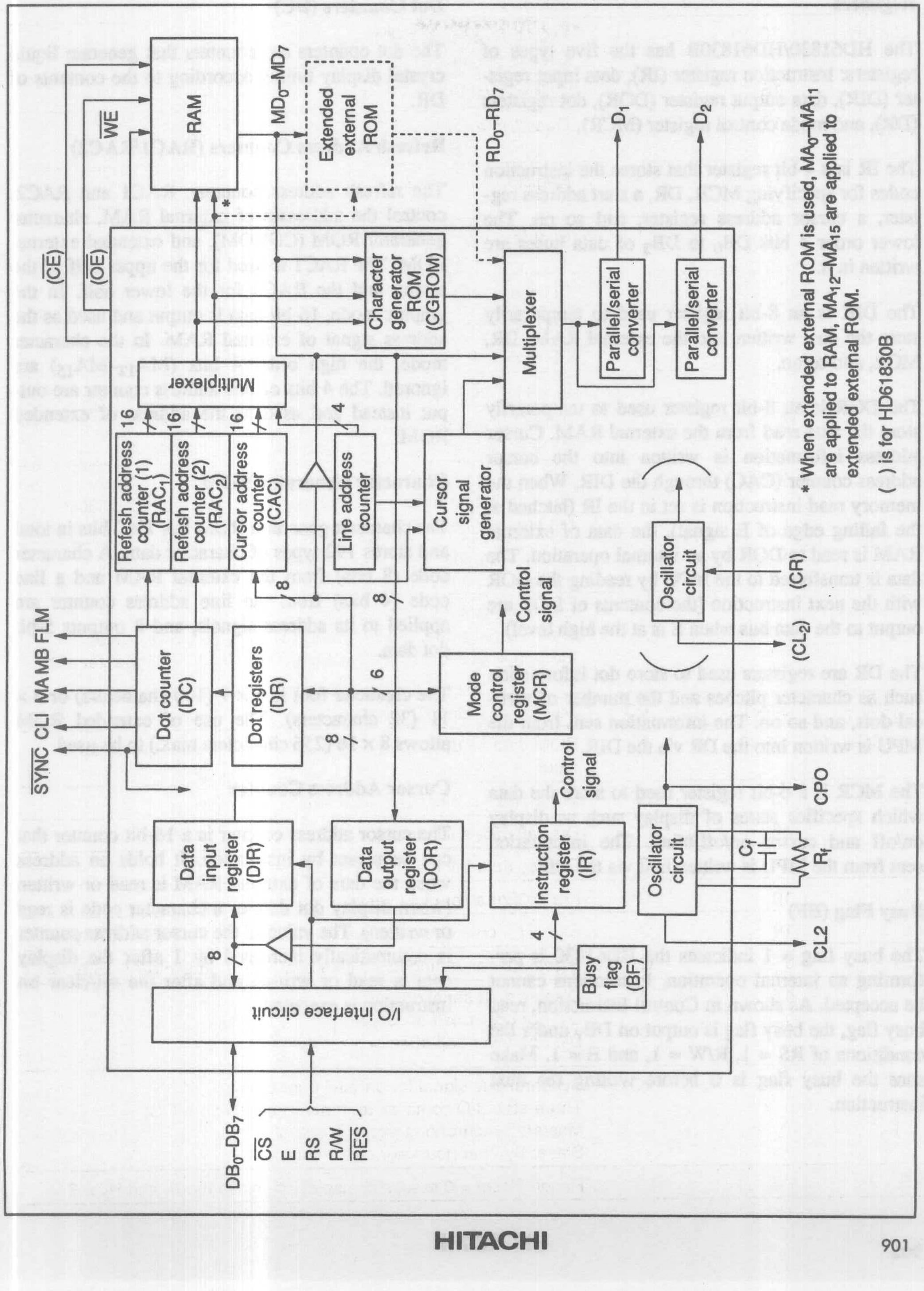


( ) is for HD61830B

Terminal Functions

Symbol	Pin Number	I/O	Function
DB_0–DB_7	28–21	I/O	Data bus: Three-state I/O common terminal Data is transferred to MPU through DB_0 to DB_7.
$\overline{CS}$	15	I	Chip select: Selected state with $\overline{CS}$ = 0
R/W	17	I	Read/Write: R/W = 1: MPU ← HD61830B R/W = 0: MPU → HD61830B
RS	18	I	Register select: RS = 1: Instruction register RS = 0: Data register
E	16	I	Enable: Data is written at the fall of E Data can be read while E is 1
CR	8	I	CR oscillator (HD61830), External clock input (HD61830B)
C	6	—	CR oscillator to capacitor (HD61830 only)
R	7	—	CR oscillator to resistor (HD61830 only)
CPO	9	O	Clock signal for HD61830 in slave mode (HD61830 only)
$\overline{CE}$	6	O	Chip enable (HD61830B only) $\overline{CE}$ = 0: Chip enables make external RAM in active
$\overline{OE}$	7	O	Output enable (HD61830B only) $\overline{OE}$ = 1: Output enable informs external RAM that HD61830B requires data bus
NC	9	Open	Unused terminal. Don't connect any wires to this terminal (HD61830B only)
MA_0–MA_{15}	4–1, 60–49	O	External RAM address output In character mode, the lane code for external CG is output through MA12 to MA15 (O: Character 1st line, F: Character 16th line)
MD_0–MD_7	37–30	I/O	Display data bus: Three-state I/O common terminal
RD_0–RD_7	45–38	I	ROM data input: Dot data from external character generator is input
$\overline{WE}$	13	O	Write enable: Write signal for external RAM
CL_2	46	O	Display data shift clock for LCD drivers
CL_1	11	O	Display data latch signal for LCD drivers
FLM	10	O	Frame signal for display synchronization
MA	19	O	Signal for converting liquid crystal driving signal into AC, A type
MB	5	O	Signal for converting liquid crystal driving signal into AC, B type
D_1	47	O	Display data serial output D_1: For upper half of screen D_2: For lower half of screen
D_2	48		
$\overline{SYNC}$	12	I/O	Synchronous signal for parallel operation Three-state I/O common terminal (with pull-up MOS) Master: Synchronous signal is output Slave: Synchronous signal is input
$\overline{RES}$	14	I	Reset: Reset = 0 results in display off, slave mode and H_p = 6

Block Diagram



Block Functions

Registers

The HD61830/HD61830B has the five types of registers: instruction register (IR), data input register (DIR), data output register (DOR), dot registers (DR), and mode control register (MCR).

The IR is a 4-bit register that stores the instruction codes for specifying MCR, DR, a start address register, a cursor address register, and so on. The lower order 4 bits DB_0 to DB_3 of data buses are written in it.

The DIR is an 8-bit register used to temporarily store the data written into the external RAM, DR, MCR, and so on.

The DOR is an 8-bit register used to temporarily store the data read from the external RAM. Cursor address information is written into the cursor address counter (CAC) through the DIR. When the memory read instruction is set in the IR (latched at the falling edge of E signal), the data of external RAM is read to DOR by an internal operation. The data is transferred to the MPU by reading the DOR with the next instruction (the contents of DOR are output to the data bus when E is at the high level).

The DR are registers used to store dot information such as character pitches and the number of vertical dots, and so on. The information sent from the MPU is written into the DR via the DIR.

The MCR is a 6-bit register used to store the data which specifies states of display such as display on/off and cursor on/off/blink. The information sent from the MPU is written in it via the DIR.

Busy Flag (BF)

The busy flag = 1 indicates the HD61830 is performing an internal operation. Instructions cannot be accepted. As shown in Control Instruction, read busy flag, the busy flag is output on DB_7 under the conditions of RS = 1, R/W = 1, and E = 1. Make sure the busy flag is 0 before writing the next instruction.

Dot Counters (DC)

The dot counters are counters that generate liquid crystal display timing according to the contents of DR.

Refresh Address Counters (RAC1/RAC2)

The refresh address counters, RAC1 and RAC2, control the addresses of external RAM, character generator ROM (CGROM), and extended external ROM. The RAC1 is used for the upper half of the screen and the RAC2 for the lower half. In the graphic mode, 16-bit data is output and used as the address signal of external RAM. In the character mode, the high order 4 bits (MA_{12}–MA_{15}) are ignored. The 4 bits of line address counter are output instead and used as the address of extended ROM.

Character Generator ROM

The character generator ROM has 7360 bits in total and stores 192 types of character data. A character code (8 bits) from the external RAM and a line code (4 bits) from the line address counter are applied to its address signals, and it outputs 5-bit dot data.

The character font is 5×7 (160 characters) or 5×11 (32 characters). The use of extended ROM allows 8×16 (256 characters max.) to be used.

Cursor Address Counter

The cursor address counter is a 16-bit counter that can be preset by instruction. It holds an address when the data of external RAM is read or written (when display dot data or a character code is read or written). The value of the cursor address counter is automatically increased by 1 after the display data is read or written and after the set/clear bit instruction is executed.

Cursor Signal Generator

The cursor can be displayed by instruction in character mode. The cursor is automatically generated on the display specified by the cursor address and cursor position.

Parallel/Serial Conversion

The parallel data sent from the external RAM, character generator ROM, or extended ROM is converted into serial data by two parallel/serial conversion circuits and transferred to the liquid crystal driver circuits for upper screen and lower screen simultaneously.

Display Control Instructions

Display is controlled by writing data into the instruction register and 13 data registers. The RS signal distinguishes the instruction register from the data registers. 8-bit data is written into the instruction register with RS = 1, and the data register code is specified. After that, the 8-bit data is written in the data register and the specified instruction is executed with RS = 0.

During the execution of the instruction, no new instruction can be accepted. Since the busy flag is set during this, read the busy flag and make sure it is 0 before writing the next instruction.

1. **Mode Control:** Code $"00" (hexadecimal) written into the instruction register specifies the mode control register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	0
Mode control reg.	0	0	0	0	Mode data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor/blink	CG	Graphic/character display
I/O	I/O	0	0	0	0	Cursor off	Internal CG	Character display (Character mode)
		0	1			Cursor on		
		1	0			Cursor off, character blink		
		1	1			Cursor blink		
		0	0		1	Cursor off	External CG	
		0	1			Cursor on		
		1	0			Cursor off, character blink		
		1	1			Cursor blink		
		0	0	1	0			Graphic mode
Display ON/OFF	Master/slave	Blink	Cursor	Graphic/character mode	Ext./Int. CG			

DB4 (Master/slave):
1: Master mode
0: Slave mode

DB5 (Display ON/OFF):
1: Display ON
0: Display OFF

2. Set Character Pitch: Vp indicates the number of vertical dots per character. The space between the vertically-displayed characters is included in the determination. This value is meaningful only during character display (in the character mode) and becomes invalid in the graphic mode.

H_p indicates the number of horizontal dots per character in display, including the space between horizontally-displayed characters. In the graphic mode, the H_p indicates the number of bits of 1-byte display data to be displayed.

There are three H_p values (table 1).

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	1
Character pitch reg.	0	0	(V_p – 1) binary				0	(H_p – 1) binary		

Table 1 H_p Values

Hp	DB2	DB1	DB0	Horizontal Character Pitch
6	1	0	1	6
7	1	1	0	7
8	1	1	1	8

3. Set Number of Characters: H_N indicates the number of horizontal characters in the character mode or the number of horizontal bytes in the graphic mode. If the total sum of horizontal dots on the screen is taken as n,

$$n = H_p \times H_N$$

H_N can be set to an even number from 2 to 128 (decimal).

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	0
Number-of-characters reg.	0	0	0	$(H_N - 1)$ binary						

4. Set Number of Time Divisions (Inverse of Display Duty Ratio): N_X indicates the number of time divisions in multiplex display.

$1/N_X$ is the display duty ratio.

A value of 1 to 128 (decimal) can be set to N_X.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	1
Number-of-time-divisions reg.	0	0	0	$(N_X - 1)$ binary						

5. Set Cursor Position: C_p indicates the position in a character where the cursor is displayed in the character mode. For example, in 5 × 7 dot font, the cursor is displayed under a character by specifying C_p = 8 (decimal). The cursor horizontal length is equal to the horizontal character pitch H_p. A value of 1 to 16 (decimal) can be set to C_p. If a smaller value than the vertical character pitch V_p is set ($C_p \le V_p$), and a character overlaps with the cursor, the cursor has higher priority of display (at cursor display on). If C_p is greater than V_p, no cursor is displayed. The cursor horizontal length is equal to H_p.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	1	0	0
Cursor position reg.	0	0	0	0	0	0	$(C_p - 1)$ binary			

6. Set Display Start Low Order Address: Cause display start addresses to be written in the display start address registers. The display start address indicates a RAM address at which the data displayed at the top left end on the screen is stored. In the graphic mode, the start address is composed of high/low order 16 bits. In the character display, it is composed of the lower 4 bits of high order address (DB_3–DB_0) and 8 bits of low order address. The upper 4 bits of high order address are ignored.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	0
Display start address reg. (low order byte)	0	0	(Start low order address) binary							

Set Display Start High Order Address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	1
Display start address reg. (high order byte)	0	0	(Start high order address) binary							

7. Set Cursor Address (Low Order) (RAM Write Low Order Address): Cause cursor addresses to be written in the cursor address counters. The cursor address indicates an address for sending or receiving display data and character codes to or from the RAM.

That is, data at the address specified by the cursor address are read/written. In the character mode, the cursor is displayed at the character specified by the cursor address.

A cursor address consists of the low-order address (8 bits) and the high-order address (8 bits). Satisfy the following requirements setting the cursor address (table 2).

The cursor address counter is a 16-bit up-counter with set and reset functions. When bit N changes from 1 to 0, bit N + 1 is incremented by 1. When setting the low order address, the LSB (bit 1) of the high order address is incremented by 1 if the MSB (bit 8) of the low order address changes from 1 to 0. Therefore, set both the low order address and the high order address as shown in the table 2.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	0
Cursor address counter (low order byte)	0	0	(Cursor low order address) binary							

Set Cursor Address (High Order) (RAM Write High Order Address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	1
Cursor address counter (high order byte)	0	0	(Cursor high order address) binary							

Table 2 Cursor Address Setting

Condition	Requirement
When you want to rewrite (set) both the low order address and the high order address.	Set the low order address and then set the high order address.
When you want to rewrite only the low order address.	Don't fail to set the high order address again after setting the low order address.
When you want to rewrite only the high order address.	Set the high order address. You don't have to set the low order address again.

8. Write Display Data: After the code $“OC” is written into the instruction register with RS = 1, 8-bit data with RS = 0 should be written into the data register. This data is transferred to the RAM specified by the cursor address as display data or character code. The cursor address is increased by 1 after this operation.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (pattern data, character code) LSB							

9. Read Display Data: Data can be read from the RAM with RS = 0 after writing code $“OD” into the instruction register. Figure 1 shows the read procedure.

This instruction outputs the contents of data output register on the data bus (DB_0 to DB_7) and then transfers RAM data specified by the cursor address to the data output register, also increasing the cursor address by 1. After setting the cursor address, correct data is not output at the first read but at the second one. Thus, make one dummy read when reading data after setting the cursor address.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MSB (pattern data, character code) LSB							

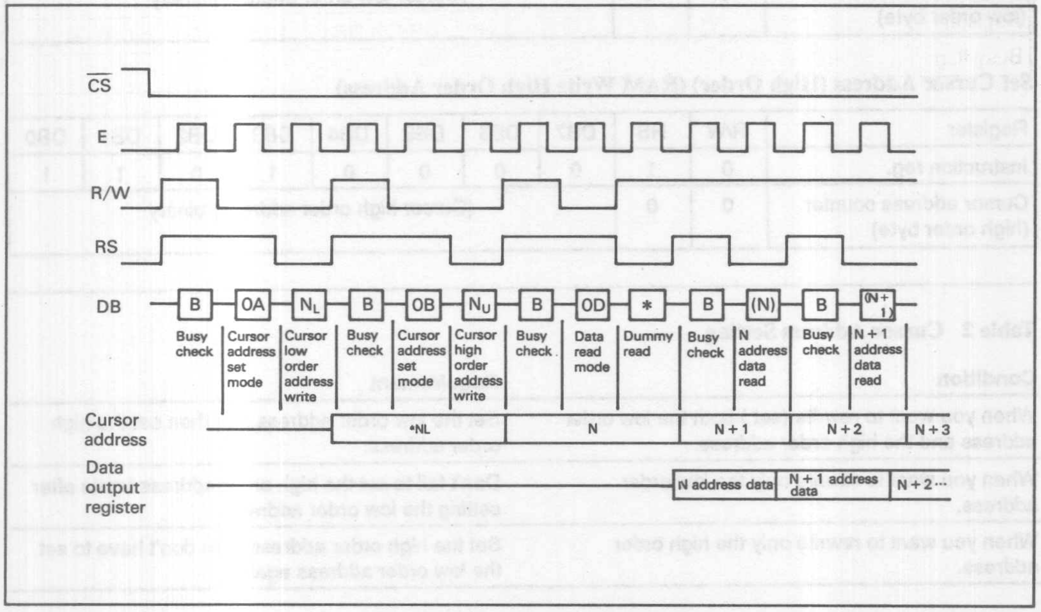


Figure 1 Read Procedure

10. Clear Bit: The clear/set bit instruction sets 1 bit in a byte of display data RAM to 0 or 1, respectively. The position of the bit in a byte is specified by N_B and RAM address is specified by cursor address. After the execution of the instruction, the cursor address is automatically increased by 1. N_B is a value from 1 to 8. $N_B = 1$ and $N_B = 8$ indicates LSB and MSB, respectively.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	0
Bit clear reg.	0	0	0	0	0	0	0	(N_B – 1) binary		

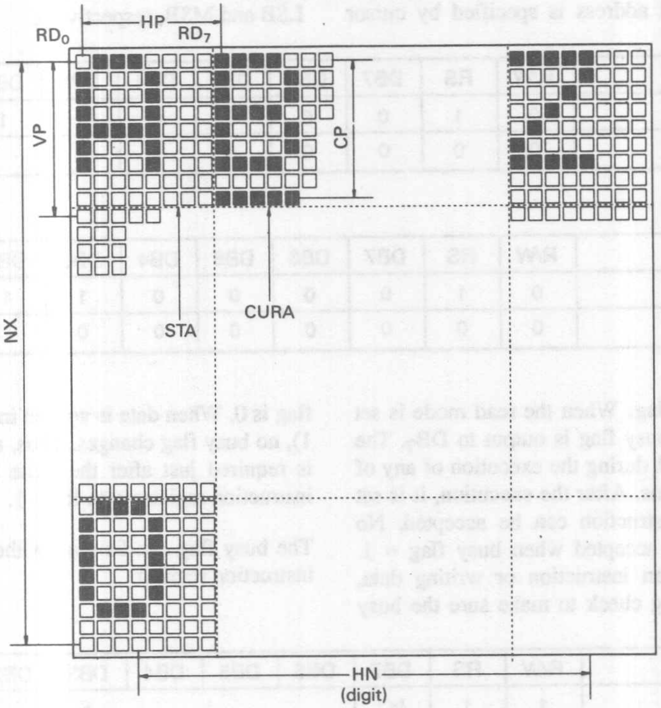
Set Bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	1
Bit set reg.	0	0	0	0	0	0	0	(N_B – 1) binary		

11. Read Busy Flag: When the read mode is set with RS = 1, the busy flag is output to DB_7. The busy flag is set to 1 during the execution of any of the other instructions. After the execution, it is set to 0. The next instruction can be accepted. No instruction can be accepted when busy flag = 1. Before executing an instruction or writing data, perform a busy flag check to make sure the busy flag is 0. When data is written in the register (RS = 1), no busy flag changes. Thus, no busy flag check is required just after the write operation into the instruction register with RS = 1.

The busy flag can be read without specifying any instruction register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Busy flag	1	1	I/O	*						



Symbol	Name	Meaning	Value
H_p	Horizontal character pitch	Horizontal character pitch	6 to 8 dots
H_N	Number of horizontal characters	Number of horizontal characters per line (number of digits) in the character mode or number of bytes per line in the graphic mode	2 to 128 digits (an even number)
V_p	Vertical character pitch	Vertical character pitch	1 to 16 dots
C_p	Cursor position	Line number on which the cursor can be displayed	1 to 16 lines
Nx	Number of time divisions	Inverse of display duty ratio	1 to 128 lines

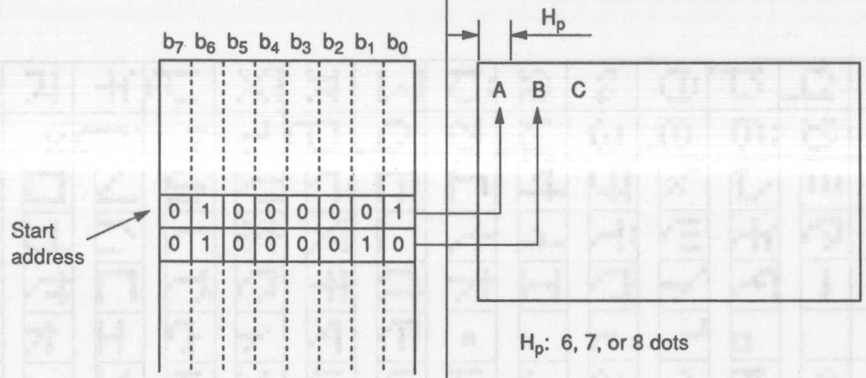
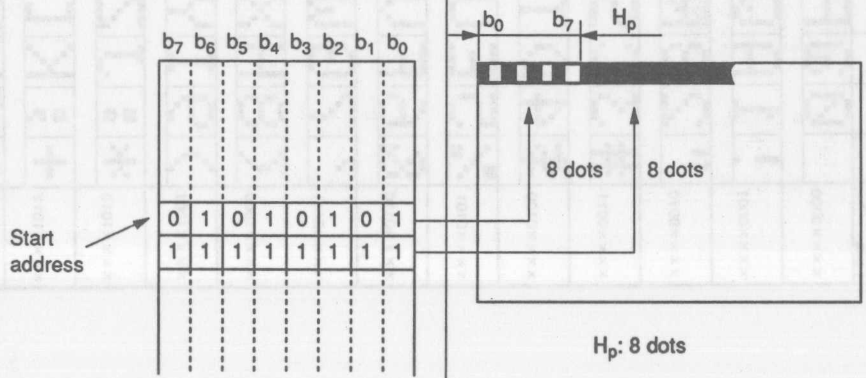
Note: If the number of vertical dots on the screen is m, and the number of horizontal dots is n,

$1/m = 1/N_X$ = display duty ratio

$n = H_p \times H_N$, m/V_p = Number of display lines

$C_p \leq V_p$

Figure 2 Display Variables

Display Mode	Display Data from MPU	RAM	Liquid Crystal Display Panel
Character display	Character code (8 bits)		Hp: 6, 7, or 8 dots
Graphic	Display pattern (8 bits)		Hp: 8 dots

Internal Character Generator Patterns and Character Codes

Lower 4 bits \ Higher 4 bits	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
××××0000		0	@	P	`	p		ー	タ	ミ	α	p
××××0001	!	1	A	Q	a	q	。	ア	チ	ム	ä	q
××××0010	"	2	B	R	b	r	「	イ	ツ	メ	β	θ
××××0011	#	3	C	S	c	s	」	ウ	テ	モ	ε	∞
××××0100	$	4	D	T	d	t	、	エ	ト	ヤ	μ	Ω
××××0101	%	5	E	U	e	u	・	オ	ナ	ユ	σ	ü
××××0110	&	6	F	V	f	v	ヲ	カ	ニ	ヨ	ρ	Σ
××××0111	'	7	G	W	g	w	ァ	キ	ヌ	ラ	g	π
××××1000	(	8	H	X	h	x	ィ	ク	ネ	リ	√	x̄
××××1001	)	9	I	Y	i	y	ゥ	ケ	ノ	ル	⁻¹	y
××××1010	*	:	J	Z	j	z	ェ	コ	ハ	レ	j	千
××××1011	+	;	K	[	k	{	ォ	サ	ヒ	ロ	ˣ	万
××××1100	,	<	L	¥	l	|	ャ	シ	フ	ワ	¢	円
××××1101	-	=	M	]	m	}	ュ	ス	ヘ	ン	Ł	÷
××××1110	.	>	N	^	n	→	ョ	セ	ホ	゛	ñ	
××××1111	/	?	O	_	o	←	ッ	ソ	マ	゜	ö	█

Example of Correspondence between External CG ROM Address Data and Character Pattern

8 × 8 Dot Font

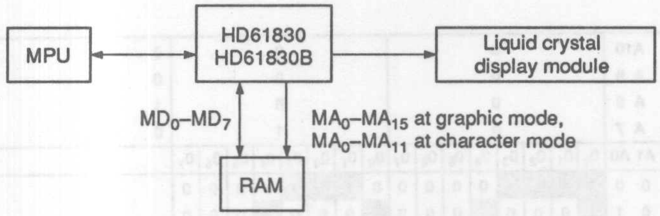
		A10	0								0								1
		A 9	0								0								1
		A 8	0								0								1
		A 7	0								1								1
A6 A5 A4 A3	A2 A1 A0		O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	
0 0 0 0	0 0 0		1	1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	
	0 0 1		1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	
	0 1 0		1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	
	0 1 1		1	1	1	1	0	0	0	0	1	0	0	0	1	0	0	0	
	1 0 0		1	0	1	0	0	0	0	0	1	0	1	0	1	0	0	0	
	1 0 1		1	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	
	1 1 0		1	0	0	0	1	0	0	0	0	1	1	0	1	0	0	0	
	1 1 1		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0 0 0 0	0 0 0		1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	
	0 0 1		1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	
	0 1 0		1	1	1	0	0	1	0	0	0	1	0	0	0	0	0	1	
	0 1 1		0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	
	1 0 0		0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	
	1 0 1		0	0	1	0	0	1	1	1	0	0	0	0	1	0	0	0	
	1 1 0		0	1	0	0	0	1	0	1	0	0	0	1	0	0	0	0	
	1 1 1		1	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	
0 0 1 0	0 0 0																		

8 × 16 Dot Font

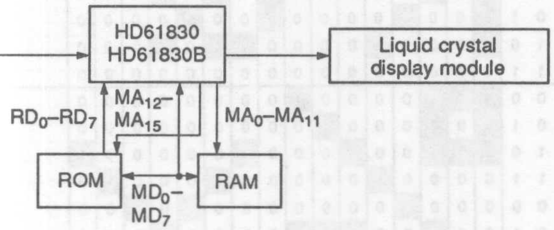
		A11	0								0								0
		A10	0								0								0
		A 9	0								0								1
		A 8	0								1								0
A7 A6 A5 A4	A3 A2 A1 A0		O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	
0 0 0 0	0 0 0 0						0	0	0	0	0	0	0	0	0	0	0	0	
	0 0 0 1			0	0	0		0	0	0	0	0	0	0	0	0	0	0	
	0 0 1 0			0	0	0		0	0	0	0	0	0	0	0	0	0	0	
	0 0 1 1						0	0	0	0		0	0	0	0	0		0	
	0 1 0 0			0		0	0	0	0	0	0		0	0	0		0	0	
	0 1 0 1			0	0		0	0	0	0	0	0		0		0	0	0	
	0 1 1 0			0	0	0		0	0	0	0	0	0		0	0	0	0	
	0 1 1 1		0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	
	1 0 0 0		0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	
	1 0 0 1		0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	
	1 0 1 0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1 0 1 1		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1 1 0 0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1 1 0 1		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1 1 1 0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1 1 1 1		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	0 0 0 0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Example of Configuration

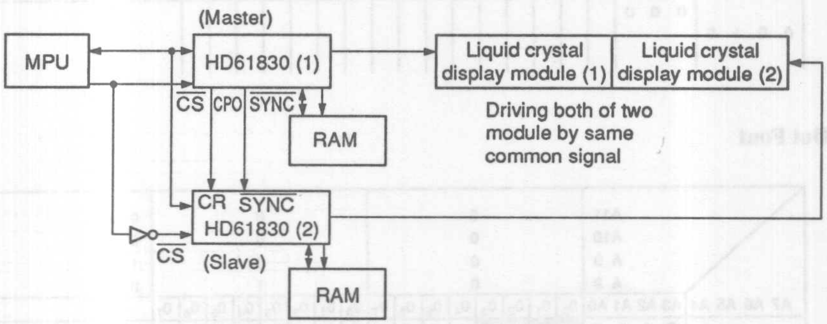
Graphic Mode or Character Mode (1) (Internal Character Generator)



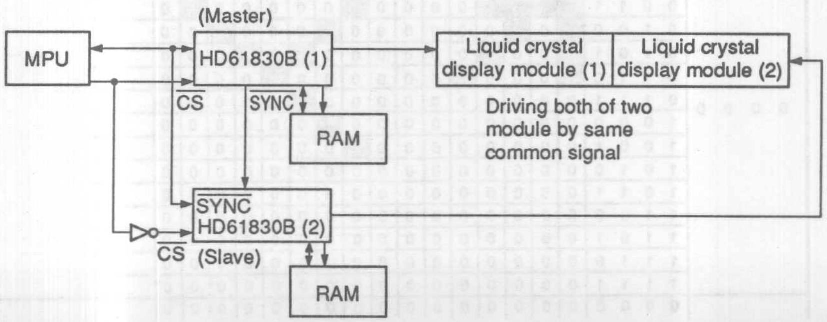
Character Mode (2) (External Character Generator)



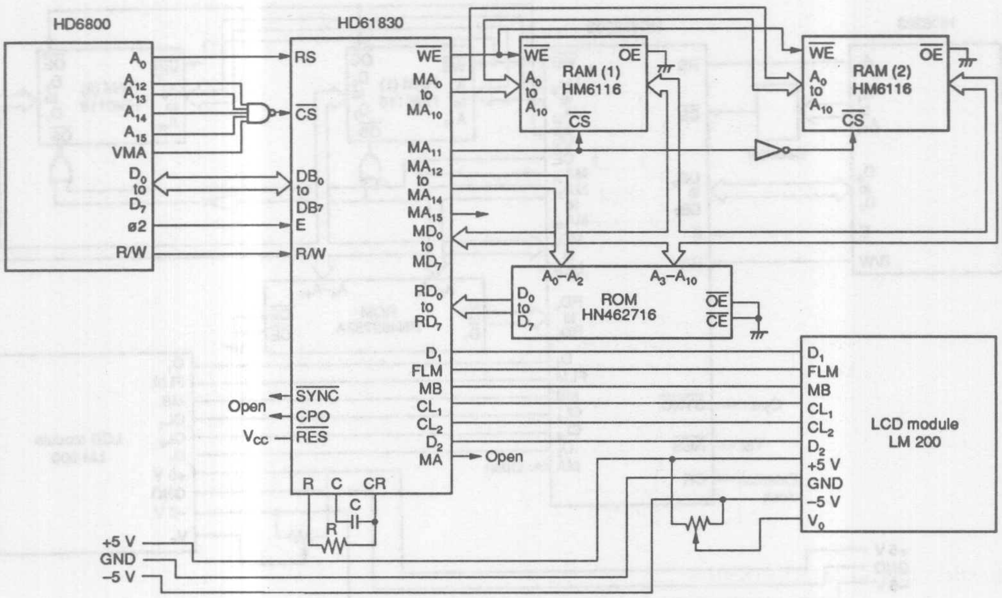
Parallel Operation (HD61830)



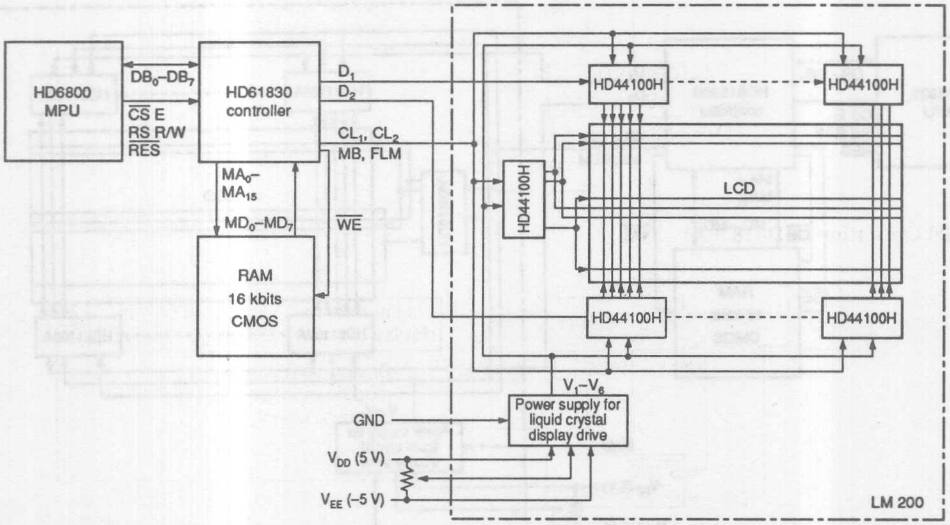
Parallel Operation (HD61830B)



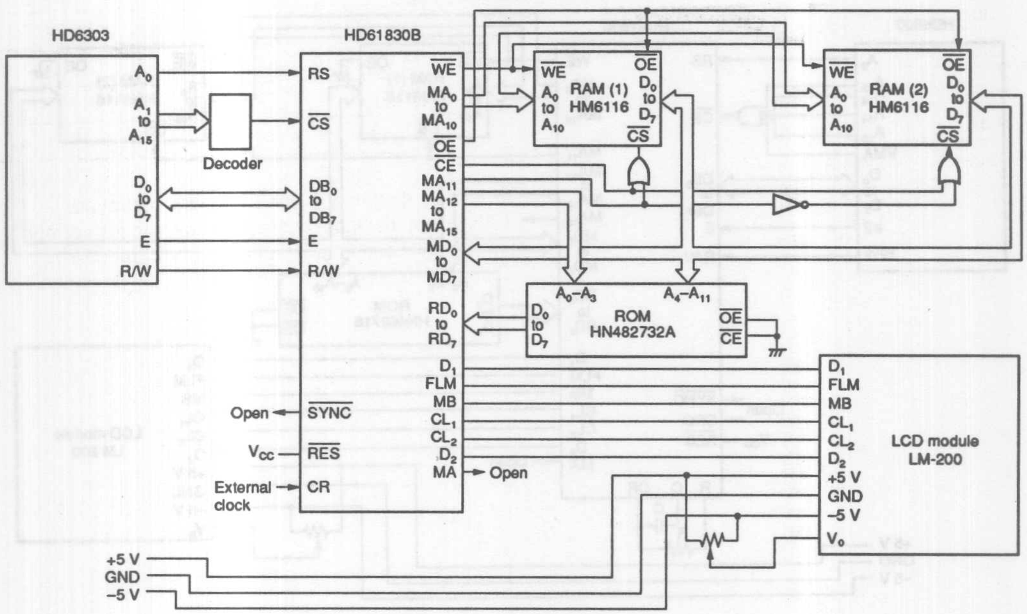
HD61830 Application (Character Mode, External CG, Character Font 8 × 8)



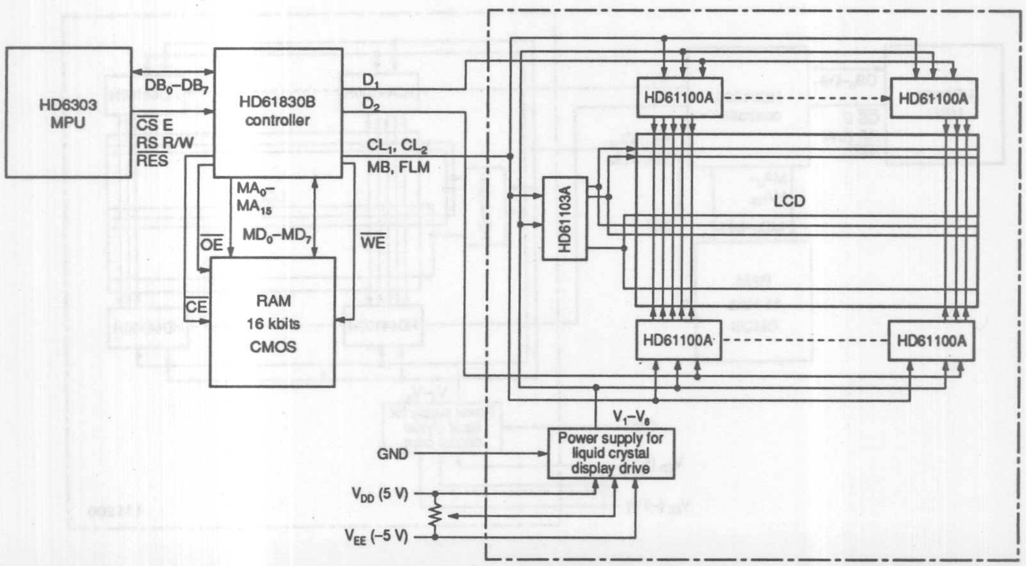
HD61830 Application (Graphic Mode)



HD61830B Application (Character Mode, External CG, Character Font 8 × 8)



HD61830B Application (Graphic Mode)



HD61830 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +0.7	V	1, 2
Terminal voltage	V_T	–0.3 to V_{CC} +0.3	V	1, 2
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. All voltages are referenced to GND = 0 V.

2. If LSIs are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend that you use the LSIs within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

HD61830 Electrical Characteristics

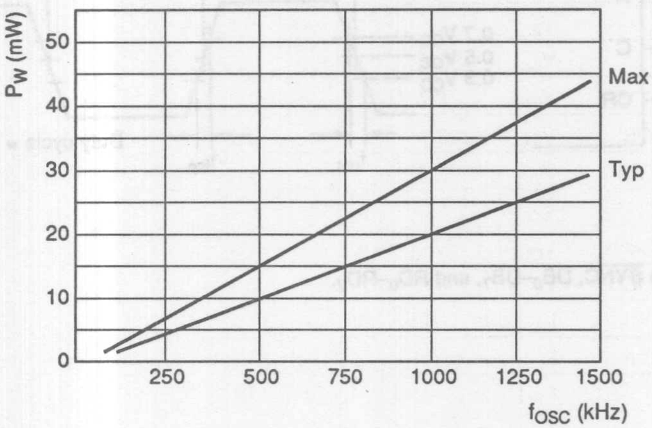
(V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage (TTL)	V_{IH}	2.2	—	V_{CC}	V		1
Input low voltage (TTL)	V_{IL}	0	—	0.8	V		2
Input high voltage	V_{IHR}	3.0	—	V_{CC}	V		3
Input high voltage (CMOS)	V_{IHC}	0.7 V_{CC}	—	V_{CC}	V		4
Input low voltage (CMOS)	V_{ILC}	0	—	0.3 V_{CC}	V		4
Output high voltage (TTL)	V_{OH}	2.4	—	V_{CC}	V	$-I_{OH}$ = 0.6 mA	5
Output low voltage (TTL)	V_{OL}	0	—	0.4	V	I_{OL} = 1.6 mA	5
Output high voltage (CMOS)	V_{OHC}	V_{CC} – 0.4	—	V_{CC}	V	$-I_{OH}$ = 0.6 mA	6
Output low voltage (CMOS)	V_{OLC}	0	—	0.4	V	I_{OL} = 0.6 mA	6
Input leakage current	I_{IN}	–5	—	5	µA	V_{IN} = 0 – V_{CC}	7
Three-state leakage current	I_{TSL}	–10	—	10	µA	V_{OUT} = 0 – V_{CC}	8
Power dissipation (1)	P_W1	—	10	15	mW	CR oscillation f_{osc} = 500 kHz	9
Power dissipation (2)	P_W2	—	20	30	mW	External clock f_{cp} = 1 MHz	9
Internal clock operation							
Clock oscillation frequency	f_{osc}	400	500	600	kHz	C_f = 15 pF ±5% R_f = 39 kΩ ±2%	10
External clock operation							
External clock operating frequency	f_{cp}	100	500	1100	kHz		11
External clock duty	Duty	47.5	50	52.5	%		11
External clock rise time	t_{rcp}	—	—	0.05	µs		11
External clock fall time	t_{fcp}	—	—	0.05	µs		11
Pull-up current	I_{PL}	2	10	20	µA	V_{IN} = GND	12

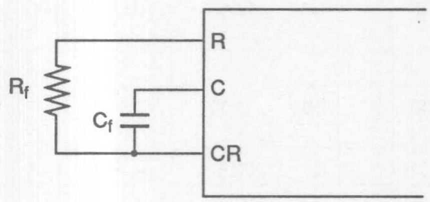
Notes: The I/O terminals have the following configuration:

1. Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$, CR, and $\overline{RES}$.
2. Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$ and CR.
3. Applied to terminal $\overline{RES}$.
4. Applied to terminals $\overline{SYNC}$ and CR.
5. Applied to terminals DB_0–DB_7, $\overline{WE}$, MA_0–MA_{15}, and MD_0–MD_7.
6. Applied to terminals $\overline{SYNC}$, CP0, FLM, CL_1, CL_2, D_1, D_2, MA, and MB.
7. Applied to input terminals.
8. Applied to I/O common terminals. However, the current which flows into the output drive MOS is excluded.

9. The current which flows into the input and output circuits is excluded. When the input of CMOS is in the intermediate level, current flows through the input circuit, resulting in the increase of power supply current. To avoid this, input must be fixed at high or low.
   The relationship between the operating frequency and the power dissipation is given below.

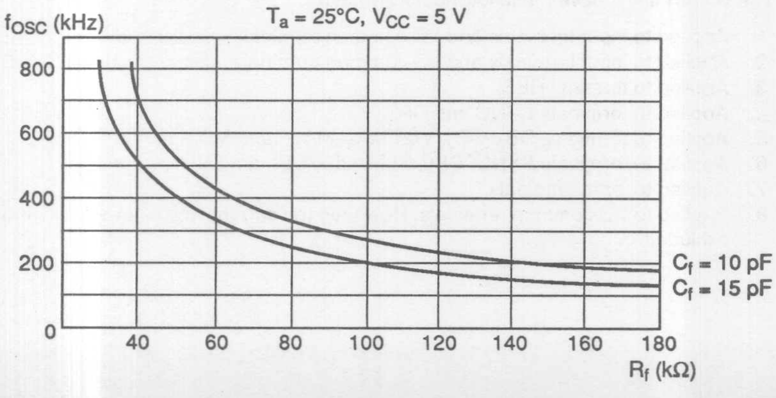


10. Applied to the operation of the internal oscillator when oscillation resistor R_f and oscillation capacity C_f are used.

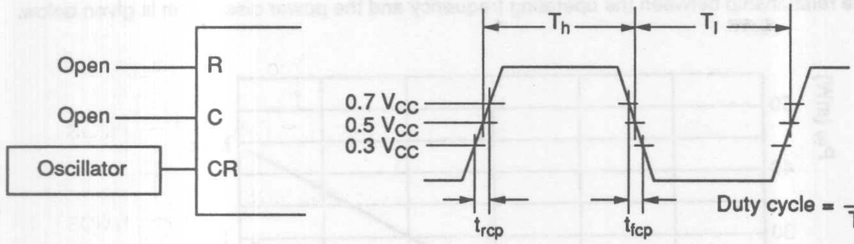


C_f = 15 pF ±5%
R_f = 39 kΩ ±2%
(when f_{OSC} = 500 kHz typ)

The relationship among oscillation frequency, R_f and C_f is given below.



11. Applied to external clock operation.

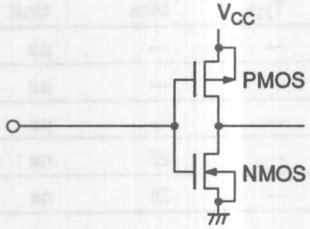


$$\text{Duty cycle} = \frac{T_h}{T_h + T_l} \times 100\%$$

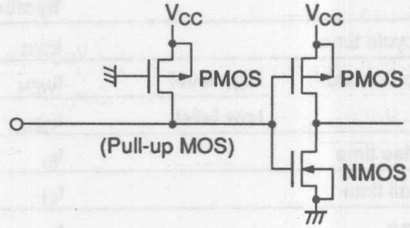
12. Applied to $\overline{\text{SYNC}}$, DB_0–DB_7, and RD_0–RD_7.

Input Terminal

Applicable terminal: $\overline{CS}$, E, RS, R/W, $\overline{RES}$, CR (without pull-up MOS)

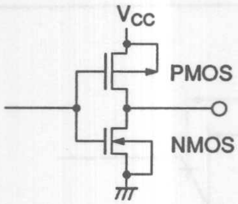


Applicable terminal: RD_0–RD_7 (with pull-up MOS)



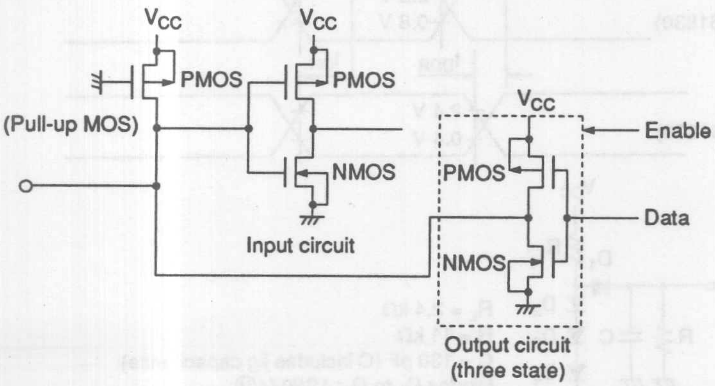
Output Terminal

Applicable terminal: CL_1, CL_2, MA, MB, FLM, D_1, D_2, $\overline{WE}$, $\overline{OE}$, $\overline{CE}$, MA_0–MA_{15}



I/O Common Terminal

Applicable terminal: DB_0–DB_7, $\overline{SYNC}$, MD_0–MD_7 (MD_0–MD_7 have no pull-up MOS)

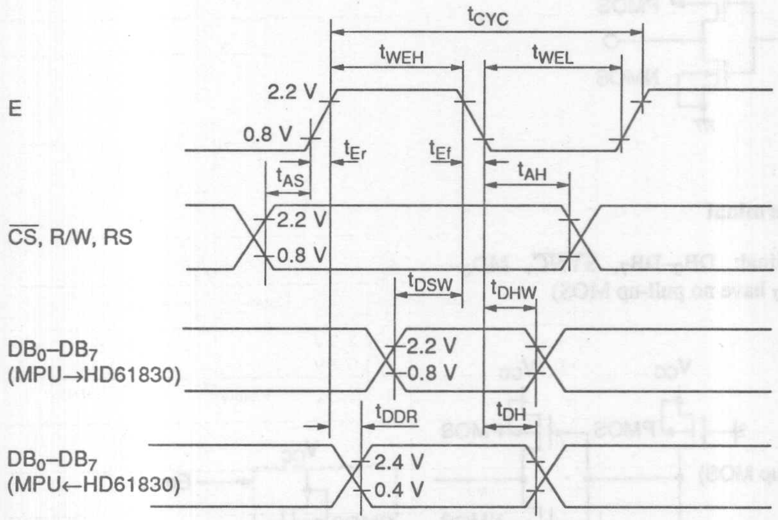


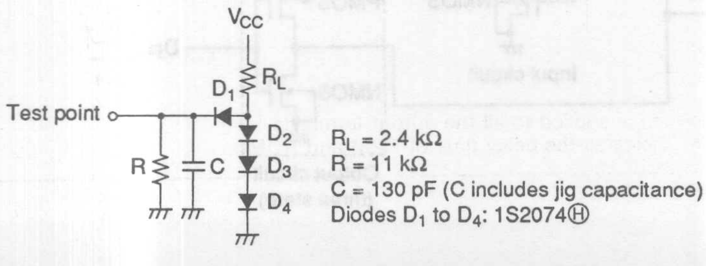
Timing Characteristics

HD61830 MPU Interface
(V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item		Symbol	Min	Typ	Max	Unit
Enable cycle time		t_{CYC}	1.0	—	—	µs
Enable pulse width	High level	t_{WEH}	0.45	—	—	µs
	Low level	t_{WEL}	0.45	—	—	µs
Enable rise time		t_{Er}	—	—	25	ns
Enable fall time		t_{Ef}	—	—	25	ns
Setup time		t_{AS}	140	—	—	ns
Data setup time		t_{DSW}	225	—	—	ns
Data delay time		t_{DDR}	—	—	225	ns *
Data hold time		t_{DHW}	10	—	—	ns
Address hold time		t_{AH}	10	—	—	ns
Data hold time		t_{DH}	20	—	—	ns

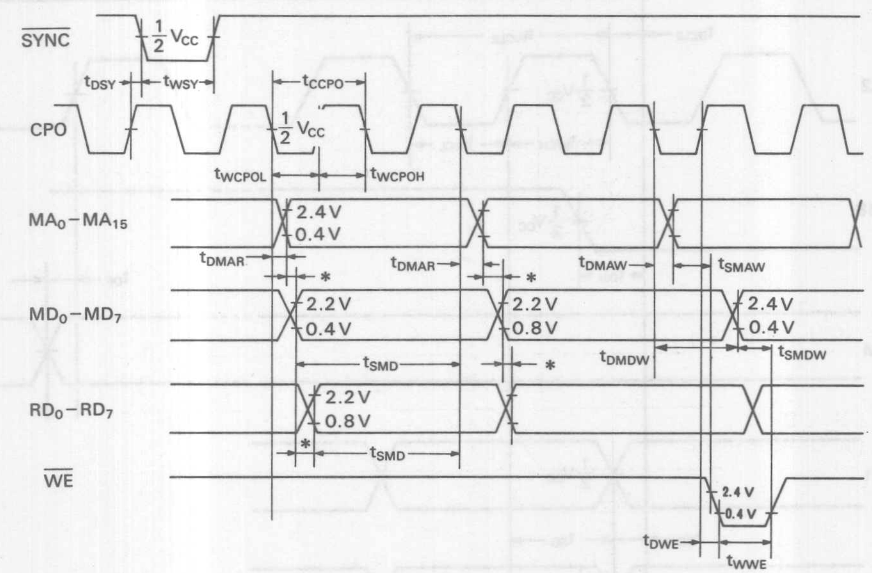
Note: * The following load circuit is connected for specification:





HD61830 External RAM and ROM Interface
(V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item		Symbol	Min	Typ	Max	Unit
$\overline{\text{SYNC}}$ delay time		t_{DSY}	—	—	200	ns
$\overline{\text{SYNC}}$ pulse width	High level	t_{WSY}	900	—	—	ns
CP0 cycle time		t_{CCP0}	900	—	—	ns
CP0 pulse width	High level	t_{WCP0H}	450	—	—	ns
	Low level	t_{WCP0L}	450	—	—	ns
MA_0 to MA_{15} refresh delay time		t_{DMAR}	—	—	200	ns
MA_0 to MA_{15} write address delay time		t_{DMAW}	—	—	200	ns
MD_0 to MD_7 write data delay time		t_{DMDW}	—	—	200	ns
MD_0 to MD_7, RD_0 to RD_7 setup time		t_{SMD}	900	—	—	ns
Memory address setup time		t_{SMAW}	250	—	—	ns
Memory data setup time		t_{SMDW}	250	—	—	ns
$\overline{\text{WE}}$ delay time		t_{DWE}	—	—	200	ns
$\overline{\text{WE}}$ pulse width (low level)		t_{WWE}	450	—	—	ns



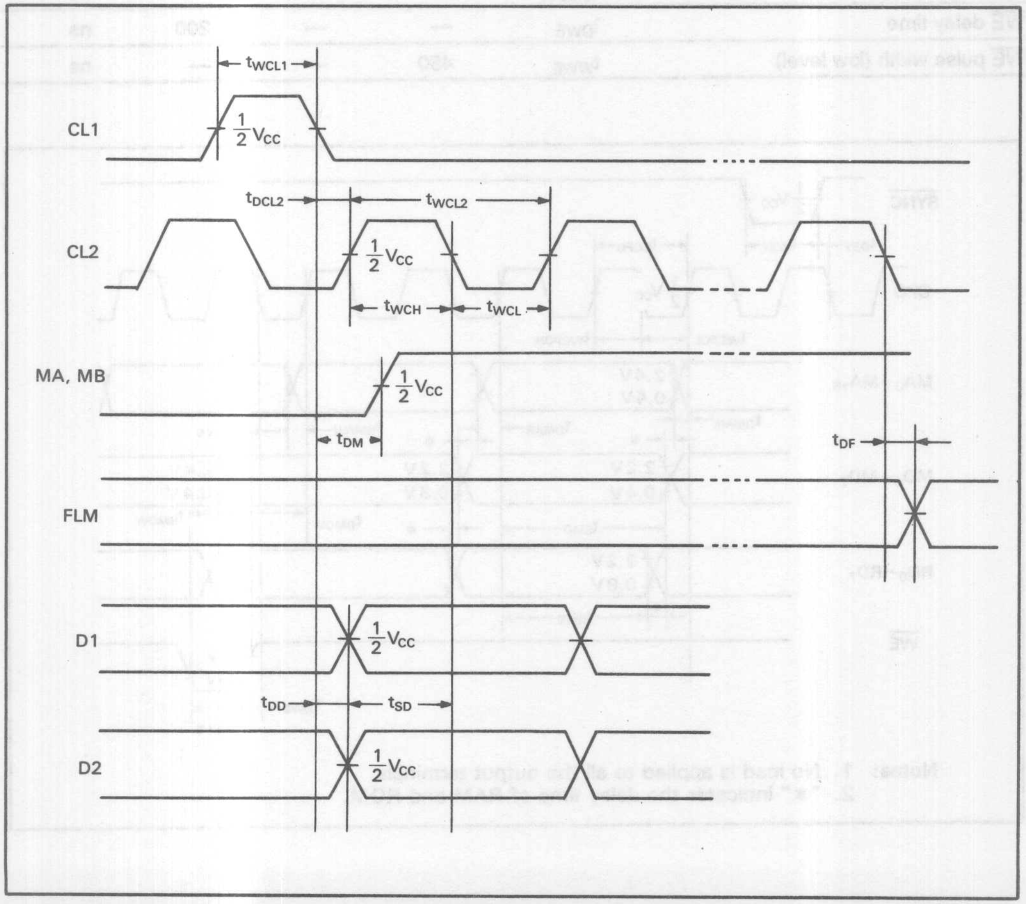
Notes: 1. No load is applied to all the output terminals.
2. "*" indicates the delay time of RAM and ROM.

HD61830 LCD Driver Interface

(V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item		Symbol	Min	Typ	Max	Unit
Clock pulse width (high level)		t_{WCL1}	450	—	—	ns
Clock delay time		t_{DCL2}	—	—	200	ns
Clock cycle time		t_{WCL2}	900	—	—	ns
Clock pulse width	High level	t_{WCH}	450	—	—	ns
	Low level	t_{WCL}	450	—	—	ns
MA, MB delay time		t_{MD}	—	—	300	ns
FLM delay time		t_{DF}	—	—	300	ns
Data delay time		t_{DD}	—	—	200	ns
Data setup time		t_{SD}	250	—	—	ns

Note: No load is applied to all the output terminals (MA, MB, FLM, D_1, and D_2).



HD61830B Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +0.7	V	1, 2
Terminal voltage	V_T	–0.3 to V_{CC} +0.3	V	1, 2
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. All voltage is referred to GND = 0 V.

2. If LSIs are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend that you use the LSIs within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

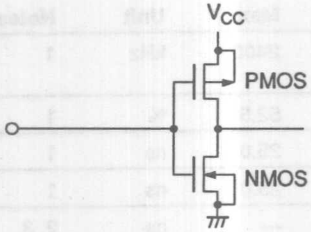
HD61830B Electrical Characteristics (V_{CC} = 5V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage (TTL)	V_{IH}	2.2	—	V_{CC}	V		1
Input low voltage (TTL)	V_{IL}	0	—	0.8	V		2
Input high voltage	V_{IHR}	3.0	—	V_{CC}	V		3
Input high voltage (CMOS)	V_{IHC}	0.7 V_{CC}	—	V_{CC}	V		4
Input low voltage (CMOS)	V_{ILC}	0	—	0.3 V_{CC}	V		4
Output high voltage (TTL)	V_{OH}	2.4	—	V_{CC}	V	$-I_{OH}$ = 0.6 mA	5
Output low voltage (TTL)	V_{OL}	0	—	0.4	V	I_{OL} = 1.6 mA	5
Output high voltage (CMOS)	V_{OHC}	V_{CC} – 0.4	—	V_{CC}	V	$-I_{OH}$ = 0.6 mA	6
Output low voltage (CMOS)	V_{OLC}	0	—	0.4	V	I_{OI} = 0.6 mA	6
Input leakage current	I_{IN}	–5	—	5	µA	V_{IN} = 0 – V_{CC}	7
Three-state leakage current	I_{TSL}	–10	—	10	µA	V_{OUT} = 0 – V_{CC}	8
Pull-up current	I_{PL}	2	10	20	µA	V_{in} = GND	9
Power dissipation	P_W	—	—	50	mW	External clock f_{cp} = 2.4 MHz	10

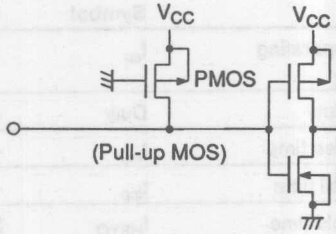
Notes: 1. Applied to input terminals and I/O common terminals, except terminals $\overline{\text{SYNC}}$, CR, and $\overline{\text{RES}}$.
2. Applied to input terminals and I/O common terminals, except terminals $\overline{\text{SYNC}}$ and CR.
3. Applied to terminal $\overline{\text{RES}}$.
4. Applied to terminals $\overline{\text{SYNC}}$ and CR.
5. Applied to terminals DB_0–DB_7, $\overline{\text{WE}}$, MA_0–MA_{15}, $\overline{\text{OE}}$, $\overline{\text{CE}}$, and MD_0–MD_7.
6. Applied to terminals $\overline{\text{SYNC}}$, FLM, CL_1, CL_2, D_1, D_2, MA, and MB.
7. Applied to input terminals.
8. Applied to I/O common terminals. However, the current which flows into the output drive MOS is excluded.
9. Applied to $\overline{\text{SYNC}}$, DB_0–DB_7, and RD_0–RD_7.
10. The current which flows into the input and output circuits is excluded. When the input of CMOS is in the intermediate level, current flows through the input circuit, resulting in the increase of power supply current. To avoid this, input must be fixed at high or low.

Input Terminal

Applicable terminal: $\overline{CS}$, E, RS, R/W, $\overline{RES}$, CR (without pull-up MOS)

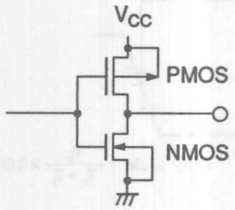


Applicable terminal: RD_0–RD_7 (with pull-up MOS)



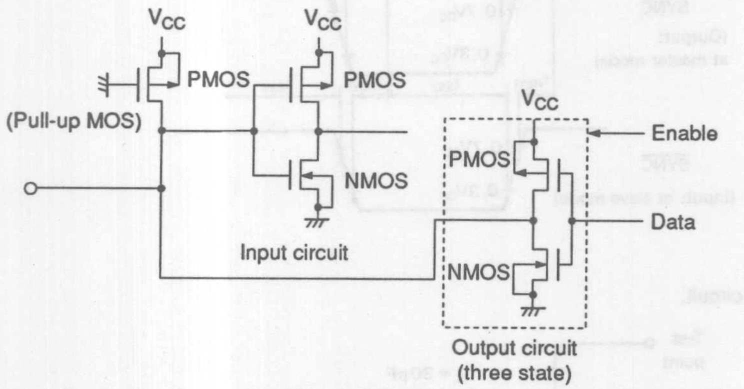
Output Terminal

Applicable terminal: CL_1, CL_2, MA, MB, FLM, D_1, D_2, $\overline{WE}$, $\overline{OE}$, $\overline{CE}$, MA_0–MA_{15}



I/O Common Terminal

Applicable terminal: DB_0–DB_7, $\overline{SYNC}$, MD_0–MD_7 (MD_0–MD_7 have no pull-up MOS)

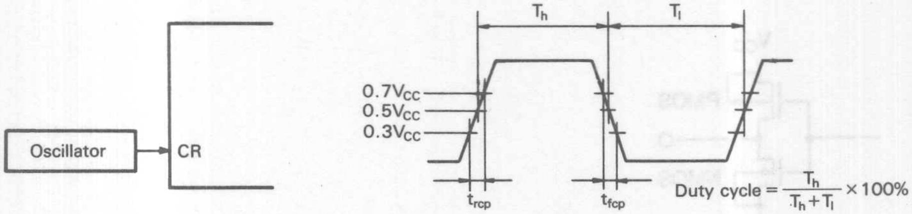


Timing Characteristics

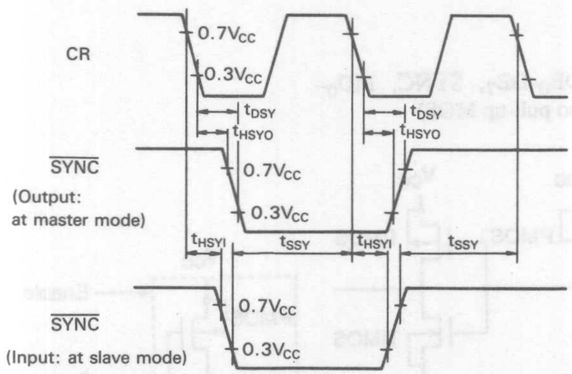
HD61830B Clock Operation
(V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
External clock operating frequency	f_{cp}	100	—	2400	kHz	1
External clock duty	Duty	47.5	50	52.5	%	1
External clock rise time	t_{rcp}	—	—	25.0	ns	1
External clock fall time	t_{fcp}	—	—	25.0	ns	1
$\overline{\text{SYNC}}$ output hold time	t_{HSYO}	30	—	—	ns	2, 3
$\overline{\text{SYNC}}$ output delay time	t_{DSY}	—	—	210	ns	2, 3
$\overline{\text{SYNC}}$ input hold time	t_{HSYI}	10	—	—	ns	2
$\overline{\text{SYNC}}$ input set-up time	t_{SSY}	—	—	180	ns	2

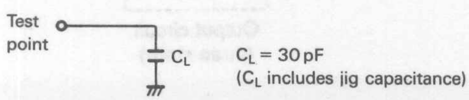
Notes: 1. Applied to external clock input terminal.



2. Applied to $\overline{\text{SYNC}}$ terminal.



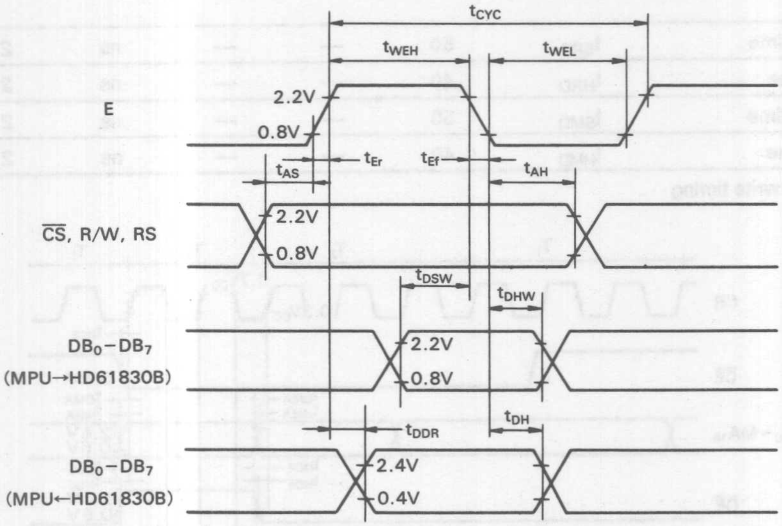
3. Testing load circuit.

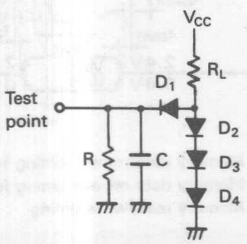


HD61830B MPU Interface
(V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item		Symbol	Min	Typ	Max	Unit
Enable cycle time		t_{CYC}	1.0	—	—	µs
Enable pulse width	High level	t_{WEH}	0.45	—	—	µs
	Low level	t_{WEL}	0.45	—	—	µs
Enable rise time		t_{Er}	—	—	25	ns
Enable fall time		t_{Ef}	—	—	25	ns
Setup time		t_{AS}	140	—	—	ns
Data setup time		t_{DSW}	225	—	—	ns
Data delay time		t_{DDR}	—	—	225	ns *
Data hold time		t_{DHW}	10	—	—	ns
Address hold time		t_{AH}	10	—	—	ns
Data hold time		t_{DH}	20	—	—	ns

Note: * The following load circuit is connected for specification:



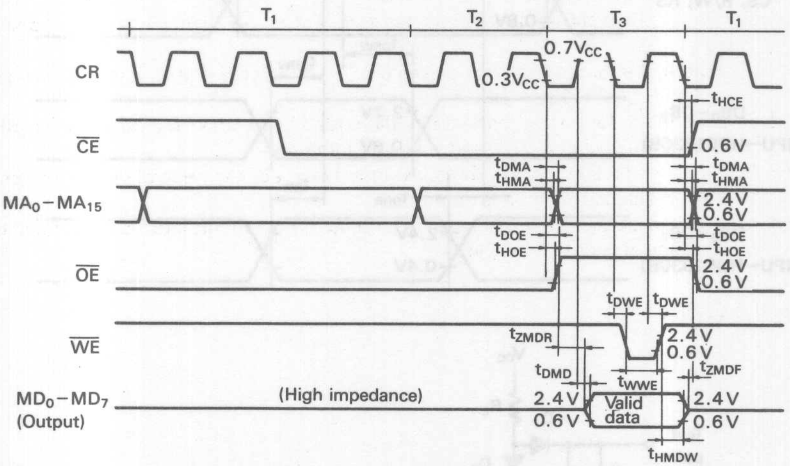


R_L = 2.4 kΩ
R = 11 kΩ
C = 130 pF (C includes jig capacitance)
Diodes D_1 to D_4: 1S2074Ⓗ

HD61830B External RAM and ROM Interface
(V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

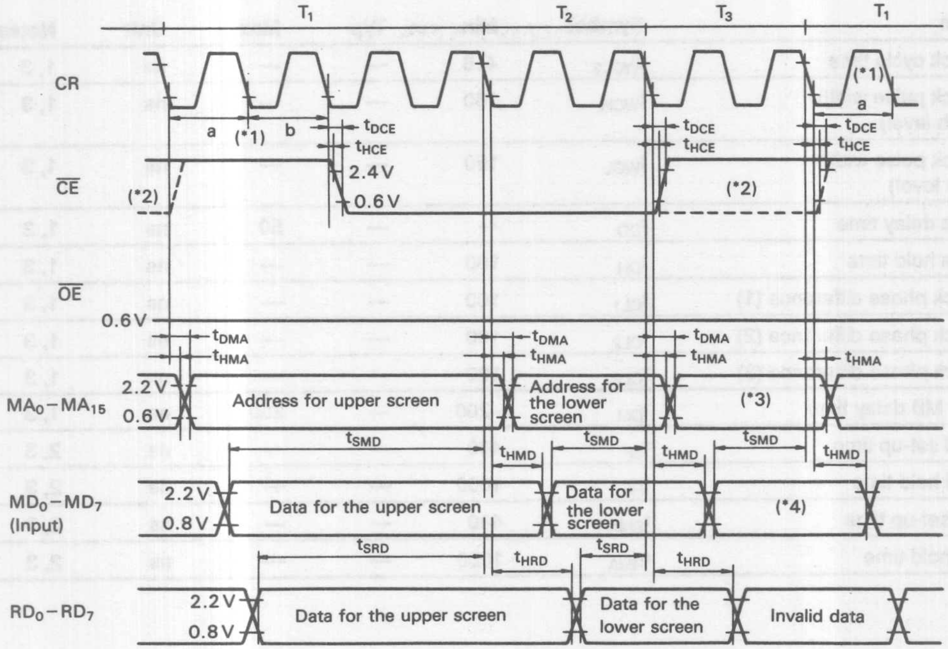
Item	Symbol	Min	Typ	Max	Unit	Notes
MA_0–MA_{15} delay time	t_{DMA}	—	—	300	ns	1, 2, 3
MA_0–MA_{15} hold time	t_{HMA}	40	—	—	ns	1, 2, 3
$\overline{CE}$ delay time	t_{DCE}	—	—	300	ns	1, 2, 3
$\overline{CE}$ hold time	t_{HCE}	40	—	—	ns	1, 2, 3
$\overline{OE}$ delay time	t_{DOE}	—	—	300	ns	1, 3
$\overline{OE}$ hold time	t_{HOE}	40	—	—	ns	1, 3
MD output delay time	t_{DMD}	—	—	150	ns	1, 3
MD output hold time	t_{HMDW}	10	—	—	ns	1, 3
$\overline{WE}$ delay time	t_{DWE}	—	—	150	ns	1, 3
$\overline{WE}$ clock pulse width	t_{WWE}	150	—	—	ns	1, 3
MD output high impedance time (1)	t_{ZMDF}	10	—	—	ns	1, 3
MD output high impedance time (2)	t_{ZMDR}	50	—	—	ns	1, 3
RD data set-up time	t_{SRD}	50	—	—	ns	2
RD data hold time	t_{HRD}	40	—	—	ns	2
MD data set-up time	t_{SMD}	50	—	—	ns	2
MD data hold time	t_{HMD}	40	—	—	ns	2

Notes: 1. RAM write timing



T1: Memory data refresh timing for upper screen
T2: Memory data refresh timing for lower screen
T3: Memory read/write timing

2. ROM/RAM read timing



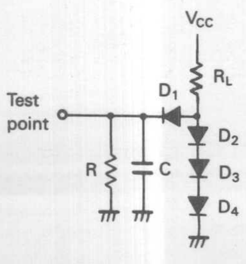
*1 This figures shows the timing for $H_p = 8$.
For $H_p = 7$, time shown by "b" becomes zero. For $H_p = 6$, time shown by "a" and "b" become zero.
Therefore, the number of clock pulses during T1 become 4, 3, or 2 in the case of $H_p = 8$, $H_p = 7$, or $H_p = 6$ respectively.

*2 The waveform for instructions with memory read is shown with a dash line. In other cases, the waveform shown with a solid line is generated.

*3 When an instruction with RAM read/write is executed, the value of cursor address is output. In other cases, invalid data is output.

*4 When an instruction with RAM read is executed, HD61830B latches the data at this timing. In other cases, this data is invalid.

3. Test load circuit

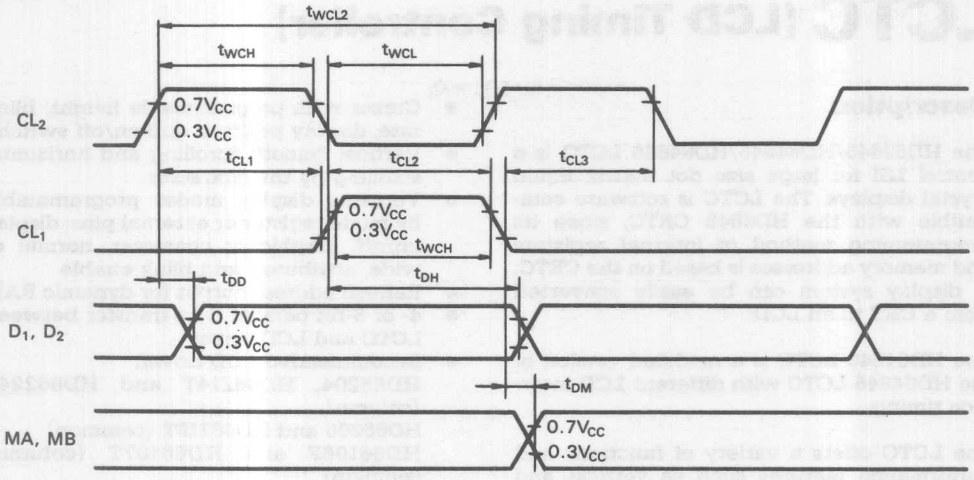


$R_L = 2.4\,k\Omega$
$R = 11\,k\Omega$
$C = 50\,pF$ (C includes jig capacitance)
Diodes D_1 to D_4: 1S2074Ⓗ

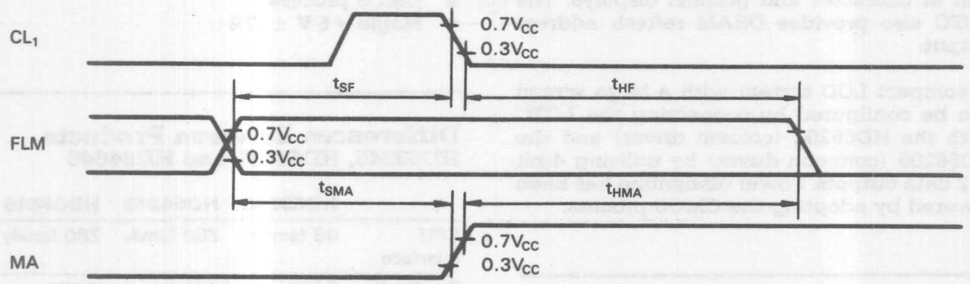
HD61830B LCD Driver Interface
(V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
Clock cycle time	t_{WCL2}	416	—	—	ns	1, 3
Clock pulse width (high level)	t_{WCH}	150	—	—	ns	1, 3
Clock pulse width (low level)	t_{WCL}	150	—	—	ns	1, 3
Data delay time	t_{DD}	—	—	50	ns	1, 3
Data hold time	t_{DH}	100	—	—	ns	1, 3
Clock phase difference (1)	t_{CL1}	100	—	—	ns	1, 3
Clock phase difference (2)	t_{CL2}	100	—	—	ns	1, 3
Clock phase difference (3)	t_{CL3}	100	—	—	ns	1, 3
MA, MB delay time	t_{DM}	–200	—	200	ns	1, 3
FLM set-up time	t_{SF}	400	—	—	ns	2, 3
FLM hold time	t_{HF}	1000	—	—	ns	2, 3
MA set-up time	t_{SMA}	400	—	—	ns	2, 3
MA hold time	t_{HMA}	1000	—	—	ns	2, 3

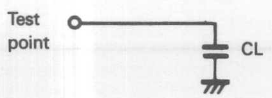
Notes: 1.



2.



3. Test load circuit



CL = 100 pF (C_L includes jig capacitance)

HD63645/HD64645/HD64646
LCTC (LCD Timing Controller)

Description

The HD63645/HD64645/HD64646 LCTC is a control LSI for large size dot matrix liquid crystal displays. The LCTC is software compatible with the HD6845 CRTC, since its programming method of internal registers and memory addresses is based on the CRTC. A display system can be easily converted from a CRT to an LCD.

The HD64646 LCTC is a modified version of the HD64645 LCTC with different LCD interface timing.

The LCTC offers a variety of functions and performance features such as vertical and horizontal scrolling, and various types of character attribute functions such as reverse video, blinking, nondisplay (white or black), and an OR function for simple superimposition of character and graphic displays. The LCTC also provides DRAM refresh address output.

A compact LCD system with a large screen can be configured by connecting the LCTC with the HD66204 (column driver) and the HD66205 (common driver) by utilizing 4-bit × 2 data outputs. Power dissipation has been lowered by adopting the CMOS process.

Features

- Software compatible with the HD6845 CRTC
- Programmable screen size:
  —Up to 1024 dots (height)
  —Up to 4096 dots (width)
- High-speed data transfer:
  —Up to 20 Mbits/s in character mode
  —Up to 40 Mbits/s in graphic mode
- Selectable single or dual screen configuration
- Programmable multiplexing duty ratio: static to 1/512 duty cycle
- Programmable character font:
  —1-32 dots (height)
  —8 dots (width)
- Versatile character attributes: reverse video, blinking, nondisplay (white), nondisplay (black)
- OR function: superimposing characters and graphics display
- Cursor with programmable height, blink rate, display position, and on/off switch
- Vertical Smooth Scrolling and horizontal scrolling by the character
- Versatile display modes programmable by mode register or external pins: display on/off, graphic or character, normal or wide, attributes, and blink enable
- Refresh address output for dynamic RAM
- 4- or 8-bit parallel data transfer between LCTC and LCD driver
- Recommended LCD driver:
  HD66204, HD66214T and HD66224T (column)
  HD66205 and HD66215T (common)
  HD66106F and HD66107T (column/common)
  HD66110RT (column)
- CPU interface:
  68 family HD63645
  Z80 family HD64645, HD64646
- CMOS process
- Single +5 V ±10%

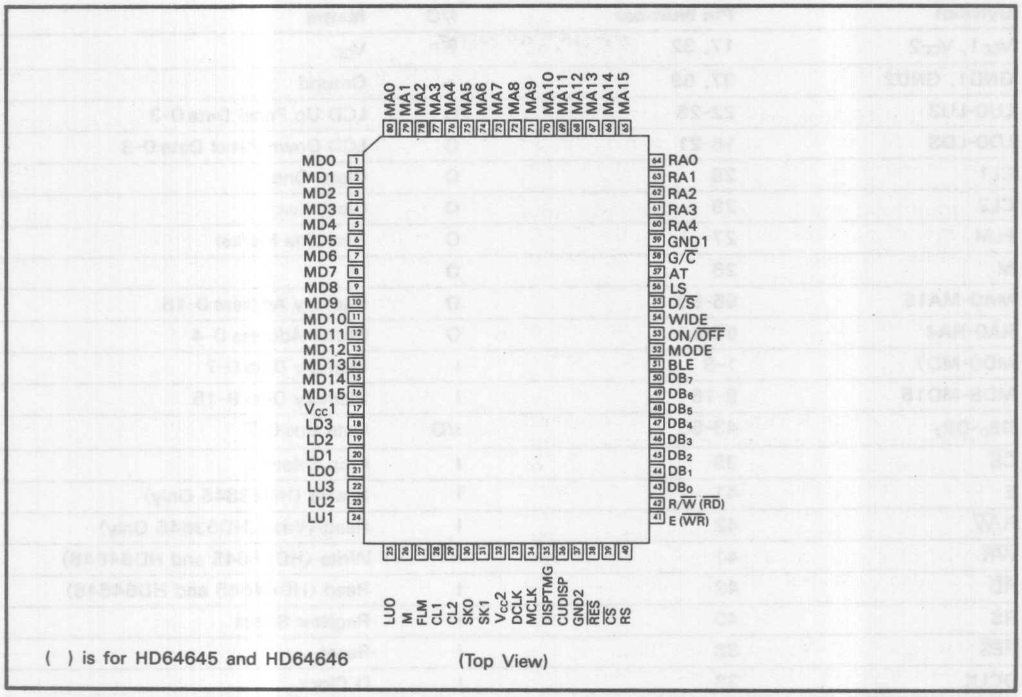
Differences Between Products HD63645, HD64645 and HD64646

	HD63645	HD64645	HD64646
CPU Interface	68 family	Z80 family	Z80 family
Bus Timing	2 MHz	4 MHz	4 MHz
Pin Arrengement and Signal name	Pin 41: R/W Pin 42: E	Pin 41: $\overline{RD}$ Pin 42: $\overline{WR}$	Pin 41: $\overline{RD}$ Pin 42: $\overline{WR}$
Other	–	–	modified LCD driver interface timing

Ordering Infomation

Type No.	CPU Interface	Package
HD63645F	68 family 2 MHz bus	80-pin plastic QFP (FP-80B)
HD64645F	Z80 family 4 MHz bus	80-pin plastic QFP (FP-80B)
HD64646FS	Z80 family 4 MHz bus	80-pin plastic QFP (FP-80B)

Pin Arrangement



Pin Description

Symbol	Pin Number	I/O	Name
$V_{CC}1$, $V_{CC}2$	17, 32	–	V_{CC}
GND1, GND2	37, 59	–	Ground
LU0-LU3	22-25	O	LCD Up Panel Data 0-3
LD0-LD3	18-21	O	LCD Down Panel Data 0-3
CL1	28	O	Clock One
CL2	29	O	Clock Two
FLM	27	O	First Line Marker
M	26	O	M
MA0-MA15	65-80	O	Memory Address 0-15
RA0-RA4	60-64	O	Raster Address 0-4
MD0-MD7	1-8	I	Memory Data 0-7
MD8-MD15	9-16	I	Memory Data 8-15
DB_0-DB_7	43-50	I/O	Data Bus 0-7
$\overline{CS}$	39	I	Chip Select
E	41	I	Enable (HD63645 Only)
R/$\overline{W}$	42	I	Read/Write (HD63645 Only)
$\overline{WR}$	41	I	Write (HD64645 and HD64646)
$\overline{RD}$	42	I	Read (HD64645 and HD64646)
RS	40	I	Register Select
$\overline{RES}$	38	I	Reset
DCLK	33	I	D Clock
MCLK	34	O	M Clock
DISPTMG	35	O	Display Timing
CUDISP	36	O	Cursor Display
SK0	30	I	Skew 0
SK1	31	I	Skew 1
ON/$\overline{OFF}$	53	I	On/Off
BLE	51	I	Blink Enable
AT	57	I	Attribute
G/$\overline{C}$	58	I	Graphic/Character
WIDE	54	I	Wide
LS	56	I	Large Screen
D/$\overline{S}$	55	I	Dual/Single
MODE	52	I	Mode

Pin Functions

Power Supply ($V_{CC}1$, $V_{CC}2$, GND)

Power Supply Pin (+5 V): Connect $V_{CC}1$ and $V_{CC}2$ with +5 V power supply circuit.

Ground Pin (0 V): Connect GND1 and GND2 with 0 V.

LCD Interface

LCD Up Panel Data (LU0–LU3), LCD Down Panel Data (LD0–LD3): LU0-LU3 and LD0-LD3 output LCD data as shown in table 1.

Clock One (CL1): CL1 supplies timing clocks for display data latch.

Clock Two (CL2): CL2 supplies timing clock for display data shift.

First Line Marker (FLM): FLM supplies first line marker.

M (M): M converts liquid crystal drive output to AC.

Memory Interface

Memory Address (MA0–MA15): MA0-MA15 supply the display memory address.

Raster Address (RA0–RA4): RA0-RA4 supply the raster address.

Memory Data (MD0–MD7): MD0-MD7 receive the character dot data and bit-mapped data.

Memory Data (MD8–MD15): MD8-MD15 receive attribute code data and bit-mapped data.

MPU Interface

Data Bus (DB0–DB7): DB0-DB7 send/receive data as a three-state I/O common bus.

Chip Select ($\overline{CS}$): $\overline{CS}$ selects a chip. Low level enables MPU read/write of the LCTC internal registers.

Enable (E): E receives an enable clock. (HD63645 only).

Read/Write (R/$\overline{W}$): R/$\overline{W}$ enables MPU read of the LCTC internal registers when R/$\overline{W}$ is high, and MPU write when low (HD63645 only).

Write ($\overline{WR}$): $\overline{WR}$ receives MPU write signal (HD64645 and HD64646).

Read ($\overline{RD}$): $\overline{RD}$ receives MPU read signal (HD64645 and HD64646).

Register Select (RS): RS selects registers. (Refer to table 5.)

Reset ($\overline{RES}$): $\overline{RES}$ performs external reset of the LCTC. Low level of $\overline{RES}$ stops and zero-clears the LCTC internal counter. No register contents are affected.

Timing Signal

D Clock (DCLK): DCLK inputs the system clock.

M Clock (MCLK): MCLK indicates memory cycle; DCLK is divided by four.

Display Timing (DISPTMG): DISPTMG high indicates that the LCTC is reading display data.

Cursor Display (CUDISP): CUDISP supplies cursor display timing; connect with MD12 in character mode.

Skew 0 (SK0)/Skew 1 (SK1): SK0 and SK1 control skew timing. Refer to table 2.

Mode Select

The mode select pins ON/$\overline{OFF}$, BLE, AT, G/$\overline{C}$,

Table 1 LCD Up Panel Data and LCD Down Panel Data

Pin name	Single Screen: 4-Bit Data	Single Screen: 8-Bit Data	Dual Screen
LU0-LU3	Data output	Data output	Data output for upper screen
LD0-LD3	Disconnected	Data output	Data output for lower screen

and WIDE are ORed with the mode register (R22) to determine the mode.

On/Off (ON/$\overline{OFF}$): ON/$\overline{OFF}$ switches display on and off (High = display on).

Blink Enable (BLE): BLE high level enables attribute code "blinking" (MD13) and provides normal/blank blinking of specified characters for 32 frames each.

Attribute (AT): AT controls character attribute functions.

Graphic/Character (G/$\overline{C}$): G/$\overline{C}$ switches between graphic and character display mode (graphic display when high).

Wide (WIDE): WIDE switches between normal and wide display mode (high = wide display, low = normal display).

Large Screen (LS): LS controls a large screen. LS high provides a data transfer rate of 40 Mbits/s for a graphic display. Also used to specify 8-bit LCD interface mode. For more details, refer to table 10.

Dual/Single (D/$\overline{S}$): D/$\overline{S}$ switches between single and dual screen display (dual screen display when high).

Mode (MODE): MODE controls easy mode. MODE high sets duty ratio, maximum number of rasters, cursor start/end rasters, etc. (Refer to table 9.)

Table 2 Skew Signals

SK0	SK1	Skew Function
0	0	No skew
1	0	1-character time skew
0	1	2-character time skew
1	1	Prohibited combination

Function Overview

LCD and CRT Display Systems

Figure 1 shows a system using both LCD and CRT displays.

Main Features of HD63645/HD64645/HD64646

Main features of the LCTC are:

- High-resolution liquid crystal display screen control (up to 720 × 512 dots)
- Software compatible with HD6845 (CRTC)
- Built-in character attribute control circuit

Table 3 shows how the LCTC can be used.

Table 3 Functions, Application, and Configuration

Classification	Item	Description
Functions	Screen Format	● Programmable horizontal scanning cycle by the character clock period ● Programmable multiplexing duty ratio from static up to 1/512 ● Programmable number of vertical displayed characters ● Programmable number of rasters per character row (number of vertical dots within a character row + space between character rows)
	Cursor Control	● Programmable cursor display position, corresponding to RAM address ● Programmable cursor height by setting display start/end rasters ● Programmable blink rate, 1/32 or 1/64 frame rate
	Memory Rewriting	● Time for rewriting memory set either by specifying number of horizontal total characters or by cycle steal utilizing MCLK
	Memory Addressing	● 16-bit memory address output, up to 64 kbytes x 2 memory accessible ● DRAM refresh address output
	Paging and Scrolling	● Paging by updating start address ● Horizontal scrolling by the character, by setting horizontal virtual screen width ● Vertical smooth scrolling by updating display start raster
	Character Attributes	● Reverse video, blinking, nondisplay (white or black), display ON/OFF
Application	CRTC Compatible	● Facilitates system replacement of CRT display with LCD
	OR Function	● Enables superimposing display of character screen and graphic screen
Configuration	LCTC Configuration	● Single 5 V power supply ● I/O TTL compatible except $\overline{RES}$, MODE, SK0, SK1 ● Bus connectable with HMCS 6800 family (HD63645) ● Bus connectable with 80 family (HD64645 and HD64646) ● CMOS process ● Internal logic fully static ● 80-pin flat plastic package

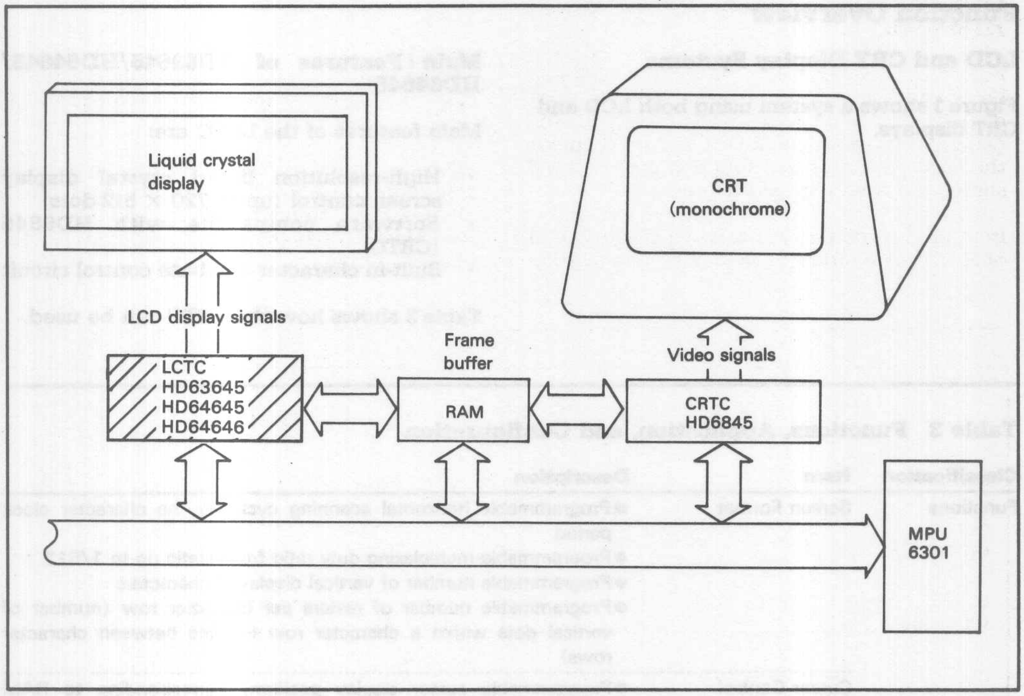


Figure 1 LCD and CRT Displays

Differences Between HD64645 and HD64646

Figure 2 and figure 3 show the relation between display data transfer period, when display data shift clock CL2 changes, and display data latch clock CL1. Figure 2 shows the case without skew function and figure 3 shows the case with skew function.

In figure 2, high period between CL2 and CL1 of HD64645 overlap. HD64646 has no overlap like HD64645, and except for this overlap. HD64646 is the same as HD64645 functionally.

Also for the skew function, phase relation between CL1 and CL2 changes. As figure 3 shows, data transfer period and CL1 high period of HD64646 never overlap with the skew function.

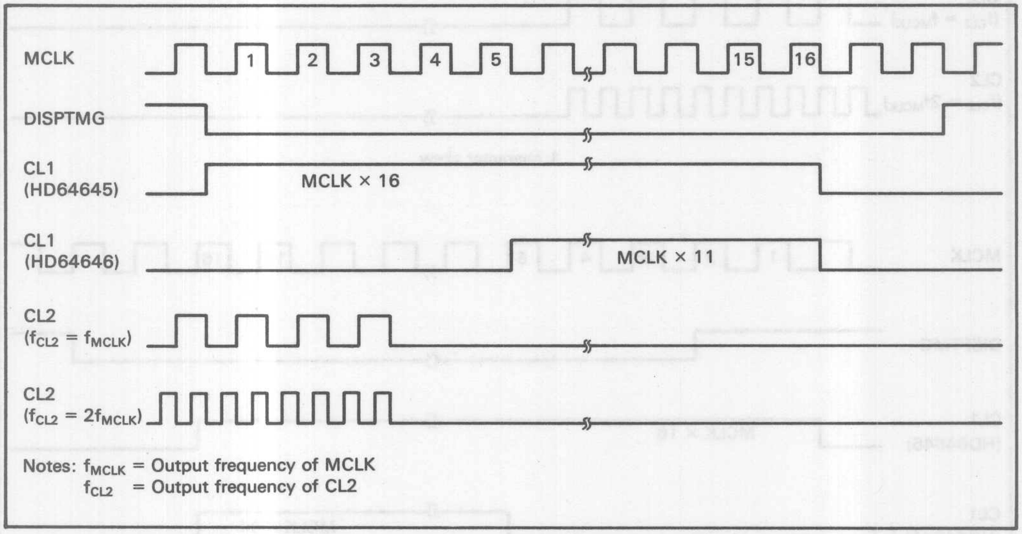


Figure 2 Differences between HD64645 and HD64646 (no skew)

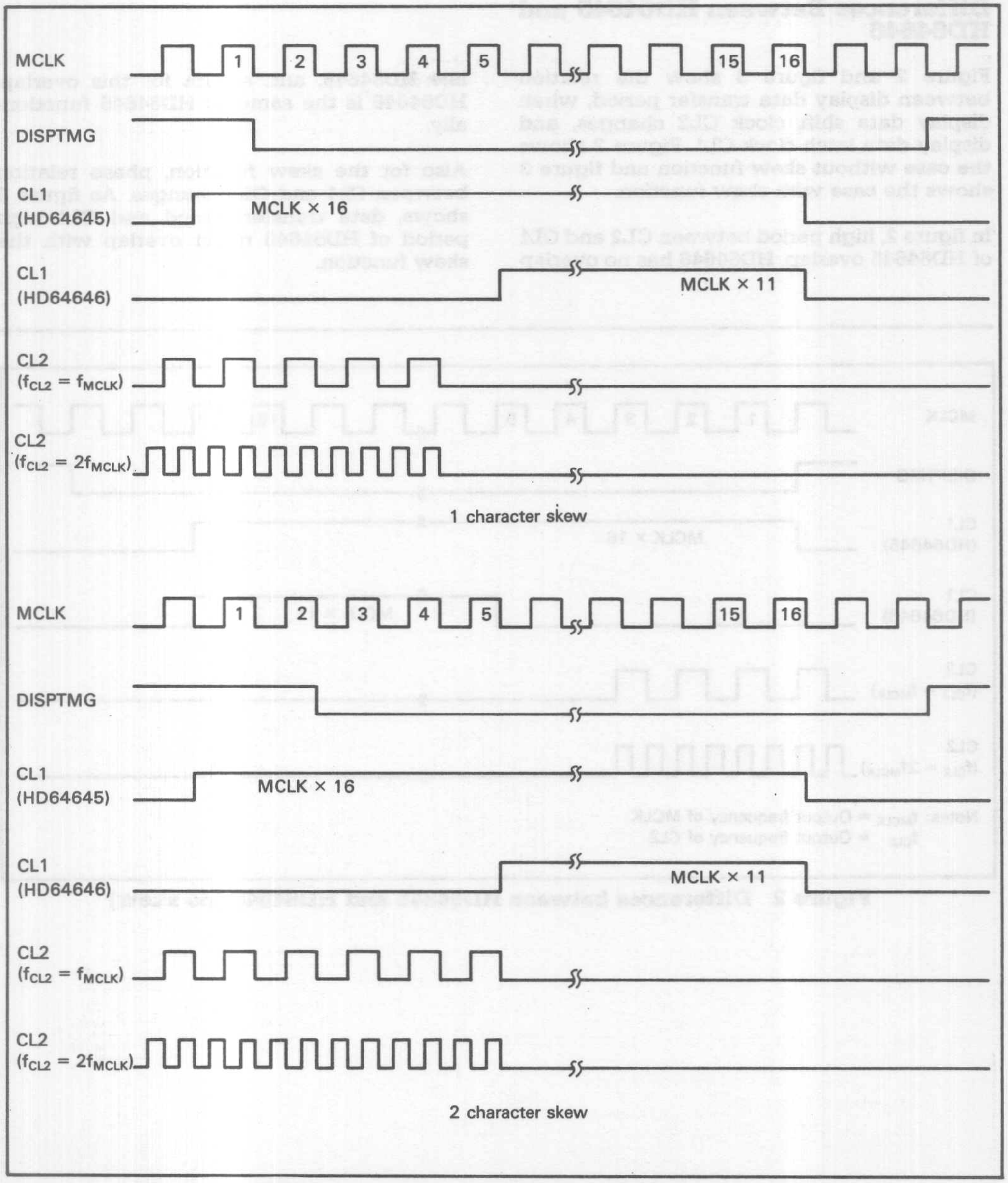
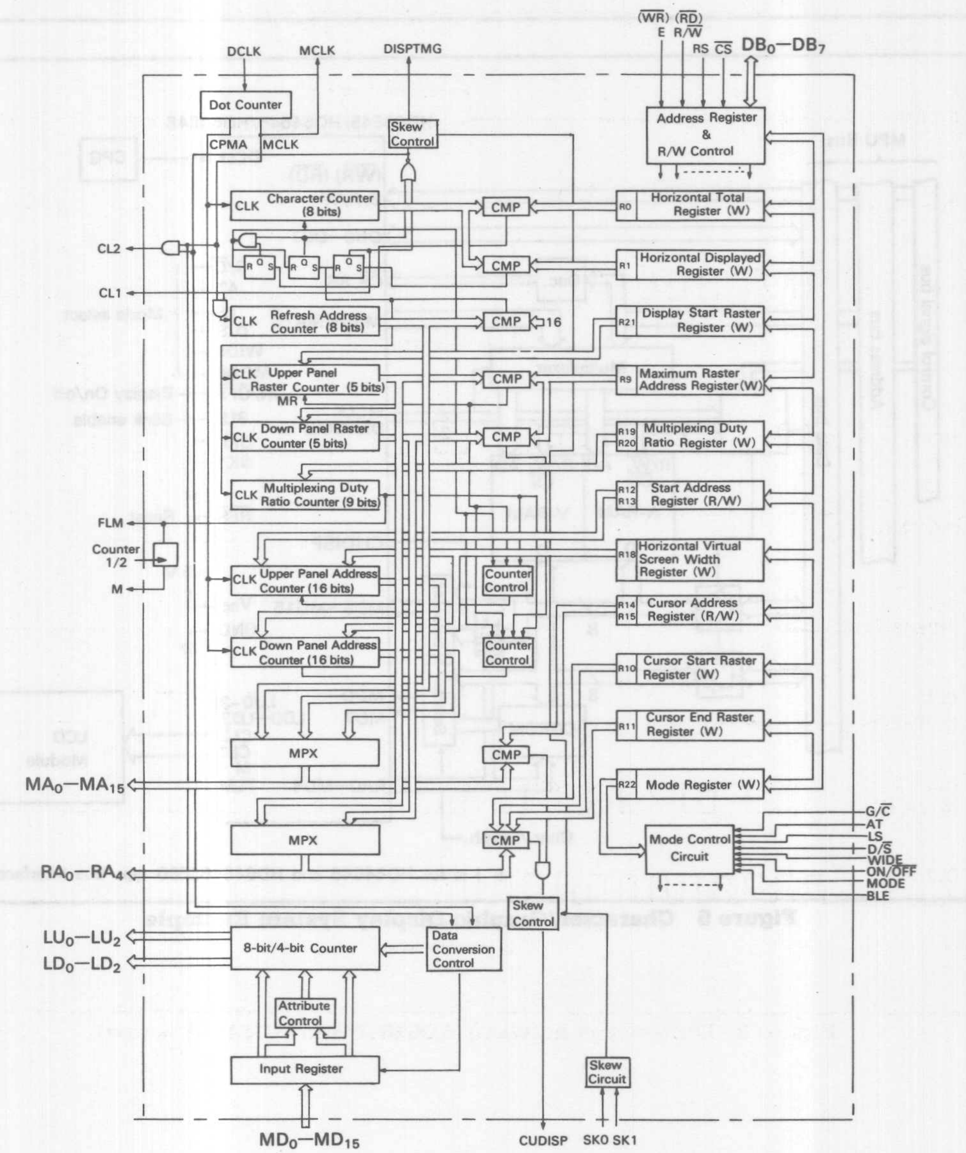


Figure 3 Differences between HD64645 and HD64646 (skew)

Internal Block Diagram

Figure 4 is a block diagram of the LCTC.



( ) is for HD64645 and HD64646 (Z80 types bus interface)

Figure 4 LCTC Block Diagram

System Block Configuration Examples

Figure 5 is a block diagram of a character/graphic display system. Figure 5 shows two examples using LCD drivers.

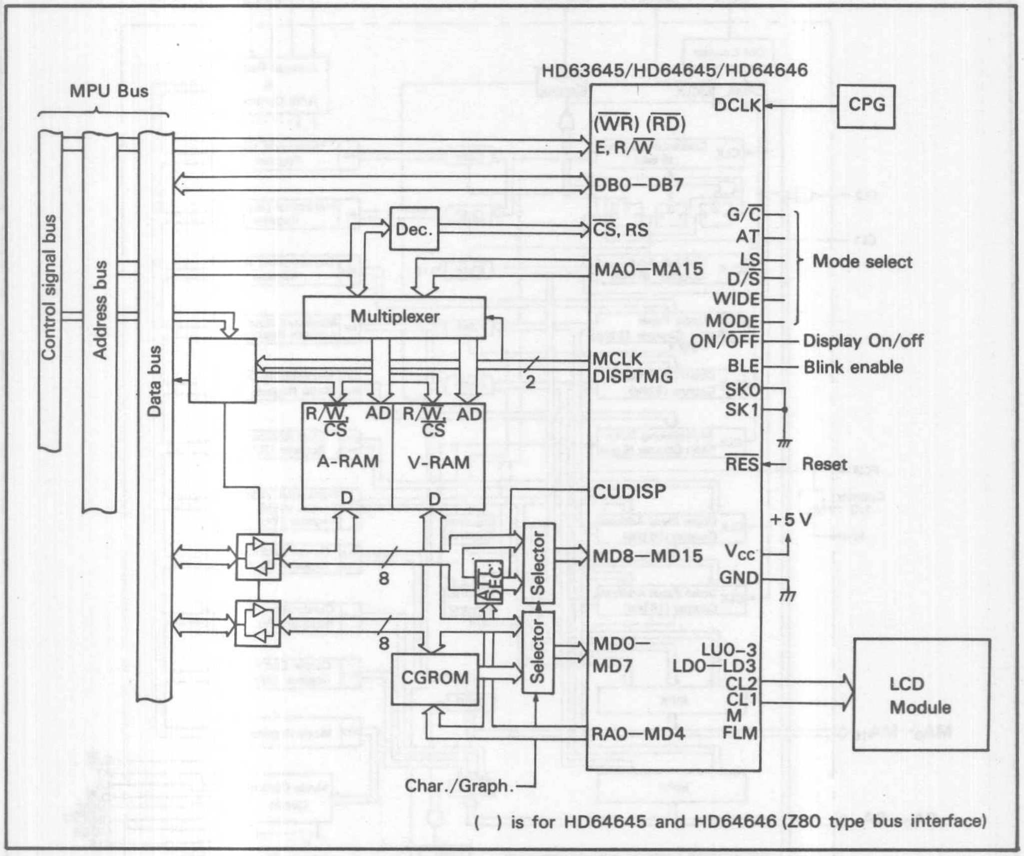
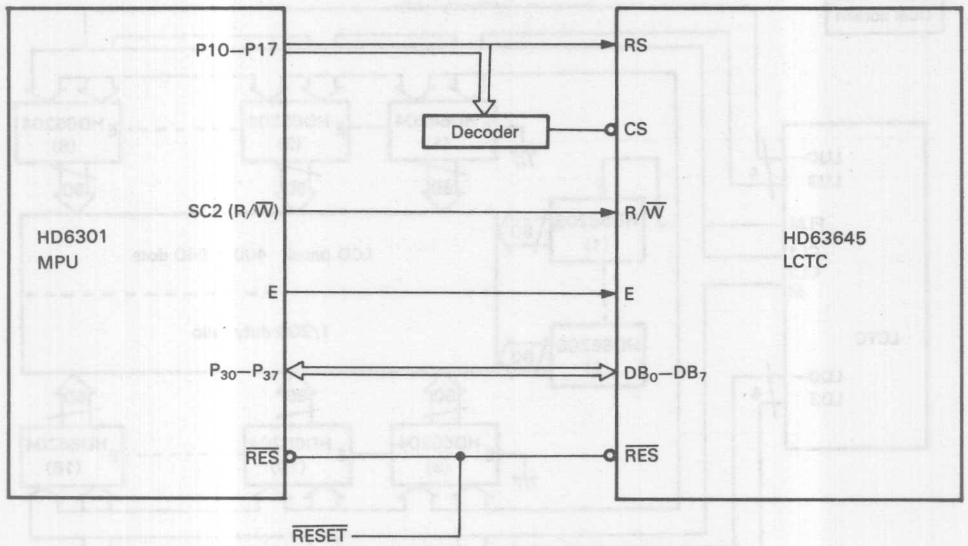


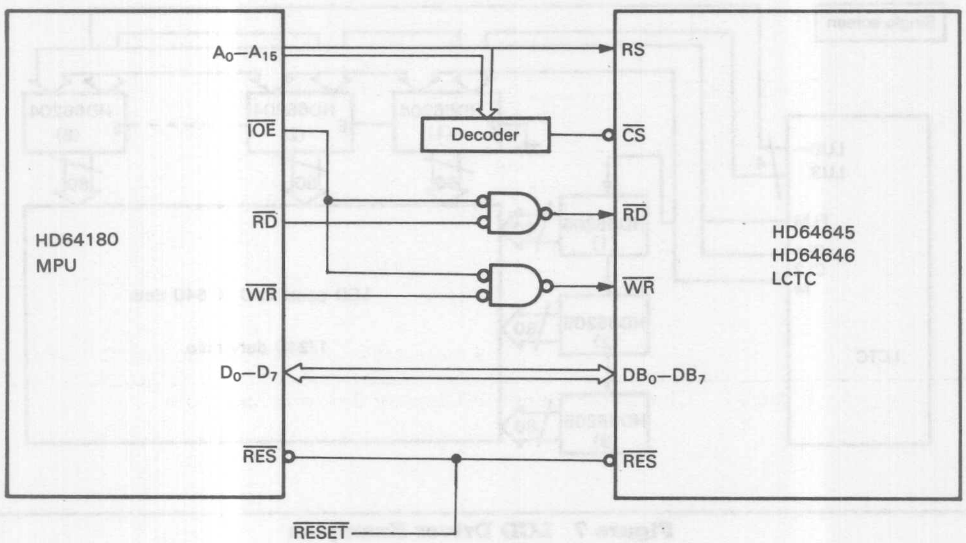
Figure 5 Character/Graphic Display System Example

Interface to MPU



Note: HD6301 is set in mode 5. P10—P17 are used as output ports, and P30—P37 as data buses. SC2 outputs R/$\overline{W}$ here.

Interface between HD6301 and HD63645



Note: In 80 family MPUs, I/O space is separate from memory space in software. Thus the LCTC, a part of I/O, needs the ORed signals of the interface signals and IOE. So $\overline{IOE}$ and $\overline{RD}$, and $\overline{IOE}$ and $\overline{WR}$ should be ORed to satisfy t_{AS}, the timing of $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$.

Interface between HD64180, HD64645 and HD64646

Figure 6 Interface to MPU

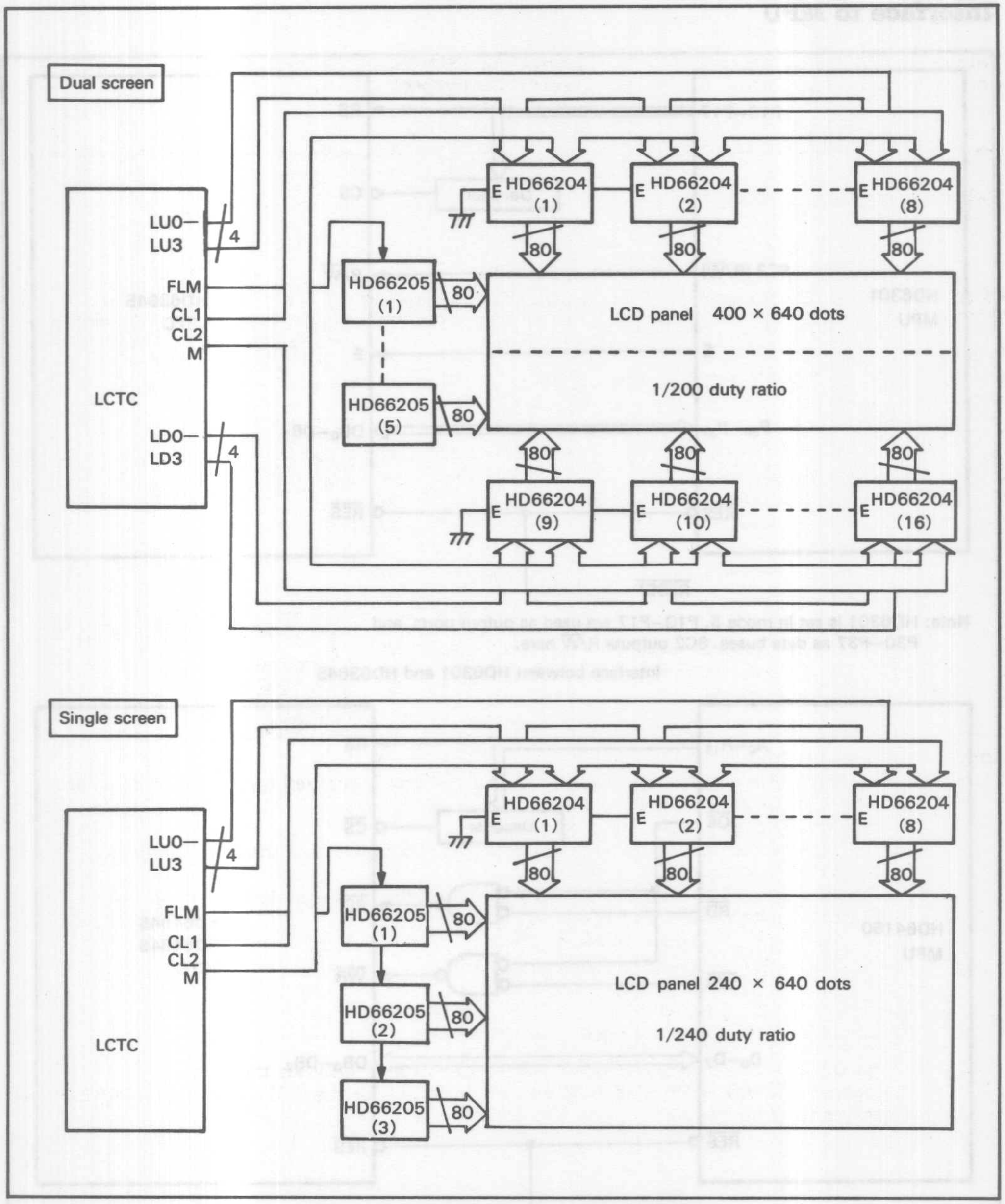


Figure 7 LCD Driver Examples

Registers

Table 4 shows the register mapping. Table 5 describes their function. Table 6 shows the differences between CRTC and LCTC registers.

Table 4 Registers Mapping

CS	RS	Address Register 4 3 2 1 0	Reg. no.	Register Name	Program Unit	Symbol	R/W	Data Bit 7	6	5	4	3	2	1	0
1	—	—————		Invalid	—	—	—								
0	0	—————	AR	Address Register	—	—	W								
0	1	0 0 0 0 0	R0	Horizontal Total Characters	Character[3]	Nht	W								
0	1	0 0 0 0 1	R1	Horizontal Displayed Char.s	Character	Nhd	W								
0	1	0 1 0 0 1	R9	Maximum Raster Address	Raster	Nr	W								
0	1	0 1 0 1 0	R10	Cursor Start Raster	Raster[4]	Ncs	W		B	P					
0	1	0 1 0 1 1	R11	Cursor End Raster	Raster	Nce	W								
0	1	0 1 1 0 0	R12	Start Address (H)	Memory Address	—	R/W								
0	1	0 1 1 0 1	R13	Start Address (L)	Memory Address	—	R/W								
0	1	0 1 1 1 0	R14	Cursor Address (H)	Memory Address	—	R/W								
0	1	0 1 1 1 1	R15	Cursor Address (L)	Memory Address	—	R/W								
0	1	1 0 0 1 0	R18	Horizontal Virtual Screen Width	Character	Nir	W								
0	1	1 0 0 1 1	R19	Multiplexing Duty Ratio (H)	Raster[3]	Ndh	W								
0	1	1 0 1 0 0	R20	Multiplexing Duty Ratio (L)	Raster[3]	Ndl	W								
0	1	1 0 1 0 1	R21	Display Start Raster	Raster	Nsr	W								
0	1	1 0 1 1 0	R22	Mode Register	—Note[5]	—	W				ON/OFF	G/C	WIDE	BLE	AT

Notes: 1. (shaded) : Invalid data bits

2. R/W indicates whether write access or read access is enabled to/from each register.
   W: Only write accessible
   R/W: Both read and write accessible
3. The "value to be specified minus 1" should be programmed in these registers: R0, R1 and R20.
4. Data bits 5 and 6 of cursor start register control the cursor status as shown below. (For more details, refer to page 27).

B	P	Cursor Blink Mode
0	0	Cursor on; without blinking
0	1	Cursor off
1	0	Blinking once every 32 frames
1	1	Blinking once every 64 frames

5. The OR of mode pin status and mode register data determines the mode.
6. Registers R2-R8, R16, and R17 are not assigned for the LCTC. Programming to these registers will be ignored.

Table 5 Internal Register Description

Reg. No.	Register Name	Size(Bits)	Description
AR	Address Register	5	Specifies the internal control registers (R0, R1, R9-R15, R18-R22) address to be accessed
R0	Horizontal Total Characters	8	Specifies the horizontal scanning period
R1	Horizontal Displayed Characters	8	Specifies the number of displayed characters per character row
R9	Maximum Raster Address	5	Specifies the number of rasters per character row, including the space between character rows
R10	Cursor Start Raster	5 + 2	Specifies the cursor start raster address and its blink mode
R11	Cursor End Raster	5	Specifies the cursor end raster address
R12 R13	Start Address (H) Start Address (L)	16	Specify the display start address
R14 R15	Cursor Address (H) Cursor Address (L)	16	Specify the cursor display address
R18	Horizontal Virtual Screen Width	8	Specifies the length of one row in memory space for horizontal scrolling
R19 R20	Multiplexing Duty Ratio (H) Multiplexing Duty Ratio (L)	9	Specify the number of rasters for one screen
R21	Display Start Raster	5	Specifies the display start raster within a character row for smooth scrolling
R22	Mode Register	5	Controls the display mode

Note: For more details of registers, refer to "Internal Registers".

Table 6 Internal Register Comparison between LCTC and CRTC

Reg. No.	LCTC HD63645/HD64645/HD64646	Comparison	CRTC HD6845
AR	Address Register	Equivalent to CRTC	Address Register
R0	Horizontal Total Characters		Horizontal Total Characters
R1	Horizontal Displayed Characters		Horizontal Displayed Characters
R2	—	Particular to CRTC ;	Horizontal Sync Position
R3		unnecessary for LCTC	Sync Width
R4			Vertical Total Characters
R5			Vertical Total Adjust
R6			Vertical Displayed Characters
R7			Vertical Sync Position
R8			Interlace and Skew
R9	Maximum Raster Address	Equivalent to CRTC	Maximum Raster Address
R10	Cursor Start Raster		Cursor Start Raster
R11	Cursor End Raster		Cursor End Raster
R12	Start Address (H)		Start Address (H)
R13	Start Address (L)		Start Address (L)
R14	Cursor Address (H)		Cursor (H)
R15	Cursor Address (L)		Cursor (L)
R16		Particular to CRTC ;	Light Pen (H)
R17		unnecessary for LCTC	Light Pen (L)
R18	Horizontal Virtual Screen Width	Additional registers for LCTC	
R19	Multiplexing Duty Ratio (H)		
R20	Multiplexing Duty Ratio (L)		
R21	Display Start Raster		
R22	Mode Register		

Functional Description

Programmable Screen Format

Figure 8 illustrates the relation between LCD display screen and registers. Figure 9 shows a timing chart of signals output from the LCTC in mode 5 as an example.

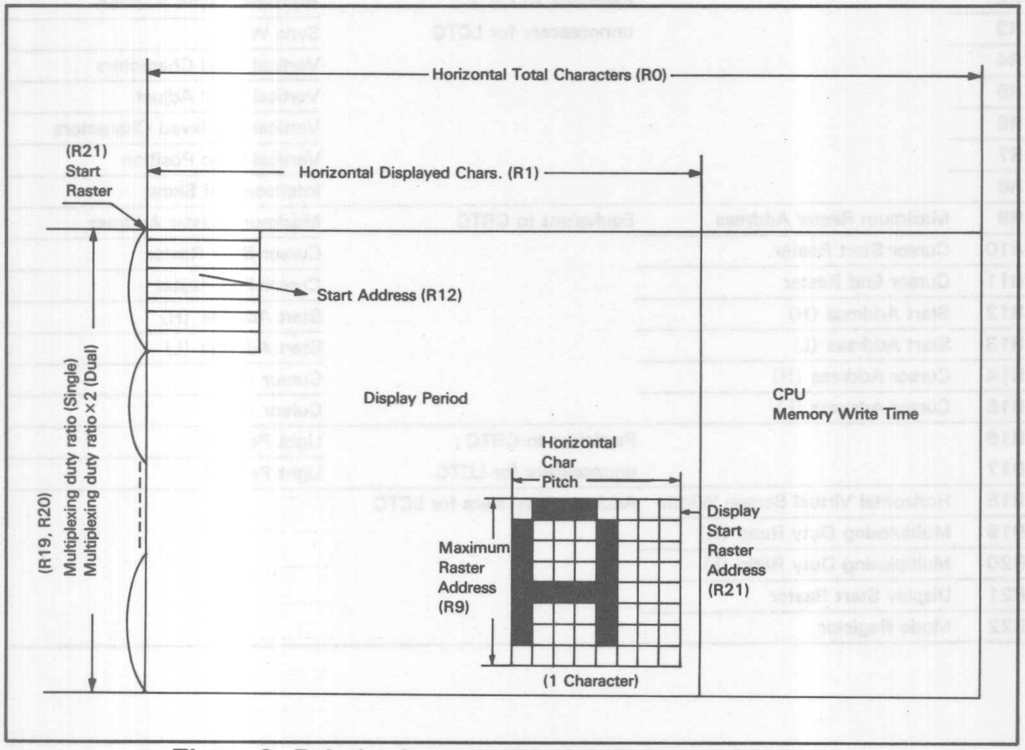
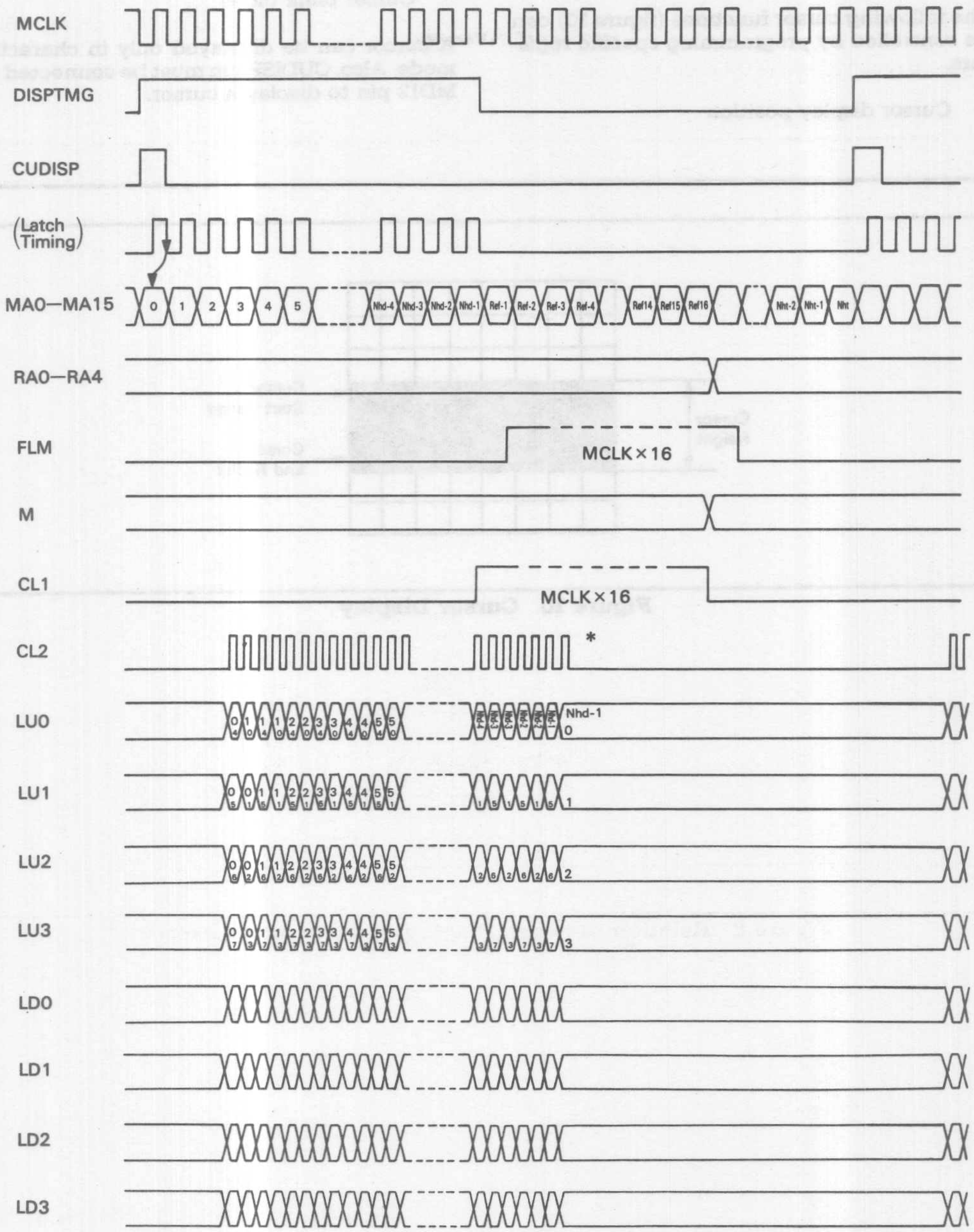


Figure 8 Relation between Display Screen and Registers



Note* : Relation between CL1 and CL2 in the case of HD64646 is differene from one shown in this chart. Refer to "Difference between HD64645 and HD64646".

Figure 9 LCTC Timing Chart (In Mode 5: Single Screen, 4-Bit Transfer, Normal Character Display)

Cursor Control

The following cursor functions (figure 10) can be controlled by programming specific registers.

- Cursor display position
- Cursor height
- Cursor blink mode

A cursor can be displayed only in character mode. Also, CUDISP pin must be connected to MD12 pin to display a cursor.

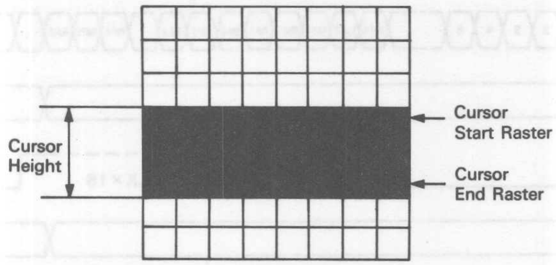


Figure 10 Cursor Display

Character Mode and Graphic Mode

The LCTC supports two types of display modes; character mode and graphic mode. Graphic mode 2 is provided to utilize software for a system using the CRTC (HD6845).

The display mode is controlled by an OR between the mode select pins (D/$\overline{S}$, G/$\overline{C}$, LS, WIDE, AT) and mode register (R22).

Character Mode: Character mode displays characters by using CG-ROM. The display data supplied from memory is accessed in 8-bit units. A variety of character attribute functions are provided, such as reverse video, blinking, nondisplay (white or black),by storing the attribute data in attribute RAM (A-RAM).

Figure 11 illustrates the relation between character display screen and memory contents.

Graphic Mode 1: Graphic mode 1 directly displays data stored in a graphic memory buffer. The display data supplied from memory is accessed in 16-bit units. Character attribute functions or wide mode are not provided. Figure 12 illustrates the relation between graphic display screen and memory contents.

Graphic Mode 2: Graphic mode 2 utilizes software for a system using the CRTC (HD6845). The display data supplied from memory is accessed in 16-bit units. Character attribute functions or wide mode are not provided. The same memory addresses are output repeatedly the number of times specified by maximum raster register (R9). The raster address is output in the same way as in character mode.

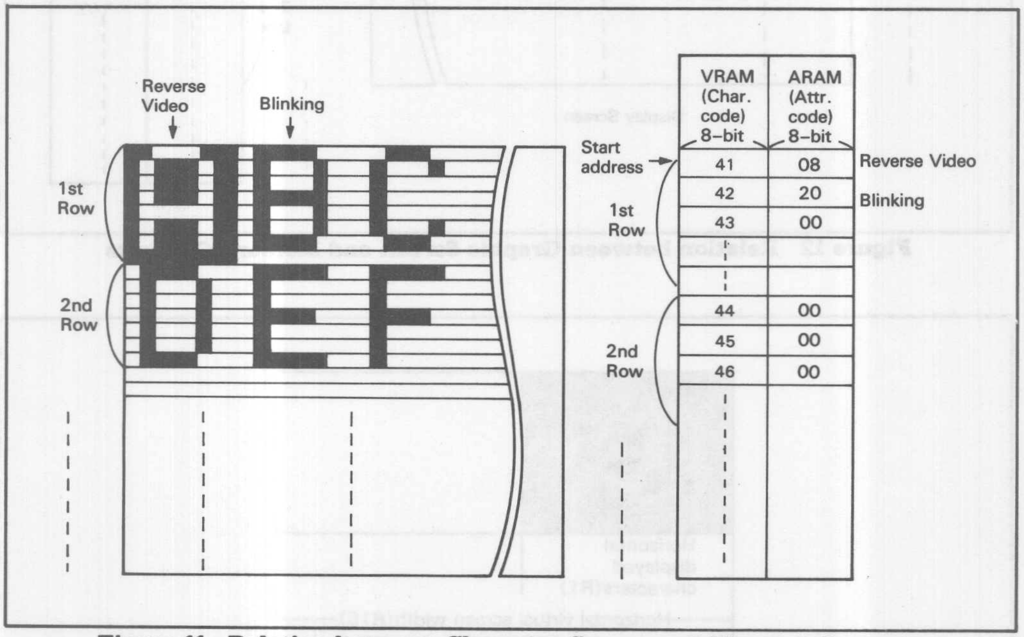


Figure 11 Relation between Character Screen and Memory Contents

Horizontal Virtual Screen Width

Horizontal virtual screen width can be specified by the character in addition to the number of horizontal displayed characters (figure 13).

The display screen can be scrolled in any direction by the character, by setting the horizontal virtual screen width and updating the start address. This function is enabled by programming the horizontal virtual screen width register (R18).

Figure 14 shows an example.

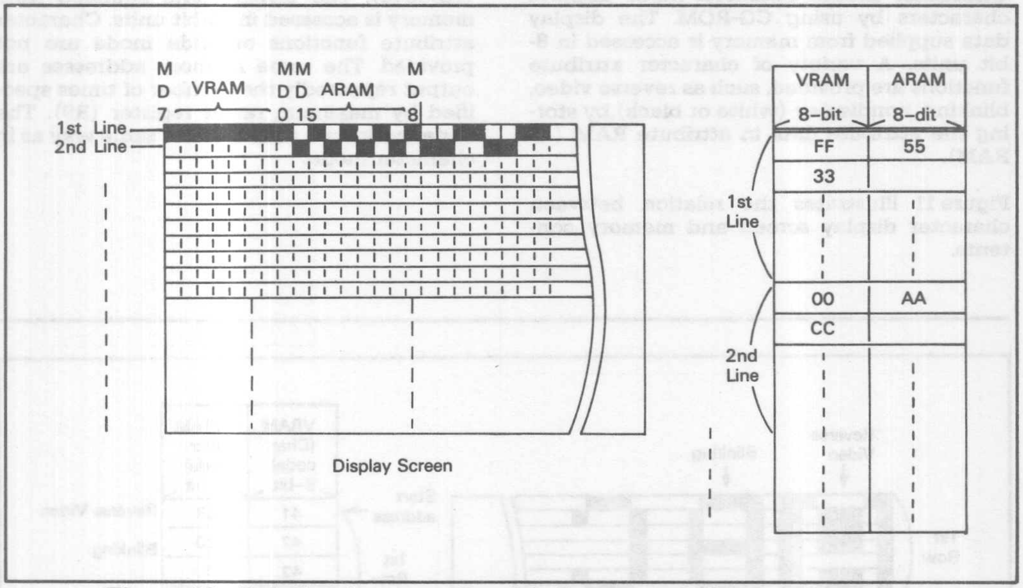


Figure 12 Relation between Graphic Screen and Memory Contents

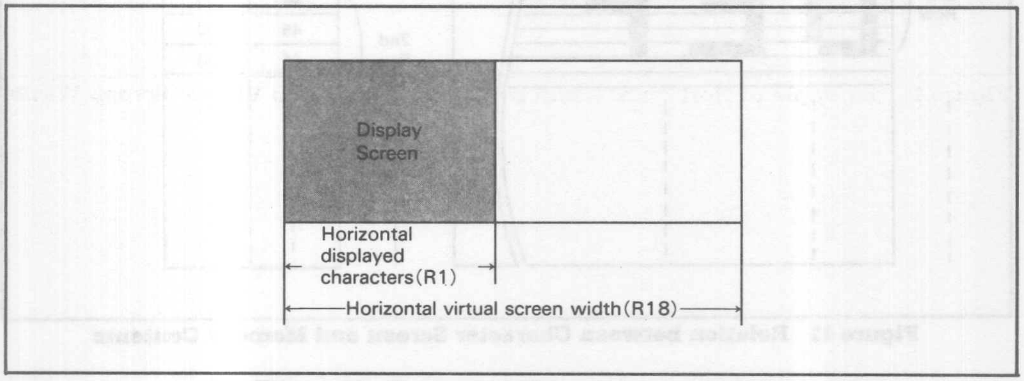


Figure 13 Horizontal Virtual Screen Width

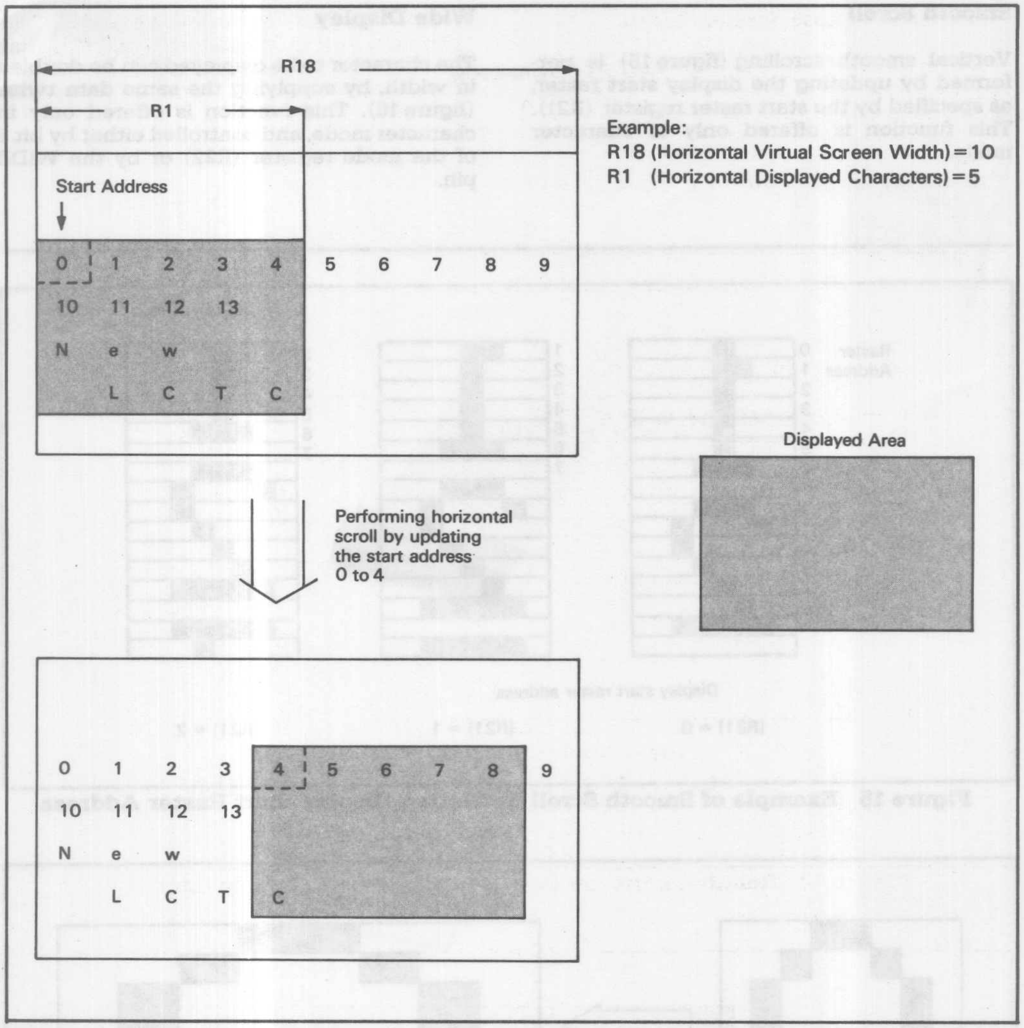


Figure 14 Example of Horizontal Scroll by Setting Horizontal Virtual Screen Width

Smooth Scroll

Vertical smooth scrolling (figure 15) is performed by updating the display start raster, as specified by the start raster register (R21). This function is offered only in character mode.

Wide Display

The character to be displayed can be doubled in width, by supplying the same data twice (figure 16). This function is offered only in character mode, and controlled either by bit 2 of the mode register (R22) or by the WIDE pin.

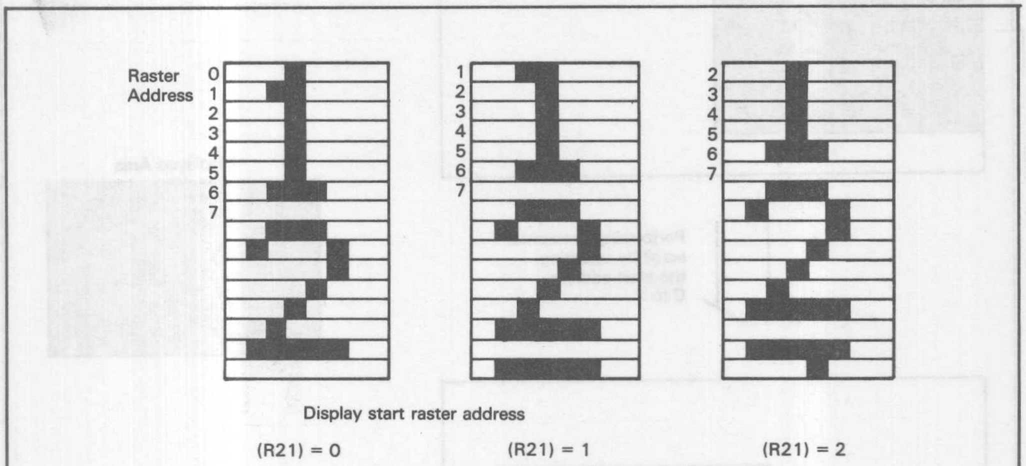


Figure 15 Example of Smooth Scroll by Setting Display Start Raster Address

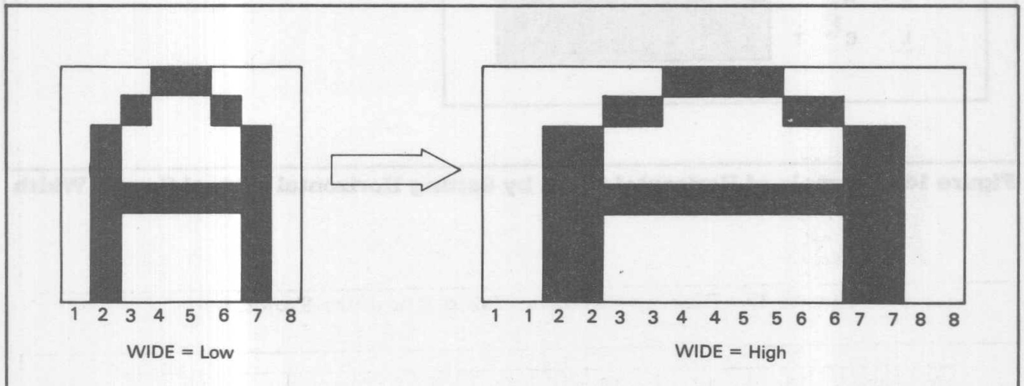


Figure 16 Example of Wide Display

Attribute Functions

A variety of character attribute functions such as reverse video, blinking, nondisplay (white) or nondisplay (black) can be implemented by storing the attribute data in A-RAM (attribute RAM). Figure 17 shows a display example using each attribute function.

The attribute functions are offered only in character mode, and controlled either by bit 0 of the mode register (R22) or the AT pin. As shown in figure 18, a character attribute can be specified by placing the character code on MD0-MD7, and the attribute code on MD11-MD15. MD8-MD10 are invalid.

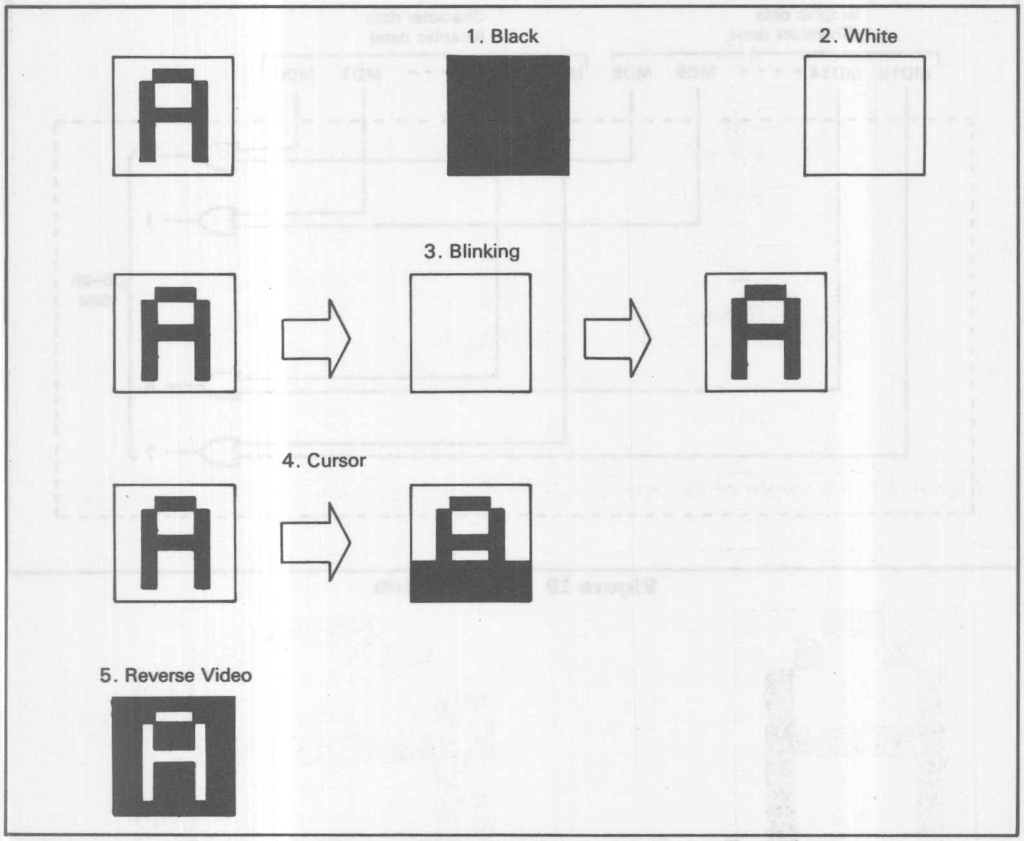


Figure 17 Display Example Using Attribute Functions

MD Input	15	14	13	12	11	10-8	7-0
Function	Non-display (black)	Non-display (white)	Blinking	Cursor	Reverse video	* * *	Character Code

* : Invalid

Figure 18 Attribute Code

OR Function—Superimposing Characters and Graphics

The OR function (figure 19) generates the OR of the data entered into MD0-MD7 (e.g. character data) and the data into MD8-MD15 (e.g. graphic data) in the LCTC and transfers this data as 1 byte.

This function is offered only in character mode, and controlled by bit 0 of the mode register (R22) or by the AT pin. Any attribute functions are disabled when using the OR function.

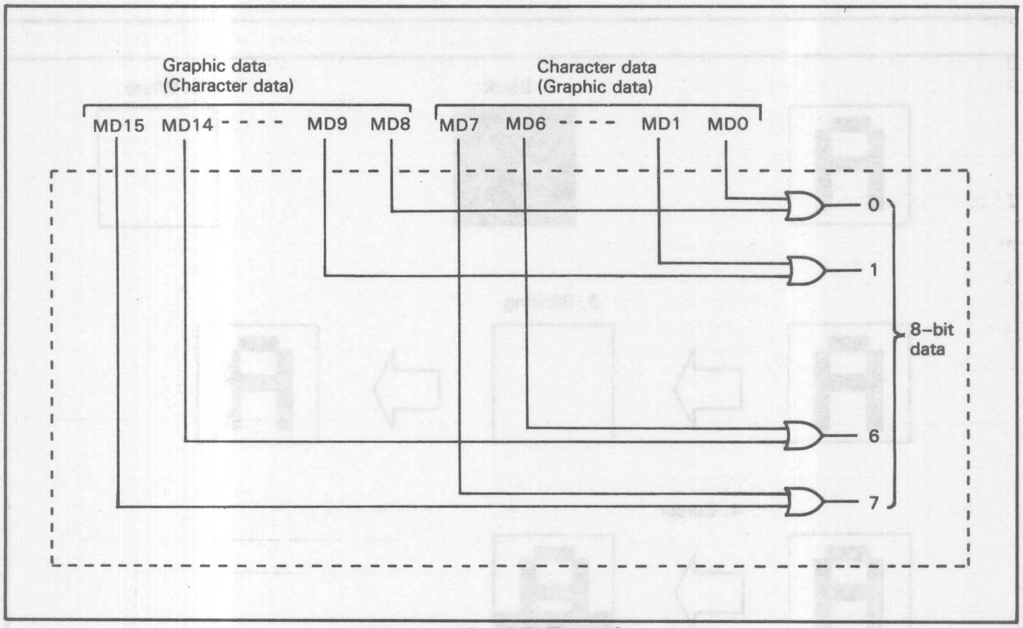


Figure 19 OR Function

DRAM Refresh Address Output Function

The LCTC outputs the address for DRAM refresh while CL1 is high, as shown in figure 20. The 16 refresh addresses per scanned line are output 16 times, from $00-$FF.

Skew Function

The LCTC can specify the skew (delay) for CUDISP, DISPTMG, CL2 outputs and MD inputs.

If buffer memory and character generator ROM cannot be accessed within one horizontal character display period, the access is retarded to the next cycle by inserting a latch to memory address output and buffer memory output. The skew function retards the CUDISP, DISPTMG, CL2 outputs, and MD inputs in the LCTC to match phase with the display data signal.

By utilizing this function, a low-speed memory can be used as a buffer RAM or a character generator ROM.

This function is controlled by pins SK0 and SK1 as shown in table 7.

Table 7 Skew Function

SK0	SK1	Skew Function
0	0	No skew
1	0	1 character time skew
0	1	2 character time skew
1	1	Inhibited combination

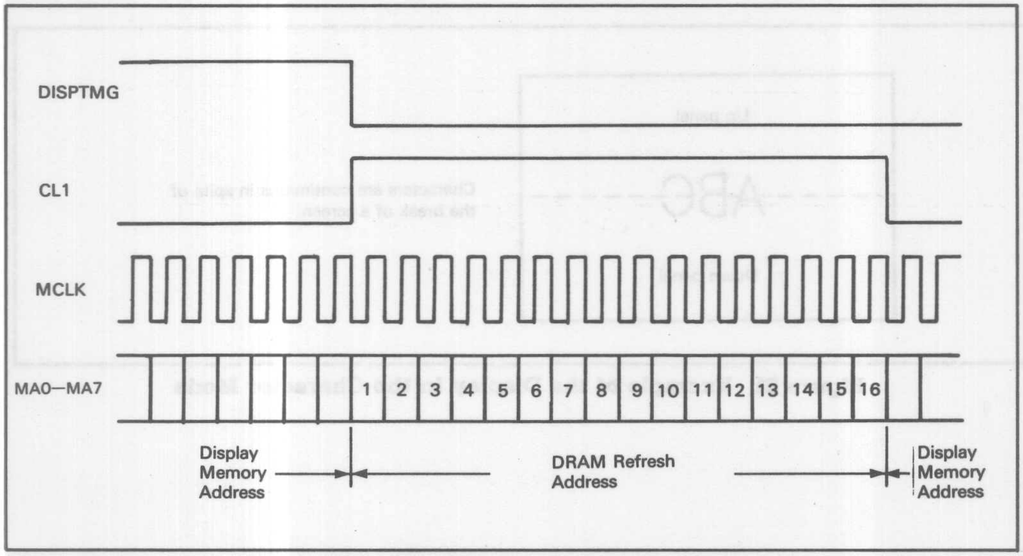


Figure 20 DRAM Refresh Address Output

Easy Mode

This mode utilizes software for systems using the CRTC (HD6845). By setting MODE pin to high, the display mode and screen format are fixed as shown in table 8. With this mode, software for a CRT screen can be utilized in a system using the LCTC, without changing the BIOS.

Automatic Correction of Down Panel Raster Address

When the LCTC mode is set for character display and dual screen, memory addresses (MA) and raster addresses (RA) are output in such a way as to keep continuity of a display spread over the two panels. Therefore users can use the LCTC without considering the multiplexing duty ratio (the number of vertical dots of a screen) or the character font. (See figure 21.)

Table 8 Fixed Values in Easy Mode

Reg. No.	Register Name	Fixed Value (decimal)
R9	Maximum raster address	7
R10	Cursor start raster	6
R11	Cursor end raster	7
R18	Horizontal virtual screen width	Same value as (R1)
R19	Multiplexing duty ratio (H)	99 (in dual screen mode)
R20	Multiplexing duty ratio (L)	199 (in single screen mode)
R21	Display start raster	0
R22	Mode register	0

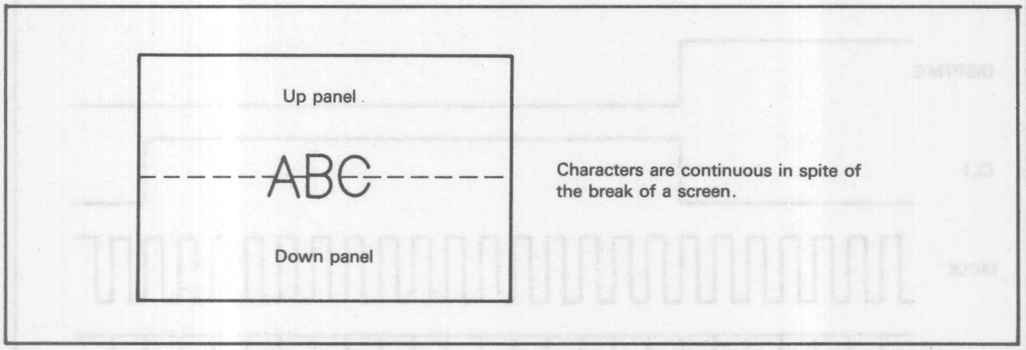


Figure 21 Example of the Display in the Character Mode

System Configuration and Mode Setting

LCD System Configuration

The screen configuration, single or dual, must be specified when using the LCD system (figure 22).

Using the single screen configuration, you can construct an LCD system with lower cost than a dual screen system, since the required number of column drivers is smaller and the manufacturing process for mounting them is simpler. However, there are some limitations, such as duty ratio, breakdown voltage of a driver, and display quality of the liquid crystal, in single screen configuration. Thus, a dual screen configuration may be more suitable to an application.

The LCTC also offers an 8-bit LCD data transfer function to support an LCD screen with a smaller interval of signal input terminals. For a general size LCD screen, such as 640 × 200 single, or 640 × 400 dual, the usual 4-bit LCD data transfer is satisfactory.

Hardware Configuration and Mode Setting

The LCTC supports the following hardware configurations:

- Single or dual screen configuration
- 4-or 8-bit LCD data transfer

and the following screen format:

- Character, graphic 1, or graphic 2 display
- Normal or wide display (only in character mode)
- OR or attribute display (only in character mode)

Also, the LCTC supports up to 40 Mbits/s of large screeen mode (mode 13) for large screen display. This mode is provided only in graphic 1 mode.

Table 9 shows the mode selection method according to hardware configuration and screen format. Table 10 shows how they are specified.

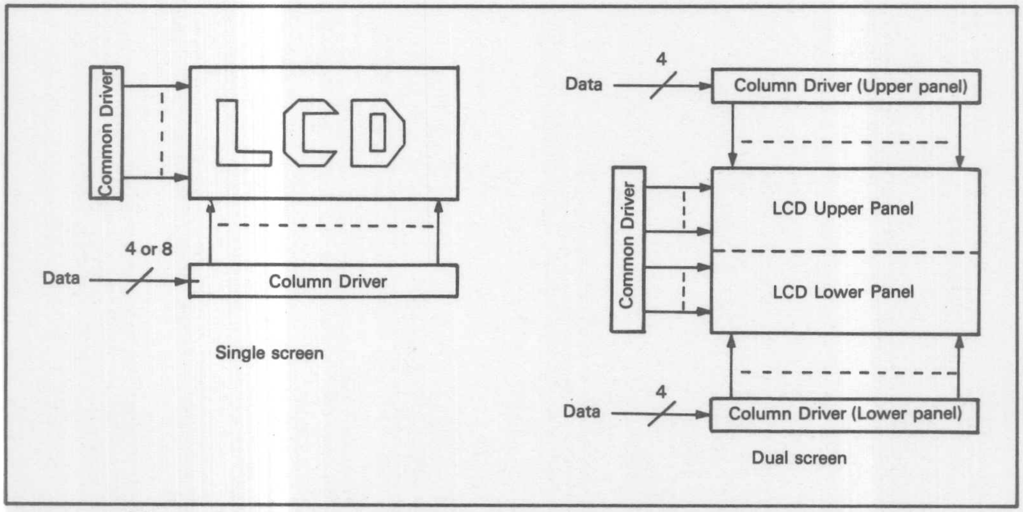


Figure 22 Hardware Configuration According to Screen Format

Table 9 Mode Selection

Hardware Configuration			Screen Format				
LCD Data Transfer	**Screen Configu-ration**	**Screen Size**	**Character/ Graphic**	**Normal/ Wide**	**Attribute/ OR**	**Maximum data transfer speed (Mbps)**	**Mode No.**
4-bit	Single	Normal	Character	Normal	AT / OR	20	5
				Wide	AT / OR	10	6
			Graphic 1			20	7
			Graphic 2			20	8
	Dual	Normal	Character	Normal	AT / OR	20	1
				Wide	AT / OR	10	2
			Graphic 1			20	3
			Graphic 2			20	4
		Large	Graphic 1			40	13
8-bit	Single	Normal	Character	Normal	AT / OR	20	9
				Wide	AT / OR	10	10
			Graphic 1			20	11
			Graphic 2			20	12

Note: Maximum data transfer speed indicates amount of the data read out of a memory. Thus, the data transfer speed sent to the LCD driver in wide function is 20 Mbps.

Mode List

Table 10 Mode List

No.	Mode Name	D/$\overline{S}$	G/$\overline{C}$	LS	WIDE	AT	Screen Config.	Graphic/ Character	Data Transfer	Wide Display	Attribute
1	Dual-screen character	1	0	0	0	0	Dual screen	Character	4-bit × 2	Normal	OR
		1	0	0	0	1					AT
2	Dual-screen wide character	1	0	0	1	0				Wide	OR
		1	0	0	1	1					AT
3	Dual-screen graphic 1	1	1	0	0	1		Graphic			
4	Dual-screen graphic 2	1	1	0	0	0					
5	Single-screen character	0	0	0	0	0	Single screen	Character	4-bit	Normal	OR
		0	0	0	0	1					AT
6	Single-screen wide character	0	0	0	1	0				Wide	OR
		0	0	0	1	1					AT
7	Single-screen graphic 1	0	1	0	0	1		Graphic		—	—
8	Single-screen graphic 2	0	1	0	0	0					
9	8-bit character	0	0	1	0	0	Single screen	Character	8-bit	Normal	OR
		0	0	1	0	1					AT
10	8-bit wide character	0	0	1	1	0				Wide	OR
		0	0	1	1	1					AT
11	8-bit graphic 1	0	1	1	0	1		Graphic		—	—
12	8-bit graphic 2	0	1	1	0	0					
13	Large screen	1	1	1	0	1	Dual screen		4-bit × 2		

The LCTC display mode is determined by pins D/$\overline{S}$ (pin 55), G/$\overline{C}$ (pin 58), LS (pin 56), WIDE (pin 54), and AT (pin 57). As for G/C, WIDE, and AT, the OR is taken between data bits 0, 2, and 3 of the mode register (R22). The display mode can be controlled by either one of the external pins or the data bits of R22.

Note: The above 5 pins have 32 status combinations (high and low). Any combinations other than the above are prohibited, because they may cause malfunctions. If you set an prohibited combination, set the right combination again.

Internal Registers

The HD63645/HD64645/HD64646 has one address register and fourteen data registers. In order to select one out of fourteen data registers, the address of the data register to be selected must be written into the address register. The MPU can transfer data to/from the data register corresponding to the written address.

To be software compatible with the CRTC (HD6845), registers R2-R8, R16, and R17, which are not necessary for an LCD are defined as invalid for the LCTC.

Address Register (AR)

AR register (figure 23) specifies one out of 14 data registers. Address data is written into the address register when RS is low. If no register corresponding to a specified address exists, the address data is invalid.

Horizontal Total Characters Register (R0)

R0 register (figure 24) specifies a horizontal scanning period. The total number of horizontal characters less 1 must be programmed into this 8-bit register in character units. Nht indicates the horizontal scanning period including the period when the CPU occupies memory (total number of horizontal characters minus the number of horizontal displayed characters). Its units are, then, converted from time into the number of characters. This value should be specified according to the specification of the LCD system to be used.

Note the following restrictions

$$\text{Nhd} + \frac{16}{m} \leq \text{Nht} + 1$$

Mode No.	**m**
5, 9	1
1, 6, 7, 8, 10, 11, 12, 13	2
2, 3, 4	4

Horizontal Displayed Characters Register (R1)

R1 register (figure 25) specifies the number of characters displayed per row. The horizontal character pitches are 8 bits for normal character display and 16 dots for wide character display and graphic display.

Nhd must be less than the total number of horizontal characters.

Maximum Raster Address Register (R9)

R9 register (figure 26) specifies the number of rasters per row in characters mode, consisting of 5 bits. The programmable range is 0 (1 raster/row) to 31 (32 rasters/row).

Cursor Start Raster Register (R10)

R10 register (figure 27) specifies the cursor start raster address and its blink mode. Refer to table 11.

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	—	W
—	—	—	Register address						

Figure 23 Address Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	Character	W
Nht (Total characters − 1)									

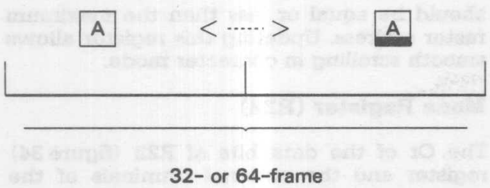
Figure 24 Horizontal Total Characters Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	Character	W
Nhd (Displayed characters)									

Figure 25 Horizontal Displayed Characters Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	Raster	W
—	—	—	Nr						

Figure 26 Maximum Raster Address Register



Cursor End Raster Register (R11)

R11 register (figure 28) specifies the cursor end raster address.

Start Address Register (H/L)(R12/R13)

R12/R13 register (figure 29) specifies a buffer memory read start address. Updating this register facilitates paging and scrolling. R14/R15 register can be read and written to/from the MPU.

Cursor Address Register (H/L)(R14/R15)

R14/R15 register (figure 30) specifies a cursor display address. Cusor display requires setting R10 and R11, and CUDISP should be connected with MD12 (in character mode). This register can be read from and written to the MPU.

Table 11 Cursor Blink Mode

B	P	Cursor blink mode
0	0	Cursor on; without blinking
0	1	Cursor off
1	0	Blinking once every 32 frames
1	1	Blinking once every 64 frames

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	B	P	Ncs (Raster address)					Raster	W

Figure 27 Cursor Start Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Nce (Raster address)					Raster	W

Figure 28 Cursor End Raster Register

Horizontal Virtual Screen Width Register (R18)

R18 register (figure 31) specifies the memory width to determine the start address of the next row. By using this register, memory width can be specified larger than the number of horizontal displayed characters. Updating the display start address facilitates scrolling in any direction within a memory space.

The start address of the next row is that of the previous row plus Nir. If a larger memory width than display width is unnecessary, Nir should be set equal to the number of horizontal displayed characters.

Multiplexing Duty Ratio Register (H/L) (R19/R20)

R19/R20 register (figure 32) specifies the number of vertical dots of the display screen. The programmed value differs according to the LCD screen configuration.

In single screen configuration :

(Programmed value) = (Number of vertical dots) − 1.

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Memory address (H) (R12)								Memory address	R/W
Memory address (L) (R13)									

Figure 29 Start Address Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Memory address (H) (R14)								Memory address	R/W
Memory address (L) (R15)									

Figure 30 Cursor Address Register

In dual screen configuration :

$$(\text{Programmed value}) = \frac{(\text{Number of vertical dots})}{2} - 1$$

Display Start Raster Register (R21)

R21 register (figure 33) specifies the start raster of the character row displayed on the top of the screen. The programmed value should be equal or less than the maximum raster address. Updating this register allows smooth scrolling in character mode.

Mode Register (R22)

The Or of the data bits of R22 (figure 34) register and the external terminals of the same name determines a particular mode. (figure 35)

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Nir (No. of chars. of virtual width)								Character	W

Figure 31 Horizontal Virtual Screen Width Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	—	—	—	— (R19)	Ndh*	Raster	W
Ndl (Number of rasters − 1) (R20)									

* : Number of rasters

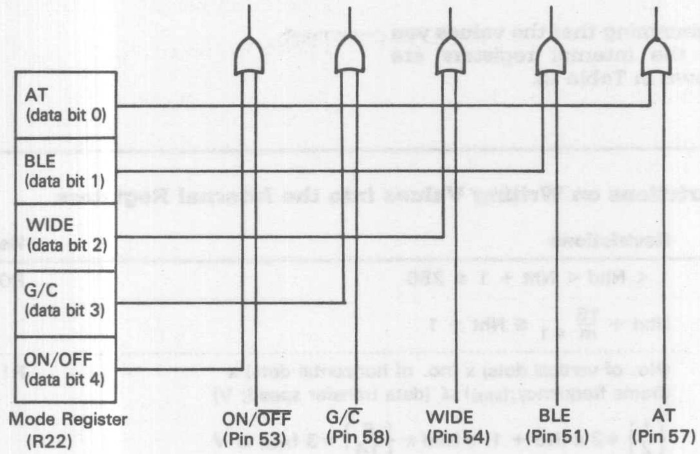
Figure 32 Multiplexing Duty Ratio Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
			Raster address					Raster	W

Figure 33 Display Start Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	ON/OFF	G/C	WIDE	BLE	AT	—	W

Figure 34 Mode Register



Notes:
1. AT (valid only when G/$\overline{\text{C}}$ is low (character mode))
   AT = High: Attribute functions enabled, OR function disabled.
   AT = Low: OR function enabled, attribute functions disabled.
2. BLE (valid only when G/$\overline{\text{C}}$ is low (character mode))
   BLE = High: Blinking enable on the character specified by attribute RAM
   BLE = Low: No blinking
3. WIDE (valid only when G/$\overline{\text{C}}$ is low (character mode))
   WIDE = High: Wide display enabled
   WIDE = Low: Normal display
4. G/$\overline{\text{C}}$
   G/C = High: Graphic 1 display (when AT = Low) or Graphic 2 display (when AT = High)
   G/C = Low: Character display
5. ON/$\overline{\text{OFF}}$
   ON/$\overline{\text{OFF}}$ = High: Display on state
   ON/$\overline{\text{OFF}}$ = Low: Display off state

Figure 35 Correspondence between Mode Register and External Pins

Restrictions on Programming Internal Registers

Note when programming that the values you can write into the internal registers are restricted as shown in Table 12.

Table 12 Restrictions on Writing Values into the Internal Registers

Function	Restrictions	Register
Display Format	$1 < Nhd < Nht + 1 \leqq 256$	R0, R1
	$Nhd + \frac{16}{m} *1 \leqq Nht + 1$	
	(No. of vertical dots) x (no. of horizontal dots) x (frame frequency; f_{FRM}) $\leqq$ (data transfer speed; V)	R1, R19, R20
	$\left\{ \begin{matrix} 1 \\ 2 \end{matrix} \right\} *2 \times (Nd + 1) \times Nhd \times \left\{ \begin{matrix} 8 \\ 16 \end{matrix} \right\} *3\ f_{FRM} \leqq V$	
	$Nhd \leqq Nir$	R1, R18
	$0 \leqq Nd \leqq 511$	R19, R20
Cursor Control	$0 \leqq Ncs \leqq Nce$	R10, R11
	$Nce \leqq Nr$	R10, R9
Smooth Scroll	$Nsr \leqq Nr$	R21, R9
Memory Width Set	$0 \leqq Nir \leqq 255$	R18

Notes' *1 m varies according to the modes. See the following table.

Mode No.	m
5,9	1
1,6,7,8,10,11,12,13	2
2,3,4	4

*2 Set 1 when an LCD screen is a single screen, and set 2 when dual. Modes are classified as shown in the following table.

Mode No.	Value
5,6,7,8,9,10,11,12	1
1,2,3,4,13	2

*3 Set 8 when a character is constructed with 8 dots, and set 16 when with 16 dots. Modes are classified as shown in the following table.

Mode No.	Value
1,5,9	8
2,3,4,6,7,8,10,11,12,13	16

Reset

$\overline{\text{RES}}$ pin determines the internal state of LSI counters and the like. This pin does not affect register contents nor does it basically control output terminals.

Reset is defined as follows (Figure 36):

- At reset: the time when $\overline{\text{RES}}$ goes low
- During reset: the period while $\overline{\text{RES}}$ remains low
- After reset: the period on and after the $\overline{\text{RES}}$ transition from low to high
- Make sure to hold the reset signal low for at least 1 μs

$\overline{\text{RES}}$ pin should be pulled high by users during operation.

Reset State of Pins

$\overline{\text{RES}}$ pin does not basically control output pins, and operates regardless of other input pins.

1. Preserve states before reset: LU0-LU3, LD0-LD3, FLM, CL1, RA0-RA4
2. Fixed at high level: MLCK
3. Preserve states before reset or fixed at low level according to the timing when the reset signal is input: DISPTMG, CUDISP, MA0-MA15
4. Fixed at high or low according to mode: CL2
5. Unaffected: DB_0-DB_7

Reset State of Registers

$\overline{\text{RES}}$ pin does not affect register contents. Therefore, registers can be read or written even during a reset state; their contents will be preserved regardless of reset until they are rewritten to.

Notes for HD63645/HD64645/HD64646

1. The HD63645/HD64645/HD64646 are CMOS LSIs, and it should be noted that input pins must not be left disconnected, etc.
2. At power-on, the state of internal registers becomes undefined. The LSI operation is undefined until all internal registers have been programmed.

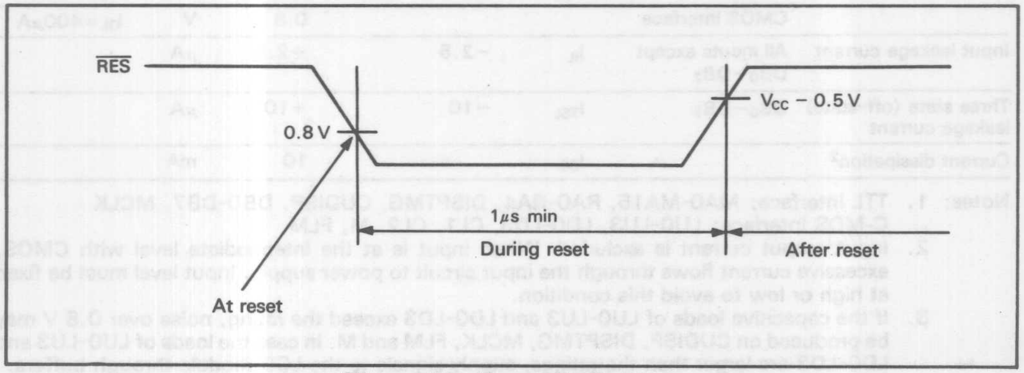


Figure 36 Reset Definition

Absolute Maximum Ratings

Item	Symbol	Value	Note
Supply voltage	V_{CC}	−0.3 to +7.0 V	2
Terminal voltage	V_{in}	−0.3 to V_{CC} +0.3 V	2
Operating temperature	T_{opr}	−20°C to +75°C	
Storage temperature	T_{stg}	−55°C to +125°C	

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ±10%, GND = 0 V, Ta = −20°C to +75°C). If these conditions are exceeded, it could affect reliability of LSI.

2. With respect to ground (GND = 0 V)

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0 V ±10%, GND = 0 V, T_a = −20°C to +75°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	RES, MODE, SK0, SK1	V_{IH}	V_{CC}−0.5		V_{CC}+0.3	V	
	DCLK, ON/OFF		2.2		V_{CC}+0.3	V	
	All others		2.0		V_{CC}+0.3	V	
Input low voltage	All others	V_{IL}	−0.3		0.8	V	
Output high voltage	TTL interface[1]	V_{OH}	2.4			V	I_{OH}=−400μA
	CMOS interface[1]		V_{CC}−0.8			V	I_{OH}=−400μA
Output low voltage	TTL interface	V_{OL}			0.4	V	I_{OL}=1.6mA
	CMOS interface				0.8	V	I_{OL}=400μA
Input leakage current	All inputs except DB_0-DB_7	I_{IL}	−2.5		+2.5	μA	
Three state (off-state) leakage current	DB_0-DB_7	I_{TSL}	−10		+10	μA	
Current dissipation[2]		I_{CC}			10	mA	

Notes: 1. TTL Interface; MA0-MA15, RA0-RA4, DISPTMG, CUDISP, DB0-DB7, MCLK
C-MOS Interface; LU0-LU3, LD0-LD3, CL1, CL2, M, FLM

2. Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to power supply. Input level must be fixed at high or low to avoid this condition.

3. If the capacitive loads of LU0-LU3 and LD0-LD3 exceed the rating, noise over 0.8 V may be produced on CUDISP, DISPTMG, MCLK, FLM and M. In case the loads of LU0-LU3 and LD0-LD3 are larger than the ratings, supply signals to the LCD module through buffers.

AC Characteristics

CPU Interface (HD63645 —— 68 family)
(V_{CC} = 5.0 V ± 10 %, GND = 0 V, T_a = −20 °C to + 75 °C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Figure
Enable cycle time	t_{CYCE}	500			ns	37
Enable pulse width (high)	P_{WEH}	220			ns	
Enable pulse width (low)	P_{WEL}	220			ns	
Enable rise time	t_{Er}			25	ns	
Enable fall time	t_{Ef}			25	ns	
$\overline{CS}$, RS, R/$\overline{W}$ setup time	t_{AS}	70			ns	
$\overline{CS}$, RS, R/$\overline{W}$ hold time	t_{AH}	10			ns	
DB_0-DB_7 setup time	t_{DS}	60			ns	
DB_0-DB_7 hold time	t_{DHW}	10			ns	
DB_0-DB_7 output delay time	t_{DDR}			150	ns	
DB_0-DB_7 output hold time	t_{DHR}	20			ns	

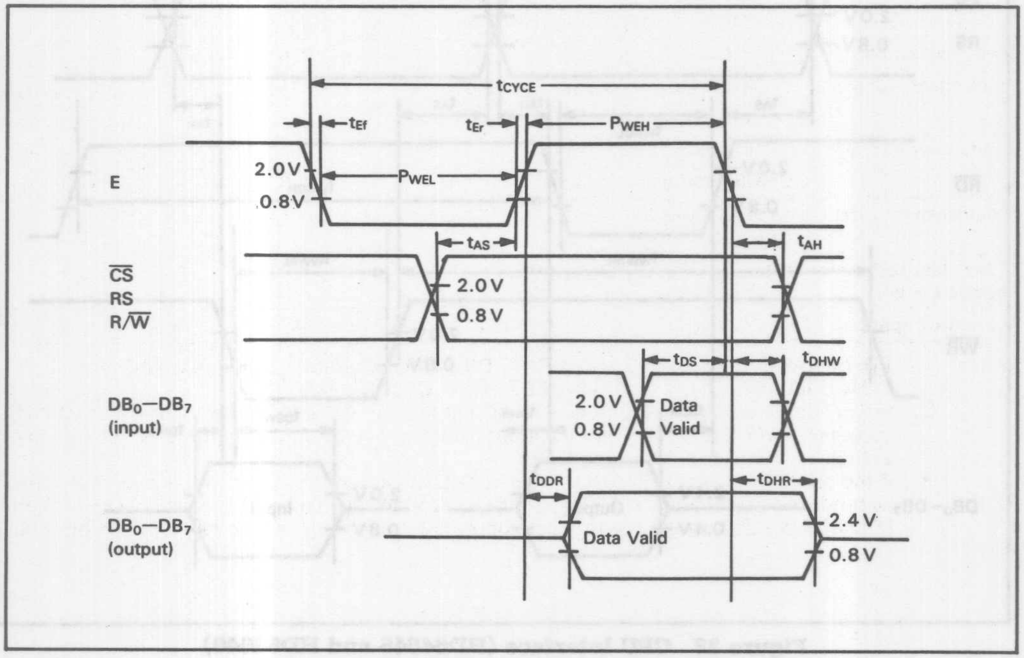


Figure 37 CPU Interface (HD63645)

CPU Interface (HD64645 and HD64646 —— 80 family)
(V_{CC} = 5.0 V ± 10 %, GND = 0 V, T_a = −20 °C to + 75 °C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Figure
$\overline{RD}$ high level width	t_{WRDH}	190			ns	38
$\overline{RD}$ low level width	t_{WRDL}	190			ns	
$\overline{WR}$ high level width	t_{WWRH}	190			ns	
$\overline{WR}$ low level width	t_{WWRL}	190			ns	
$\overline{CS}$, RS setup time	t_{AS}	0			ns	
$\overline{CS}$, RS hold time	t_{AH}	0			ns	
DB_0-DB_7 setup time	t_{DSW}	100			ns	
DB_0-DB_7 hold time	t_{DHW}	0			ns	
DB_0-DB_7 output delay time	t_{DDR}			150	ns	
DB_0-DB_7 output hold time	t_{DHR}	20			ns	

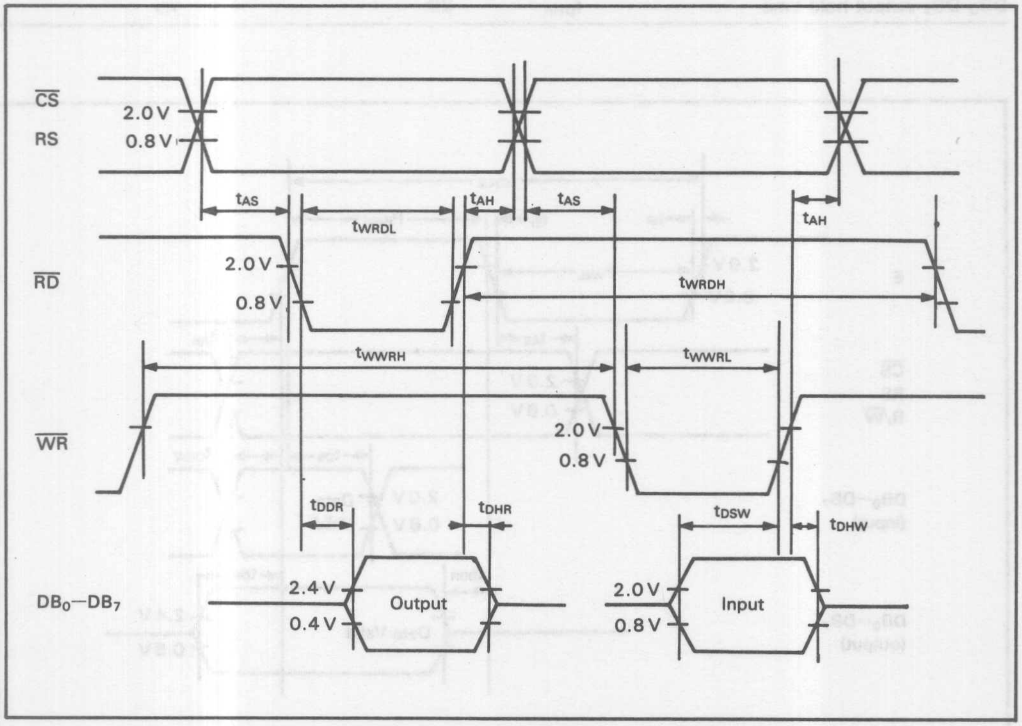


Figure 38 CPU Interface (HD64645 and HD64646)

AC Characteristics (Cont)

Memory Interface
(V_{CC} = 5.0 V ± 10 %, GND = 0 V, T_a = −20 °C to + 75 °C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Figure
DCLK cycle time	t_{CYCD}	100	—	—	ns	39
DCLK high level width	t_{WDH}	30	—	—	ns	
DCLK low level width	t_{WDL}	30	—	—	ns	
DCLK rise time	t_{Dr}	—	—	20	ns	
DCLK fall time	t_{Df}	—	—	20	ns	
MCLK delay time	t_{DMD}	—	—	60	ns	
MCLK rise time	t_{Mr}	—	—	30	ns	
MCLK fall time	t_{Mf}	—	—	30	ns	
MA0-MA15 delay time	t_{MAD}	—	—	150	ns	
MA0-MA15 hold time	t_{MAH}	10	—	—	ns	
RA0-RA4 delay time	t_{RAD}	—	—	150	ns	
RA0-RA4 hold time	t_{RAH}	10	—	—	ns	
DISPTMG delay time	t_{DTD}	—	—	150	ns	
DISPTMG hold time	t_{DTH}	10	—	—	ns	
CUDISP delay time	t_{CDD}	—	—	150	ns	
CUDISP hold time	t_{CDH}	10	—	—	ns	
CL1 delay time	t_{CL1D}	—	—	150	ns	
CL1 hold time	t_{CL1H}	10	—	—	ns	
CL1 rise time	t_{CL1r}	—	—	50	ns	
CL1 fall time	t_{CL1f}	—	—	50	ns	
MD0-MD15 setup time	t_{MDS}	30	—	—	ns	
MD0-MD15 hold time	t_{MDH}	15	—	—	ns	

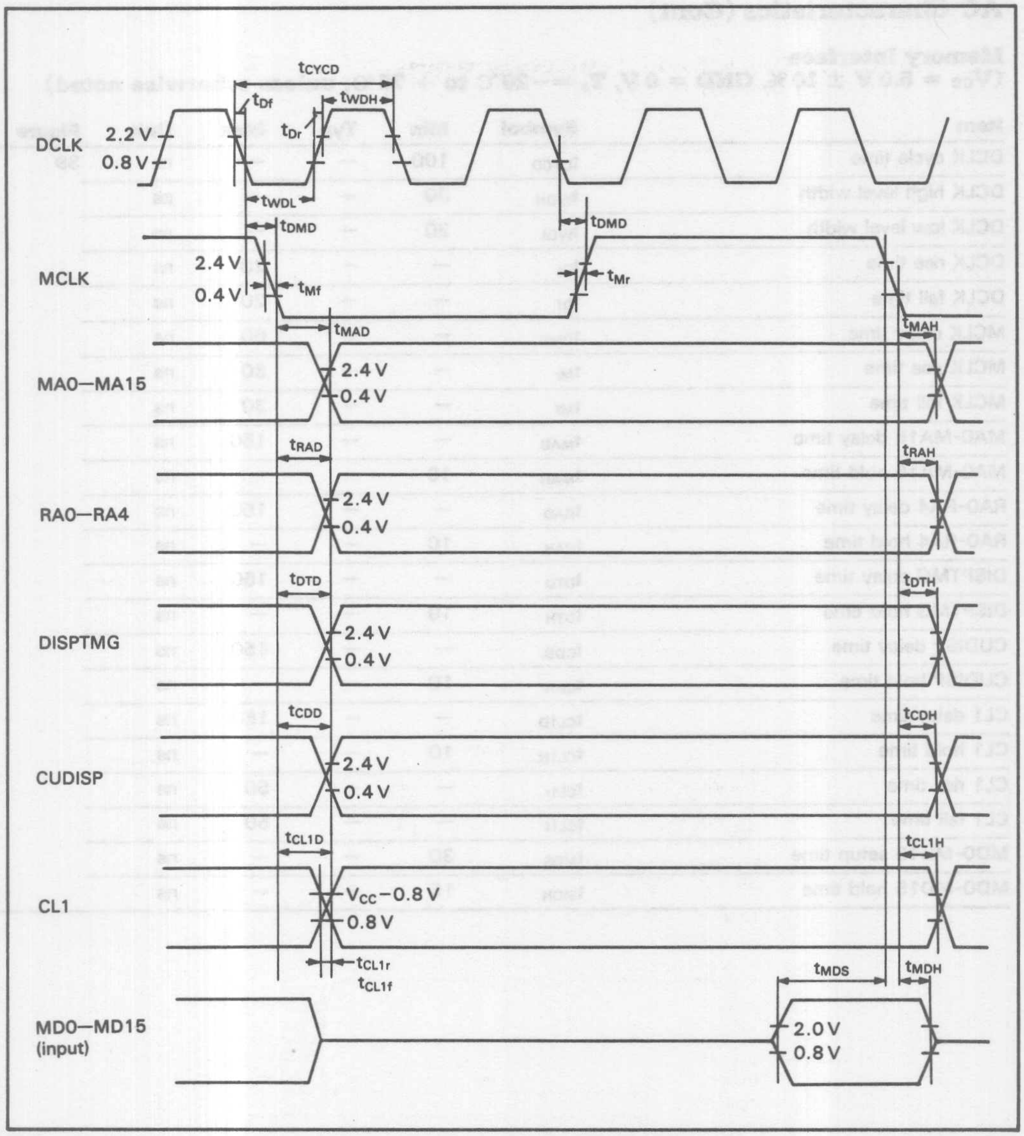


Figure 39 Memory Interface

AC Characteristics (Cont)

LCD Interface 1 (HD63645 and HD64645)
(V_{CC} = 5.0 V ± 10 %, GND = 0 V, T_a = −20 ℃ to + 75 ℃)

Item	Symbol	Min	Typ	Max	Unit	Figure
Display data setup time	t_{LDS}	50	—	—	ns	40
Display data hold time	t_{LDH}	100	—	—	ns	
CL2 high level width	t_{WCL2H}	100	—	—	ns	
CL2 low level width	t_{WCL2L}	100	—	—	ns	
FLM setup time	t_{FS}	500	—	—	ns	
FLM hold time	t_{FH}	300	—	—	ns	
CL1 rise time	t_{CL1r}	—	—	50	ns	
CL1 fall time	t_{CL1f}	—	—	50	ns	
CL2 rise time	t_{CL2r}	—	—	50	ns	
CL2 fall time	t_{CL2f}	—	—	50	ns	

Note : At fCL2 = 3 MHz

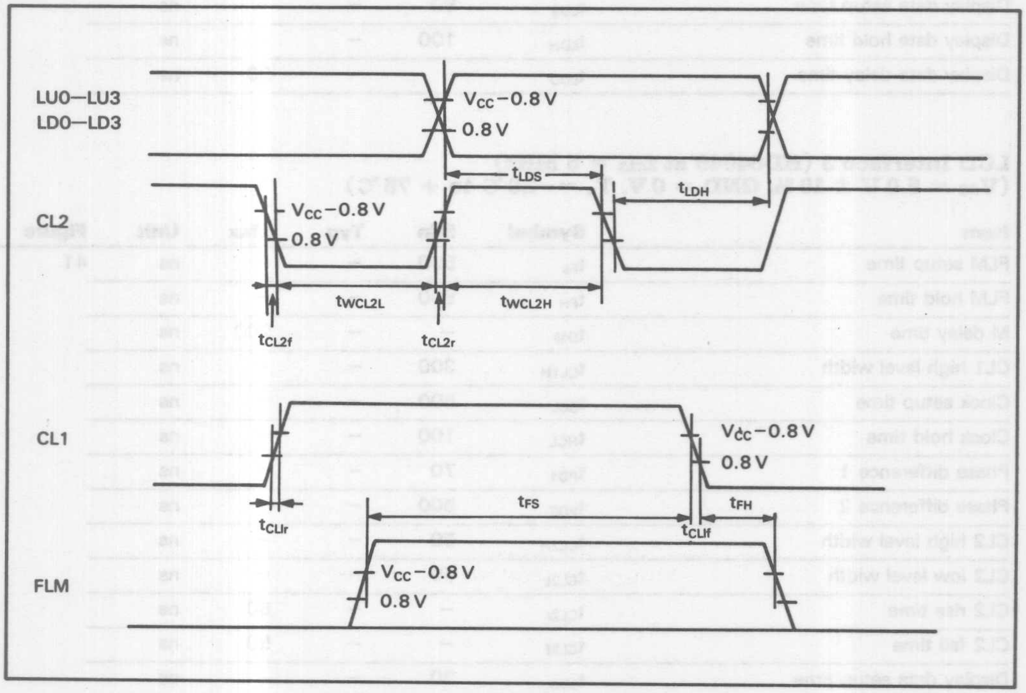


Figure 40 LCD Interface

AC Characteristics (Cont)

LCD Interface 2 (HD64646 at f_{CL2} = 3 MHz)
(V_{CC} = 5.0 V ± 10 %, GND = 0 V, T_a = −20 °C to + 75 °C)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM stetup time	t_{Fs}	500	–	–	ns	41
FLM hold time	t_{FH}	300	–	–	ns	
M delay time	t_{DM}	–	–	200	ns	
CL1 high level width	t_{CL1H}	300	–	–	ns	
Clock setup time	t_{SCL}	500	–	–	ns	
Clock hold time	t_{HCL}	100	–	–	ns	
Phase difference 1	t_{PD1}	100	–	–	ns	
Phase difference 2	t_{PD2}	500	–	–	ns	
CL2 high level width	t_{CL2H}	100	–	–	ns	
CL2 low level width	t_{CL2L}	100	–	–	ns	
CL2 rise time	t_{CL2r}	–	–	50	ns	
CL2 fall time	t_{CL2f}	–	–	50	ns	
Display data setup time	t_{LDS}	80	–	–	ns	
Display data hold time	t_{LDH}	100	–	–	ns	
Display data delay time	t_{LDD}	–	–	30	ns	

LCD Interface 3 (HD64646 at f_{CL2} = 5 MHz)
(V_{CC} = 5.0 V ± 10 %, GND = 0 V, T_a = −20 °C to + 75 °C)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM setup time	t_{Fs}	500	–	–	ns	41
FLM hold time	t_{FH}	500	–	–	ns	
M delay time	t_{DM}	–	–	200	ns	
CL1 high level width	t_{CL1H}	300	–	–	ns	
Clock setup time	t_{SCL}	500	–	–	ns	
Clock hold time	t_{HCL}	100	–	–	ns	
Phase difference 1	t_{PD1}	70	–	–	ns	
Phase difference 2	t_{PD2}	500	–	–	ns	
CL2 high level width	t_{CL2H}	50	–	–	ns	
CL2 low level width	t_{CL2L}	50	–	–	ns	
CL2 rise time	t_{CL2r}	–	–	50	ns	
CL2 fall time	t_{CL2f}	–	–	50	ns	
Display data setup time	t_{LDS}	30	–	–	ns	
Display data hold time	t_{LDH}	30	–	–	ns	
Display data delay time	t_{LDD}	–	–	30	ns	

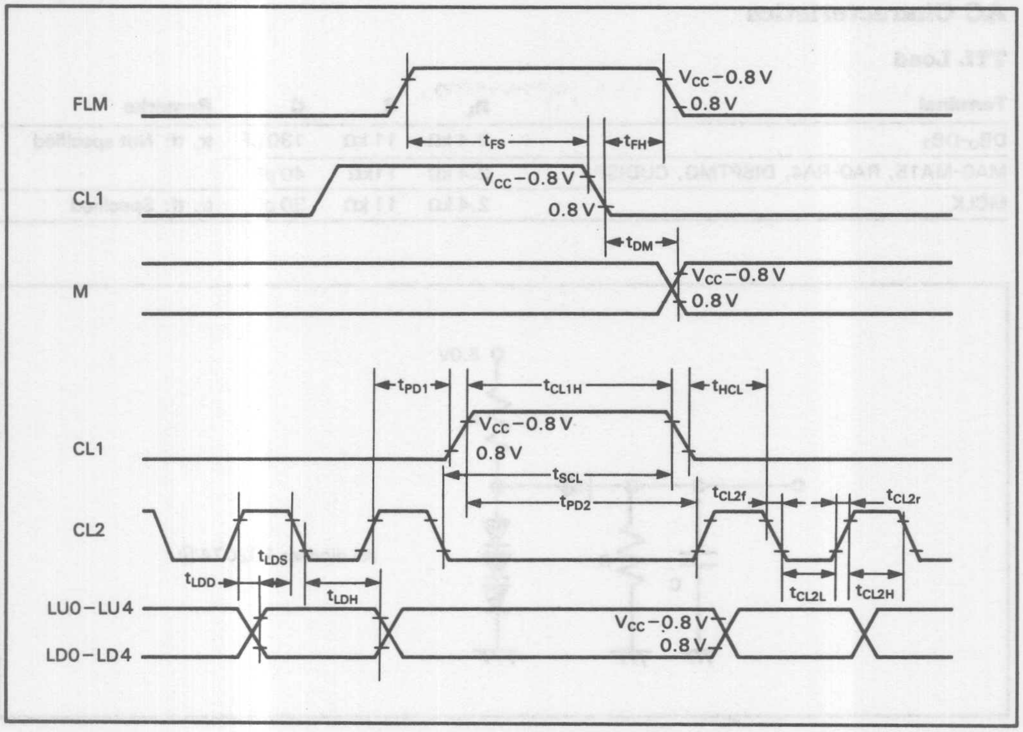
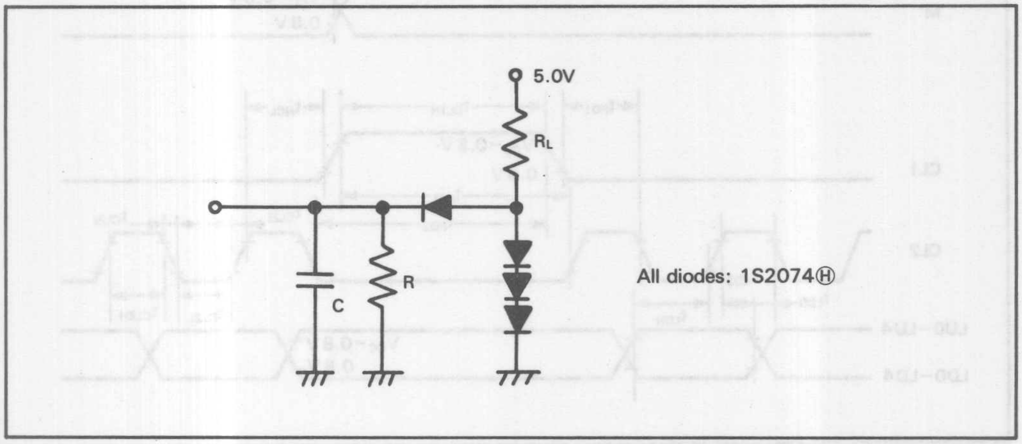


Figure 41 LCD Interface

AC Characteristics

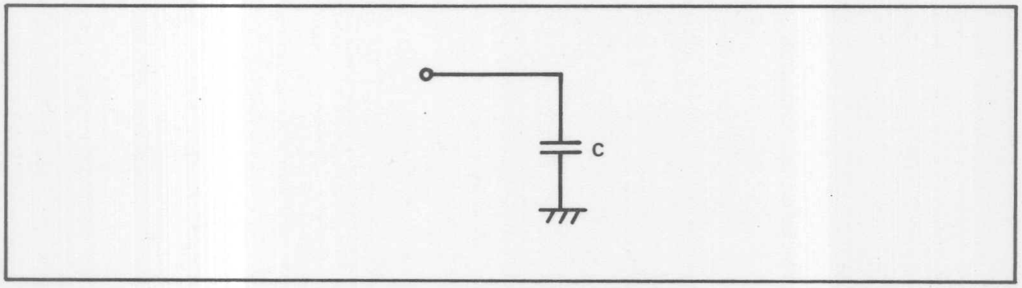
TTL Load

Terminal	R_L	R	C	Remarks
DB_0-DB_7	2.4 kΩ	11 kΩ	130 pF	tr, tf: Not specified
MA0-MA15, RA0-RA4, DISPTMG, CUDISP	2.4 kΩ	11kΩ	40 pF	
MCLK	2.4 kΩ	11 kΩ	30 pF	tr, tf: Specified



Capacitive Load

Terminal	C	Remarks
CL2	150 pF	tr, tf: Specified
CL1	200 pF	
LU0-LU3, LD0-LD3, M	150 pF	tr, tf: Not specified
FLM	50 pF	



Refer to user's manual (No. 68-1-160) and application note (No. ADE-502-003) for detail of this product.

HD66503
(240-Channel Row Driver with Internal LCD Timing Circuit)

—Preliminary—

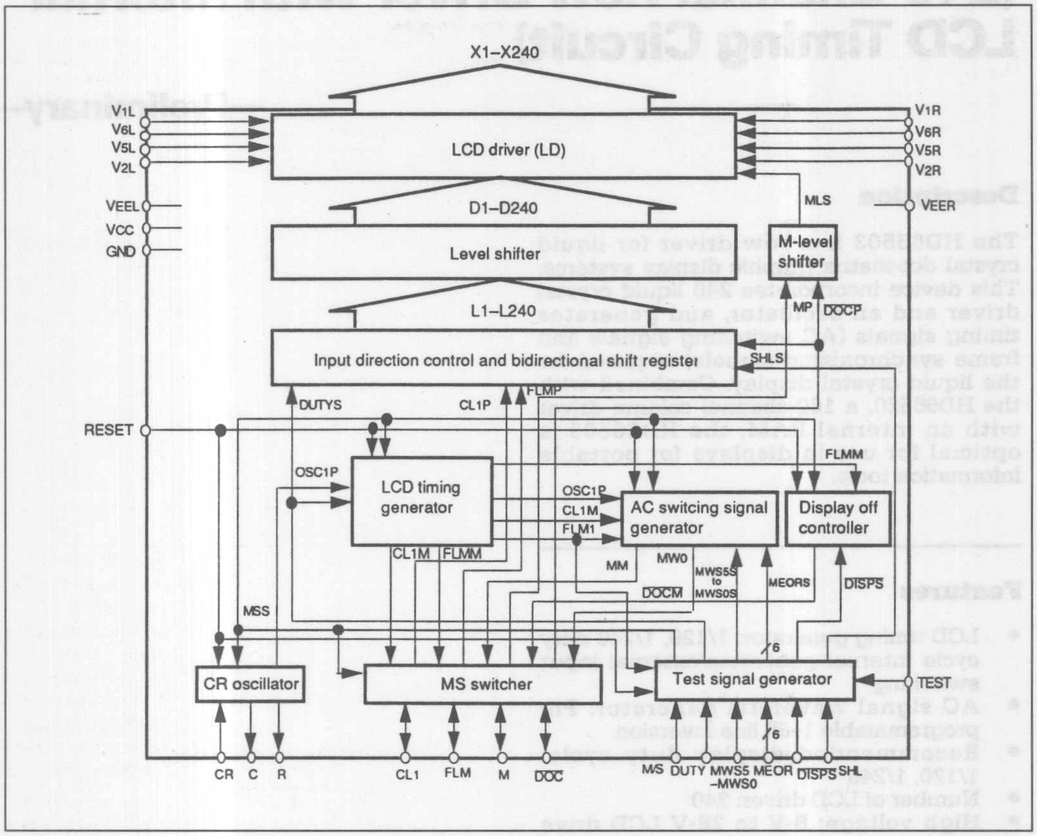
Description

The HD66503 is a row driver for liquid crystal dot-matrix graphic display systems. This device incorporates 240 liquid crystal driver and an oscillator, and generates timing signals (AC switching signals and frame synchronizing signals) required for the liquid crystal display. Combined with the HD66520, a 160-channel column driver with an internal RAM, the HD66503 is optimal for use in displays for portable information tools.

Features

- LCD timing generator: 1/120, 1/240 duty cycle internal generator/external input switching
- AC signal waveform generator: Pin programmable 1–63 line inversion
- Recommended display duty cycle: 1/120, 1/240
- Number of LCD driver: 240
- High voltage: 8-V to 28-V LCD drive voltage
- Low power consumption: 100 μA (during display)
- Internal display off function
- Oscillator circuit with standby function: 130 kHz (max)
- Display timing operation clock: 65 kHz (max) (operating at 1/2 system clock)

Internal Block Diagram



1. LCD driver

Selects one of four LCD drive voltage levels (V1, V2, V5, and V6) depending on a combination of shift register data and the value of M, the AC switching signal, and transfers that voltage to the output circuit.

2. Level shifter

Boosts 5-V signals to high voltage signals for the LCD drive.

3. Bidirectional shift register (240 bits)

Shifts internally generated data or data input from the FLM pin at each falling edge of the data transfer clock CL1. Shift direction can be switched using SHL signals.

Pin Description

Classification	Symbol	Pin No.	Pin Name	I/O	Number of Pins	Functions
Power supply	V_{CC1}, V_{CC2}	246 267	V_{CC1}, V_{CC2}	Power supply	2	V_{CC}–GND: logic power supply
	GND	250	GND	Power supply	1	
	$V_{EE}L$, $V_{EE}R$	245 268	LCD drive level power supply	Power supply	2	V_{CC}–V_{EE}: LCD drive circuits power supply
	V1L, V1R	244 269	LCD select high-level voltage	Input	2	LCD drive level power supply See figure 1.
	V2L, V2R	241 272	LCD select low-level voltage	Input	2	
	V5L, V5R	242 271	LCD deselect low-level voltage	Input	2	
	V6L, V6R	243 270	LCD deselect high-level voltage	Input	2	
Control signals	M/$\overline{S}$	266	Master/slave switching	Input	1	Control signal enabling/disabling LCD timing generator operation. Timing generator halts at low level. Timing generator operates at high level. (Refer to **Pin Functions** for details.)
	DUTY	259	Display duty ratio select	Input	1	Low level: 1/120 display duty ratio High level: 1/240 display duty ratio
	MWS_0 to MWS_5	257 256 255 254 253 252	AC switching signal cycle select	Input	6	Sets cycle for AC switching signal M in a line unit (1 to 63). The term 0 is for external input. (Refer to **Pin Functions** for details.)
	MEOR	258	AC switching signal EOR	Input	1	Selects EOR processing for frame inversion waveform and AC signal M.
	CR, C, R	247 248 249	Oscillator		3	These pins are used as shown in figure 2 in master mode, and as shown in figure 3 in slave mode.

Pin Description (Cont'd.)

Classification	Symbol	Pin No.	Pin Name	I/O	Number of Pins	Functions
Control signals	$\overline{\text{RESET}}$	261	Reset	Input	1	Stops oscillator circuits, initializes internal counter, and switches display off. (Refer to **Pin Functions** for details.)
LCD timing	CL1	263	Display data transfer	I/O	1	Display-data transfer clock I/O pin. (Refer to **Pin Functions** for details.)
	FLM	264	First line marker	I/O	1	First line marker I/O pin. (Refer to **Pin Functions** for details.)
	M	262	AC switching signal	I/O	1	AC control I/O pin for LCD drive output.
	SHL	251	Shift direction select	Input	1	FLM -> X1 -> X240 at low, and FLM -> X240 -> X1 at high.
	$\overline{\text{DISPOFF}}$	260	Display off signal	Output	1	Fixes LCD drive output to select high level. When low level, LCD drive outputs X1 to X240 are set to V1, the LCD select high level. Display can be turned off by setting a segment driver to level V1.
	$\overline{\text{DOC}}$	265	Display off control signal	I/O	1	Inputs and outputs a display-off control signal in response to the $\overline{\text{DISPOFF}}$ signal and oscillator startup sequence. (Refer to **Pin Functions** for details.
LCD drive output	X1 to X240	240 1	LCD drive output	Output	240	Selects one from among four levels (V1, V2, V5, and V6) depending on the combination of M signal and display data. See figure 4.

Note: 30 input/outputs (excluding driver block)

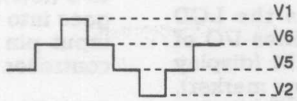


Figure 1 LCD Drive Levels

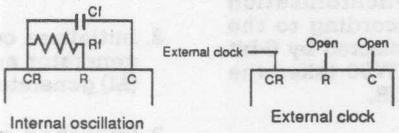


Figure 2 Oscillator Connection in Master Mode

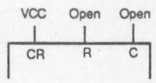


Figure 3 Oscillator Connection in Slave Mode

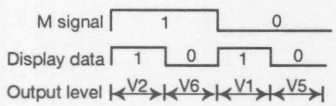


Figure 4 LCD Drive Output

Pin Functions

M/$\overline{S}$ (Input): Starts and stops the LCD timing generator. Also determines I/O of the following four signal pins: CL1 (display data transfer clock), FLM (first line marker), M (AC switching signal), and $\overline{DOC}$ (display off control), depending on whether the LCD timing generator is operating or not. See table 1.

MWS0 to MWS5, MEOR (Input): AC switching signal M, in synchronization with CL1, is generated according to the value (an integer 1 to 63) selected by 6-bit MWS0 to MWS5, where MWS0 takes the LSB and MWS5 takes the MSB.

When the AC switching signal EOR (MEOR) is high, M is exclusively ORed with the B-waveform AC signal synchronized with the first line marker (FLM) before being output from the M pin.

When the MWS0 to MWS5 bits are all set to 0 (low), the AC switching signal (M) pin goes into the input state, and becomes the input pin for AC signals from an external controller.

$\overline{RESET}$ (Input): The following initialization operations are performed when $\overline{RESET}$ is low:

1. Stops internal oscillator or external oscillator clock input.
2. Initializes counters for the LCD timing generator and the AC switching signal (M) generator.
3. Switches off the display by driving display-off control output (DOC) low. After reset release, the display off control (DOC) is held low for four frame cycles (four FLM clock cycles) to prevent erroneous display during startup.

Table 1 M/$\overline{S}$ Function

M/$\overline{S}$	Mode	LCD Timing Generator	CL1, FLM, M, and $\overline{DOC}$ I/O State
Low	Slave	Stop	Input
High	Master	1/120 or 1/240 duty cycle control	Output

$\overline{\text{DOC}}$ (Input/Output): Outputs the AND of the display-off control status after reset release and the display-off signal ($\overline{\text{DISPOFF}}$) in master mode. The pin is connected to the $\overline{\text{DISPOFF}}$ pin of the HD66520, which is normally paired with the HD66503. The pin inputs an external display-off control signal from the outside in slave mode.

CL1 (Input/Output): In master mode, CL1 outputs a 50% duty-ratio data-transfer clock with double cycles of an internal oscillator or external clock input cycles.

In slave mode, CL1 operates as the input pin for the external data-transfer clock.

In bidirectional shift-register timing, data is shifted at the rising edge of CL1 in accordance with the specifications of the HD66520 with built-in RAM when used in a paired configuration. As this is the opposite of the standard common driver arrangement, the transfer clock must be in an inverse phase when paired with general-purpose column drivers such as HD66240 and HD66224T.

FLM (Input/Output): In master mode, FLM outputs the first line marker. In slave mode, FLM inputs the first line marker. The shift direction of the FLM can be selected according to the DUTY and SHL signals, as shown in table 2.

In slave mode, use the DUTY signal at high level in normal.

Table 2 Selection of FLM Shift Direction

DUTY	SHL	Shift Direction of FLM
High	High	X240 to X1
	Low	X1 to X240
Low	High	X120 to X1, and X240 to X121
	Low	X1 to X120, and X121 to X240

DUTY (Input): Selects display duty cycle. The pin selects a 1/120 duty cycle at low level, and a 1/240 duty cycle at high level.

Liquid Crystal Display Timing

Timing Generator

CL1 is a 50% duty-ratio clock that changes at the falling edge of oscillator clock OSC1. FLM is a clock signal output once every 240 CL1 clock cycles at the rising edge of CR when the DUTY signal is high, and every 120 CL1 clock cycles at the rising edge of CR when the DUTY signal is low.

Reset State

The reset state fixes all clocks at low and clears the internal counter to 0. After reset release, the display-off function continues for four frame cycles even when the DISP pin is high.

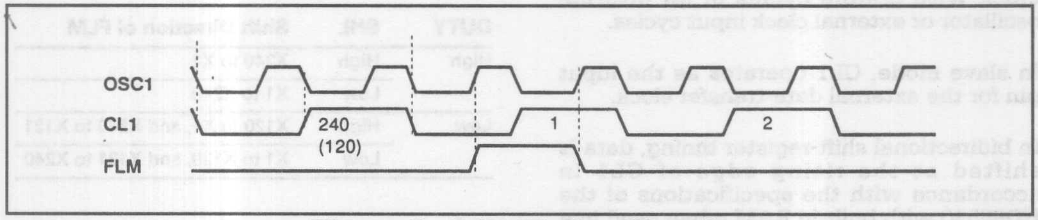


Figure 5 LCD Timing Signals

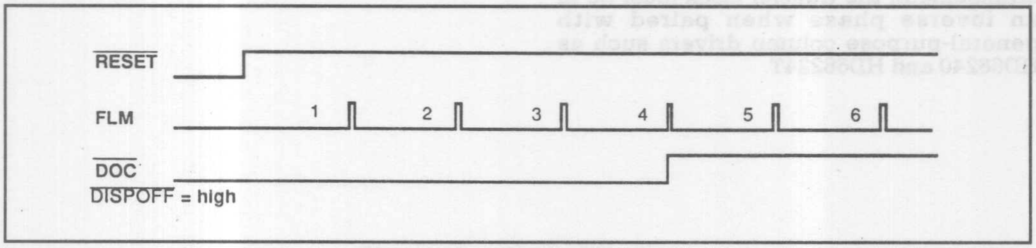


Figure 6 Reset Timing

Example of System Configuration

Figure 7 shows a system configuration for a 240 × 320-dot LCD panel using segment driver HD66520 with internal bit-map RAM. All required functions can be prepared for liquid crystal display with just three chips except for liquid crystal display power supply circuit functions.

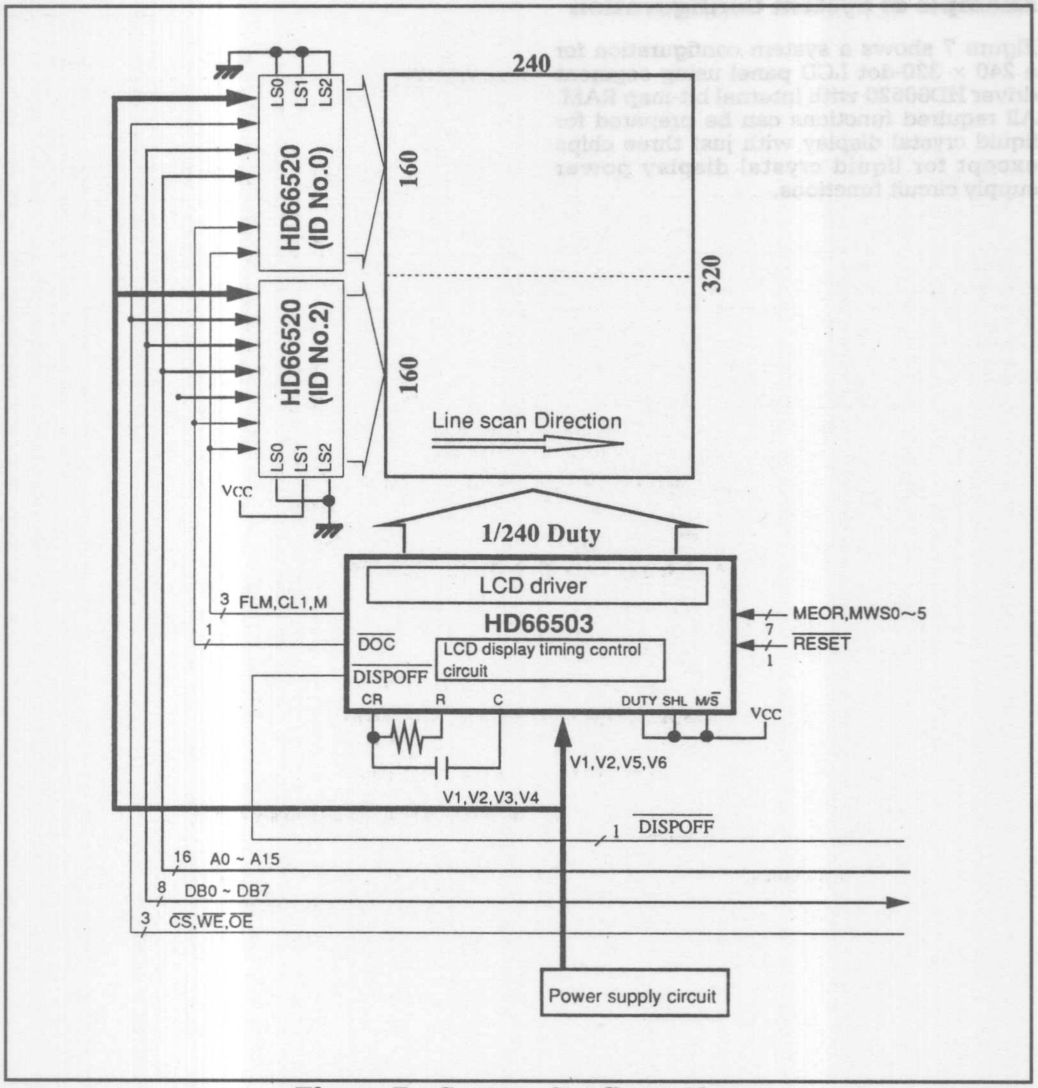


Figure 7 System Configuration

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Notes
Power voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	2
	LCD drive circuit	V_{EE}	V_{CC} –30.0 to V_{CC} +0.3	V	5
Input voltage		V_{T1}	–0.3 to V_{CC} +0.3	V	2, 3
Input voltage		V_{T2}	V_{EE} –0.3 to V_{CC} +0.3	V	4, 5
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–40 to +125	°C	

Notes:
1. If the LSI is used beyond its absolute maximum rating, it may be permanently damaged. It should always be used within the limits of its electrical characteristics in order to prevent malfunction or unreliability.
2. Measured relative to GND (0 V).
3. Applies to all input pins except for V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{5L}, V_{5R}, V_{6L}, and V_{6R}, and to input/output pins in high-impedance state.
4. Applies to pins V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{5L}, V_{5R}, V_{6L}, and V_{6R}.
5. Apply the same voltage to pairs V_{1L} and V_{1R}, V_{2L} and V_{2R}, V_{5L} and V_{5R}, V_{6L} and V_{6R}, and V_{EEL} and V_{EER}.
   It is important to preserve the relationships $V_{CC} \geqslant V_{IL} = V_{1R} \geqslant V_{6L} = V_{6R} \geqslant V_{5L} = V_{5R} \geqslant V_{2L} = V_{2R} \geqslant V_{EE}$.

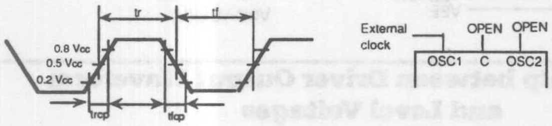
Electrical Characteristics

DC Characteristics (V_{CC} = 2.7 V to 5.5 V, V_{EE} = 8 V to 28 V, GND = 0 V, T_a = –20°C to +75°C)

Item	Symbol	Measurement Condition	Min	Typ	Max	Unit	Notes
Input high level voltage	V_{IH}		0.8 V_{CC}	—	V_{CC}	V	1
Input low level voltage	V_{IL}		0	—	0.2 V_{CC}	V	1
Output high level voltage	V_{OH}	I_{OH} = –0.4 mA	V_{CC} –0.4	—	—	V	
Output low level voltage	V_{OL}	I_{OL} = +0.4 mA	—	—	0.4	V	2
Driver "on" resistance	R_{ON}	$V_{CC} - V_{EE}$ = 28 V, load current: ±150 μA	—	—	2.0	kΩ	7
Input leakage current (1)	I_{IL1}	V_{IN} = 0 to V_{CC}	–1.0	—	1.0	μA	1
Input leakage current (2)	I_{IL2}	V_{IN} = V_{EE} to V_{CC}	–25	—	25	μA	3
Operating frequency (1)	f_{opr1}	Master mode (external clock operation)	10	—	200	kHz	4
Operating frequency (2)	f_{opr2}	Slave mode (shift register)	0.5	—	500	kHz	
Oscillation frequency (1)	f_{OSC1}	Cf = 100 pf ±5%, Rf = 47 kΩ ±2%	70	100	130	kHz	5
Oscillation frequency (2)	f_{OSC2}	Cf = 220 pf ±5%, Rf = 51 kΩ ±2%	21	30	39	kHz	5
Power consumption (1)	I_{GND1}	Master mode 1/240 duty cycle, Cf = 220 pF, Rf = 51 kΩ	—	—	80	μA	6
Power consumption (2)	I_{GND2}	Master mode 1/240 duty cycle external clock f_{opr2} = 30 kHz	—	—	10	μA	6
Power consumption (3)	I_{GND3}	Slave mode 1/240 duty cycle during operation	—	—	10	μA	6
Power consumption	I_{EE}	Master mode 1/240 duty cycle, Cf = 220 pF, Rf = 51 kΩ	—	—	20	μA	6

Notes:

1. Applies to input pins TEST, MEOR, MWS0 to MWS5, DUTY, SHL, $\overline{\text{DISP}}$, $\overline{\text{MS}}$, $\overline{\text{RESET}}$, and OSC1, and when inputting to input/output pins CL1, FLM, $\overline{\text{DOC}}$, and M.
2. Applies when outputting from input/output pins CL1, FLM $\overline{\text{DOC}}$, and M.
3. Applies to V1L/V1R, V2L/V2R, V5L/V5R, and V6L/V6R. X1 to X240 are open.
4. Figure 5 shows the external clock specifications.



$$\text{Duty} = \frac{TH}{TH + TL} \times 100\%$$

	Min.	Typ.	Max.	Unit
Duty	45	50	55	%
trcp	—	—	50	ns
tfcp	—	—	50	ns

Figure 8 External Clock

5. Connect resistance Rf and capacitance Cf as follows:

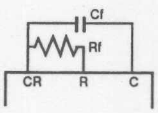


Figure 9 Timing Components

6. Input and output currents are excluded. When a CMOS input is floating, excess current flows from the power supply through to the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.
7. Indicates the resistance between one pin from X1 to X240 and another pin from the V pins V1L/V1R, V2L/V2R, V5L/V5R, and V6L/V6R, when a load current is applied to the X pin; defined under the following conditions:

   $V_{CC} - V_{EE} = 28$ V
   V1L/V1R, V6L/V6R = $V_{CC} - 1/10\ (V_{CC} - V_{EE})$
   V5L/V5R, V2L/V2R = $V_{EE} + 1/10\ (V_{CC} - V_{EE})$

   V1L/V1R and V6L/V6R should be near the V_{CC} level, and V5L/V5R and V2L/V2R should be near the V_{EE} level. All these voltage pairs should be separated by less than ΔV, which is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltages $V_{CC} - V_{EE}$. See figure 7.

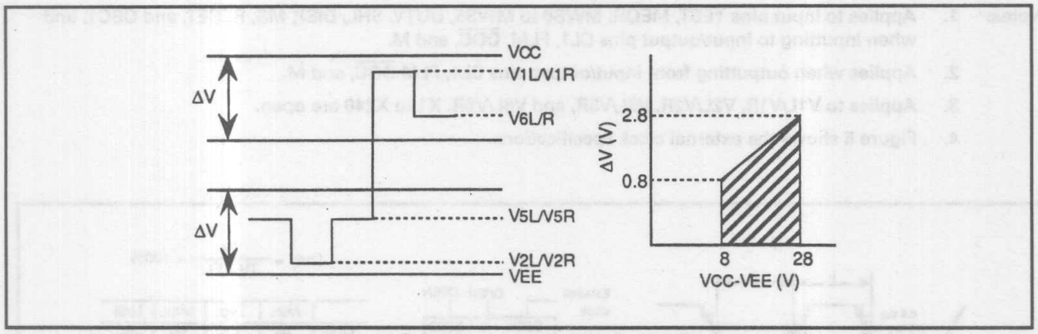


Figure 10 Relationship between Driver Output Waveform and Level Voltages

AC Characteristics (V_{CC} = 2.7 V to 5.5 V, V_{EE} = 8 V to 28 V, GND = 0 V, T_a = –20°C to +75°C)

Slave Mode (M/S = GND)

Item	Symbol	Min	Typ	Max	Unit	Notes
CL1 high-level width	t_{CWH}	500	—	—	ns	1
CL1 low-level width	t_{CWL}	500	—	—	ns	1
FLM setup time	t_{FS}	100	—	—	ns	1
FLM hold time	r_{FH}	100	—	—	ns	1
CL1 rise time	t_r	—	—	50	ns	1
CL1 fall line	t_f	—	—	50	ns	1

Note: 1. Based on the load circuit shown in figure 8.

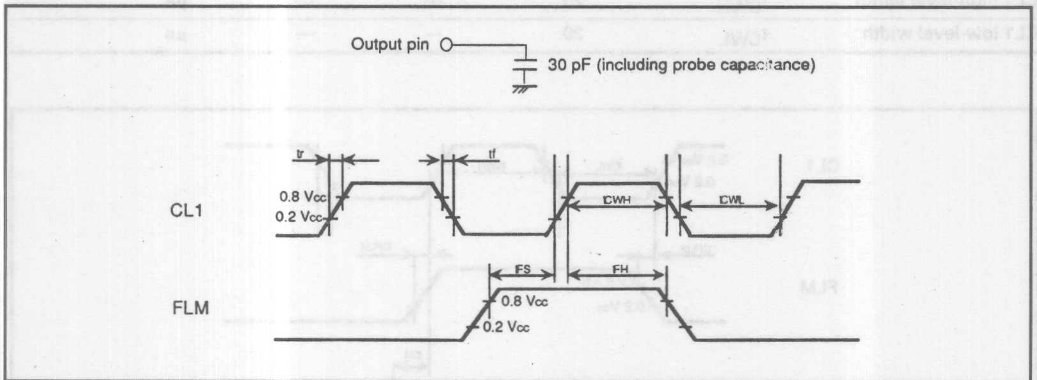


Figure 11 Slave Mode Timing

Master Mode (M/S = V_{CC}, Cf = 100 pF, Rf = 47 kΩ)

Item	Symbol	Min	Typ	Max	Unit	Notes
FLM delay time	t_{DFLM}	—	—	500	ns	
M delay time	t_{DM}	—	—	500	ns	
CL1 high-level width	t_{CWH}	5	—	—	µs	
CL1 low-level width	t_{CWL}	5	—	—	µs	

Master Mode (M/S = V_{CC}, Cf = 220 pF, Rf = 51 kΩ)

Item	Symbol	Min	Typ	Max	Unit	Notes
FLM delay time	t_{DFLM}	—	—	500	ns	
M delay time	t_{DM}	—	—	500	ns	
CL1 high-level width	t_{CWH}	20	—	—	µs	
CL1 low-level width	t_{CWL}	20	—	—	µs	

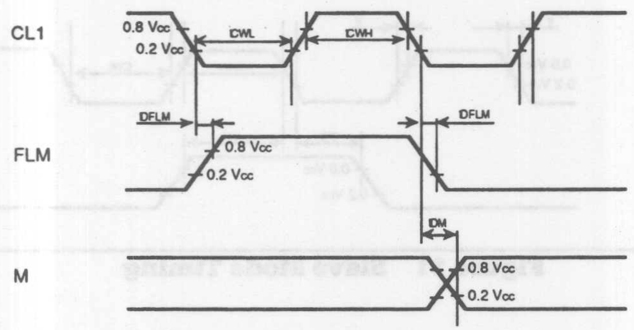
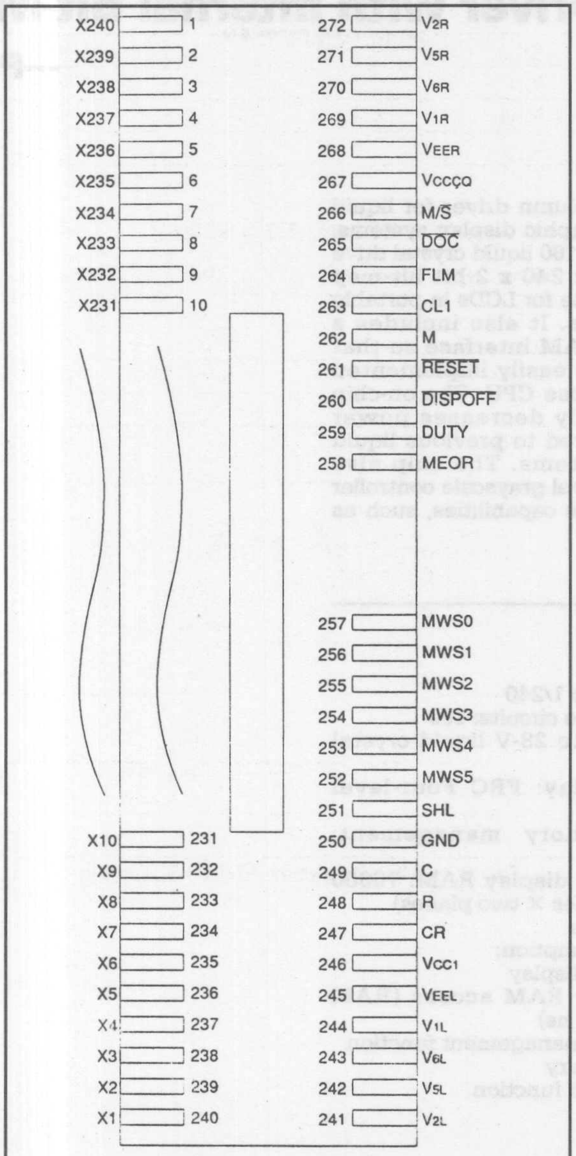


Figure 12 Master Mode Timing

Pin Arrangement



Top view (not a TCP view)

HD66520

(160-Channel 4-Level Grayscale Display Column Driver with Internal Bit-Map RAM)

—Preliminary—

Description

The HD66520 is a column driver for liquid crystal dot-matrix graphic display systems. This LSI incorporates 160 liquid crystal drive circuits and a 160 x 240 x 2-bit bit-map RAM, which is suitable for LCDs in portable information devices. It also includes a general-purpose SRAM interface so that draw access can be easily implemented from a general-purpose CPU. The on-chip display RAM greatly decreases power consumption compared to previous liquid crystal display systems. The chip also incorporates a four-level grayscale controller for enhanced graphics capabilities, such as icons on a screen.

Features

- Duty cycle: 1/64 to 1/240
- Liquid crystal drive circuits: 160
- High voltage: 8 to 28-V liquid crystal drive voltage
- Grayscale display: FRC Four-level grayscale display
- Grayscale memory management: Packed pixel
- Internal bit-map display RAM: 76800 bits (160 × 240 lines × two planes)
- Access time: 80 ns
- Low power consumption:
  —100 µA during display
  —20 mA during RAM access (RAM access time 250 ns)
- On-chip memory management function
- Refresh unnecessary
- Internal display off function

Pin Description

Classification	Symbol	Pin No.	Pin Name	I/O	Number of Pins	Function
Power supply	$V_{CC}1$ $V_{CC}2$		V_{CC} V_{CC}		1 1	V_{CC}–GND: logic power supply
	GND		GND	Input	1	
	$V_{EE}1$, $V_{EE}2$		LCD drive circuit power supply	Input	1	V_{CC}–V_{EE}: LCD drive circuit power supply
	V1L, V1R		LCD select high-level voltage	Input	2	LCD drive level power supplies See figure 1.
	V2L, V2R		LCD select low-level voltage	Input	2	
	V3L, V3R		LCD deselect high-level voltage	Input	2	
	V4L, V4R		LCD deselect low-level voltage	Input	2	
Control signals	LS0, LS1		LSI ID select switch pin 0 and 1	Input	2	Pins for setting LSI ID no. (refer to **Pin Functions** for details).
	SHL		Shift direction control signal	Input	1	Reverses the relationship between LCD drive output pins Y and addresses.
	FLM		First line marker	Input	1	First line select signal
	CL1		Data transfer clock	Input	1	Clock signal to transfer the line data to an LCD display driver block.
	M		AC switching signal	Input	1	Switching signal to convert LCD drive output to AC
	$\overline{\text{DISPOFF}}$		Display off signal	Input	1	Control signal to fix LCD driver outputs to LCD select high level. When low, LCD drive outputs Y1 to Y160 set to V1, or LCD select high level. Display can be turned off by setting a common driver to V1.
	TEST		Test pin	Input	1	LSI test pin (refer to **Pin Functions** for details).

Pin Description (Cont'd.)

Classification	Symbol	Pin No.	Pin Name	I/O	Number of Pins	Functions
Bus interface	A0 to A15		Address Input	Input	16	Upper 9 bits (A15–A7) are used for the duty-directional addresses, and lower 7 bits (A6–A0) for the output-pin directional addresses (refer to **Pin Functions** for details).
	DB0 to DB7		Data input/ output	I/O	8	Packed-pixel 2-bit/ pixel display data transfer (refer to **Pin Functions** for details.)
	$\overline{CS}$		Chip select signal	Input	1	LSI select signal during draw access (refer to **Pin Functions** for details.)
	$\overline{WE}$		Write signal	Input	1	Write-enable signal during draw access (refer to **Pin Functions** for details).
	$\overline{OE}$		Output enable signal	Input	1	Output-enable signal during draw access (refer to **Pin Functions** for details).
LCD drive output	Y1 to Y160		LCD drive output	Output	160	Each Y outputs one of the four voltage levels V1, V2, V3, or V4, depending on the combination of the M signal and data levels.

Note: The number of input outer leads: 47

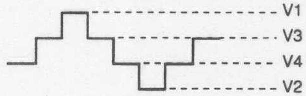


Figure 1 LCD Drive Levels

Pin Functions

• **Control Signals**

LS0 and LSI (Input): The LS pins can assign four (0 to 3) ID numbers to four LSIs, thus making it possible to connect a maximum of four HD66520s sharing the same $\overline{CS}$ pin to the same bus.

Various memory maps can be configured by combining the LS pins with the SHL pin.

SHL (Input): This pin reverses the relationship between LCD drive output pins Y and addresses. When the pin is low, output pins Y1 to Y160 correspond to the direction from start data to end data in the display lines, and when the pin is high, from end data to start data.

FLM (Input): When the pin is high, it resets the display line counter, returns the display line to the start line, and synchronizes common signals with frame timing.

CL1 (Input): At each rising edge of data transfer clock pulses input to this pin, the latch circuits latch horizontal-line RAM data and transfers it to the liquid crystal display driver section.

M (Input): AC voltage needs to be applied to liquid crystals to prevent deterioration due to DC voltage application. The M pin is a switch signal for liquid crystal drive voltage and determines the AC cycle.

$\overline{\text{DISPOFF}}$ (Input): A control signal to fix liquid crystal driver output to liquid crystal select high level. When this pin is low, liquid crystal drive outputs Y1 to Y160 are set to liquid crystal select high level V1. If Y pins of the paired common driver are also set to V1 level, the display can be deleted. When $\overline{\text{DISP}}$ becomes high, display returns to normal state.

TEST (Input): An LSI test pin. Use GND level for normal operations.

• **Bus Interface**

$\overline{CS}$ (Input): A basic signal of the RAM area. When $\overline{CS}$ is low (active), the system can access the on-chip RAM of the LSI whose address space, set by LS0, LS1, and SHL pins, contains the input address. When $\overline{CS}$ is high, RAM is in standby.

A0 to A15 (Input): A bus to transfer addresses during RAM access. Upper nine bits (A15 to A7) are duty-direction addresses, and lower seven bits (A6 to A0) are output pin direction addresses.

$\overline{WE}$ (Input): $\overline{WE}$, an active low signal, is used to write display data to the RAM. Only the LSI whose address space, set by pins LS0, LS1, and SHL, contains the input address can be written to when $\overline{CS}$ is low.

$\overline{OE}$ (Input): $\overline{OE}$, an active low signal, is used to read display data from the RAM. Only the LSI whose address space, set by pins LS0, LS1, and SHL, contains the input address can be read from when $\overline{CS}$ is low.

DB0 to DB7 (Input/Output): The pins function as data input/output pins. They can accommodate to a data format with 2 bits/pixel, which implement packed-pixel four-level grayscale display.

Block Diagram

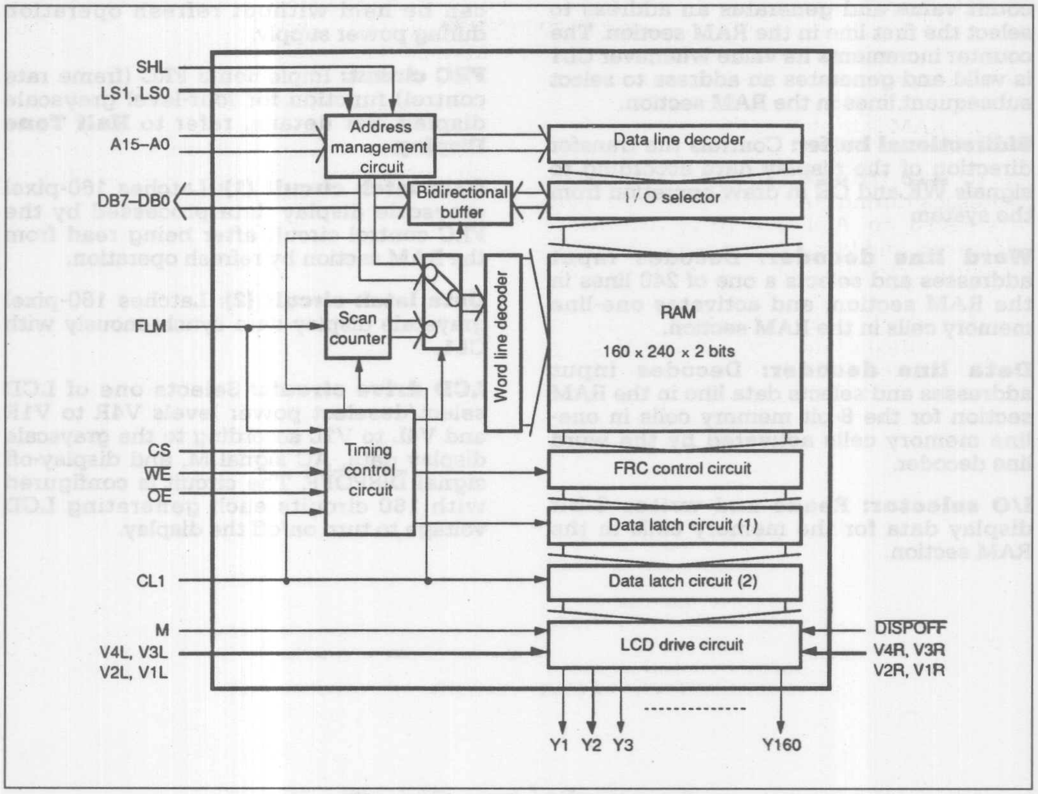


Figure 2 Block Diagram

Address management circuit: Converts the addresses input via A15–A0 from the system to the addresses for a memory map of the on-chip RAM. When several LSIs (HD66520s) are used, only the LSI whose address space, set by pins LS0, LS1, and SHL, contains the input address accepts the access from the system and enables the inside. The address management circuit enables configuration of the LCD display system with memory addresses not affected by the connection direction, and reduces burdens of software and hardware in the system.

Timing control circuit: Inputs signals FLM and CL1 for refresh operation to transfer the line data to the LCD drive circuit and signals $\overline{CS}$, $\overline{WE}$, and $\overline{OE}$ for display data access (draw operation) of the on-chip RAM by the system, while arbitrating refresh and draw operations. This circuit enables the system to access the display data of the on-chip RAM independent of refresh operation. Moveover, this circuit generates a timing signal for the FRC control circuit to implement four-level grayscale display.

Scan counter: Operates refresh functions. When FLM is high, the counter clears the count value and generates an address to select the first line in the RAM section. The counter increments its value whenever CL1 is valid and generates an address to select subsequent lines in the RAM section.

Bidirectional buffer: Controls the transfer direction of the display data according to signals $\overline{WE}$ and $\overline{OE}$ in draw operation from the system

Word line decoder: Decodes input addresses and selects a one of 240 lines in the RAM section, and activates one-line memory cells in the RAM section.

Data line decoder: Decodes input addresses and selects data line in the RAM section for the 8-bit memory cells in one-line memory cells activated by the word line decoder.

I/O selector: Reads and writes 8-bit display data for the memory cells in the RAM section.

RAM: 160 × 240 × 2-bit memory cell array. Since the memory is static, display data can be held without refresh operation during power supply.

FRC circuit: Implements FRC (frame rate control) function for four-level grayscale display. For details, refer to **Half Tone Display.**

Data latch circuit (1): Latches 160-pixel grayscale display data processed by the FRC control circuit after being read from the RAM section by refresh operation.

Data latch circuit (2): Latches 160-pixel grayscale display data synchronously with CL1.

LCD drive circuit: Selects one of LCD select/deselect power levels V4R to V1R and V4L to V1L according to the grayscale display data, AC signal M, and display-off signal $\overline{DISPOFF}$. The circuit is configured with 160 circuits each generating LCD voltage to turn on/off the display.

Driver Layout and Address Management

The Y lines on a liquid crystal panel and memory data in a driver are inverted horizontally depending on the connection direction of the liquid crystal panel and the driver. When several drivers are connected, address management is needed for each driver. Although reinverted bit-map plotting or address management by the $\overline{CS}$ pin in each driver are possible by using special write addressing, the load on the software is significantly increased. To avoid this, the HD66520 provides memory addresses independent of connection direction, but responds to the setting of pins LS0, LS1, and SHL.

How to Use the SHL Pin: It is possible to invert the relationship between the addresses and output pins Y1 to Y160 by setting the SHL pin. If the HD66520 is placed on any side of the LCD panel, the upper left section on the screen can be assigned to address H0000.

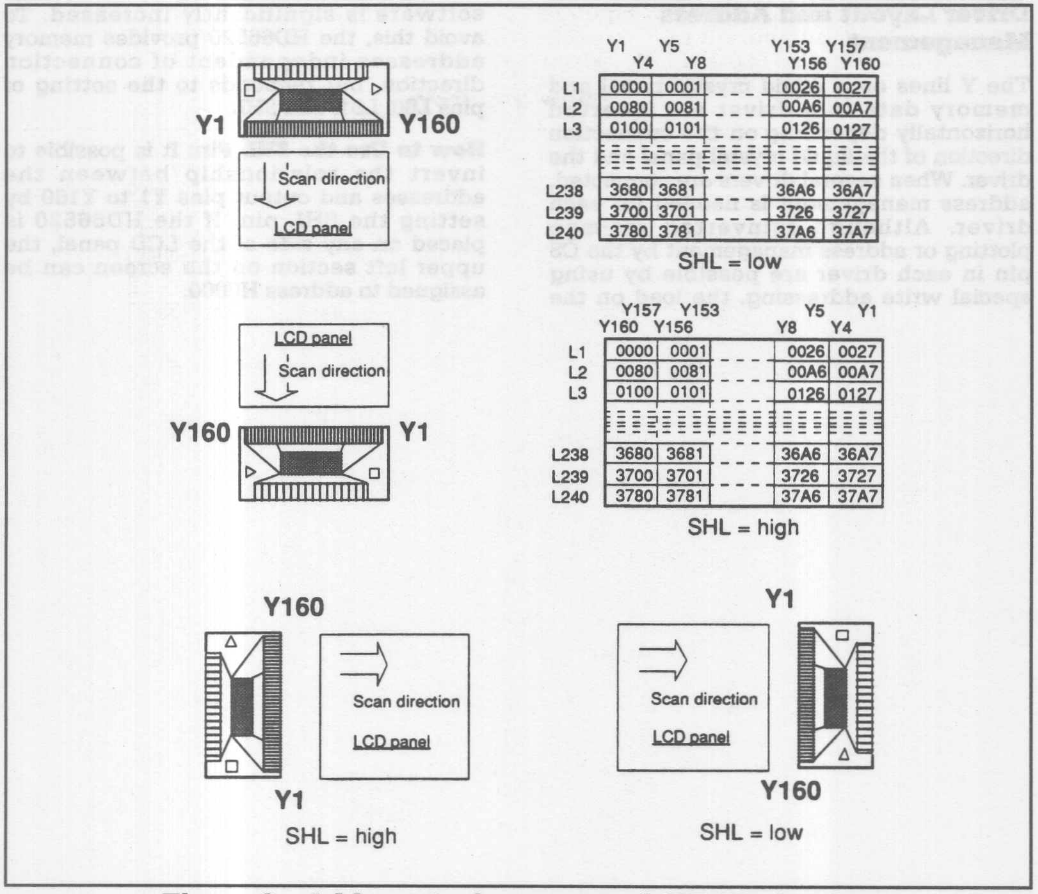


Figure 3 Address Assignment and SHL Pin Setting

How to Use the LS1 and LS0 pins

The memory map of the HD66520 can be most efficiently used in three display sizes: a 240-dot-wide by 160-dot-long display; a 320-dot-wide by 240-dot-long display; and a 480-dot-wide by 320-dot-long display, all of them are standard sizes for portable information devices.

Therefore, up to four HD66520s can be connected to the same bus or with the $\overline{CS}$ pin.

LSIs can be mapped as shown in figure 4 by assigning ID numbers 0 to 3 to each HD66520 by using pins LS0 and LS1.

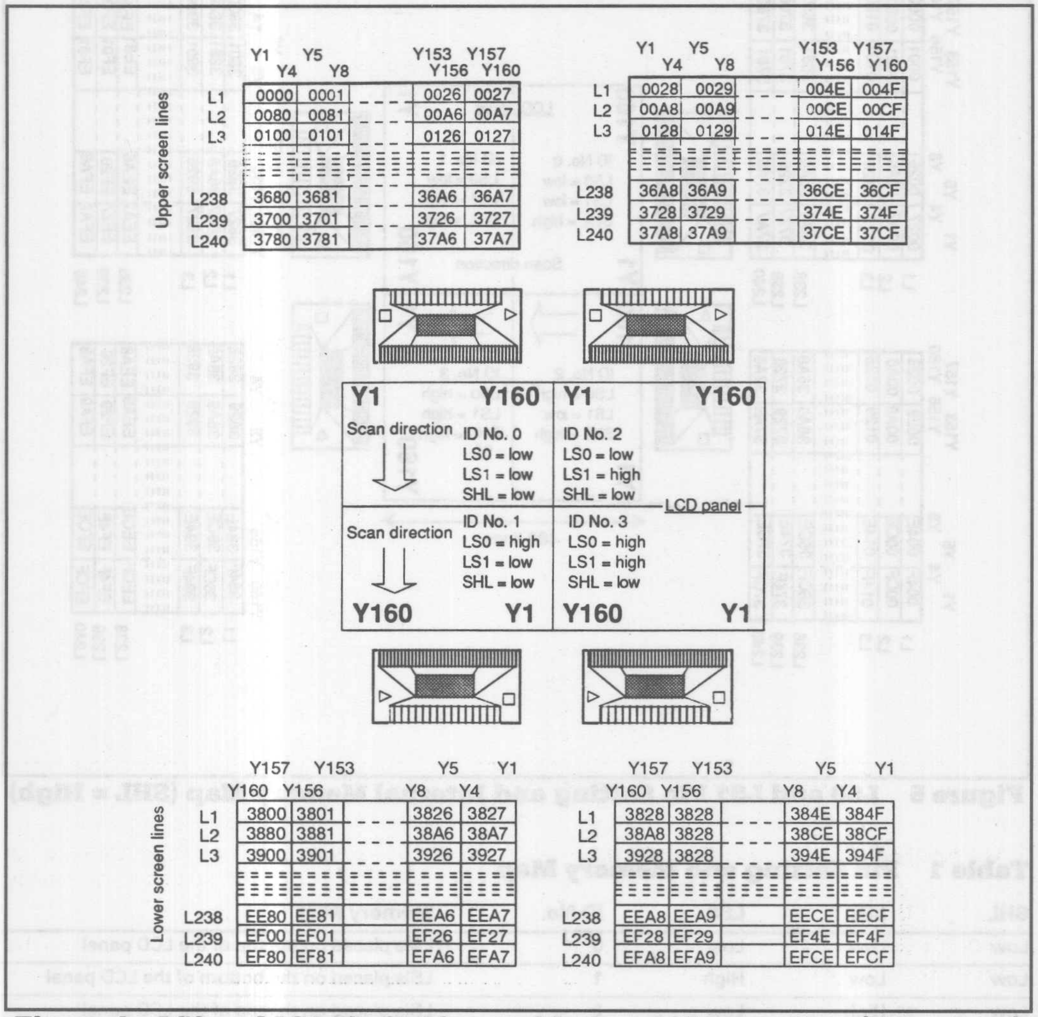


Figure 4 LS0 and LS1 Pin Setting and Internal Memory Map (SHL = Low)

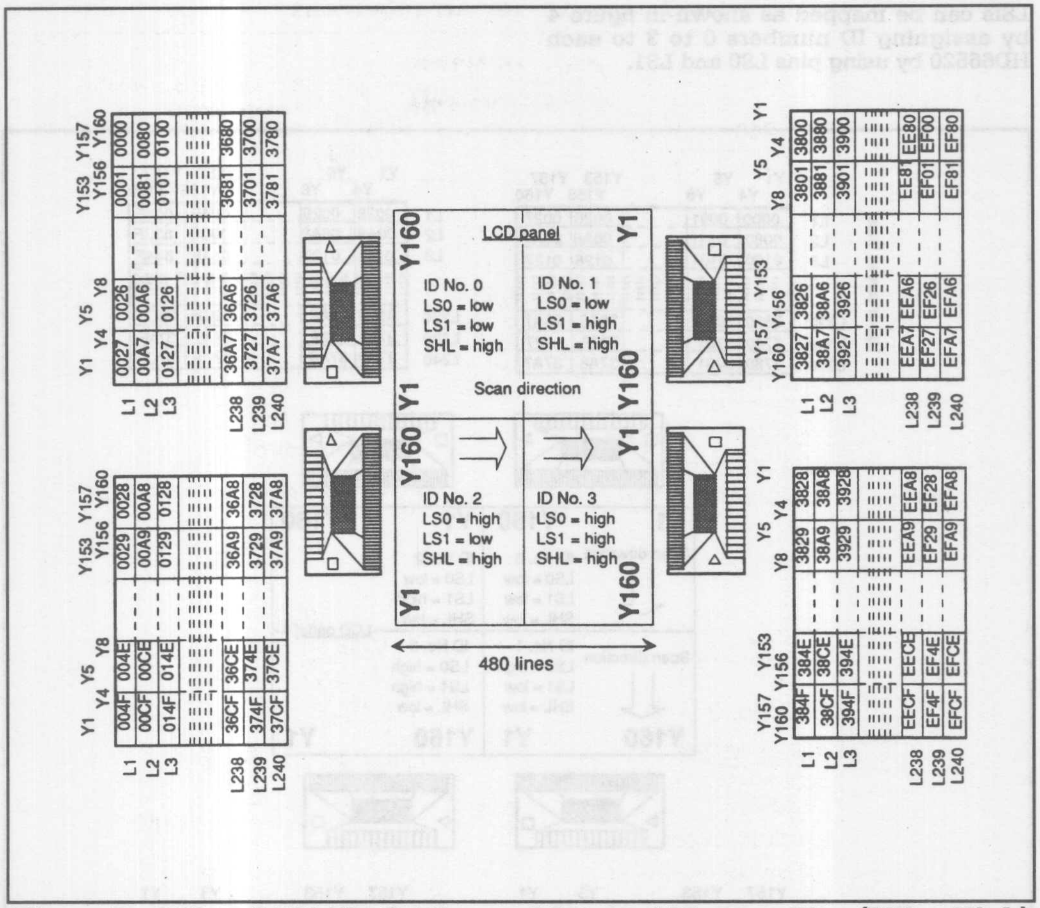
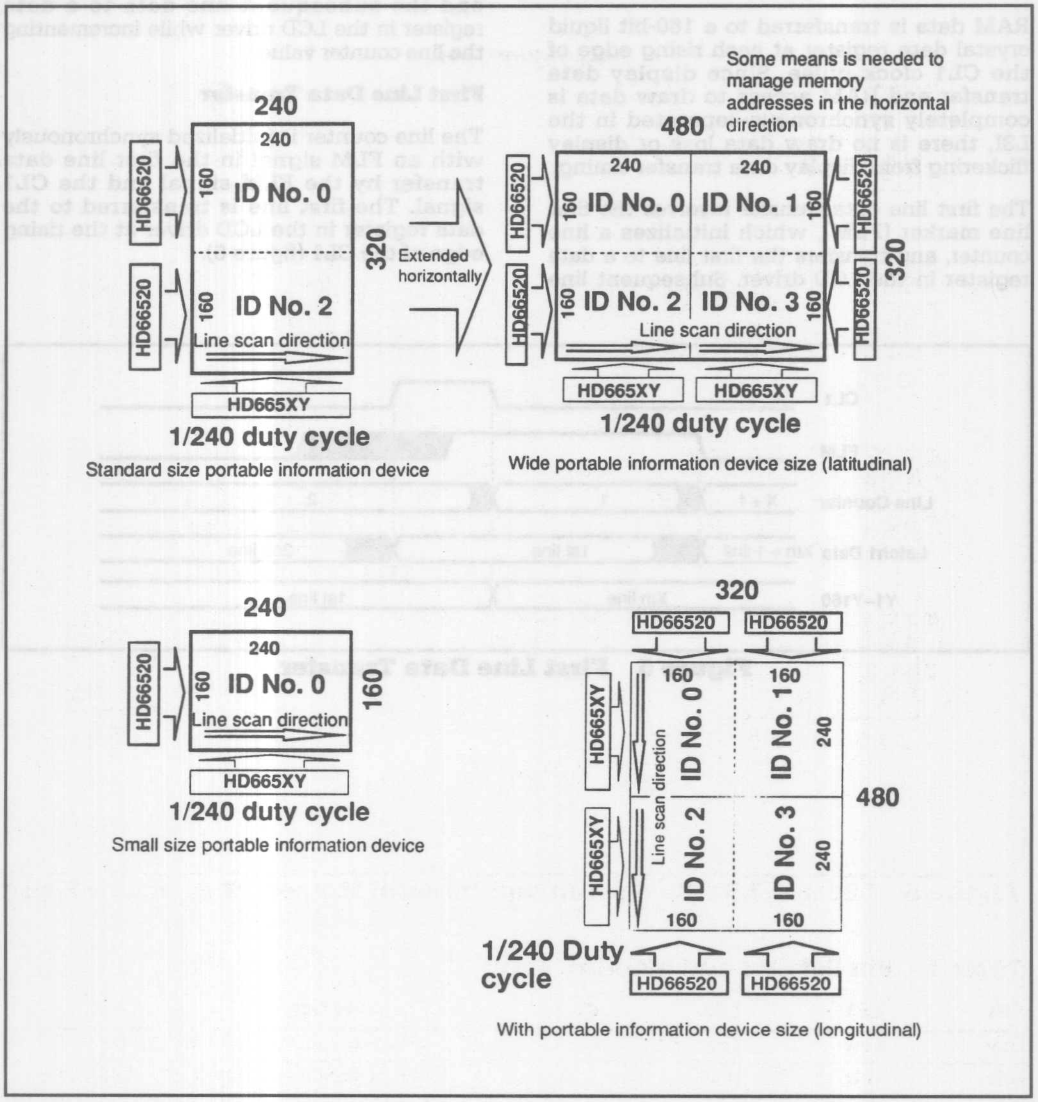


Figure 5 LS0 and LS1 Pin Setting and Internal Memory Map (SHL = High)

Table 1 Pin Setting and Memory Map

SHL	LS1	LS0	ID No.	Memory Map
Low	Low	Low	0	LSIs placed on the top of the LCD panel
Low	Low	High	1	LSIs placed on the bottom of the LCD panel
Low	High	Low	2	LSIs placed on the top of the LCD panel
Low	High	High	3	LSIs placed on the bottom of the LCD panel
High	Low	Low	0	LSIs placed on the left of the LCD panel
High	Low	High	1	LSIs placed on the right of the LCD panel
High	High	Low	2	LSIs placed on the left of the LCD panel
High	High	High	3	LSIs placed on the right of the LCD panel

Application Example for System-Driver Arrangement



Display-Data Transfer

RAM data is transferred to a 160-bit liquid crystal data register at each rising edge of the CL1 clock pulse. Since display data transfer and RAM access to draw data is completely synchronous-separated in the LSI, there is no draw data loss or display flickering from display data transfer timing.

The first line data transfer involves the first line marker (FLM), which initializes a line counter, and transfers the first line to a data register in the LCD driver. Subsequent line data transfer involves transferring the second and the subsequent line data to a data register in the LCD driver while incrementing the line counter value.

First Line Data Transfer

The line counter is initialized synchronously with an FLM signal in the first line data transfer by the FLM signal and the CL1 signal. The first line is transferred to the data register in the LCD driver at the rising edge of the CL1 (figure 6).

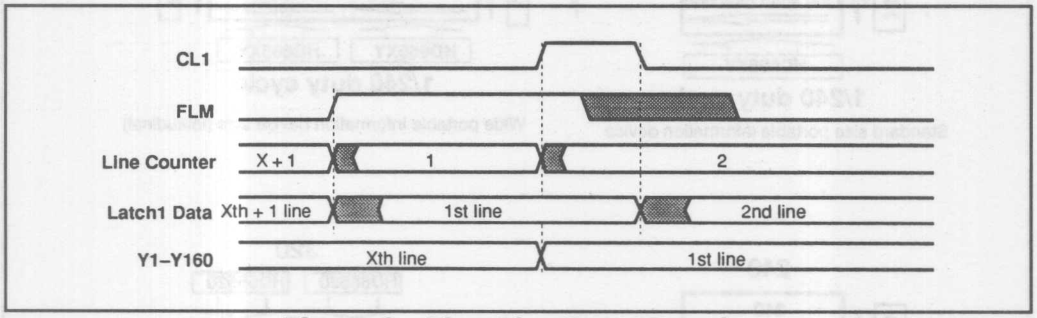


Figure 6 First Line Data Transfer

Subsequent Line Data Transfer

In display access 2, the second and the subsequent line data are transferred to the data register in the LCD driver at the rising edge of the CL1 to update the line counter value (figure 7).

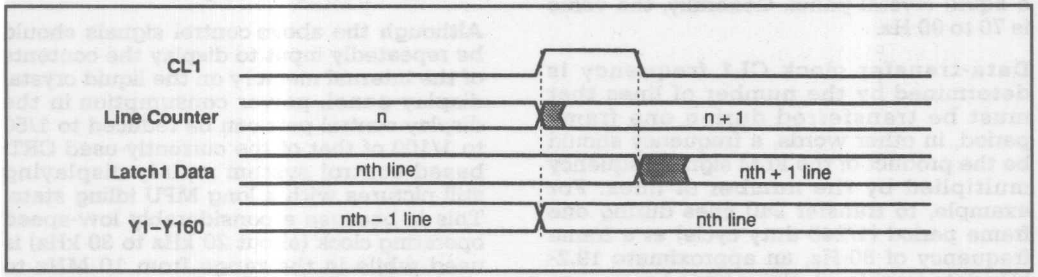


Figure 7 Subsequent Line Data Transfer

Display-Data Transfer Method

The liquid crystal panel display needs to repeatedly execute first line data transfers and successive line data transfers based on a regular cycle to achieve continuous operation.

The FLM signal cycle is determined by a frame frequency value which is required by a liquid crystal panel. Generally, the value is 70 to 90 Hz.

Data-transfer clock CL1 frequency is determined by the number of lines that must be transferred during one frame period, in other words, a frequency should be the product of the FLM signal frequency multiplied by the number of lines. For example, to transfer 240 lines during one frame period (1/240 duty cycle) at a frame frequency of 80-Hz, an approximate 19.2-kHz data transfer clock is needed.

The M signal, which converts a liquid crystal drive waveform to an AC signal, should be either a frame-reverse waveform synchronized with the FLM signal or an n-line reverse waveform synchronized with the n count of CL1. The latter should be initialized by FLM. Since the M cycle is closely related to optical characteristics and the display quality of the liquid crystal panel, it should be determined through actually verifying the display.

Although the above control signals should be repeatedly input to display the contents of the internal memory on the liquid crystal display panel, power consumption in the display control part can be reduced to 1/50 to 1/100 of that of the currently-used CRT-based control system mainly displaying still pictures with a long MPU idling state. This is because a considerably low-speed operating clock (about 20 kHz to 30 kHz) is used while in the range from 10 MHz to about 50 MHz are used for a liquid crystal controller based on existing CRT display control techniques.

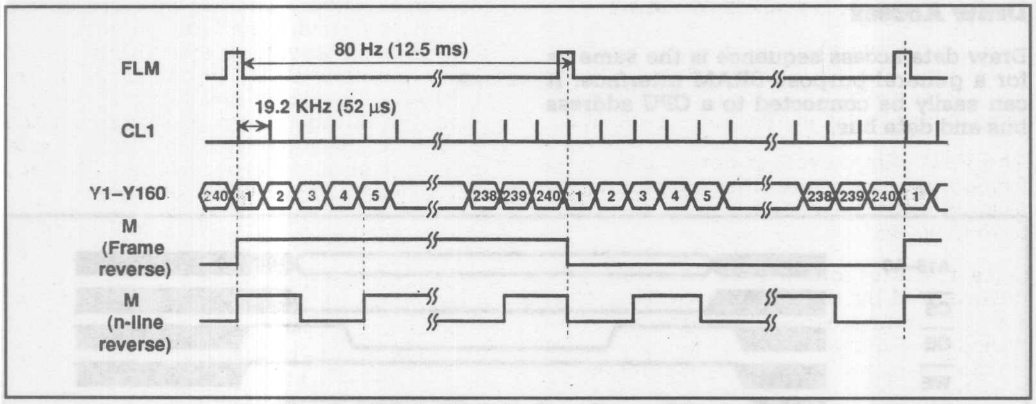


Figure 8 LCD Display Data Timing

Draw Access

Draw data access sequence is the same as for a general-purpose SRAM interface. It can easily be connected to a CPU address bus and data bus.

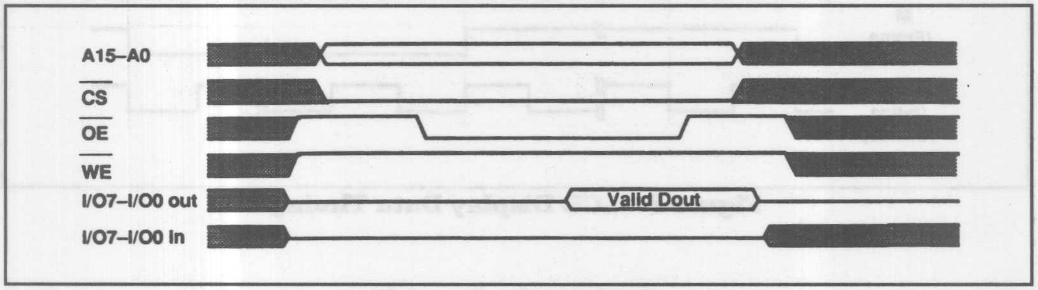


Figure 9 Read Cycle

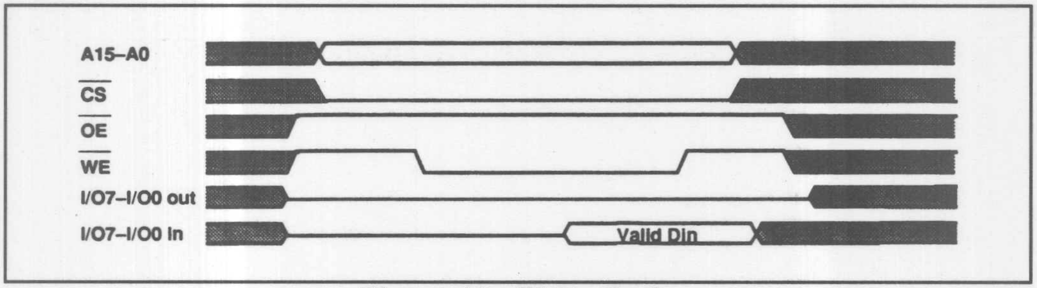


Figure 10 Write Cycle

Configuration of Display Data Bit

Packed Pixel Method

For grayscale display, multiple bits are needed for one pixel. In the HD66520, two bits are assigned to one pixel, enabling a four-level grayscale display.

One address (eight bits) specifies four pixels, and pixel bits 0 and 1 are managed as consecutive bits. When grayscale display data is manipulated in bit units, one memory access is sufficient, which enables smooth high-speed data rewriting.

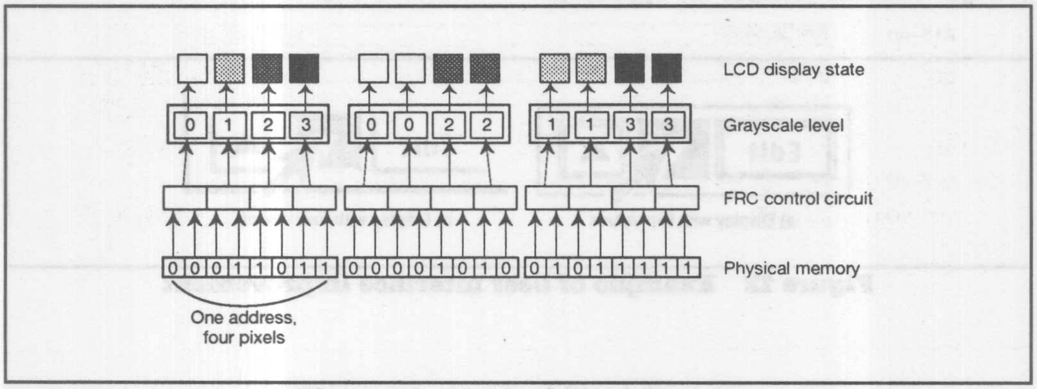


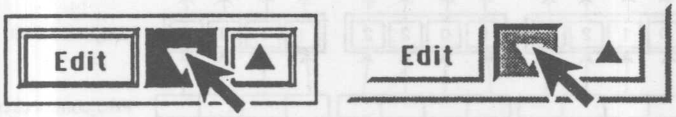
Figure 11 Packed Pixel System

Half Tone Display (FRC: Frame Rate Control Function)

The HD66520 incorporates an FRC function to display four-level grayscale half tone.

The FRC function utilizes liquid crystal characteristics whose brightness is changed by an effective value of applied voltage. Different voltages are applied to each frame and half brightness is expressed in addition to display on/off.

Since the HD66520 has two-bit gray-scale data per one pixel, it can display four-level grayscale and improve user interface (figure 12). Figure 13 shows the relationships between voltage patterns applied to each frame, the effective voltage value, and brightness obtained.



a) Display with two values

b) Display with four values

Figure 12 Example of User Interface Improvement

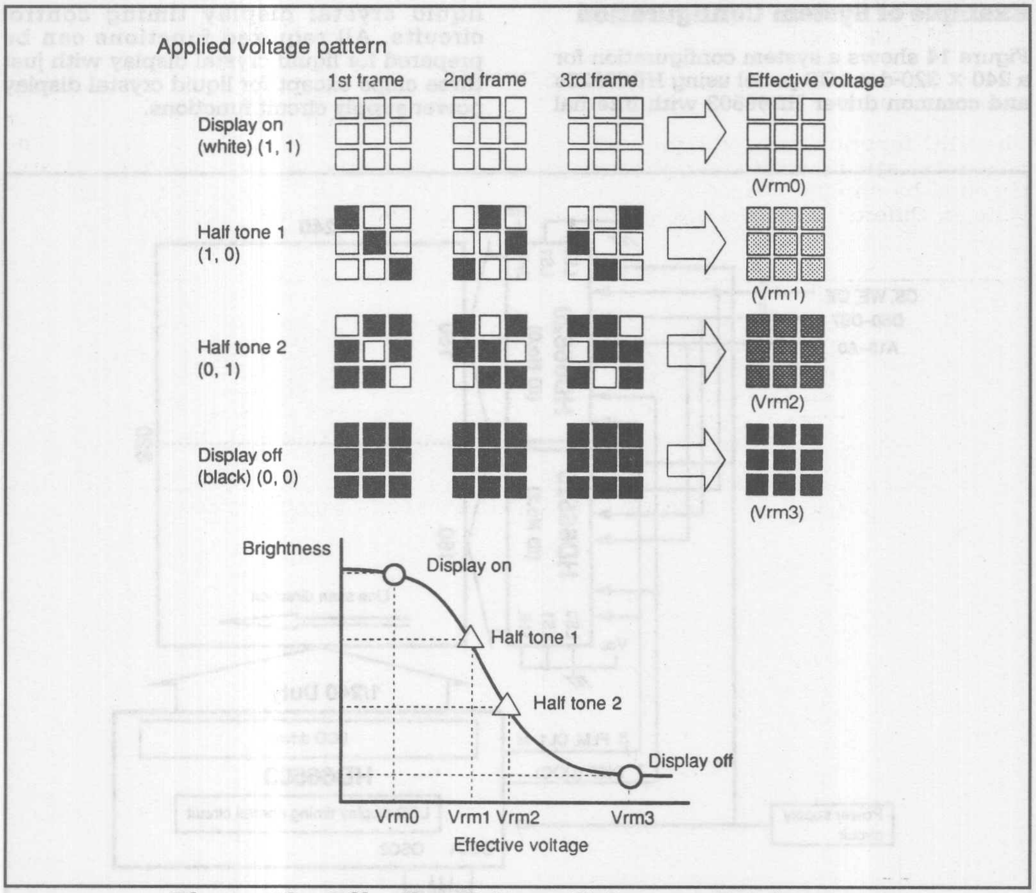


Figure 13 Effective Voltage Values vs. Brightness

Example of System Configuration

Figure 14 shows a system configuration for a 240 × 320-dot LCD panel using HD66520s and common driver HD66503 with internal liquid crystal display timing control circuits. All required functions can be prepared for liquid crystal display with just three chips except for liquid crystal display power supply circuit functions.

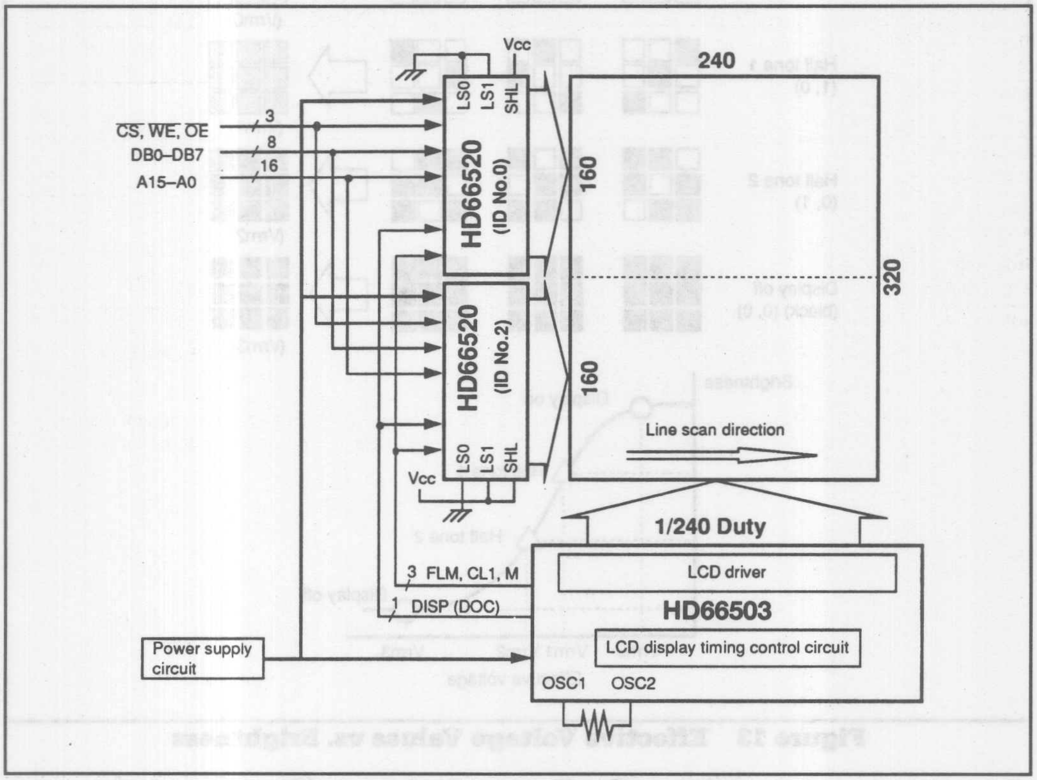


Figure 14 System Configuration

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Notes
Power voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	1
	LCD drive circuit	V_{EE}	V_{CC} –30.0 to V_{CC} +0.3	V	
Input voltage (1)		V_{T1}	–0.3 to V_{CC} +0.3	V	1, 2
Input voltage (2)		V_{T2}	V_{EE} –0.3 to V_{CC} +0.3	V	1, 3
Allowable output current		$\lvert Io \rvert$	<TBD>	mA	
Allowable total output current		$\lvert \Sigma Io \rvert$	<TBD>	mA	
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–40 to +125	°C	

Notes:
1. The reference point is GND (0 V).
2. Applies to pins LS_0, LS_1, SHL, FLM, CL_1, M, A_0 to A_{15}, DB_0 to DB_7, DISP, $\overline{CS}$, $\overline{WE}$, and $\overline{OE}$.
3. Applies to pins V_1, V_2, V_3, and V_4.
4. If the LSI is used beyond its absolute maximum rating, it may be permanently damaged. It should always be used within the limits of its electrical characteristics in order to prevent malfunction or unreliability.

Recommended Operating Conditions[1]

Item		Symbol	Min	Typ	Max	Unit	Notes
Power voltage	Logic circuit	V_{CC}	2.7	3.3	3.6	V	
	LCD drive circuit	V_{EE}	$V_{CC} - 10$	—	$V_{CC} - 28$	V	
Input high voltage for logic circuit		V_{IH}	$0.7 \times V_{CC}$	—	V_{CC}	V	1
Input low voltage for logic circuit		V_{IL}	0	—	$0.3 \times V_{CC}$	V	2
Operating temperature		T_{opr}	–20	25	75	°C	

Notes: 1. Max value is V_{CC} + 1 V when the pulse width is 10 ns or less.
2. Min value is – 1 V when the pulse width is 10 ns or less.

Recommended Operating Conditions[2]

Item		Symbol	Min	Typ	Max	Unit	Notes
Power voltage	Logic circuit	V_{CC}	4.5	5.0	5.5	V	
	LCD drive circuit	V_{EE}	$V_{CC} - 10$	—	$V_{CC} - 28$	V	
Input high voltage for logic circuit		V_{IH}	$0.7 \times V_{CC}$	—	V_{CC}	V	1
Input low voltage for logic circuit		V_{IL}	0	—	$0.3 \times V_{CC}$	V	2
Operating temperature		T_{opr}	–20	25	75	°C	

Notes: 1. Max value is V_{CC} + 1 V when the pulse width is 10 ns or less.
2. Min value is – 1 V when the pulse width is 10 ns or less.

Capacitance

Item	Symbol	Min	Typ	Max	Unit	Measuring Condition
Input capacitance	C_{in}	—		<TBD>	pF	V_{in} = 0 V
I/O capacitance	$C_{I/O}$	—	—	<TBD>	pF	T_a = 25°C f = 1 MHz

All these parameters are not measured but are sample values.

Electrical Characteristics

DC Characteristics[1] (V_{CC} = 2.7 V to 5.5 V, GND = 0 V, $V_{CC} - V_{EE}$ = 8 V to 28 V, T_a = –20°C to +75°C)

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Measurement Condition	Notes
Input high level voltage	V_{IH}		0.7 × V_{CC}	—	V_{CC}	V		
Input low level voltage	V_{IL}		0	—	0.3 × V_{CC}	V		
Output high level voltage	V_{OH}		V_{CC} – 0.4	—	—	V	I_{OH} = – 0.4 mA	
Output low level voltage	V_{OL}		—	—	0.4	V	I_{OL} = – 0.4 mA	
Vi–Yj on resistance	R_{ON}	Y1 to Y160 V1L/V1R, V2L/V2R, V3L/V3R, and V4L/V4R	—	1.0	2.0	kΩ	I_{ON} = 100 μA	1

Notes: 1. Indicates the resistance between one pin from Y1 to Y160 and another pin from V2L/V2R, V3L/V3R, V4L/V4R, and V_{EE}, when load current is applied to the Y pin; defined under the following conditions:

$V_{CC} - V_{LCD}$ = 28 V
V1L/V1R, V3L/V3R = V_{CC} – 2/10 ($V_{CC} - V_{EE}$)
V4L/V4R, V2L/V2R = V_{EE} + 2/10 ($V_{CC} - V_{EE}$)

V1L/V1R and V3L/V3R should be near the V_{CC} level, and V2L/V2R and V4L/V4R should be near the V_{EE} level. All voltage must be within ΔV. ΔV is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltages $V_{CC} - V_{EE}$. See figure 15.

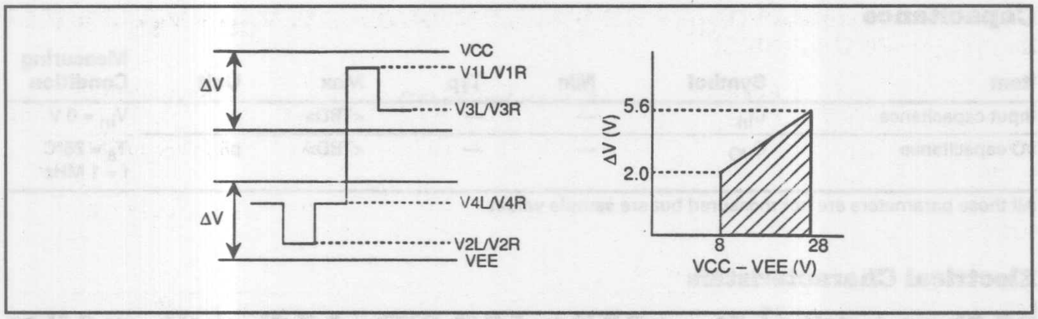


Figure 15 Relationship between Driver Output Waveform and Level Voltages

DC Characteristics[2] (V_{CC} = 2.7 V to 3.6 V, GND = 0 V, $V_{CC} - V_{EE}$ = 10 V to 28 V, T_a = –20°C to +75°C)

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Measurement Condition	Notes
Input leakage current (1)	I_{IL1}		–1.0	—	1.0	µA	$V_{IN} = V_{CC}$ to GND	
Input leakage current (2)	I_{IL2}	V1L/V1R, V2L/V2R, V3L/V3R, and V4L/V4R	–25	—	25	µA	$V_{IN} = V_{CC}$ to V_{EE}	
Power consumption during RAM access	I_{OC}	—	—	TBD	TBD	mA	t_{cyc} = 150 ns $V_{CC} - V_{EE}$ = 28 V	1
Power consumption in LCD drive part	I_{EE}	—	—	TBD	TBD	µA		
Power consumption during display operation	I_{DIS}	—	—	TBD	TBD	µA	T_{cyc} = 500 ms	1, 2

Notes: 1. Input and output currents are excluded. When a CMOS input is floating, excess current flows from the power supply through to the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.

2. Indicates the current when the display-operation memory access is idling.

DC Characteristics[3] (V_{CC} = 4.5 V to 5.5 V, GND = 0 V, $V_{CC} - V_{EE}$ = 8 V to 28 V, T_a = –20°C to +75°C)

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Measurement	Notes
Input leakage current (1)	I_{IL1}		–1.0	—	1.0	µA	$V_{IN} = V_{CC}$ to GND	
Input leakage current (2)	I_{IL2}	V1L/V1R, V2L/V2R, V3L/V3R, and V4L/V4R	–25	—	25	µA	$V_{IN} = V_{CC}$ to V_{EE}	
Power consumption during RAM access	I_{OC}	—	—	TBD	TBD	mA	t_{cyc} = 150 ns $V_{CC} - V_{EE}$ = 28 V	1
Power consumption in LCD drive part	I_{LCD}	—	—	TBD	TBD	µA		
Power consumption during display operation	I_{DIS}	—	—	TBD	TBD	µA	T_{cyc} = 500 ms	1, 2

Notes: 1. Input and output currents are excluded. When a CMOS input is floating, excess current flows from the power supply through to the input circuit. To avoid this, V_{IH}, and V_{IL} must be held to V_{CC} and GND levels, respectively.

2. Indicates the current when the display-operation memory access is idling.

AC Characteristics[1] (V_{CC} = 2.7 V to 5.5 V, GND = 0 V, $V_{CC} - V_{EE}$ = 8 V to 28 V, T_a = –20°C to +75°C)

Display-Data Transfer Timing

No.	Item	Symbol	Applicable Pins	Min	Max	Unit	Notes
1	Clock cycle time	t_{CYC}	CL1	10		µs	
2	CL1 high-level width	t_{CWH}	CL1	<TBD>		ns	
3	CL1 low-level width	t_{CWL}	CL1	1.0	—	µs	
4	CL1 rise time	t_r	CL1	—	50	ns	
5	CL1 fall time	t_f	CL1	—	50	ns	
6	FLM setup time	t_{FS}	FLM, CL1	<TBD>	—	ns	
7	FLM hold time	r_{FH}	FLM, CL1	<TBD>	—	ns	

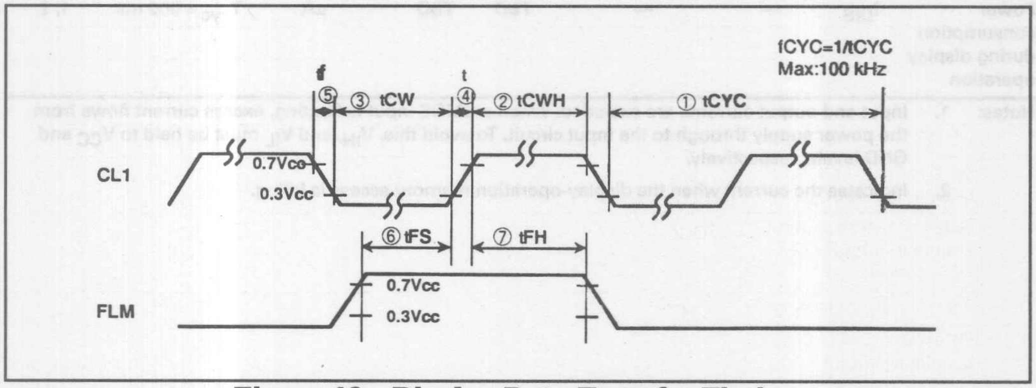


Figure 16 Display Data Transfer Timing

AC Characteristics[1] (V_{CC} = 4.5 V to 5.5 V, GND = 0 V, $V_{CC} - V_{EE}$ = 8 V to 28 V, T_a = –20°C to +75°C)

Draw Access Timing 1

Common Items

No.	Item	Symbol	Min	Max	Unit	Notes
1	Address setup time	t_{AS}	20	—	ns	
2	Address hold time	t_{AH}	0	—	ns	
3	Chip select time	t_{CW}	40	$t_{CYC} - 50$	ns	

Read Cycle

No.	Item	Symbol	Min	Max	Unit	Notes
1	Read cycle time	t_{RC}	60	—	ns	
2	Address access time	t_{AA}	—	20	ns	
3	Chip select access time	t_{ACS}	—	20	ns	
4	CS output set time	t_{CLZ}	0	—	ns	
5	CS setup time	t_{CSS}	0	—	ns	
6	CS hold time	t_{CSH}	0	—	ns	
7	OE low level width	t_{OLW}	40	—	ns	
8	Delay time from output-enable to output	t_{OE}	0	20	ns	
9	Delay time from output-enable to output (low impedance)	t_{OLZ}	0	—	ns	
10	CS and output floating	t_{CHZ}	0	10	ns	
11	Delay time from output-disable to output	t_{OHZ}	0	10	ns	
12	Output hold time	t_{OH}	5	—	ns	
13	Output voltage rise/fall time	t_T	—	50	ns	

Write Cycle

No.	Item	Symbol	Min	Max	Unit	Notes
1	Write cycle time	t_{WC}	60	—	ns	
2	Address valid time	t_{AW}	60	—	ns	
3	Write pulse width	t_{WP}	40	20	ns	
4	Delay time from output-disable to output	t_{OHZ}	0	10	ns	
5	Input data set time	t_{DW}	30	—	ns	
6	Input data hold time	t_{DH}	5	—	ns	

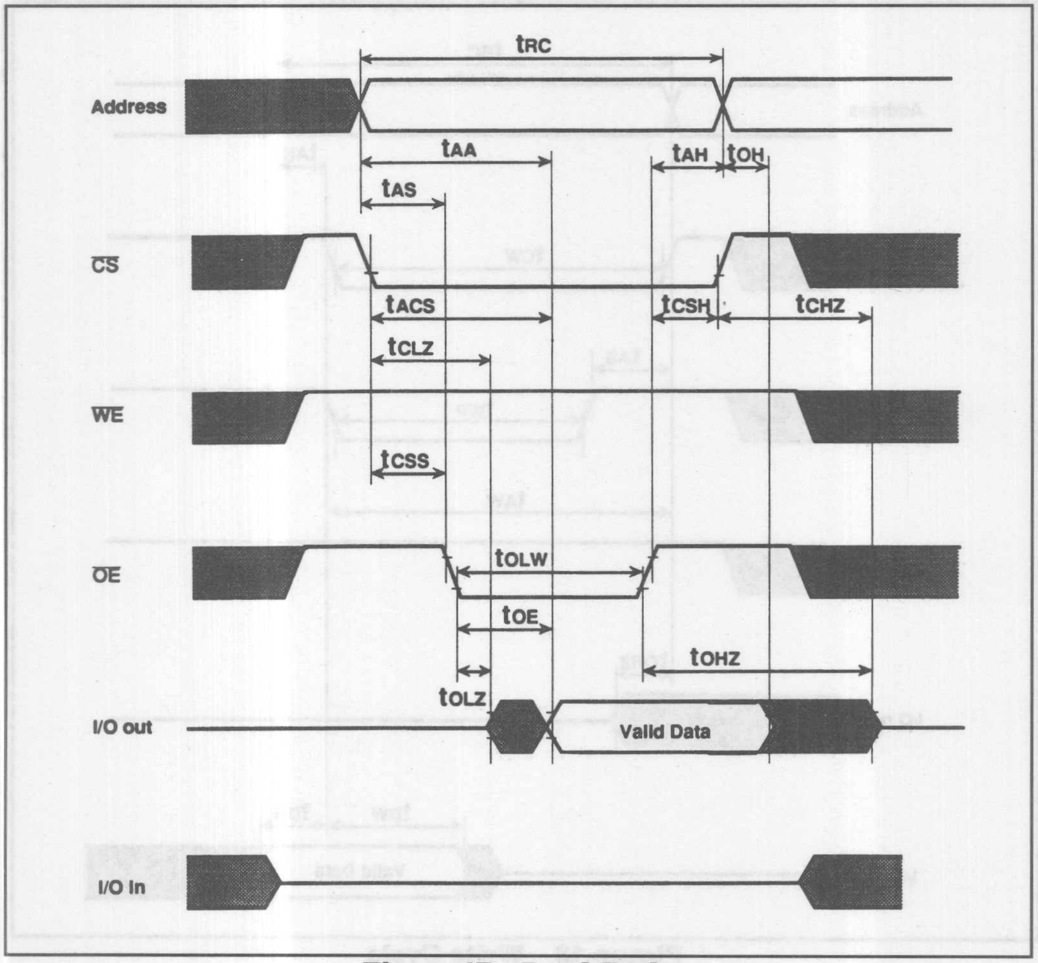


Figure 17 Read Cycle

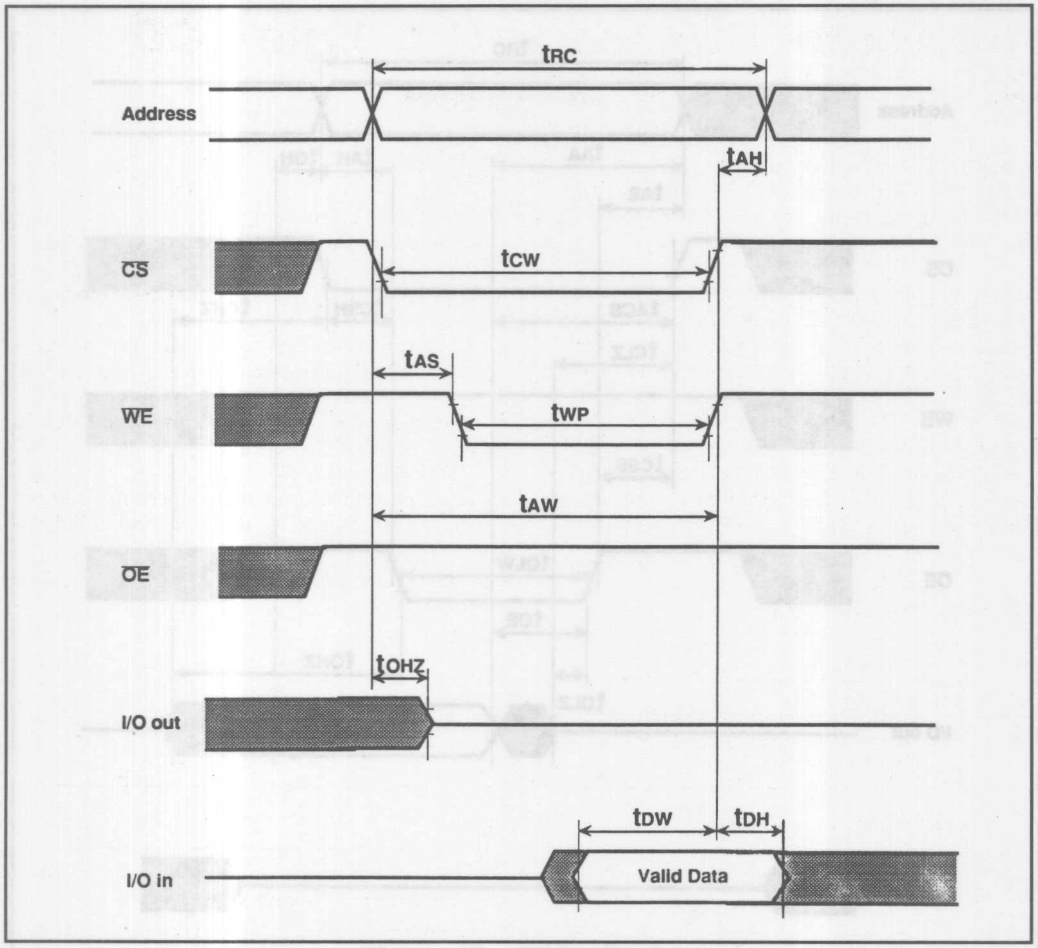


Figure 18 Write Cycle

HD66300T (Horizontal Driver for TFT-Type LCD Color TV)

The HD66300T is a horizontal driver used for TFT-type (Thin Film Transistor) LCD color TVs. Specifically, it drives the drain bus signals of a TFT-type LCD panel.

The HD66300T receives as input three video signals R, G, B, and their inverted signals $\overline{R}$, $\overline{G}$ and $\overline{B}$. Internal sample and hold circuitry then samples and holds these signals before outputting them via voltage followers to drive a TFT-type LCD panel.

The HD66300T can drive LCD panels from 480 x 240 pixels middle-resolution up to 720 x 480 pixels high-resolution. It has 120 LCD drive outputs and enables design of a compact LCD TV due to TCP (Tape Carrier Package) technology.

Features

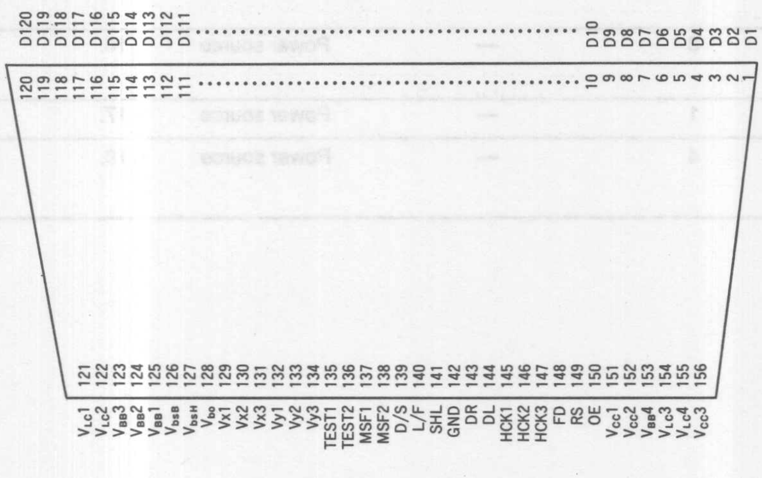
- LCD drive outputs: 120
- Internal sample and hold circuits: 480 (4 circuits per output)
- Support of single-rate sequential drive mode and double-rate sequential drive mode
- Support of various types of color filter arrangements through an internal color sequence controller
- Vertical pixels: 240 (middle-resolution) or 480 (high-resolution)
- Horizontal pixels: 480 to 720
- Support of monodirectional connection mode and interleaved connection mode through a bidirectional shift register
- Dynamic range: 15 V_{PP}
- Power supply: +5 V and –15 V
- CMOS process

Ordering Information

Type No.	Package
HD66300T00	156-pin TCP

Note: The details of TCP pattern are shown in "The Information of TCP."

Pin Arrangement



(Top View)

Note: This does not apply to TCP dimensions.

Pin Description

Pin List

Pin Name	Number of Pins	Input/Output	Connected to	Functions (Refer to)
D1 - D120	120	O	LCD panel	1.
HCK1, HCK2, HCK3	3	I	Controller	2.
DL, DR	2	I/O	Controller or next HD66300T	3.
FD	1	I	Controller	4.
RS	1	I	GND	5.
OE	1	I	Controller	6.
SHL	1	I	V_{CC} or GND	7.
D/S	1	I	V_{CC} or GND	8.
L/F	1	I	V_{CC} or GND	9.
MSF1, MSF2	2	I	V_{CC} or GND	10.
TEST1, TEST2	2	I	GND	11.
Vx1, Vx2, Vx3, Vy1, Vy2, Vy3	6	I	Inverter	12.
V_{bo}	1	I	Power source	13.
V_{bsB}, V_{bsH}	2	I	Power source	14.
$V_{LC}1$, $V_{LC}2$, $V_{LC}3$, $V_{LC}4$	4	—	Power source	15.
$V_{CC}1$, $V_{CC}2$, $V_{CC}3$	3	—	Power source	16.
GND	1	—	Power source	17.
$V_{BB}1$, $V_{BB}2$, $V_{BB}3$, $V_{BB}4$	4	—	Power source	18.

Pin Functions

1. D1 - D120: These pins output LCD drive signals.

2. HCK1, HCK2, HCK3: These pins input three-phase clock pulses, which determine the signal sampling timing for sample and hold circuits.

3. DL, DR: These pins input or output data into or from the internal bidirectional shift register. The state of pin SHL determines whether these pins input or output data.

SHL	DL	DR
V_{CC}	Output	Input
GND	Input	Output

4. FD: This pin inputs the field determination signal, which allows the sample and hold circuitry and the shift matrix circuit to operate synchronously with TV signals, at its rising and falling edge.

FD = high: First field

FD = low: Second field

When a non-interlace signal is applied, it must be inverted every field.

When an interlace signal is applied in double-rate sequential drive mode with per-line inversion (mode 1, 2, 3), the signal must be set high in both fields. The signal must be set low, however, in each field's horizontal retrace period.

5. RS: This pin inputs a test signal and should be connected to pin GND.

6. OE: This pin inputs the signal which controls the controller of the shift matrix circuit; it changes the selection of a sample and hold circuit and the shift matrix (combination of color data), at its rising edge. It also switches the bias current of the output buffer, as shown in the following table.

OE	Bias Current of Output Buffer
High	Large current (determined by VbsB)
Low	Small current (determined by VbsH)

7. SHL: This pin selects the shift direction of the shift register.

SHL	Shift Direction
High	DL ← DR
Low	DL → DR

8. D/S: This pin selects the LCD drive mode.

D/S	Mode
High	Double-rate sequential drive mode
Low	Single-rate sequential drive mode

9. L/F: This pin selects the inversion mode of LCD drive signals.

L/F	Mode
High	Per-line inversion mode
Low	Per-field inversion mode

10. MSF1, MSF2: These pins select the function of the shift matrix circuit; they should be set according to both the type of color filter arrangement on a TFT-type LCD panel and the drive mode.

Filter Arrangement	Drive Mode	MSF1	MSF2
Diagonal mosaic pattern	Single-rate	GND	V_{CC}/GND*
	Double-rate	GND	V_{CC}/GND*
Vertical stripe pattern	Single-rate	V_{CC}	V_{CC}
	Double-rate	V_{CC}	V_{CC}
Unicolor triangular pattern	Single-rate	V_{CC}	V_{CC}
	Double-rate	V_{CC}	GND
Bicolor triangular pattern	Single-rate	V_{CC}	GND
	Double-rate	V_{CC}	GND

Single-rate: Single-rate sequential drive mode
Double-rate: Double-rate sequential drive mode
Note * Refer to table2 and timing charts of each mode

11. TEST1, TEST2: These pins input test signals and should be connected to pin GND.

12. Vx1, Vx2, Vx3, Vy1, Vy2, Vy3: Video signals are applied to these pins; in general, positive video signals are connected to pins Vxi and negative video signals to pins Vyi.

13. V_{bo}: Bias voltage is applied to this pin for the differential amplifier in the sample and hold circuitry.

14. V_{bsB}, V_{bsH}: Bias voltage is applied to this pin for the two power sources of the output buffer.
VbsB: The voltage for driving a capacitive load
VbsH: The voltage for holding the output voltage

15. V_{LC}1, V_{LC}2, V_{LC}3, V_{LC}4: +5 V LCD drive voltage is applied to these pins.

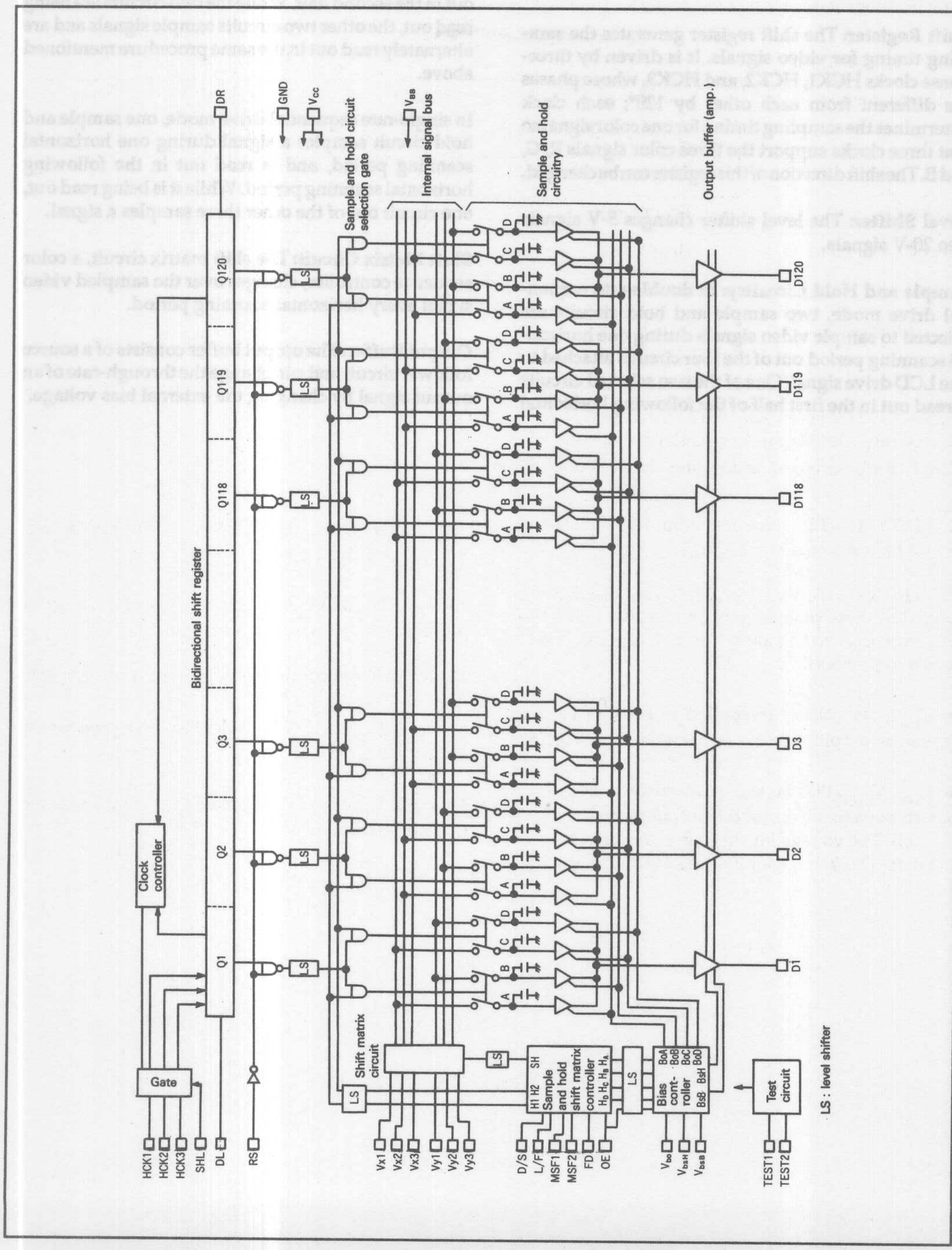
16. V_{CC}1, V_{CC}2, V_{CC}3, V_{CC}4: +5 V is applied to these pins for the logic and the analog units.

17. GND: 0 V is applied to this pin for the logic unit.

18. V_{BB}1, V_{BB}2: –15 V is applied to these pins for the LCD drive unit.

19. V_{BB}3, V_{BB}4: –15 V is applied to these pins for the LCD drive unit.

Internal Block Diagram



Block Functions

Shift Register: The shift register generates the sampling timing for video signals. It is driven by three-phase clocks HCK1, HCK2, and HCK3, whose phases are different from each other by 120°; each clock determines the sampling timing for one color signal so that three clocks support the three color signals R, G, and B. The shift direction of this register can be changed.

Level Shifter: The level shifter changes 5-V signals into 20-V signals.

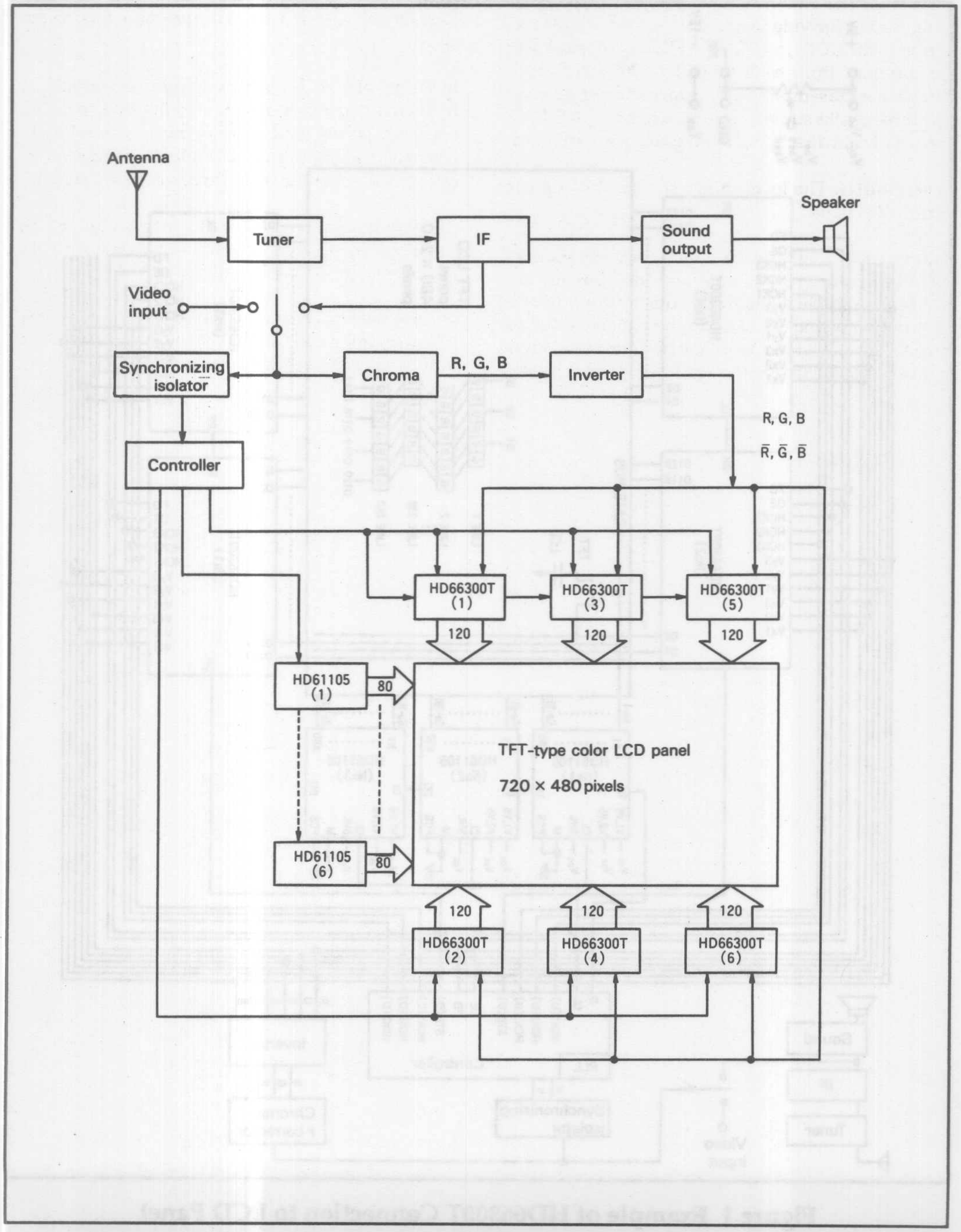
Sample and Hold Circuitry: In double-rate sequential drive mode, two sample and hold circuits are selected to sample video signals during one horizontal scanning period out of the four circuits attached to one LCD drive signal. One of the two selected circuits is read out in the first half of the following horizontal scanning period, and the other selected circuit is read out in the second half. While the two circuits are being read out, the other two circuits sample signals and are alternately read out in the same procedure mentioned above.

In single-rate sequential drive mode, one sample and hold circuit samples a signal during one horizontal scanning period, and is read out in the following horizontal scanning period. While it is being read out, one circuit out of the other three samples a signal.

Shift Matrix Circuit: The shift matrix circuit, a color sequence controller, changes over the sampled video signal every horizontal scanning period.

Output Buffer: The output buffer consists of a source follower circuit and can change the through-rate of an output signal by changing the external bias voltage.

System Block Configuration Example



Example of HD66300T Connection to LCD Panel

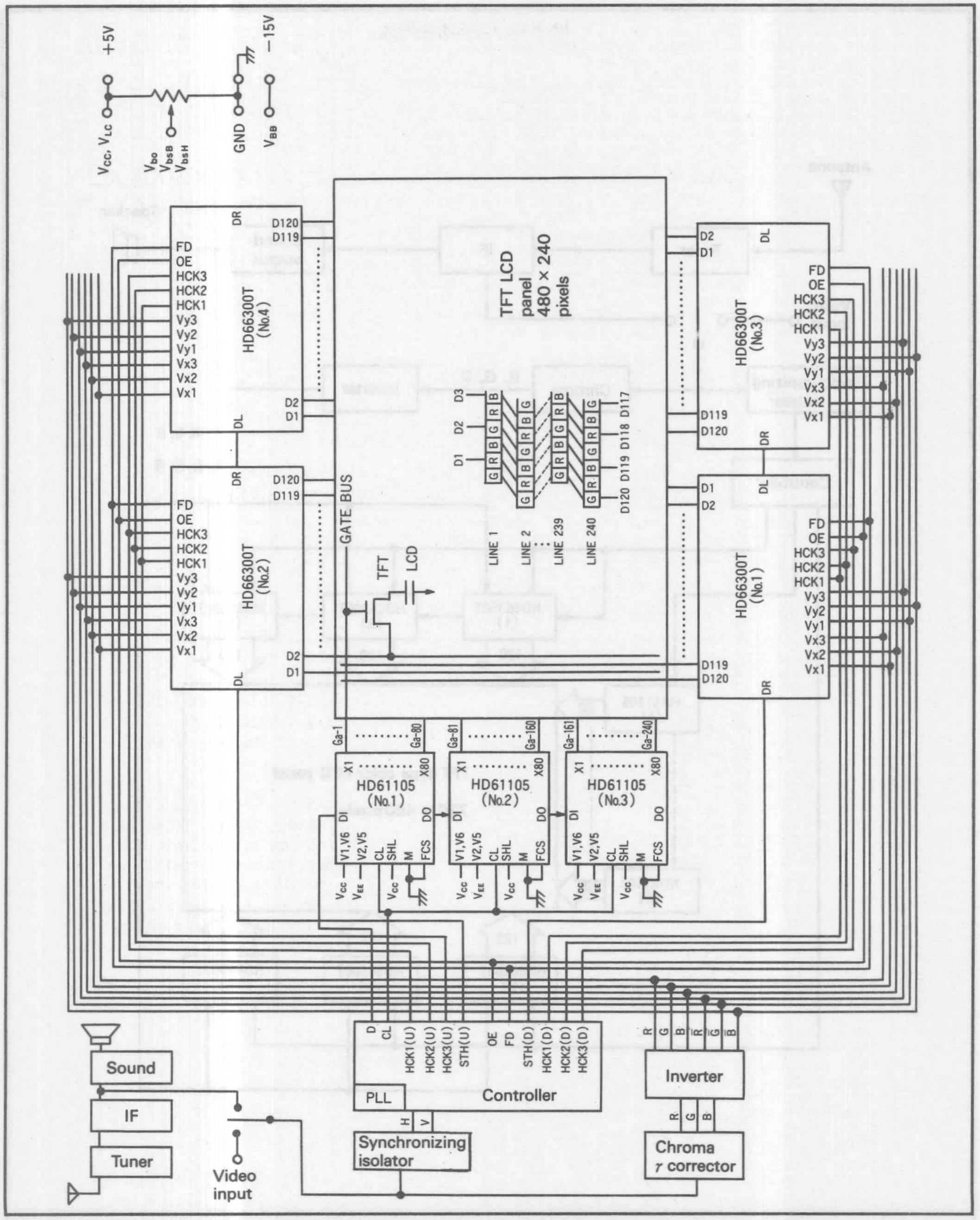


Figure 1 Example of HD66300T Connection to LCD Panel

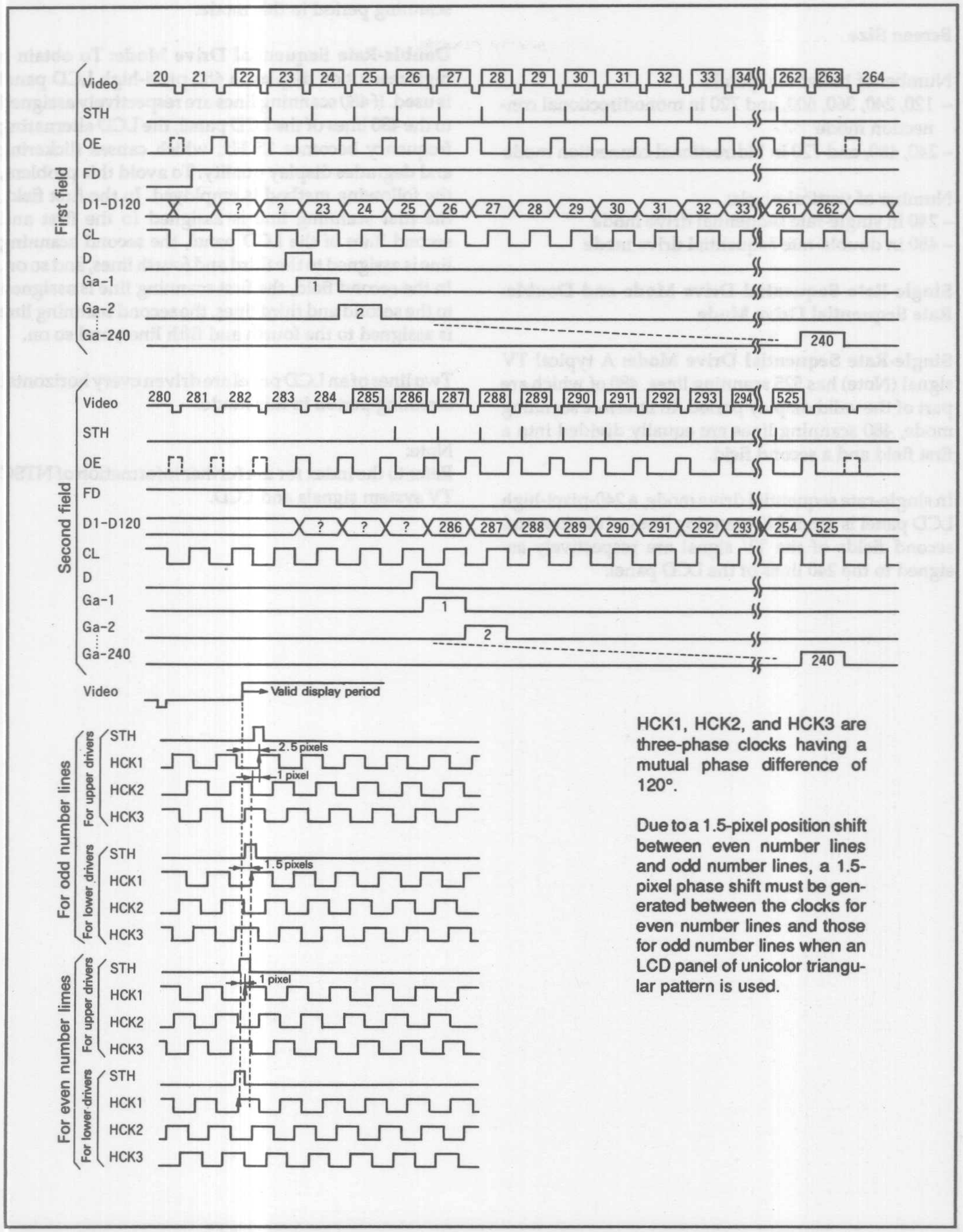


Figure 2 Timing chart

Functional Description

Screen Size

Number of horizontal pixels:
- 120, 240, 360, 600, and 720 in monodirectional connection mode
- 240, 480, and 720 in bidirectional connection mode

Number of vertical pixels:
- 240 in single-rate sequential drive mode
- 480 in double-rate sequential drive mode

Single-Rate Sequential Drive Mode and Double-Rate Sequential Drive Mode

Single-Rate Sequential Drive Mode: A typical TV signal (Note) has 525 scanning lines, 480 of which are part of the valid display period. In interlace scanning mode, 480 scanning lines are equally divided into a first field and a second field.

In single-rate sequential drive mode, a 240-pixel-high LCD panel is used. 240 scanning lines of the first and second fields of the TV signal are respectively assigned to the 240 lines of the LCD panel.

One line of an LCD panel is driven every horizontal scanning period in this mode.

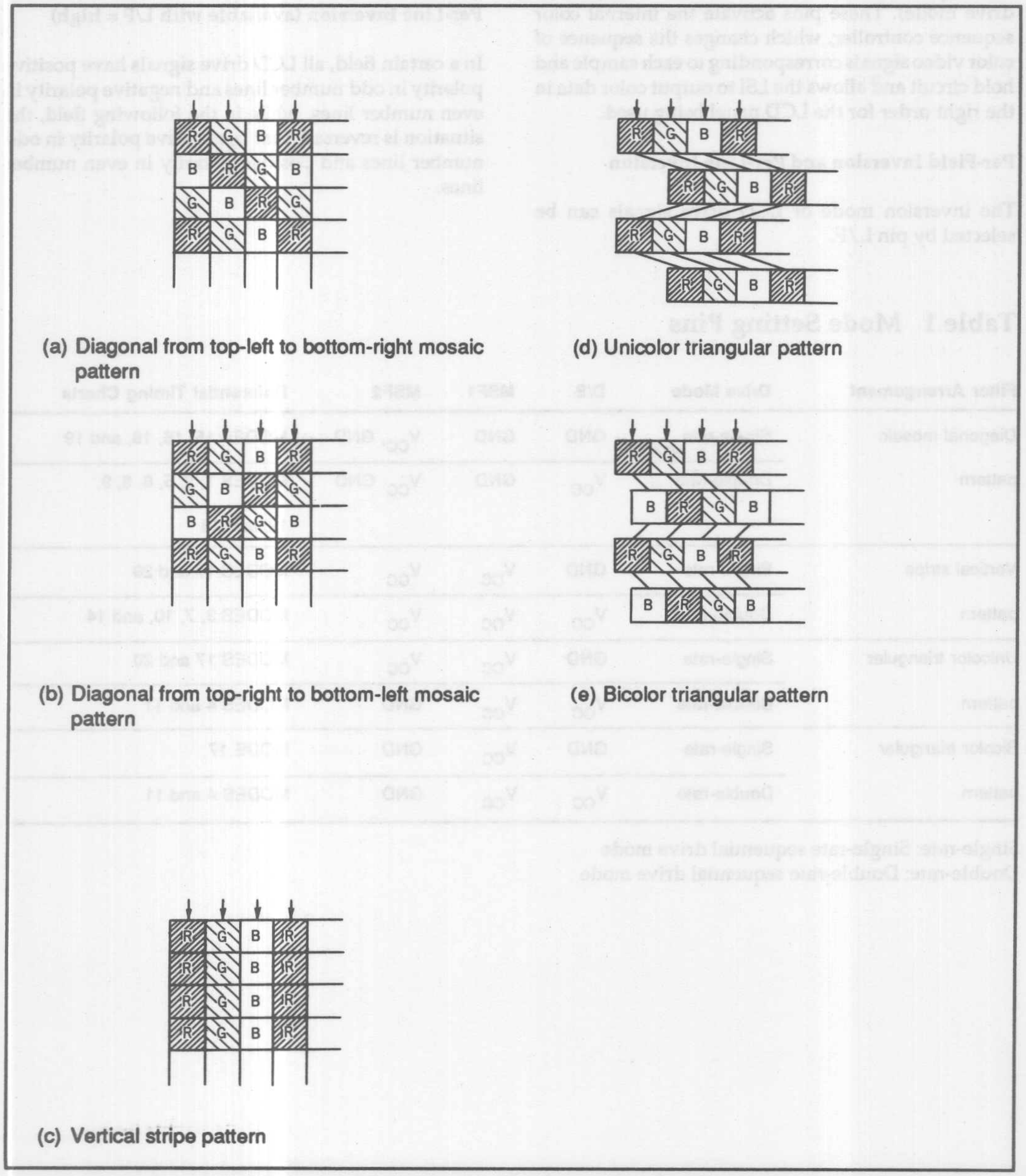
Double-Rate Sequential Drive Mode: To obtain a high-resolution display, a 480-pixel-high LCD panel is used. If 480 scanning lines are respectively assigned to the 480 lines of the LCD panel, the LCD alternating frequency becomes 15 Hz, which causes flickering and degrades display quality. To avoid this problem, the following method is employed. In the first field, the first scanning line is assigned to the first and second lines of the LCD panel, the second scanning line is assigned to the third and fourth lines, and so on. In the second field, the first scanning line is assigned to the second and third lines, the second scanning line is assigned to the fourth and fifth lines, and so on.

Two lines of an LCD panel are driven every horizontal scanning period in this mode.

Note:
Refer to the index for the further information of NTSC TV system signals and LCD.

Supportable Types of Color Filter Arrangements

The order and timing for the HD66300T to output color signals depend on the color filter arrangement on a TFT-type LCD panel. The HD66300T can support TFT-type LCD panels having the following color filter arrangements by specifying the operation of the internal color sequence controller and by changing the external signals to be supplied.



(a) Diagonal from top-left to bottom-right mosaic pattern

(b) Diagonal from top-right to bottom-left mosaic pattern

(c) Vertical stripe pattern

(d) Unicolor triangular pattern

(e) Bicolor triangular pattern

Figure 3 Supportable Types of Color Filter Arrangements

Mode Setting Pins

Mode setting pins MSF1, MSF2, and D/S must be set according to both the type of color filter arrangement on the TFT-type LCD panel and the drive mode (single-rate sequential drive mode or double-rate sequential drive mode). These pins activate the internal color sequence controller, which changes the sequence of color video signals corresponding to each sample and hold circuit and allows the LSI to output color data in the right order for the LCD panel being used.

Per-Field Inversion and Per-Line Inversion

The inversion mode of LCD drive signals can be selected by pin L/F.

Per-Field Inversion (available with L/F = low)

In a certain field, all LCD drive signals have one polarity and in the following field, they all have the inverted polarity.

Per-Line Inversion (available with L/F = high)

In a certain field, all LCD drive signals have positive polarity in odd number lines and negative polarity in even number lines, while in the following field, the situation is reversed, that is, negative polarity in odd number lines and positive polarity in even number lines.

Table 1 Mode Setting Pins

Filter Arrangement	Drive Mode	D/S	MSF1	MSF2	Referential Timing Charts
Diagonal mosaic	Single-rate	GND	GND	V_{CC}, GND	MODES 15, 16, 18, and 19
pattern	Double-rate	V_{CC}	GND	V_{CC}, GND	MODES 1, 2, 5, 6, 8, 9, 12, and 13
Vertical stripe	Single-rate	GND	V_{CC}	V_{CC}	MODES 17 and 20
pattern	Double-rate	V_{CC}	V_{CC}	V_{CC}	MODES 3, 7, 10, and 14
Unicolor triangular	Single-rate	GND	V_{CC}	V_{CC}	MODES 17 and 20
pattern	Double-rate	V_{CC}	V_{CC}	GND	MODES 4 and 11
Bicolor triangular	Single-rate	GND	V_{CC}	GND	MODE 17
pattern	Double-rate	V_{CC}	V_{CC}	GND	MODES 4 and 11

Single-rate: Single-rate sequential drive mode
Double-rate: Double-rate sequential drive mode

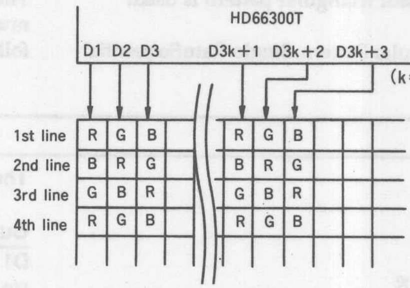
Interface

Video Signals Connection

Video signals must be connected to pins Vx1, Vx2, Vx3, Vy1, Vy2, and Vy3; in principle, positive video signals R, G, and B signals must be input to pins Vx1, Vx2, and Vx3, and negative video signals $\overline{R}$, $\overline{G}$, and $\overline{B}$ to pins Vy1, Vy2, and Vy3. For actual connection between an LCD panel and the LCD drive signal output pins, refer to the following example.

In the case of Diagonal from top-left to bottom-right mosaic pattern.

This example describes the case in which an LCD panel having a diagonal from top-left to bottom-right mosaic pattern is driven in double-rate sequential drive mode and monodirectional connection mode.



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (=D3k + 1)	R → B → G → R →
D2 (=D3k + 2)	G → R → B → G →
D3 (=D3k + 3)	B → G → R → B →

The Signal Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (=D3k + 1)	Vx1 → Vx3 → Vx2 → Vx1 →
D2 (=D3k + 2)	Vx2 → Vx1 → Vx3 → Vx2 →
D3 (=D3k + 3)	Vx3 → Vx2 → Vx1 → Vx3 →

(Refer to MODE 5)

The Connection of Signals

Signal	Color
Vx1	R
Vx2	G
Vx3	B
Vy1	$\overline{R}$
Vy2	$\overline{G}$
Vy3	$\overline{B}$

In the case of Diagonal from top-right to bottom-left mosaic pattern, Vertical stripe pattern

The same procedure for video signal connection applies to the case in which a TFT-type LCD panel having a diagonal from top-right to bottom-left mosaic pattern or a vertical stripe pattern is used, as well as to the cases where a panel of any pattern is used through the bidirectional connection mode.

Triangular Pattern, Single-Rate Sequential Drive Mode

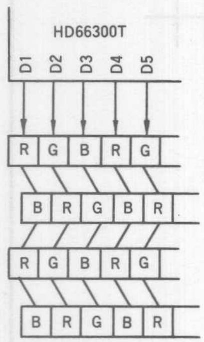
The following procedures are required when a panel of unicolor or bicolor triangular pattern is used:

1. Unicolor Triangular Pattern, Single-Rate Sequential Drive Mode

The clock phase must be changed every line because of the 1.5-pixel phase shift between even number lines and odd number lines. (Refer to the explanation of sampling clocks.)
The connection of signals here is the same as that described above.

2. Bicolor Triangular Pattern, Single-Rate Sequential Drive Mode

The clock phase must be changed every line because of the 0.5-pixel phase shift between even number lines and odd number lines. (Refer to the explanation of sampling clocks.)
The connection of video signals in the second field must be changed from that in the first field. See the following tables.



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (=D3k + 1)	R → B → R → B →
D2 (=D3k + 2)	G → R → G → R →
D3 (=D3k + 3)	B → G → B → G →

The Signal Sequence for Each Output Pin

	Output Pin	Signal Sequence
1st field	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (=D3k + 1)	Vy1 → Vx1 → Vy1 → Vx1 →
	D2 (=D3k + 2)	Vy2 → Vx2 → Vy2 → Vx2 →
	D3 (=D3k + 3)	Vy3 → Vx3 → Vy3 → Vx3 →

(Refer to Mode 17)

The Connection of Signal in Each Field

	Per-Field Inversion Mode (L/F = low)		Per-Line Inversion Mode (L/F =high)	
	1st Field	2nd Field	1st Field	2nd Field
Vx1	R	$\overline{B}$	R	B
Vx2	G	$\overline{R}$	G	R
Vx3	B	$\overline{G}$	B	G
Vy1	B	$\overline{R}$	$\overline{B}$	$\overline{R}$
Vy2	R	$\overline{G}$	$\overline{R}$	$\overline{G}$
Vy3	G	$\overline{B}$	$\overline{G}$	$\overline{B}$

Triangular Pattern, Double-Rate Sequential Drive Mode

Changing the phase of the sampling clocks is sufficient when the panel is driven in single-rate sequential drive mode. However, when the panel is driven in double-rate sequential drive mode, the above countermeasure does not work, since the display data for two lines is sampled at one time here. Consequently, delaying the input video signal for a time period corresponding to the shift between pixels is required.

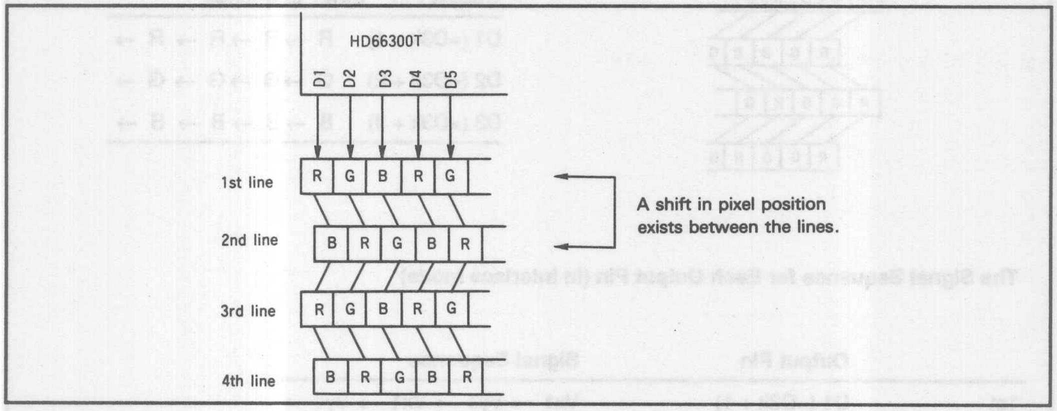


Figure 4

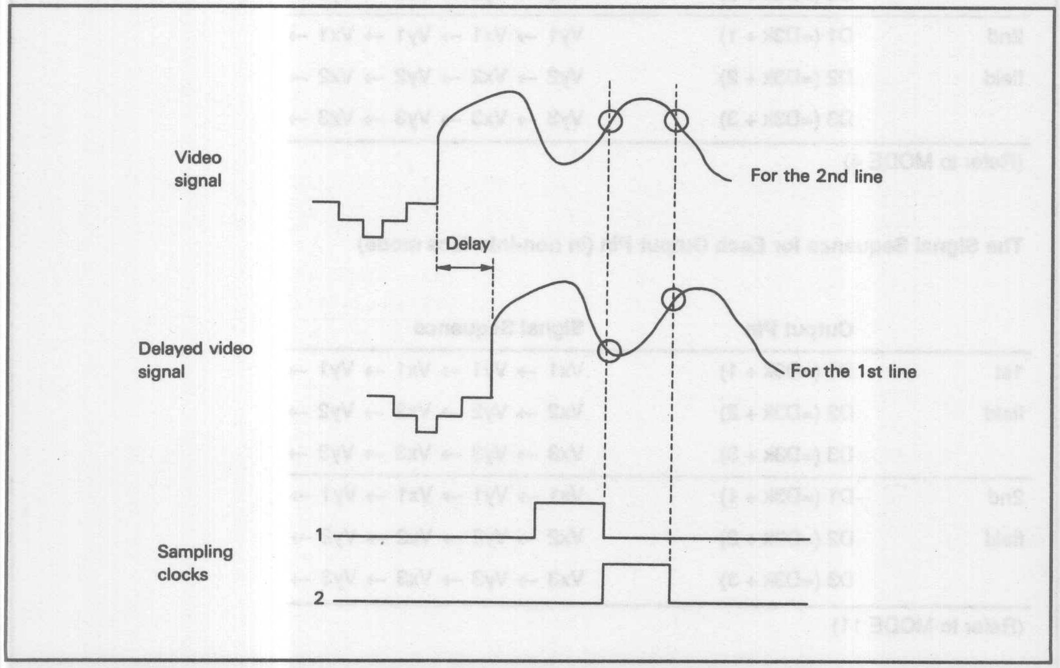
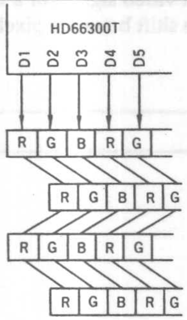


Figure 5

1. Unicolor Triangular Pattern, Double-Rate Sequential Drive Mode



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (=D3k + 1)	R → R → R → R →
D2 (=D3k + 2)	G → G → G → G →
D3 (=D3k + 3)	B → B → B → B →

The Signal Sequence for Each Output Pin (In interlace mode)

	Output Pin	Signal Sequence
1st	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
field	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd	D1 (=D3k + 1)	Vy1 → Vx1 → Vy1 → Vx1 →
field	D2 (=D3k + 2)	Vy2 → Vx2 → Vy2 → Vx2 →
	D3 (=D3k + 3)	Vy3 → Vx3 → Vy3 → Vx3 →

(Refer to MODE 4)

The Signal Sequence for Each Output Pin (In non-interlace mode)

	Output Pin	Signal Sequence
1st	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
field	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
field	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →

(Refer to MODE 11)

1. Unicolor Triangular Pattern, Double-Rate Sequential Drive Mode (Cont.)

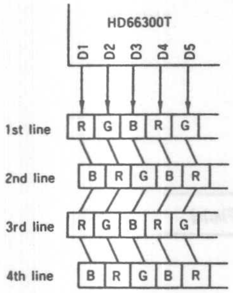
The Connection of Signals in Each Field in Interlace Mode

	Per-Field Inversion Mode (L/F = low)		Per-Line Inversion Mode (L/F =high)	
	1st Field	**2nd Field**	**1st Field**	**2nd Field**
Vx1	Delayed R	$\overline{R}$	Delayed R	R
Vx2	Delayed G	$\overline{G}$	Delayed G	G
Vx3	Delayed B	$\overline{B}$	Delayed B	B
Vy1	R	Delayed $\overline{R}$	$\overline{R}$	Delayed $\overline{R}$
Vy2	G	Delayed $\overline{G}$	$\overline{G}$	Delayed $\overline{G}$
Vy3	B	Delayed $\overline{B}$	$\overline{B}$	Delayed $\overline{B}$

The Connection of Signals in Each Field in Non-interlace Mode

	Per-Field Inversion Mode (L/F = low)		Per-Line Inversion Mode (L/F =high)	
	1st Field	**2nd Field**	**1st Field**	**2nd Field**
Vx1	Delayed R	Delayed $\overline{R}$	Delayed R	Delayed $\overline{R}$
Vx2	Delayed G	Delayed $\overline{G}$	Delayed G	Delayed $\overline{G}$
Vx3	Delayed B	Delayed $\overline{B}$	Delayed B	Delayed $\overline{B}$
Vy1	R	$\overline{R}$	$\overline{R}$	R
Vy2	G	$\overline{G}$	$\overline{G}$	G
Vy3	B	$\overline{B}$	$\overline{B}$	B

2. Bicolor Triangular Pattern, Double-Rate Sequential Drive Mode



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (=D3k + 1)	R → R → R → R →
D2 (=D3k + 2)	G→ R → G → R →
D3 (=D3k + 3)	B → G → B → G →

The Signal Sequence for Each Output Pin (In interlace mode)

	Output Pin	Signal Sequence
1st	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
field	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd	D1 (=D3k + 1)	Vy1 → Vx1 → Vy1 → Vx1 →
field	D2 (=D3k + 2)	Vy2 → Vx2 → Vy2 → Vx2 →
	D3 (=D3k + 3)	Vy3 → Vx3 → Vy3 → Vx3 →

(Refer to MODE 4)

The Signal Sequence for Each Output Pin (In non-interlace mode)

	Output Pin	Signal Sequence
1st	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
field	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
field	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →

(Refer to MODE 11)

2. Bicolor Triangular Pattern, Double-Rate Sequential Drive Mode (Cont.)

The Connection of Signals in Each Field in Interlace Mode

	Per-Field Inversion Mode (L/F = low)		Per-Line Inversion Mode (L/F =high)	
	1st Field	2nd Field	1st Field	2nd Field
Vx1	Delayed R	$\overline{B}$	Delayed R	B
Vx2	Delayed G	$\overline{R}$	Delayed G	R
Vx3	Delayed B	$\overline{G}$	Delayed B	G
Vy1	B	Delayed $\overline{R}$	$\overline{B}$	Delayed $\overline{R}$
Vy2	R	Delayed $\overline{G}$	$\overline{R}$	Delayed $\overline{G}$
Vy3	G	Delayed $\overline{B}$	$\overline{G}$	Delayed $\overline{B}$

The Connection of Signals in Each Field in Non-interlace Mode

	Per-Field Inversion Mode (L/F = low)		Per-Line Inversion Mode (L/F =high)	
	1st Field	2nd Field	1st Field	2nd Field
Vx1	Delayed R	Delayed $\overline{R}$	Delayed R	Delayed $\overline{R}$
Vx2	Delayed G	Delayed $\overline{G}$	Delayed G	Delayed $\overline{G}$
Vx3	Delayed B	Delayed $\overline{B}$	Delayed B	Delayed $\overline{B}$
Vy1	B	$\overline{B}$	$\overline{B}$	B
Vy2	R	$\overline{R}$	$\overline{R}$	R
Vy3	G	$\overline{G}$	$\overline{G}$	G

Connection to LCD Panels

There are two modes of connecting HD66300T chips to an LCD panel:

1) monodirectional connection mode
2) interleaved connection mode

In the former mode, the HD66300Ts are set on either the upper side or lower side of the panel, while in the latter mode, the HD66300Ts are set on both sides and the upper drivers and the lower drivers are alternately connected to each pixel-column.

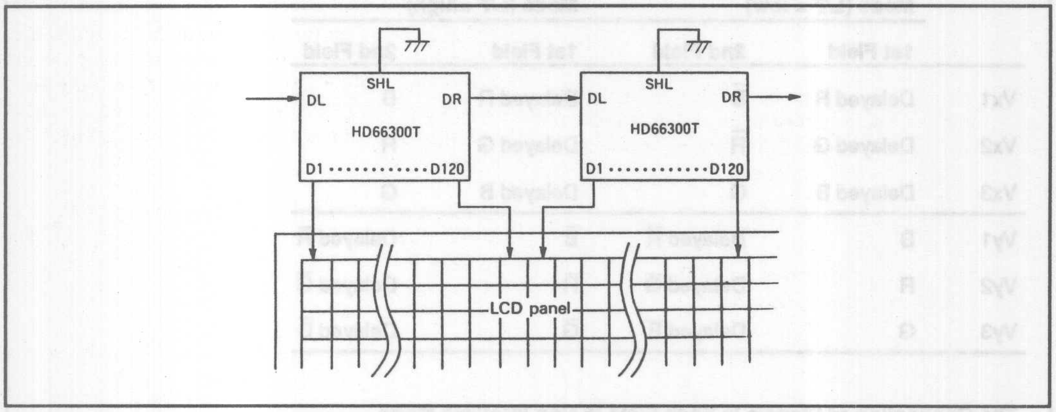


Figure 6 Monodirectional Connection Mode

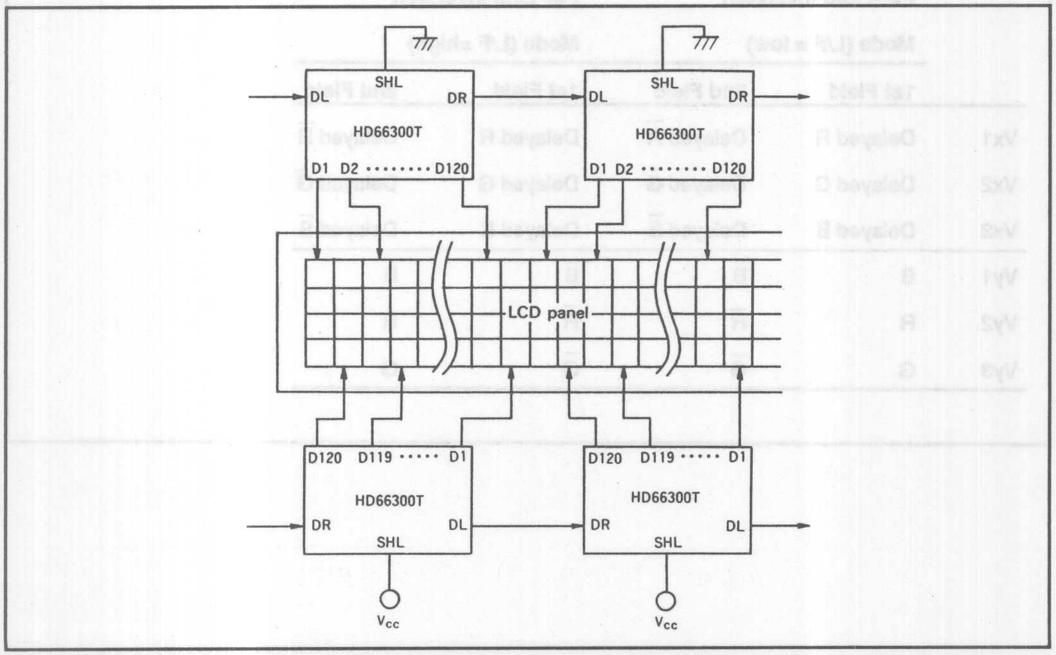


Figure 7 Interleaved Connection Mode

Internal Operation

The HD66300T has four sample and hold circuits for each outputs as shown in the block diagram, and its internal bidirectional shift register controls which circuits to sample data.

It has three-phase shift clocks with mutual phase difference of 120° to drive the shift register, which enables driving an LCD panel with mosaic pattern and triangular pattern.

The operation of sample and hold circuits and sampling operation are described below followed by the description of the relationship between three-phase shift clock phases and frequencies.

After the above description, determination of bias voltage is described; bias voltage controls driving characteristics of a differential amplifier and output buffer of the sample and hold circuits.

Finally, the OE and FD signals are described; they determine the operation of the sample and hold shift matrix circuit. Timing charts for each mode follow the description.

Sample and Hold Circuitry

Operation of Sample and Hold Circuitry

The HD66300T has four sample and hold circuits A, B, C, and D per LCD drive signal output. Sample and hold circuit pair A and B is supplied with the same sampling clock pulses as circuit pair C and D. One of the signals output by these circuits is connected to an output driver.

These sample and hold circuits repeat sampling and outputting of signals alternately to drive an TFT-type LCD panel.

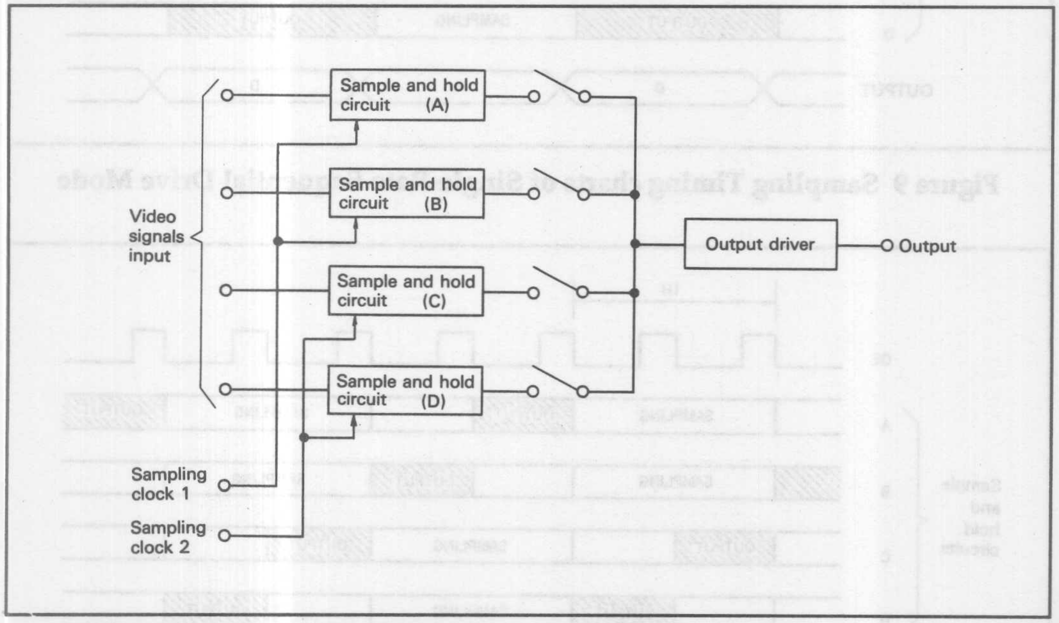


Figure 8 Sample and Hold Circuitry

In single-rate sequential drive mode, sample and hold circuits A and D are alternately used; circuits B and C perform sampling operation, but are not used since they are not connected to the output driver.

In single-rate sequential drive mode, one sample and hold circuit samples the signal during one horizontal scanning period, and outputs it as an LCD drive signal in the following horizontal scanning period.

In double-rate sequential drive mode, all sample and hold circuits A, B, C, and D are alternately used.

In double-rate sequential drive mode, two sample and hold circuits sample two signals during one horizontal scanning period, and output one of them as an LCD drive signal in the first half of the following horizontal scanning period, and output the other signal in the second half.

The following shows the timing charts of sampling and outputting operation.

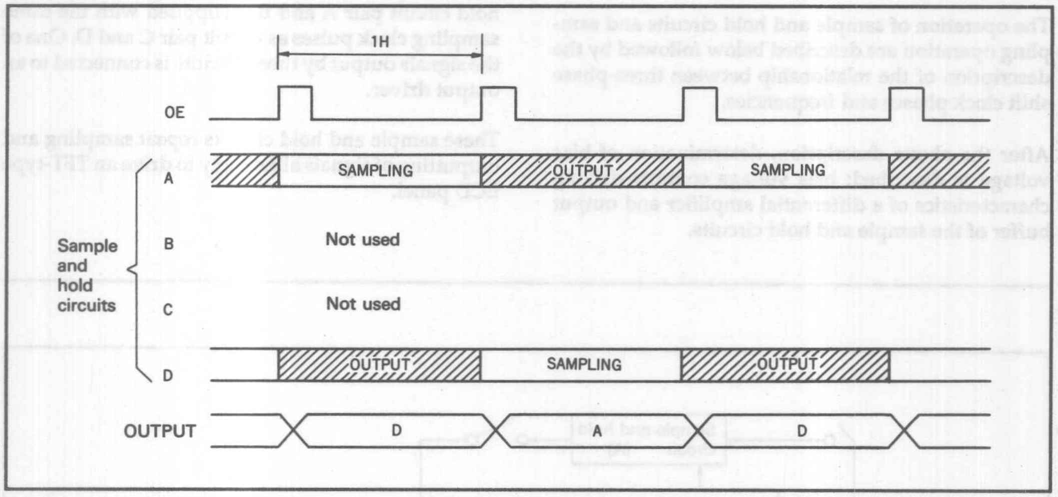


Figure 9 Sampling Timing charts of Single-Rate Sequential Drive Mode

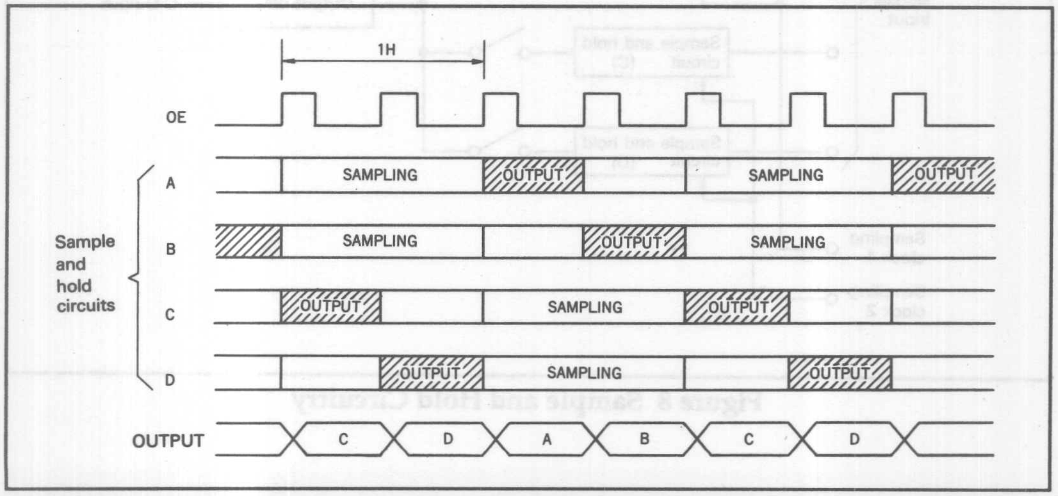


Figure 10 Sampling Timing charts of Double-Rate Sequential Drive Mode

Sampling Operation

The HD66300T has a bidirectional shift register composed of 120 bits and each bit of the shift register generates the sampling pulses to control the sampling operation of the four sample and hold circuits connected to each LCD drive signal output pin. When a bit of the shift register is 1, the corresponding sample and hold circuits are in the sampling state; when it is 0, the corresponding sample and hold circuits are in the hold state. Consequently, shifting a 1 into the shift register activates in turn the sample and hold circuits corresponding to each LCD drive signal output pin.

Figure 11 is a shift register sketch illustrating the relationship between the shift register and the shift clocks HCK1, HCK2, and HCK3. Note that the order of sampling pulse generation depends on the state of pin SHL. D1 corresponds to DL and D120 to DR.

Figure 12 is a timing chart of sampling pulses generated by the shift register.

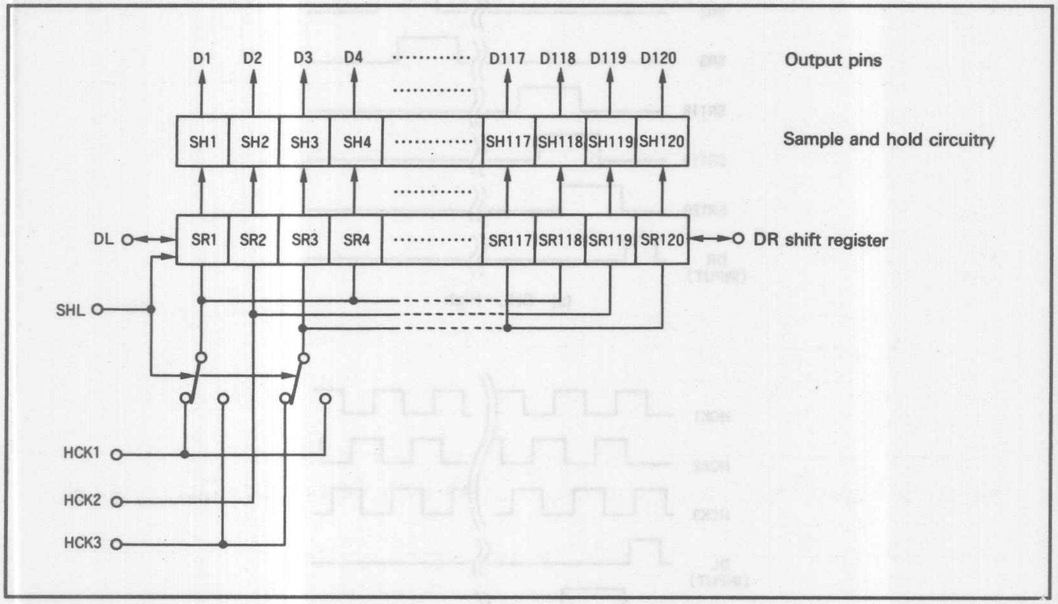


Figure 11 Shift Register Sketch

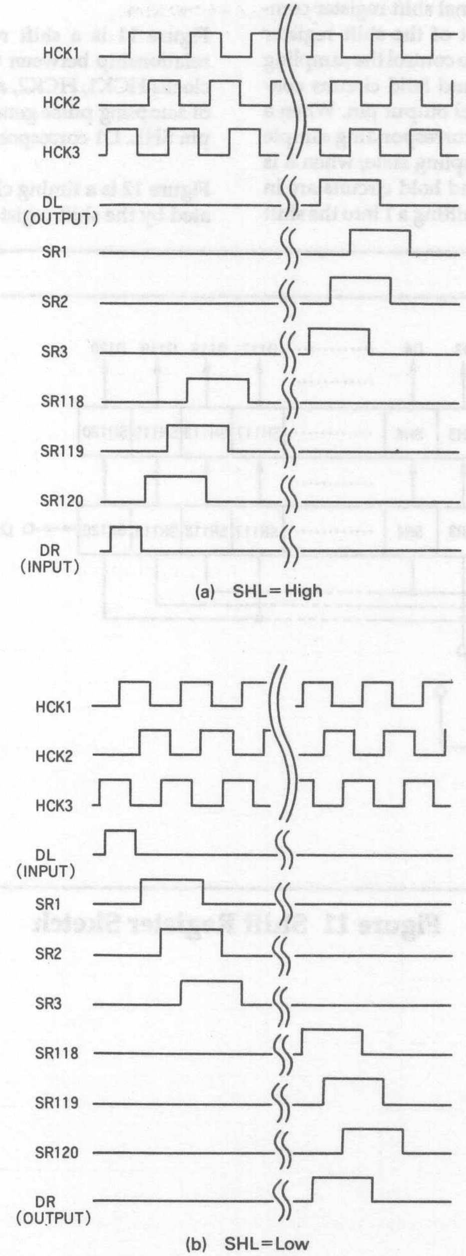


Figure 12 Sampling Pulse Timing Chart

Three-Phase Shift Clocks

Three-Phase Shift Clocks and Sample Start Signal

Shift clocks HCK1, HCK2, and HCK3, which are operation clocks for the shift register, must be three-phase clocks with 50-percent duty. The HCK2 clock must be generated 120° after the HCK1 clock, and the HCK3 clock 240° after the HCK1 clock. Sampling operation starts when 1 is input from pin DL or DR at a rising edge of the HCK1 clock pulse.

In monodirectional connection mode, all the HD66300T chips must be supplied with the same three-phase shift clock pulses. In interleaved connection mode, the frequency of the three-phase shift clocks must be half of that in monodirectional connection mode, and the phase shift between the upper drivers clocks and the lower drivers clocks must be one pixel.

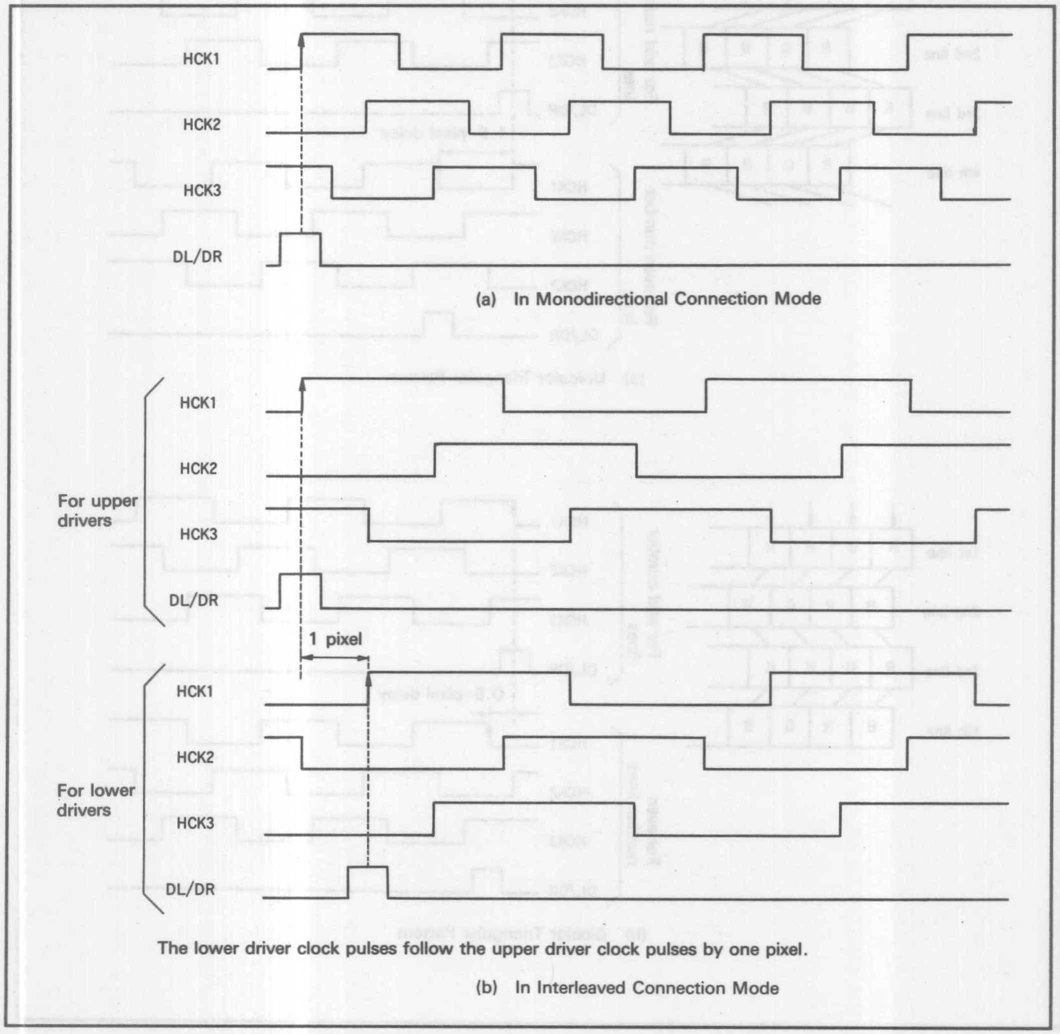


Figure 13 Three-Phase Shift Clocks and Sample Start Signal

Some position shift exists between the pixels of even number lines and those of odd number lines for LCD panels having triangular patterns. This requires generating a phase shift between the three-phase clocks for even number lines and those for odd number lines. The required phase shift is 1.5 pixels for LCD panels having a unicolor triangular pattern, while it is 0.5 pixels for those having a bicolor triangular pattern.

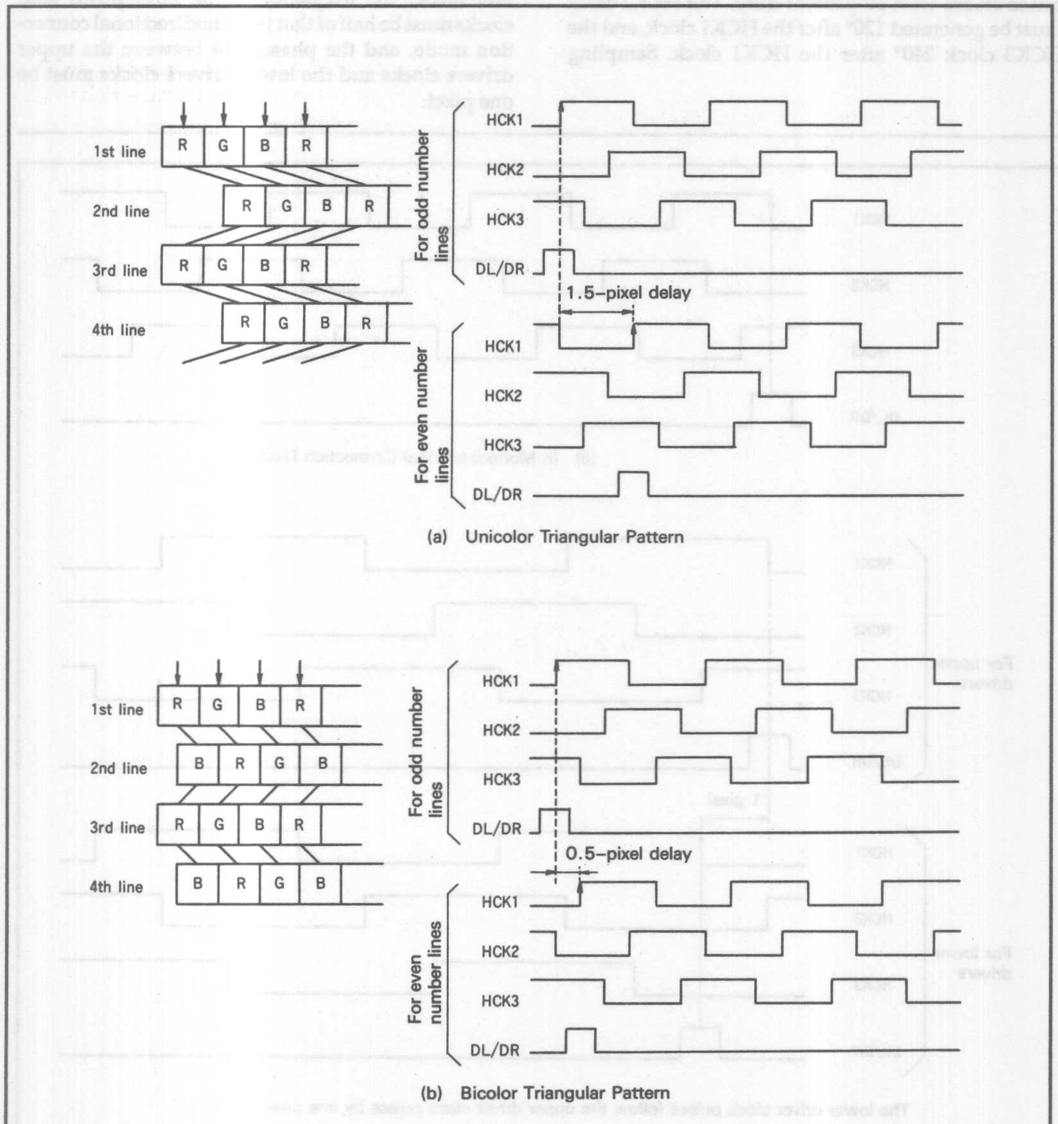


Figure 14

How to Generate Three-Phase Shift Clocks

Three-phase shift clocks can be generated by dividing the base clock, which is generated from a horizontal synchronizing clock, through the use of a frequency multiplier such as a PLL circuit.

The number of horizontal pixels of the LCD panel and the valid display ratio determines the base clock frequency f.

If the number of horizontal pixels is 480 and the valid display ratio is 95% in the NTSC system, the base clock frequency f is about 9.59 MHz according to the following equation.

f = (1/valid display period) x (no. of horizontal pixels/valid display ratio)
  = 480/(52.7 μsec x 0.95)
  = 9.59 (MHz)

The three-phase clocks can be generated by dividing f by 3 (in the monodirectional connection mode) or 6 (in the interleaved connection mode).

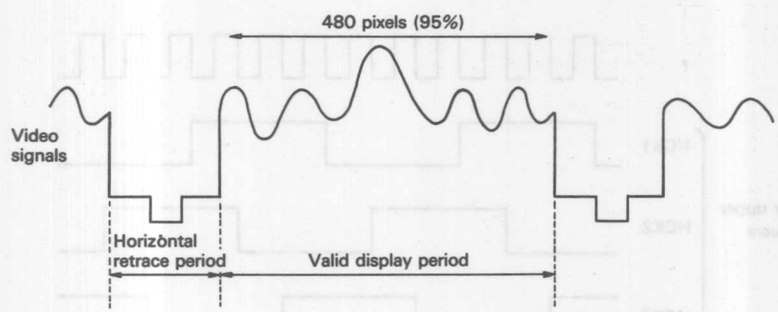
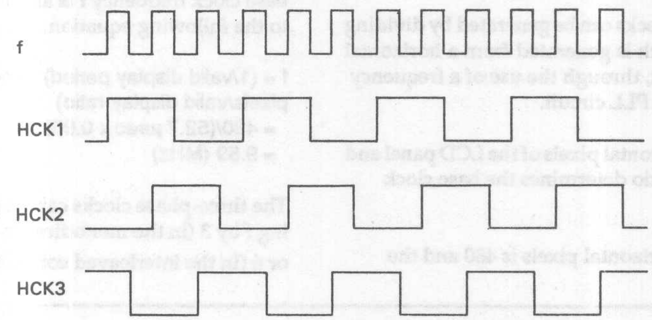
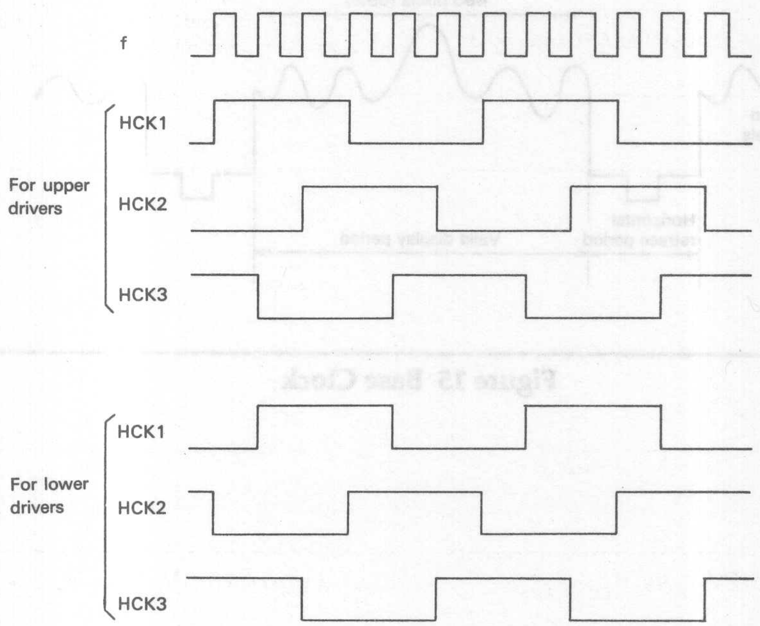


Figure 15 Base Clock



(a) In Monodirectional Connection Mode



(b) In Interleaved Connection Mode

Figure 16 Three-Phase Shift Clocks

Bias Voltage

Voltages V_{bsB}, V_{bsH}, and V_{bo} control the drive capability of the output buffer and differential amplifier. Here the LSI must be used in the range of

$$V_{CC} - 4.0\ V \leqq V_{bsB},\ V_{bsH},\ V_{bo} \leqq V_{CC} - 2.0\ V$$

V_{bsB} controls the drive current capability of the output buffer when OE is high (IV_{sB}) and V_{bsH} controls the leakage correction current of when OE is low (IV_{sH}). Figure 17 and figure 18 show the relationship between IV_{sB} and V_{bsB} and the relationship between IV_{sH} and V_{bsH}, respectively.

V_{bsB} and V_{bsH} should be to an appropriate level for the electrical characteristics of the LCD panel used.

The rise time (t_{DDR}) and the fall time (t_{DDF}) of the output buffer depend on the input level of V_{bsB}. Figure 19 shows the relationship between t_{DDR}, t_{DDF} and V_{bsB}.

V_{bo} controls the bias current of the differential amplifier (IV_{bo}).

Figure 20 shows the relationship between the rise and fall times (t_{DDR}, t_{DDF}) of the output buffer and V_{bo}. V_{bo} should be adjusted to an appropriate level for the electrical characteristics of the LCD panel used.

The increase of total current consumption is 120 times larger than that of IV_{bsB}, IV_{bsH} and IV_{bo}, because figure 17, 18 and 21 each shows the case of one output and HD66300T has 120 outputs.

Figure 17, 18, 19, 20 and 21 are just for reference and do not guarantee the characteristics.

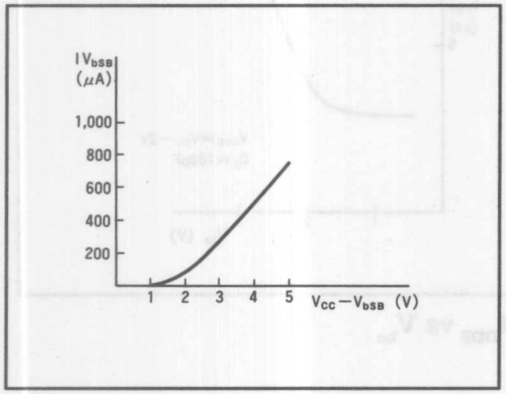


Figure 17 IV_{bsB} vs $V_{CC}-V_{bsB}$

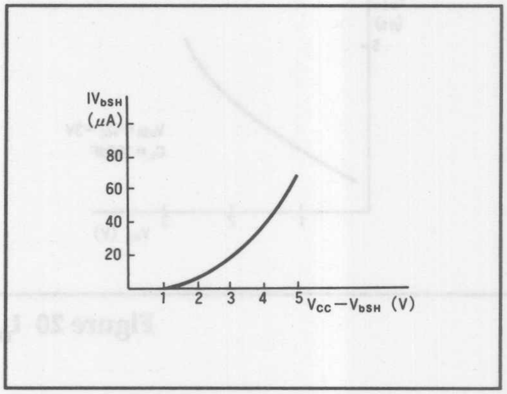


Figure 18 IV_{bsH} vs $V_{CC}-V_{bsH}$

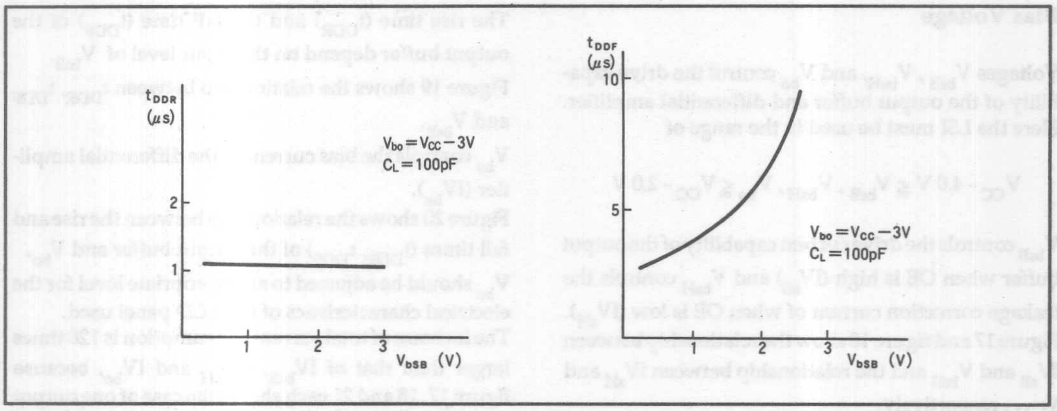


Figure 19 t_{DDR}, t_{DDF} vs V_{bsB}

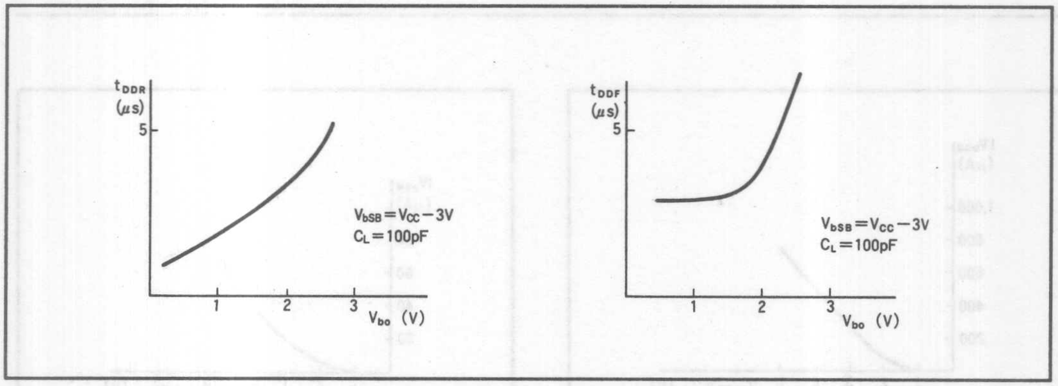


Figure 20 t_{DDR}, t_{DDF} vs V_{bo}

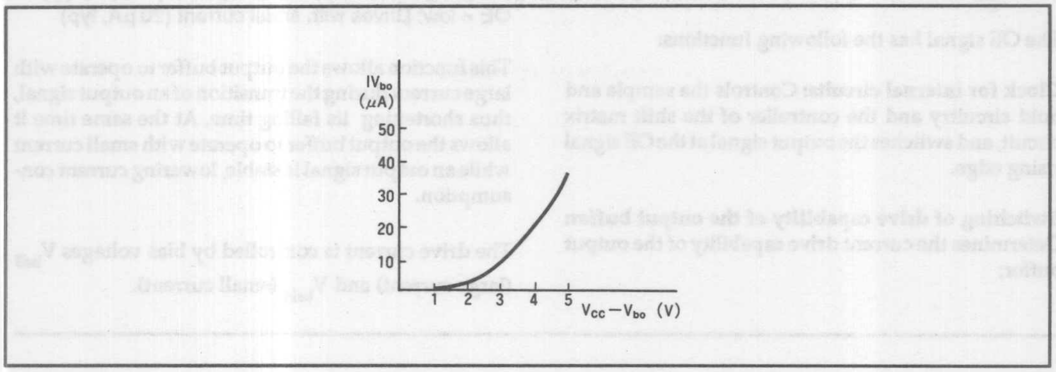


Figure 21 IV_{bo} vs V_{CC}–V_{bo}

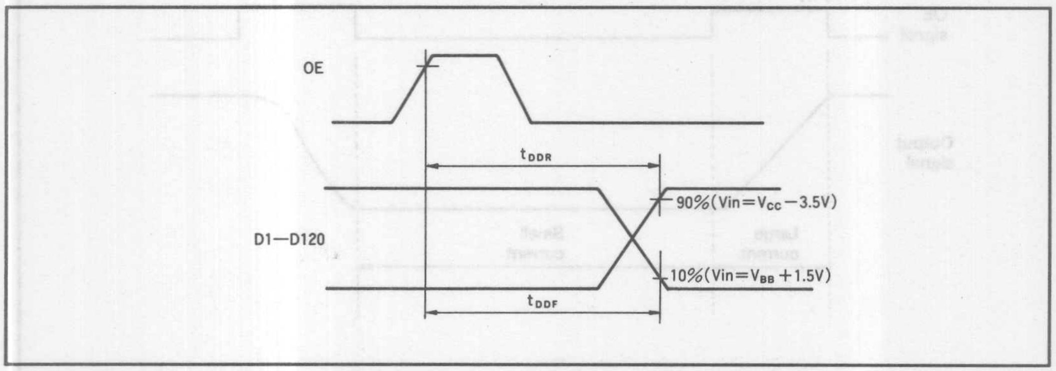


Figure 22 Definition of t_{DDR} and t_{DDF}

OE Signal

The OE signal has the following functions:

Clock for internal circuits: Controls the sample and hold circuitry and the controller of the shift matrix circuit, and switches the output signal at the OE signal rising edge.

Switching of drive capability of the output buffer: Determines the current drive capability of the output buffer;

OE = high: Drives with large current (300 μA, typ)
OE = low: Drives with small current (20 μA, typ)

This function allows the output buffer to operate with large current during the transition of an output signal, thus shortening its falling time. At the same time it allows the output buffer to operate with small current while an output signal is stable, lowering current consumption.

The drive current is controlled by bias voltages V_{bsB} (large current) and V_{bsH} (small current).

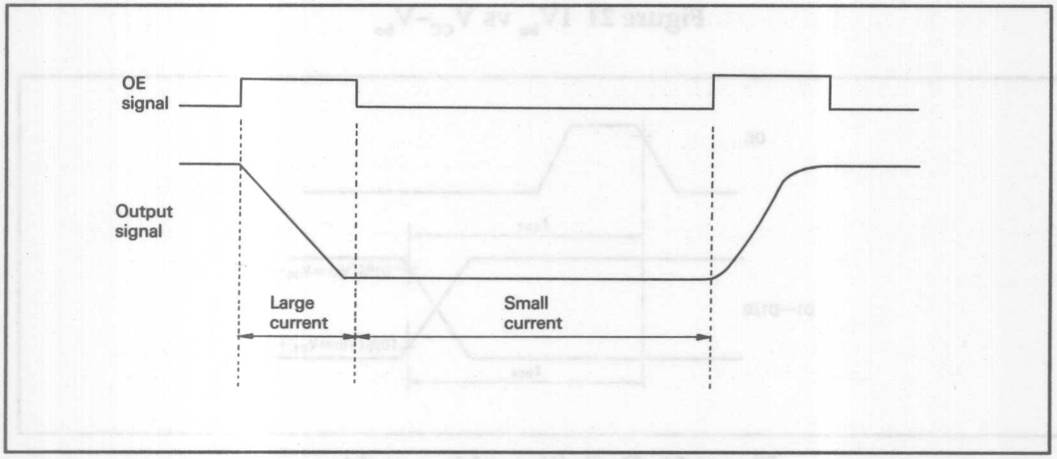


Figure 23 Switching of Drive Capability of the Output Buffer

FD Signal

The FD signal is the field determination signal; a field is determined by the state of this signal at the rising edge of the OE signal. This signal synchronizes the internal controllers with TV signals.

The order of outputting signals is determined at the fourth rising edge of the OE signal after the rising or falling edge of the FD signal in double-rate sequential drive mode, while it is determined at the third rising edge in single-rate sequential drive mode; hereinafter, as long as the FD signal is not changed, signals will be output in the determined order at most every 12 pulses of the OE signal in double-rate sequential drive mode, while at most every 6 pulses in single-rate sequential drive mode.

The FD signal should usually be high in the first field and low in the second field. In some modes, however, it should be high in both fields, but low for at least one-pulse time period of the OE signal during the horizontal scanning period.

The order of outputting signals and the timing of inputting the FD signal vary depending on the mode. For more details, refer to the appropriate timing charts.

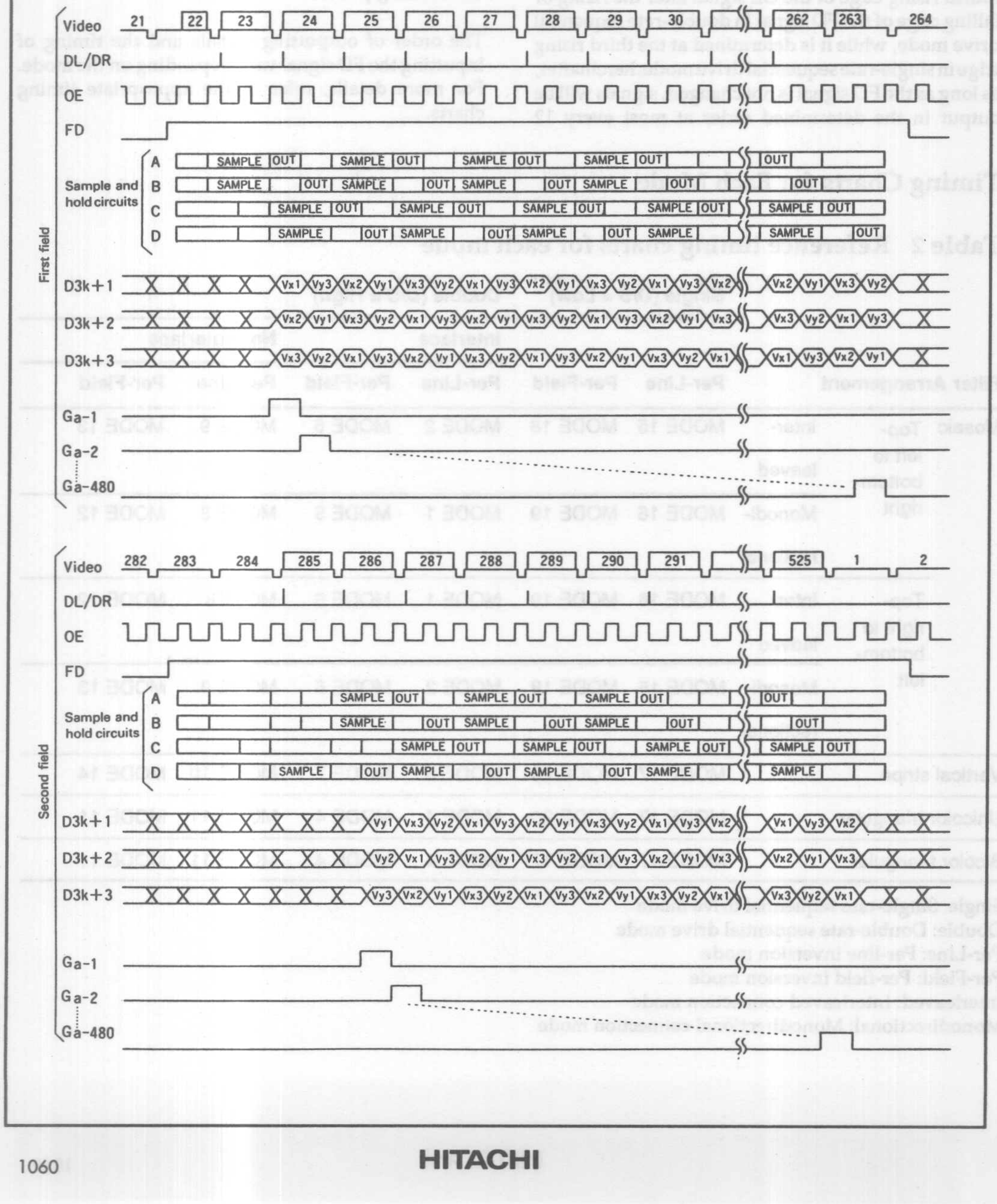
Timing Charts for Each Mode

Table 2 Reference timing charts for each mode

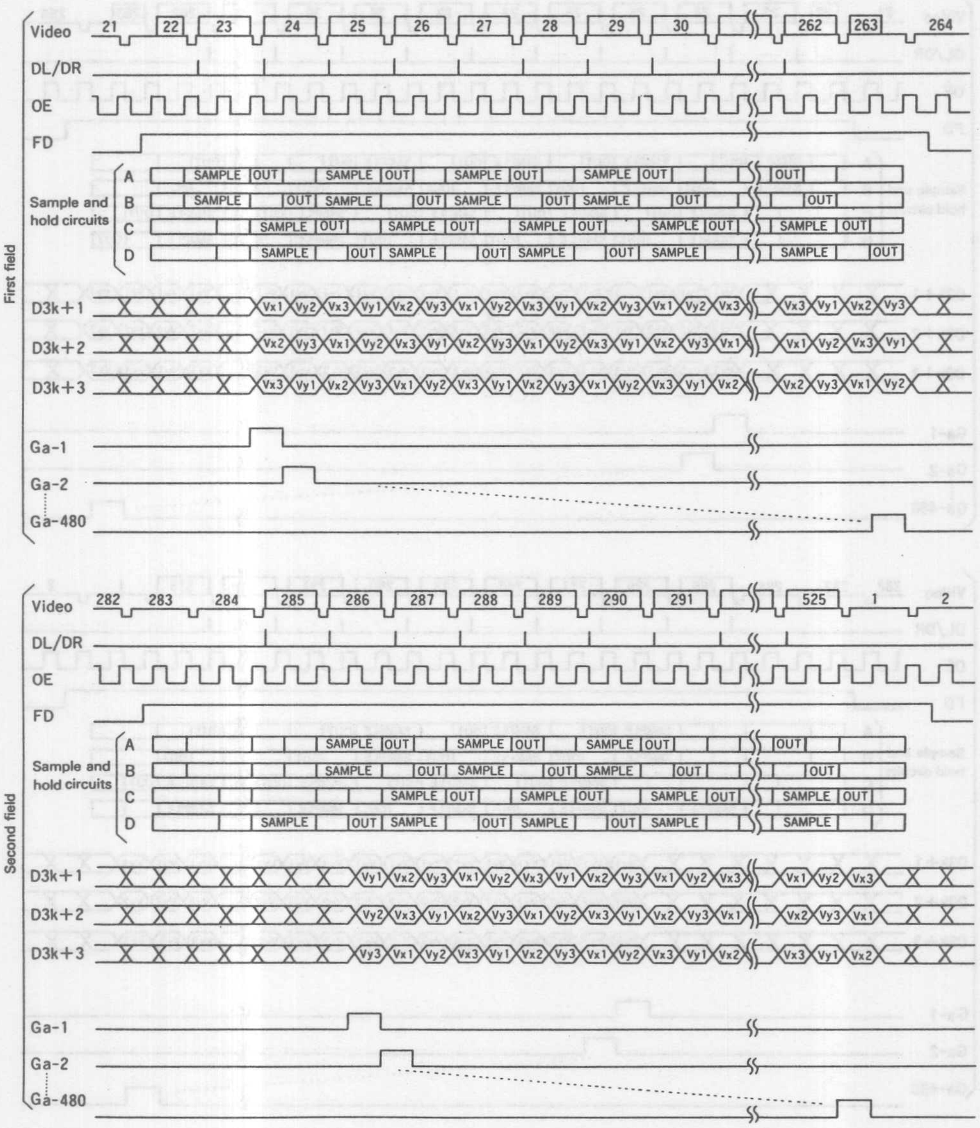
			Single (D/S = Low)		Double (D/S = High)			
					Interlace		Non-Interlace	
Filter Arrangement			Per-Line	Per-Field	Per-Line	Per-Field	Per-Line	Per-Field
Mosaic	Top-left to bottom-right	Inter-leaved	MODE 15	MODE 18	MODE 2	MODE 6	MODE 9	MODE 13
		Monodi-rectional	MODE 16	MODE 19	MODE 1	MODE 5	MODE 8	MODE 12
	Top-right to bottom-left	Inter-leaved	MODE 16	MODE 19	MODE 1	MODE 5	MODE8	MODE 12
		Monodi-rectional	MODE 15	MODE 18	MODE 2	MODE 6	MODE 9	MODE 13
Vertical stripe			MODE 17	MODE 20	MODE 3	MODE 7	MODE 10	MODE 14
Unicolor triangular			MODE 17	MODE 20	MODE 4	MODE 4	MODE 11	MODE 11
Bicolor triangular			MODE 17	MODE 17	MODE 4	MODE 4	MODE 11	MODE 11

Single: Single-rate sequential drive mode
Double: Double-rate sequential drive mode
Per-Line: Per-line inversion mode
Per-Field: Per-field inversion mode
Interleaved: Interleaved connection mode
Monodirectional: Monodirectional connection mode

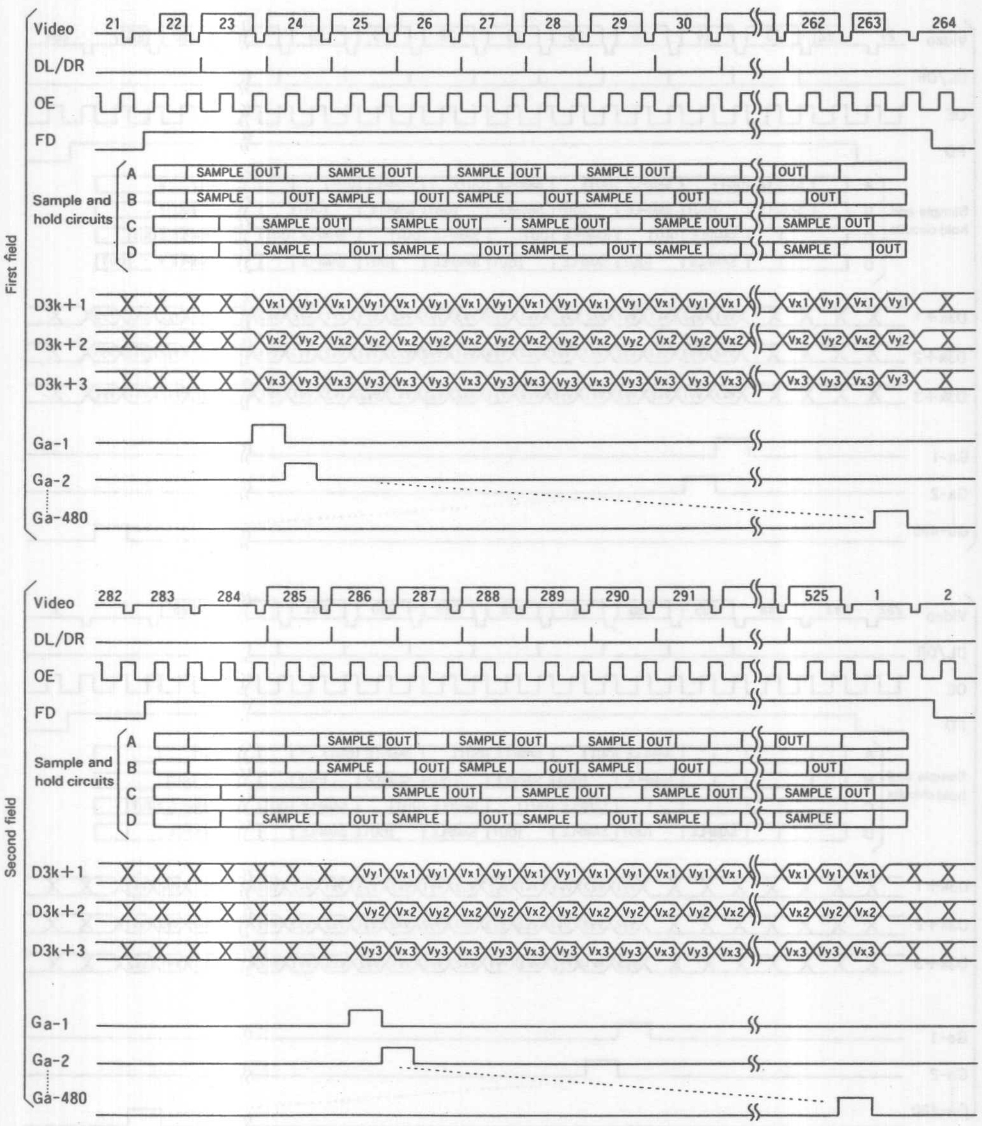
MODE 1	
D/S	V_{CC}
L/F	V_{CC}
MSF1	GND
MSF2	V_{CC}



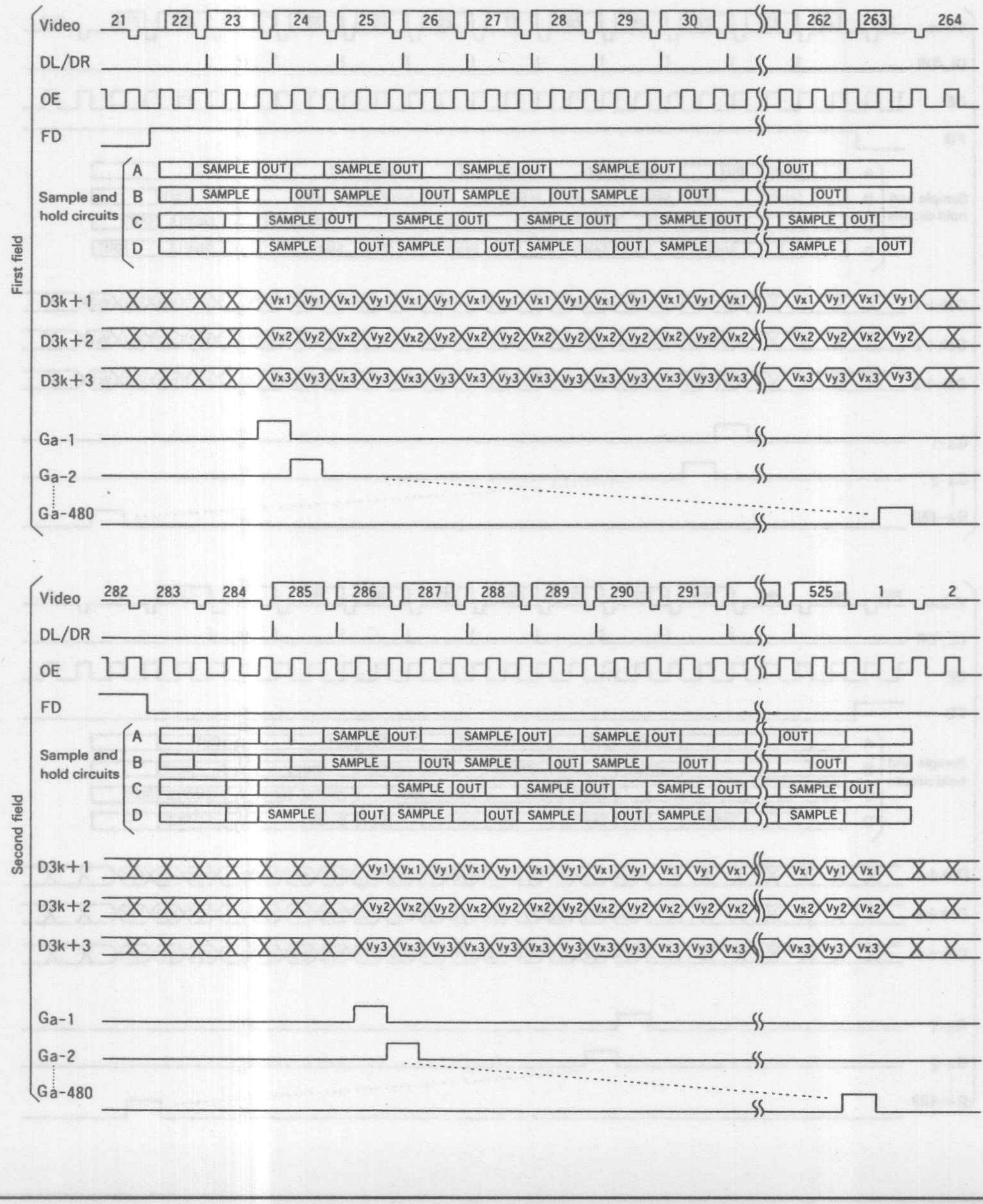
MODE 2	
D/S	V_{CC}
L/F	V_{CC}
MSF1	GND
MSF2	GND



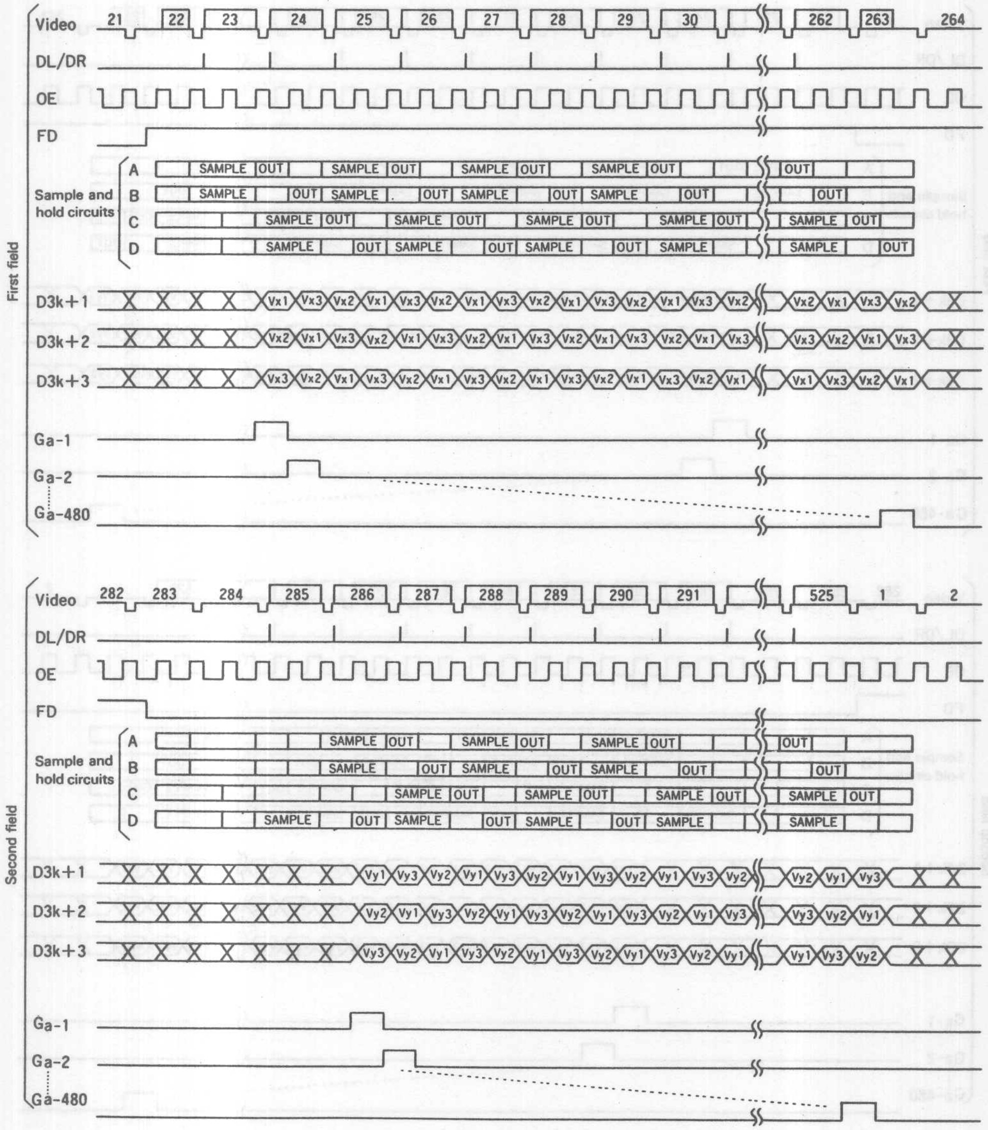
MODE 3	
D/S	V_{CC}
L/F	V_{CC}
MSF1	V_{CC}
MSF2	V_{CC}



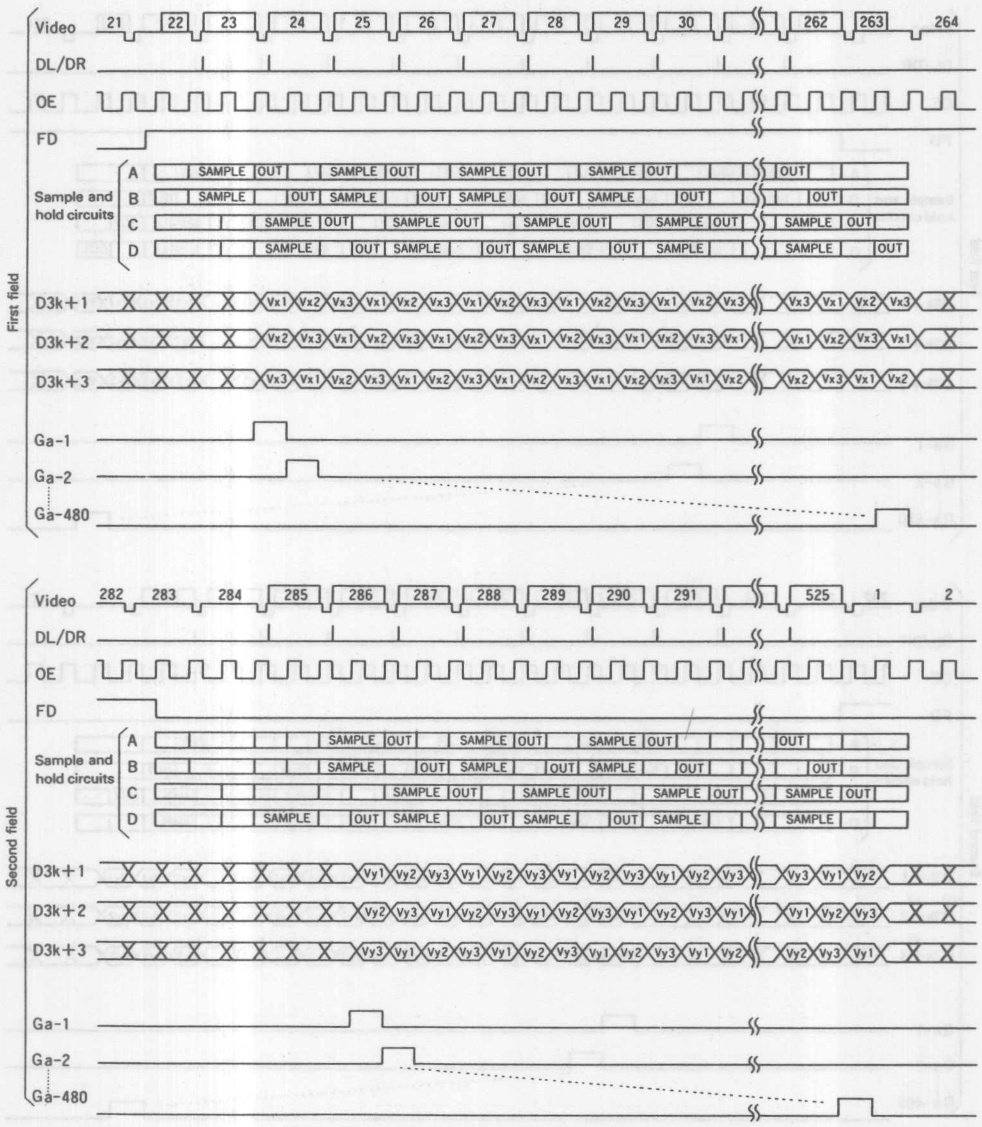
MODE 4	
D/S	V_{CC}
L/F	V_{CC}/GND
MSF1	V_{CC}
MSF2	GND



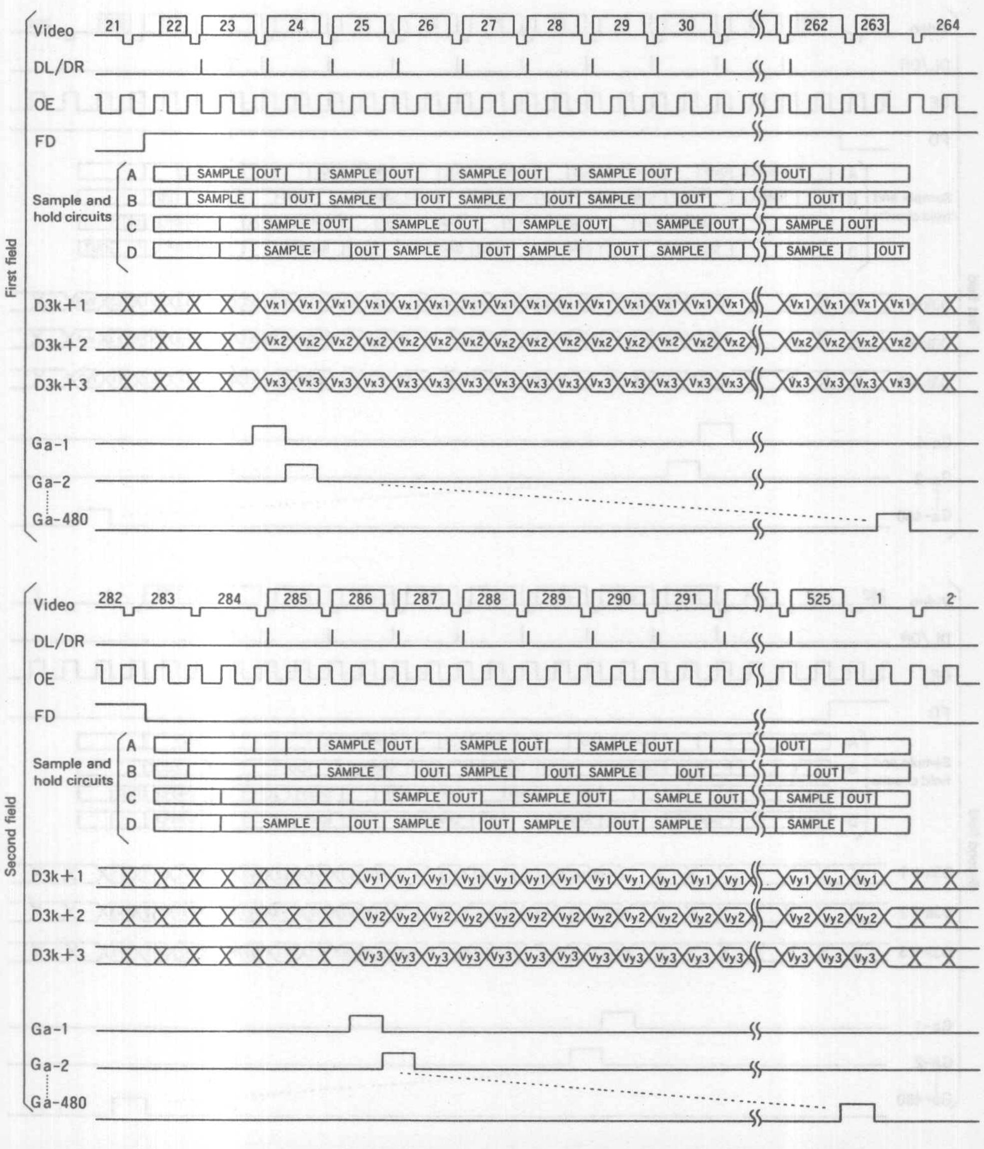
MODE 5	
D/S	V_{cc}
L/F	GND
MSF1	GND
MSF2	V_{cc}



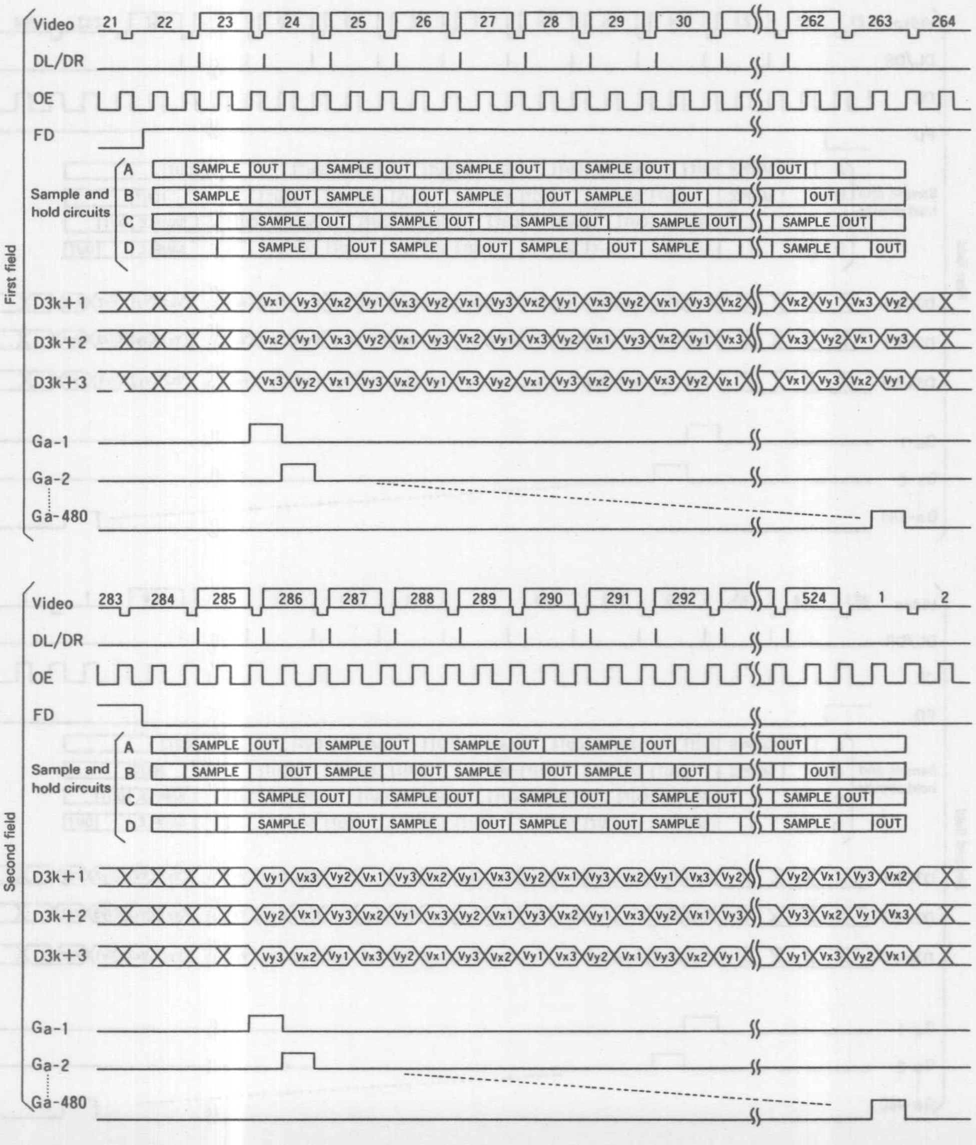
MODE 6	
D/S	V_{CC}
L/F	GND
MSF1	GND
MSF2	GND



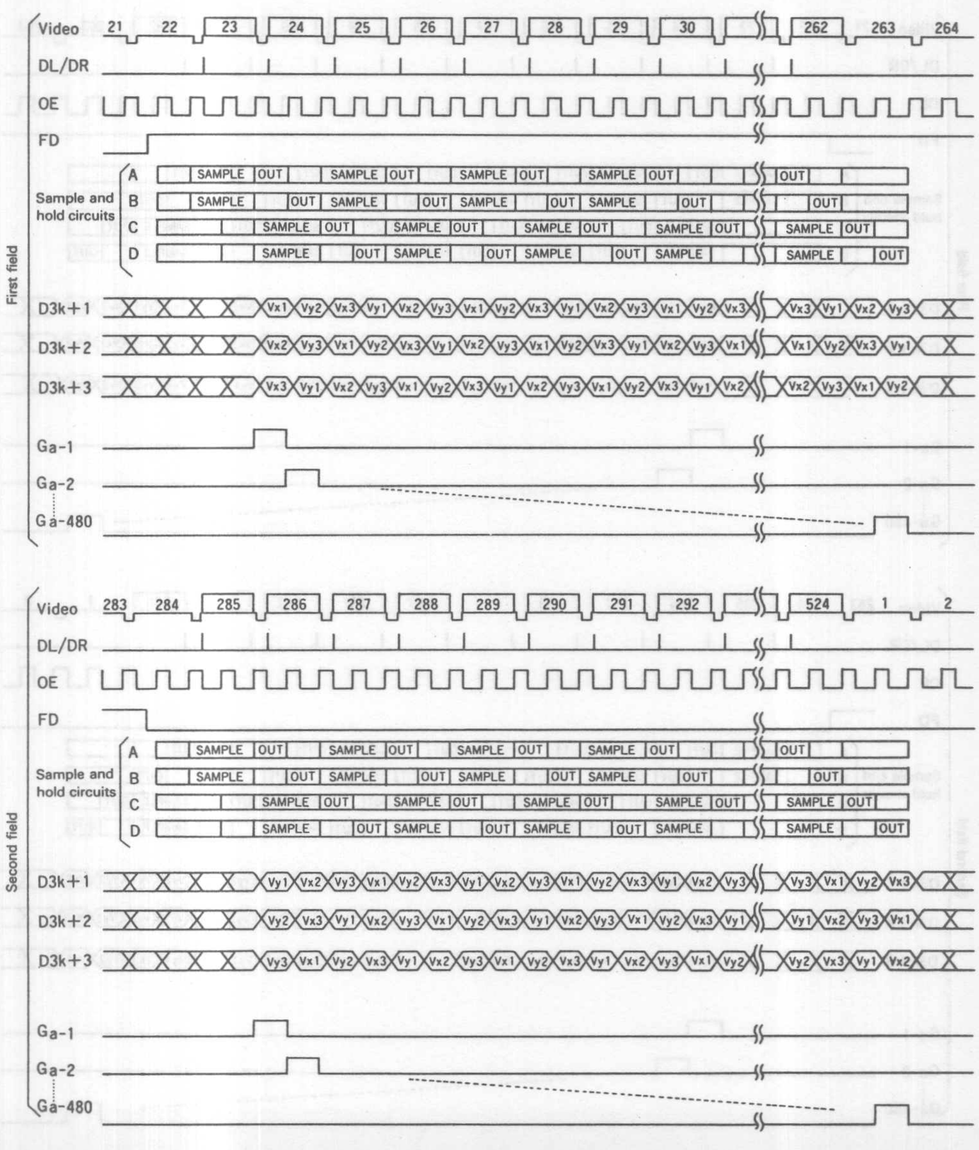
MODE 7	
D/S	V_{CC}
L/F	GND
MSF1	V_{CC}
MSF2	V_{CC}



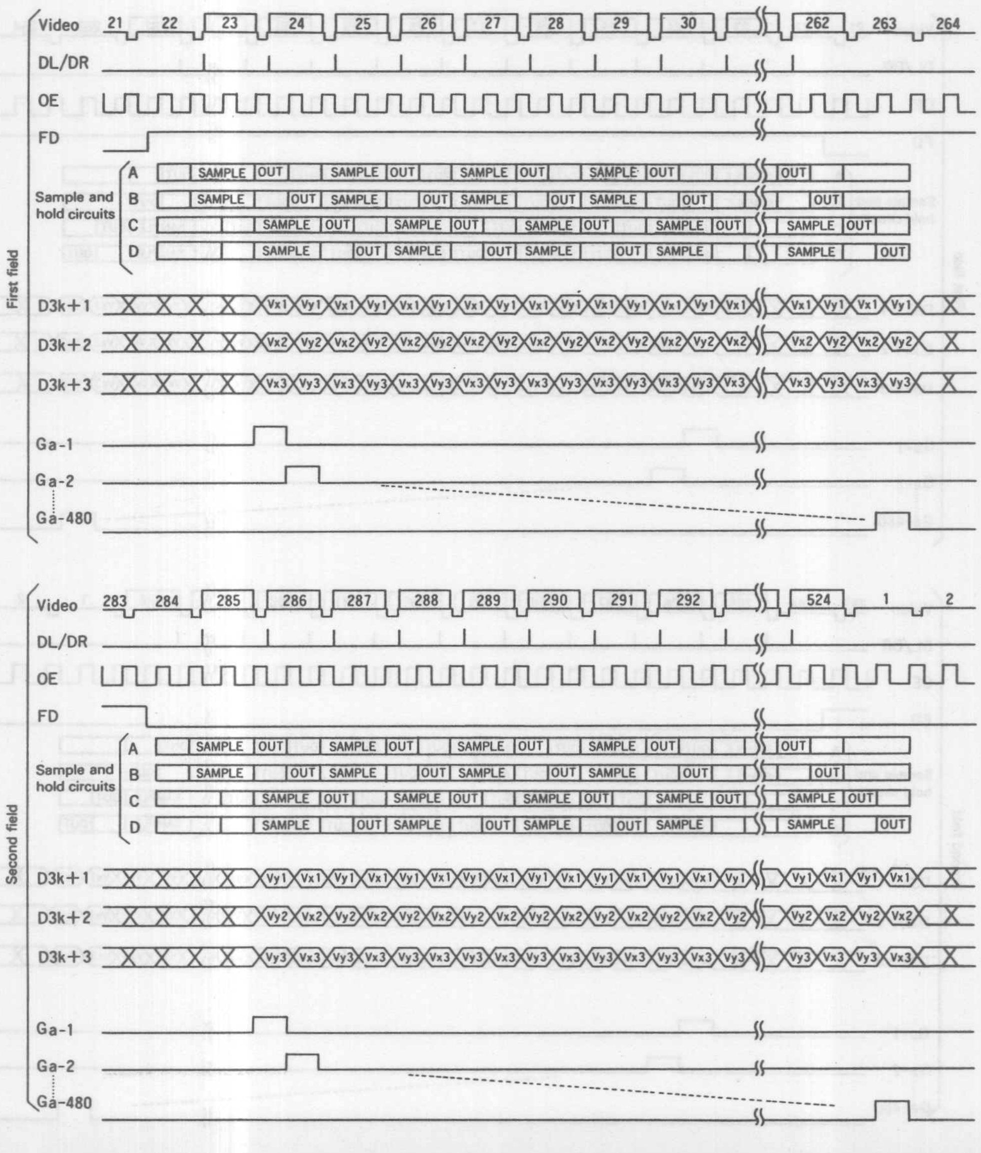
MODE 8	
D/S	V_{CC}
L/F	V_{CC}
MSF1	GND
MSF2	V_{CC}



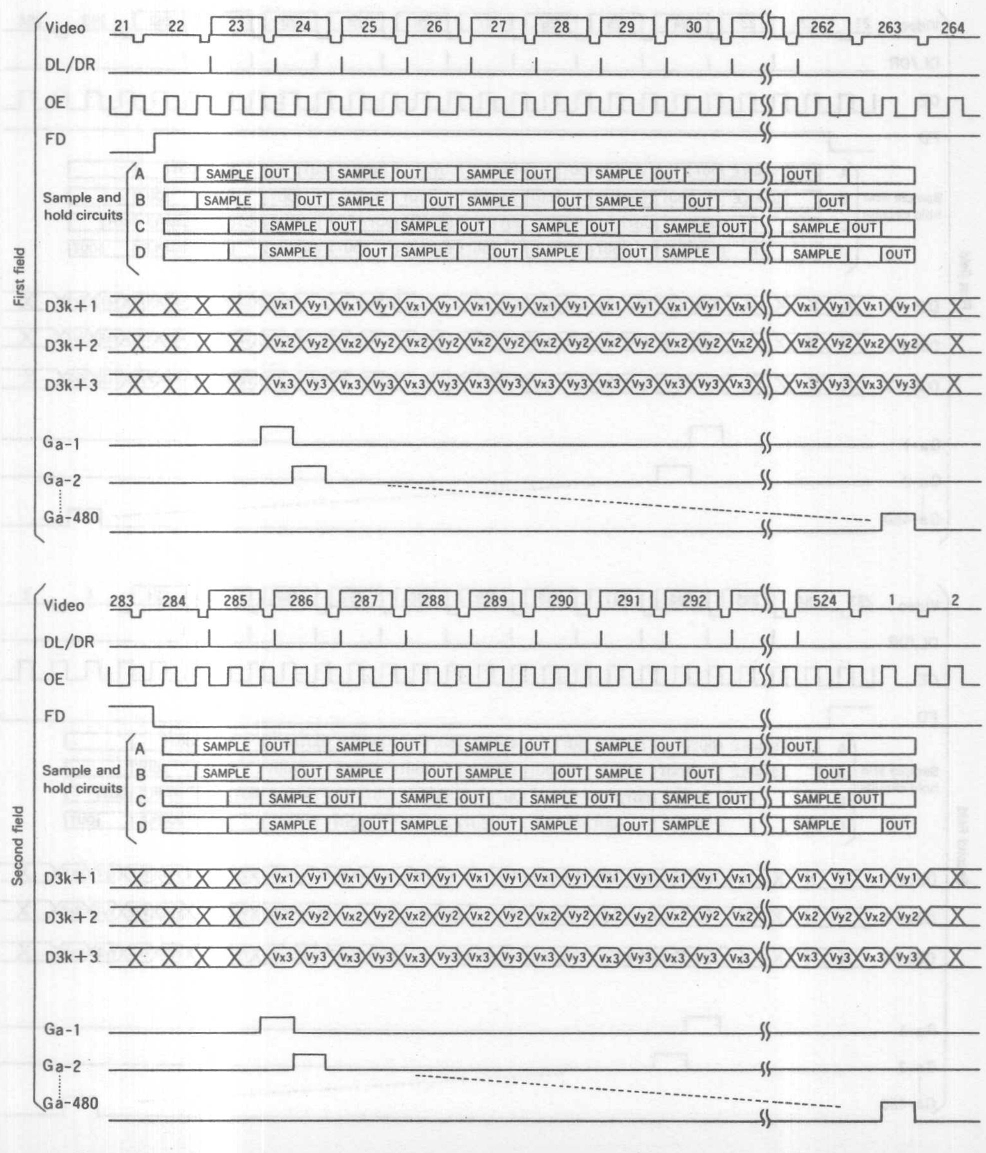
MODE 9	
D/S	V_{cc}
L/F	V_{cc}
MSF1	GND
MSF2	GND



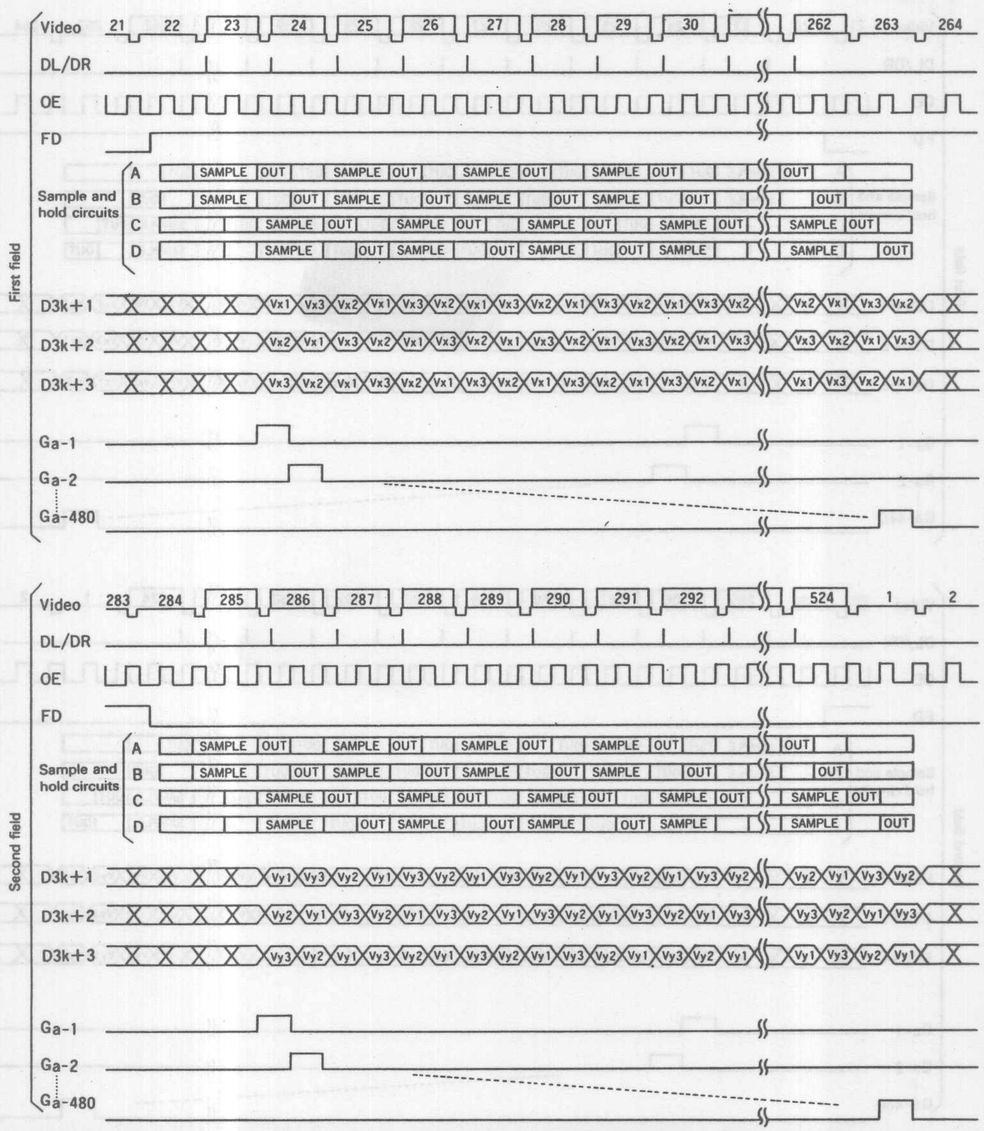
MODE10	
D/S	V_{CC}
L/F	V_{CC}
MSF1	V_{CC}
MSF2	V_{CC}



MODE11	
D/S	V_{CC}
L/F	V_{CC}/GND
MSF1	V_{CC}
MSF2	GND

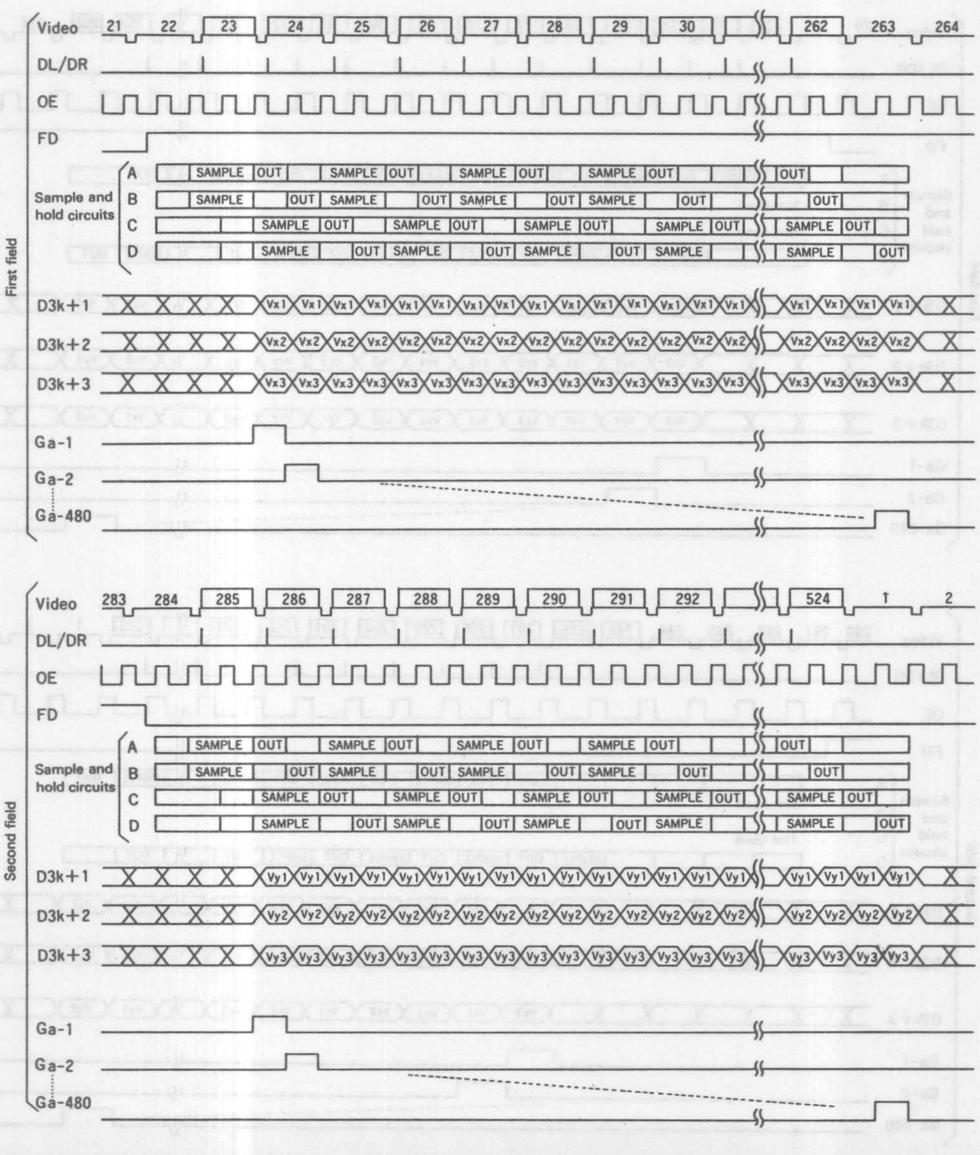


MODE12	
D/S	V_{CC}
L/F	GND
MSF1	GND
MSF2	V_{CC}

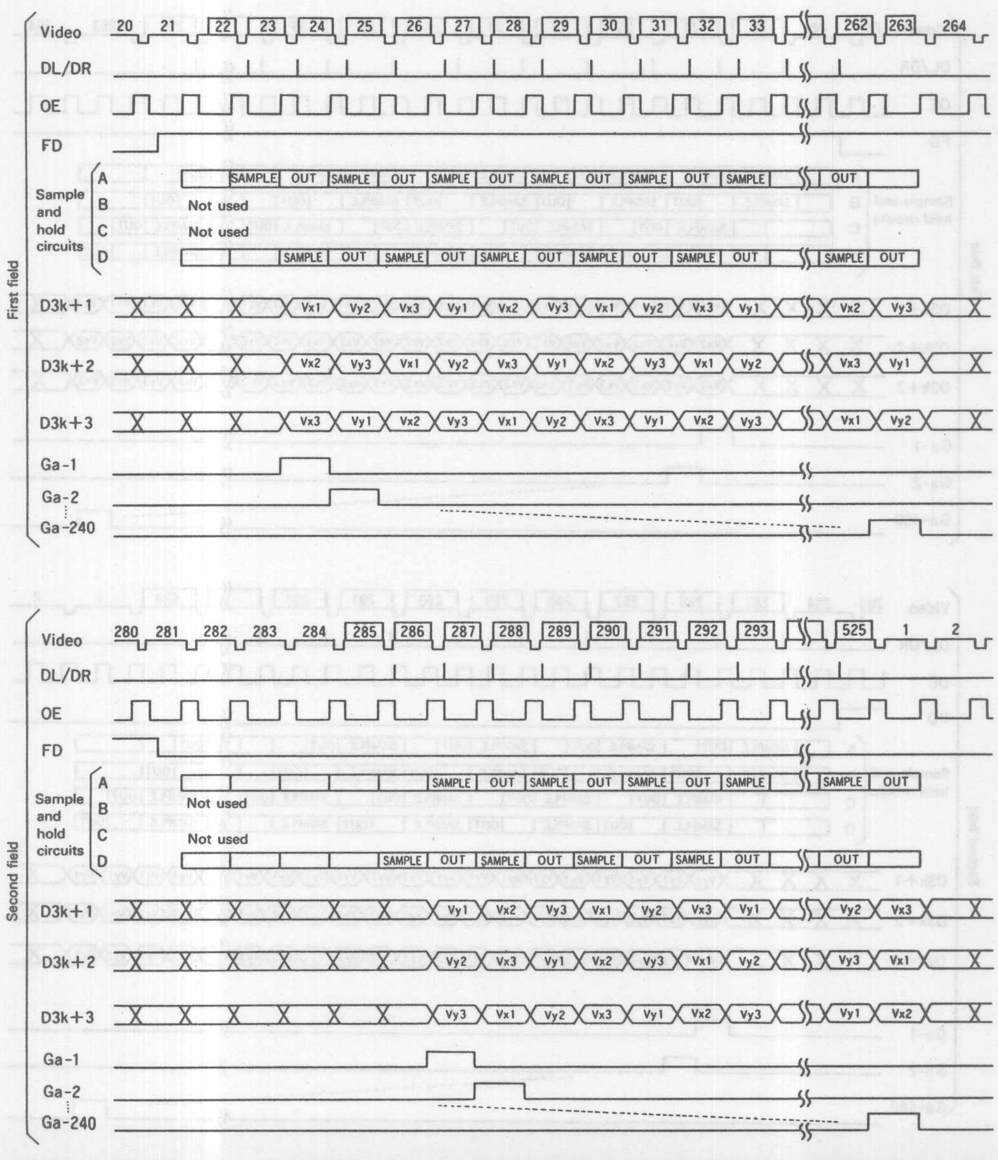


MODE13	
D/S	V_{CC}
L/F	GND
MSF1	GND
MSF2	GND

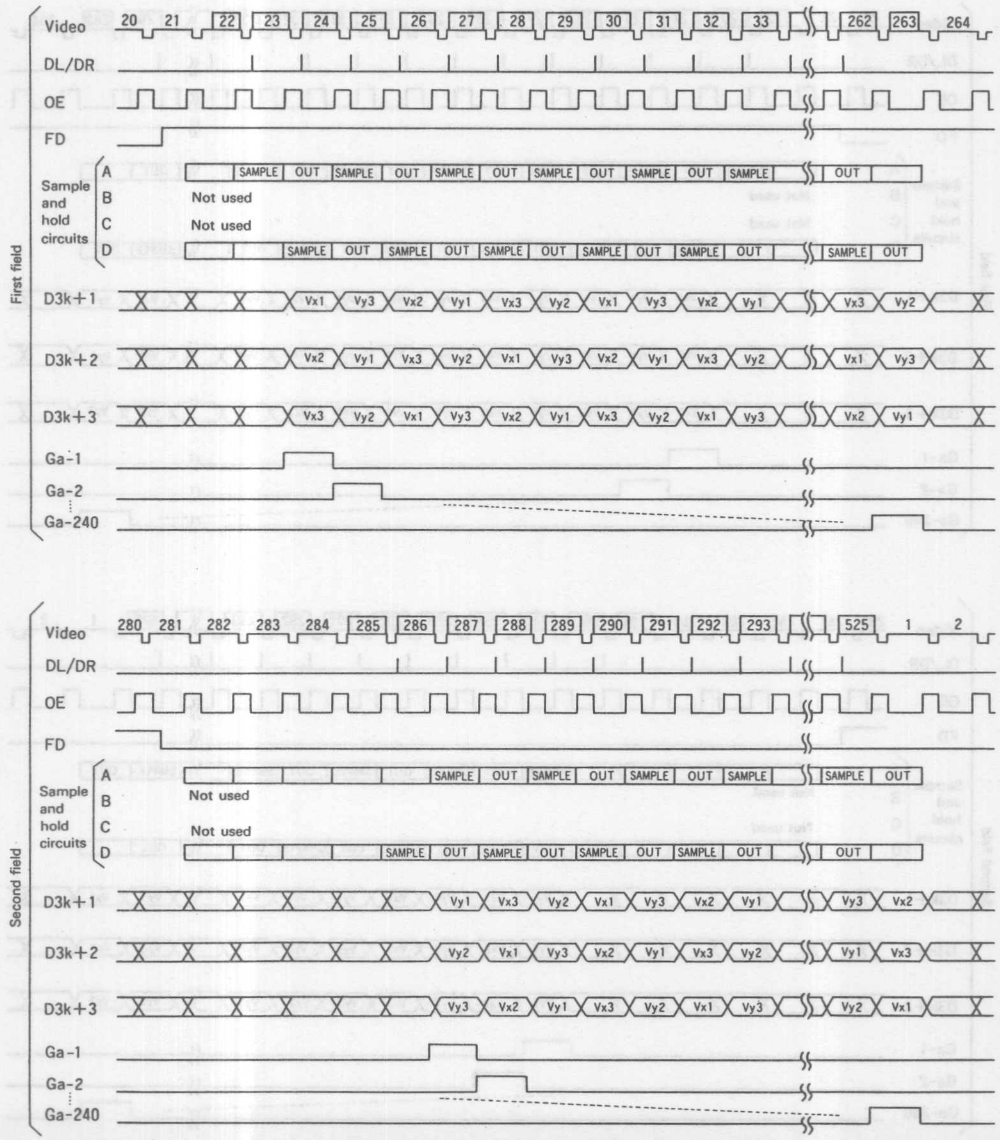
MODE14	
D/S	V_{CC}
L/F	GND
MSF1	V_{CC}
MSF2	V_{CC}



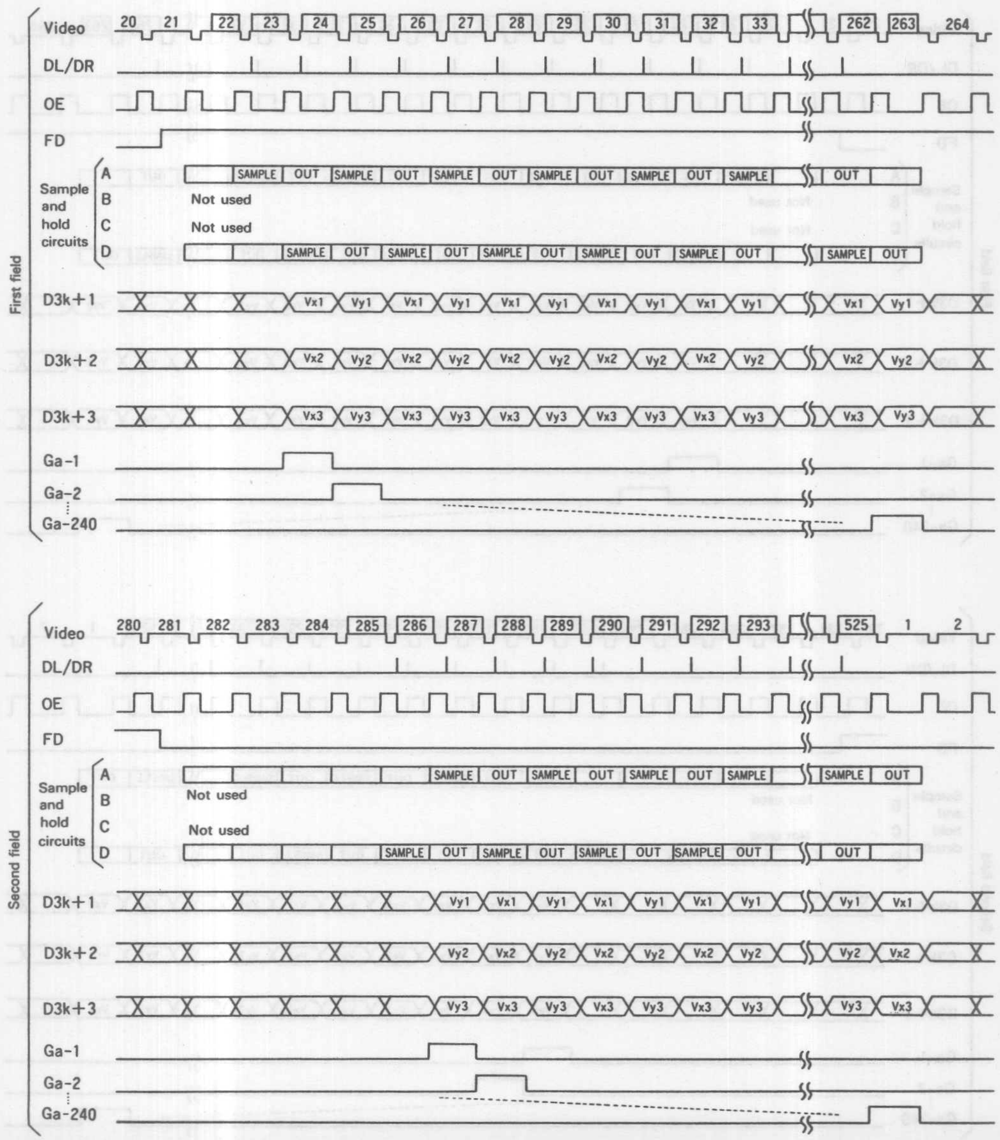
MODE15	
D/S	GND
L/F	V_{cc}
MSF1	GND
MSF2	V_{cc}



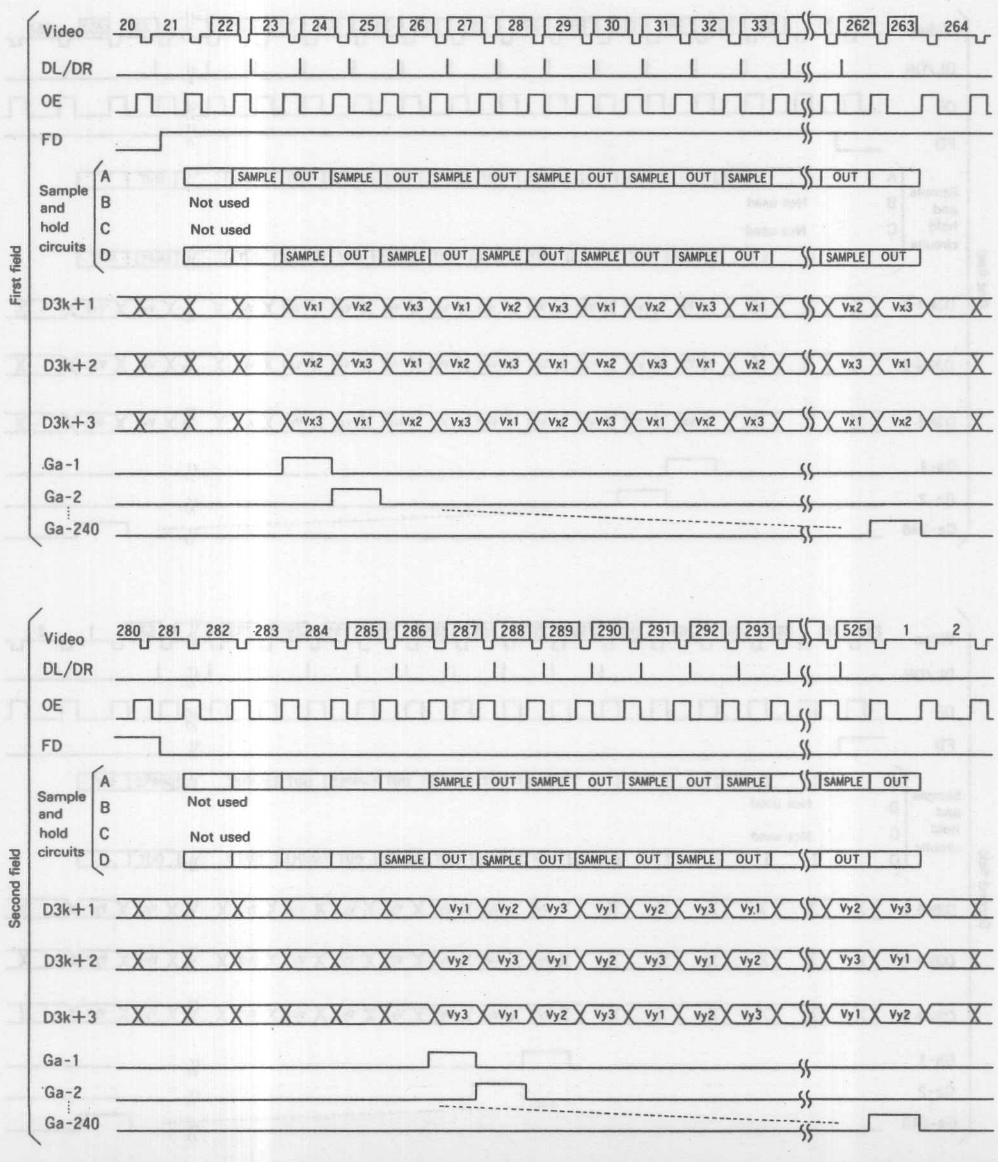
MODE16	
D/S	GND
L/F	V_{CC}
MSF1	GND
MSF2	GND



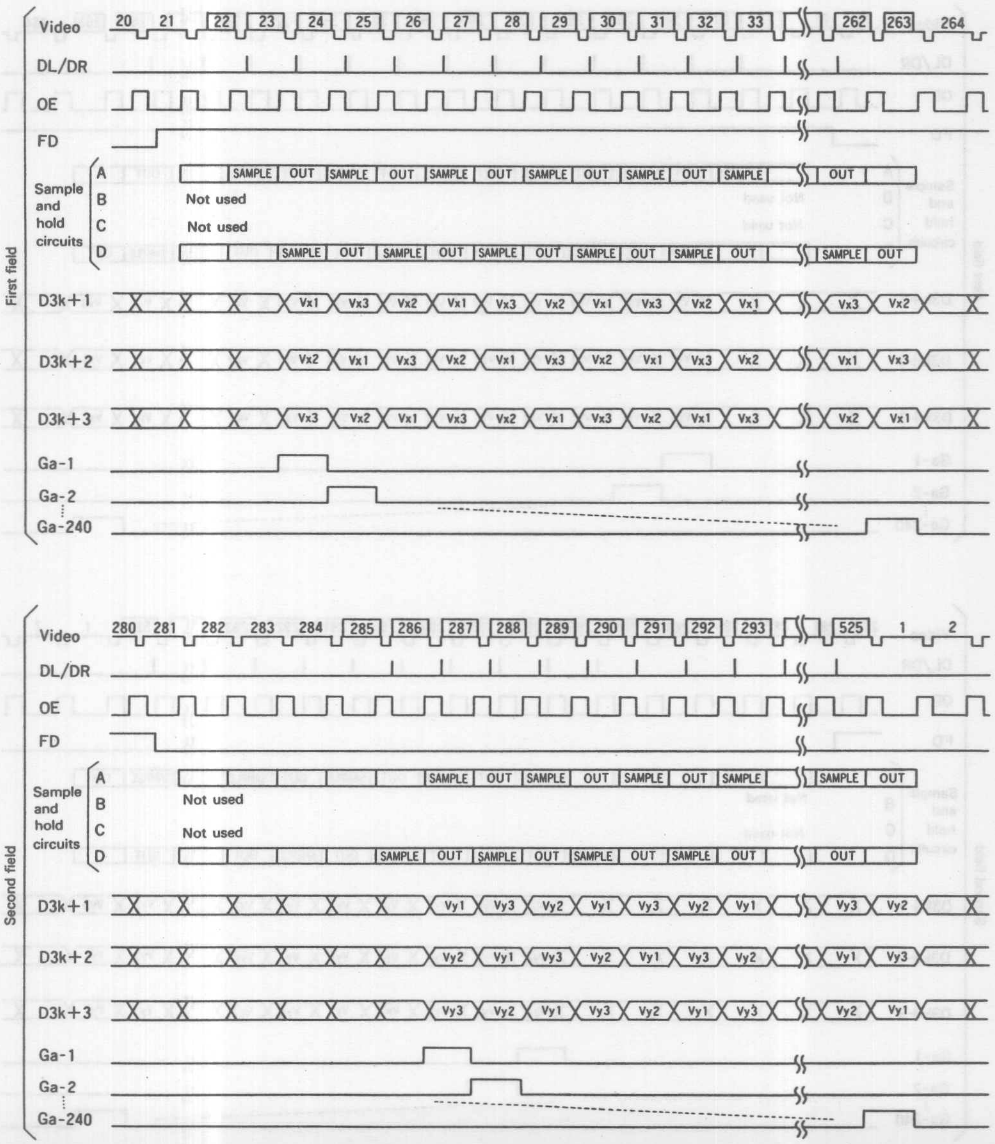
MODE17	
D/S	GND
L/F	V_{cc}
MSF1	V_{cc}
MSF2	V_{cc}

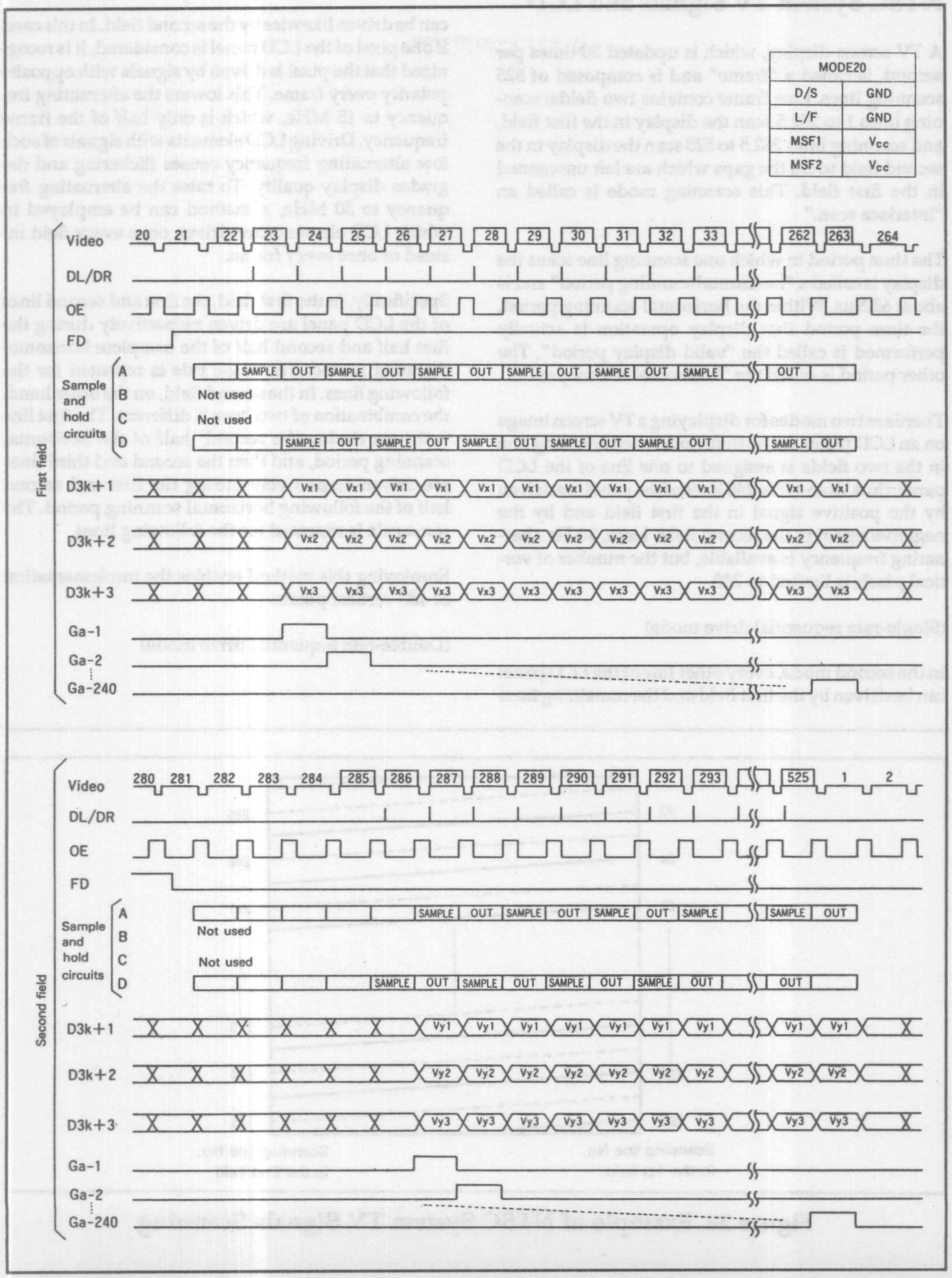


MODE18	
D/S	GND
L/F	GND
MSF1	GND
MSF2	V_{CC}



MODE19	
D/S	GND
L/F	GND
MSF1	GND
MSF2	GND




MODE20
D/S GND
L/F GND
MSF1 Vcc
MSF2 Vcc
First field
Video
20 21 22 23 24 25 26 27 28 29 30 31 32 33 262 263 264
DL/DR
OE
FD
Sample and hold circuits
A
B
C
D
SAMPLE
OUT
Not used
Not used
D3k+1
Vx1
D3k+2
Vx2
D3k+3
Vx3
Ga-1
Ga-2
Ga-240
Second field
Video
280 281 282 283 284 285 286 287 288 289 290 291 292 293 525 1 2
DL/DR
OE
FD
Sample and hold circuits
A
B
C
D
SAMPLE
OUT
Not used
Not used
D3k+1
Vy1
D3k+2
Vy2
D3k+3
Vy3
Ga-1
Ga-2
Ga-240

NTSC System TV Signals and LCD

A TV screen display, which is updated 30 times per second, is called a "frame" and is composed of 525 scanning lines. One frame contains two fields; scanning lines 1 to 262.5 scan the display in the first field, and scanning lines 262.5 to 525 scan the display in the second field to fill the gaps which are left unscanned in the first field. This scanning mode is called an "interlace scan."

The time period in which one scanning line scans the display is called a "horizontal scanning period" and is about 63.5 μs. Within the horizontal scanning period, the time period that display operation is actually performed is called the "valid display period". The other period is called the "horizontal retrace period".

There are two modes for displaying a TV screen image on an LCD panel. In the first mode, each scanning line in the two fields is assigned to one line of the LCD panel; thus, each of the 240 lines of the panel are driven by the positive signal in the first field and by the negative signal in the second field. Here, 30-Hz alternating frequency is available, but the number of vertical pixels is limited to 240.

(Single-rate sequential drive mode)

In the second mode, every other line of the LCD panel can be driven by the first field and the remaining lines can be driven likewise by the second field. In this case, if one pixel of the LCD panel is considered, it is recognized that the pixel is driven by signals with opposite polarity every frame. This lowers the alternating frequency to 15 MHz, which is only half of the frame frequency. Driving LCD elements with signals of such low alternating frequency causes flickering and degrades display quality. To raise the alternating frequency to 30 MHz, a method can be employed in which LCD elements are driven once every field instead of once every frame.

Specifically, in the first field, the first and second lines of the LCD panel are driven respectively during the first half and second half of the complete horizontal scanning period. The same rule is repeated for the following lines. In the second field, on the other hand, the combination of two lines is different. The first line is driven during the second half of the horizontal scanning period, and then the second and third lines are driven respectively during the first and second half of the following horizontal scanning period. The same rule is repeated for the following lines.

Employing this method enables the implementation of 480 vertical pixels.

(Double-rate sequential drive mode)

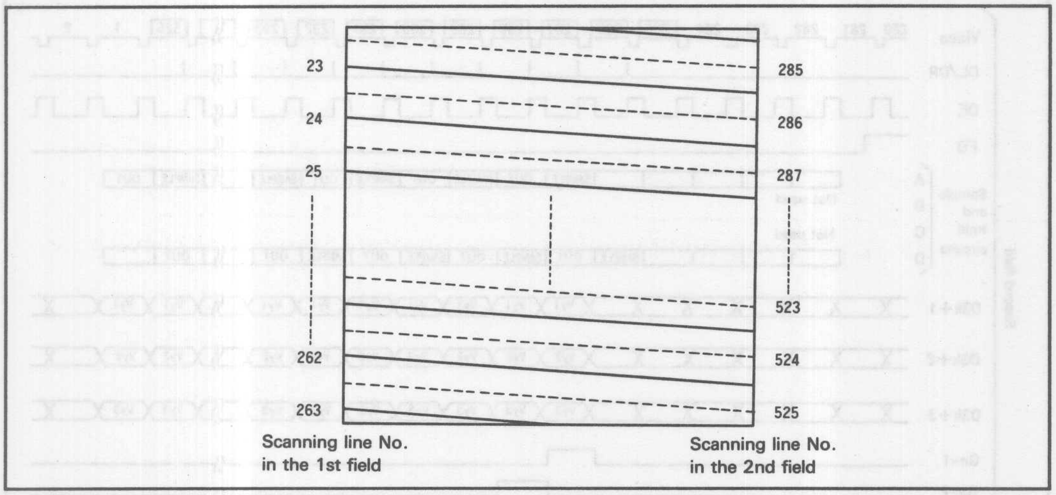


Figure 24 Example of NTSC System TV Signals Scanning

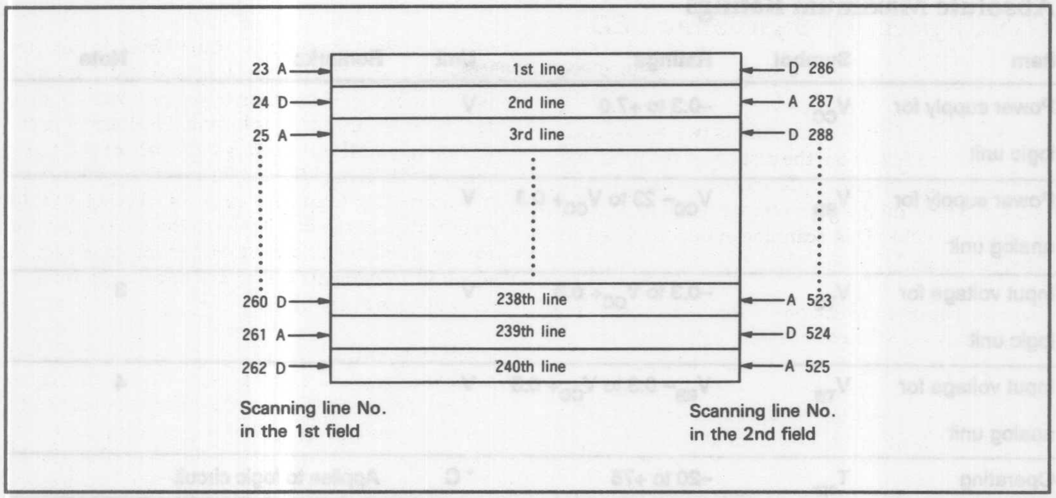


Figure 25 Middle-Resolution Display by Single-Rate Sequential Drive Mode

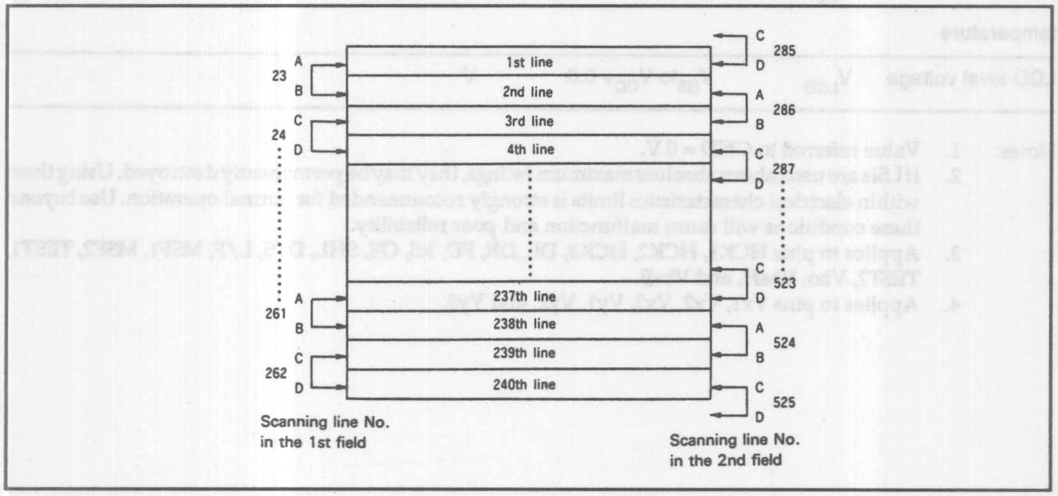


Figure 26 High-Resolution Display by Double-Rate Sequential Drive Mode

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Remarks	Note
Power supply for logic unit	V_{CC}	–0.3 to +7.0	V		
Power supply for analog unit	V_{BB}	V_{CC} – 23 to V_{CC} + 0.3	V		
Input voltage for logic unit	V_{TC}	–0.3 to V_{CC} + 0.3	V		3
Input voltage for analog unit	V_{TB}	V_{BB} – 0.3 to V_{CC} + 0.3	V		4
Operating temperature	T_{opr}	–20 to +75	°C	Applies to logic circuit	
		–10 to +60	°C	Applies to analog circuit	
Storage temperature	T_{stg}	–40 to +125	°C		
LCD level voltage	V_{LCD}	V_{BB} to V_{CC} + 0.3	V		

Notes:
1. Value referred to GND = 0 V.
2. If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.
3. Applies to pins HCK1, HCK2, HCK3, DL, DR, FD, RS, OE, SHL, D/S, L/F, MSF1, MSF2, TEST1, TEST2, Vbo, VbsH, and VbsB.
4. Applies to pins Vx1, Vx2, Vx3, Vy1, Vy2, and Vy3.

Electrical Characteristics

DC Characteristics ($V_{LCD} = V_{CC}$ = 5 V ±10%, GND = 0 V, $V_{CC} - V_{BB}$ = 16 to 20 V, Ta = –20 to +75 °C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions			Notes
Input high-level voltage	V_{IH}	$0.7\ V_{CC}$	—	V_{CC}	V				3
Input low-level voltage	V_{IL}	GND	—	$0.3V_{CC}$	V				
Output high-level voltage	V_{OH}	$V_{CC} - 0.4$	—	—	V	$-I_{OH}$ = 0.3 mA			4
Output low-level voltage	V_{OL}	—	—	0.4	V	I_{OL} = 0.3 mA			
Input leakage current (1)	I_{LI1}	–10	—	+10	µA	V_I = 0 V, V_{CC}			1
Input leakage current (2)	I_{LI2}	–10	—	+10	µA	$V_I = V_{BB}$, V_{CC}			2
Output current (1)	I_{OUT}	—	—	–150	µA	$V_{CC} - V_{BB}$ = 20 V	Dk = V_{in} – 0.5 V	OE = V_{CC}	5
		—	—	–10	µA	Apply V_{in} to Vx and Vy. $V_{in} = (V_{CC} - V_{BB})/2$		OE =GND	
Output current (2)	I_{IN}	+150	—	—	µA	$V_{bo} = V_{CC}$ – 3 V	DK = V_{in} + 0.5 V	OE = V_{CC}	
		+10	—	—	µA	$V_{bsH} = V_{CC}$ – 3 V $V_{bsB} = V_{CC}$ – 3 V		OE =GND	
Current consumption	I_{GND}	—	—	3.0	mA	f_{ck} = 2.5 MHz, $V_{bo} = V_{CC}$ – 3 V			6
	I_{BB}	—	15	30	mA	$V_{bsH} = V_{CC}$ – 3 V, $V_{bsB} = V_{CC}$ – 3 V OE = 33 kHz, FD = 30 Hz OE duty = 7/32			
Bias voltage	V_b	V_{CC} – 4.0	V_{CC} – 3.0	—	V	$V_{bo} = V_{bsH} = V_{bsB}$, C_L = 100 pF, $t_{DDR} \leq$ 6.3 µs			
Dynamic range	V_{DY}	V_{BB} + 1.5	—	V_{CC} – 3.5	V	$V_{CC} - V_{BB}$ = 20 V, T_a = –10 to +60°C –0.5 V < V_{off} < +0.5 V $V_{bo} = V_{bsH} = V_{bsB} = V_{CC}$ – 3 V			5, 7, 9

DC Characteristics ($V_{LCD} = V_{CC} = 5$ V ±10%, GND = 0 V, $V_{CC} - V_{BB} = 16$ to 20 V, Ta = –20 to +75 °C) (Cont.)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions		Notes
Offset voltage	$V_{off (L)}$	–5 – 180	—	–5 + 180	mV	$V_{CC} - V_{BB} = 20$ V $T_a = -10$ to $+60$°C $f_{ck} = 2.5$ MHz $V_{bo} = V_{bsH} = V_{bsB}$ $= V_{CC} - 3$ V	$V_{in} = -11$ V	5, 8, 9
	$V_{off (H)}$	+55 – 180	—	+55 + 180	mV		$V_{in} = -1$ V	

Notes:
1. Applies to pins HCK1, HCK2, HCK3, DL, DR, FD, RS, OE, SHL, D/S, L/F, MSF1, MSF2, TEST1, TEST2, V_{bo}, V_{bsH}, and V_{bsB}.
2. Applies to pins Vx1, Vx2, Vx3, Vy1, Vy2, and Vy3.
3. Applies to pins HCK1, HCK2, HCK3, DL, DR, FD, RS, OE, SHL, D/S, L/F, MSF1, MSF2, TEST1, and TEST2.
4. Applies to pins DL and DR.
5. Applies to pins D1 - D120.
6. The shift register is constantly shifting one 1.
   Mode setting: L/F = V_{CC}, D/S = V_{CC}, MSF1 = GND, MSF2 = V_{CC}
   (The other input pins must be V_{CC} or GND level.)
7. The operations are the same as those when offset voltage is measured.
8. Definition of "offset voltage" is shown figure 27.
9. These characteristics are defined within the temperature which is shown in the test condition.

AC Characteristics ($V_{LCD} = V_{CC} = 5\ V \pm 10\%$, GND = 0 V, $V_{CC} - V_{BB} = 16$ to 20 V, $T_a = -20$ to $+75°C$)

Item	Symbol	Min	Max	Unit	Test Condition	Notes
Three-phase clock period	t_{CKCK}	210	1000	ns		
Three-phase clock pulse width	t_{CWH} t_{CWL}	100	—	ns		
Interval between three-phase clock falling edge and rising edge	t_{fr1} t_{fr2} t_{fr3}	30	—	ns		1
Interval between three-phase clock rising edge and falling edge	t_{rf}	20	—	ns		2
Clock rise and fall times	t_{ct}	—	30	ns		
DL, DR input setup time	t_{su}	50	—	ns		
DL, DR input hold time	t_{HLI}	20	—	ns		
DL, DR output delay time	t_{pd}	—	90	ns	$C_L = 15$ pF	
DL, DR output hold time	t_{HLO}	5	—	ns		
OE input period	t_{CYCO}	30	80	µs		
OE input high-level pulse width	t_{OWH}	3	15	µs		
OE rise and fall times	t_{or} t_{of}	—	30	ns		
FD input setup time	t_{FS}	100	—	ns		
FD input hold time	t_{FH}	100	—	ns		

Notes:
1. Necessary for preventing the three-phase shift register from racing.
2. t_{rf} must satisfy the DR and DL input hold time (t_{HLI}) of the next horizontal driver. ($t_{rf} + t_{HLO} > t_{HLI}$)

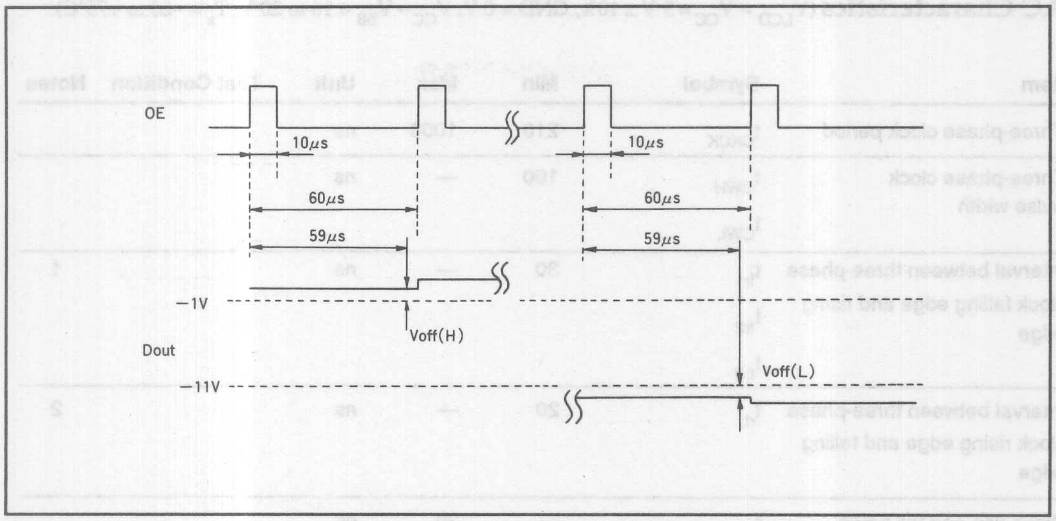


Figure 27 Offset Voltage

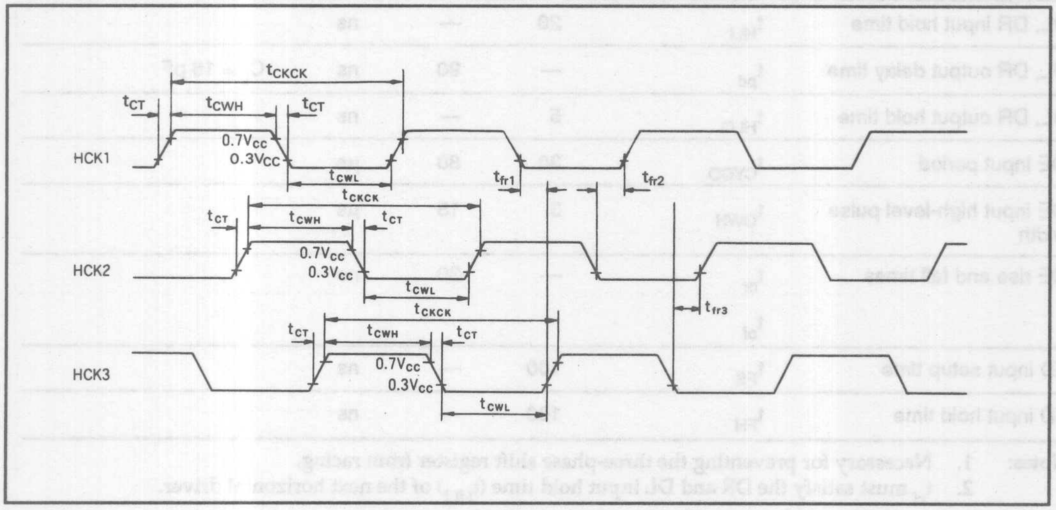


Figure 28 Three-Phase Clock Timing

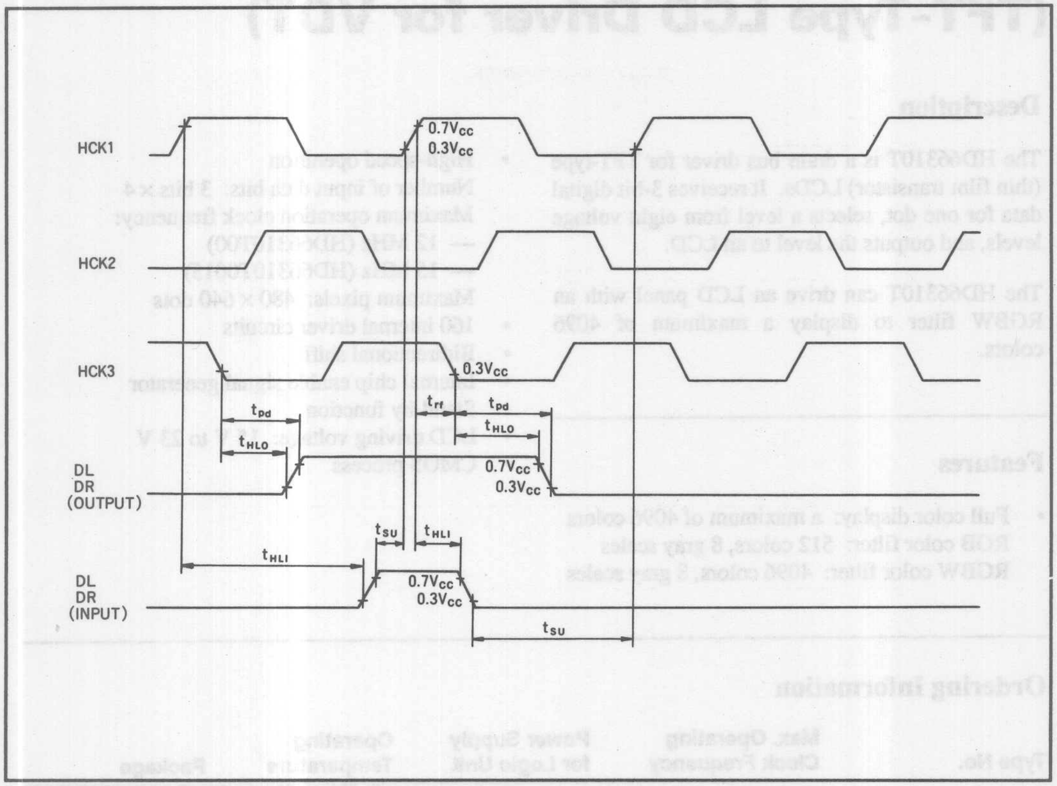


Figure 29 Input and Output Timing

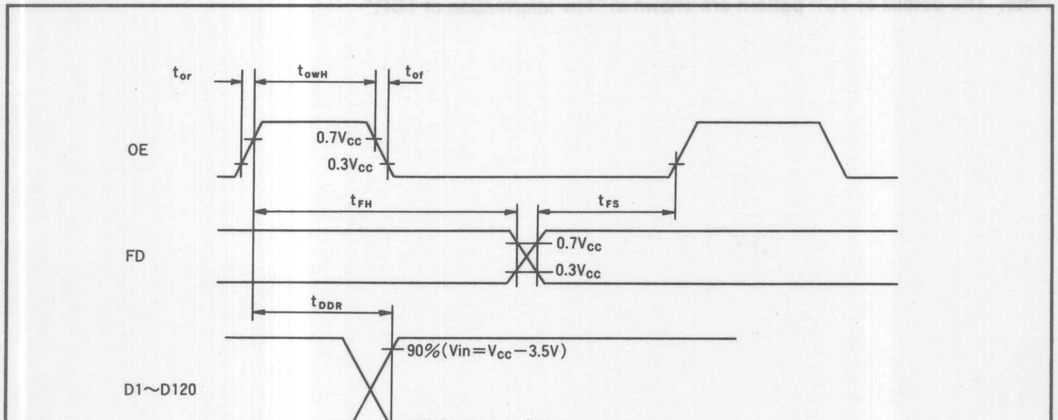


Figure 30 OE, FD Input Timing, Driver Output Timing

HD66310T
(TFT-Type LCD Driver for VDT)

Description

The HD66310T is a drain bus driver for TFT-type (thin film transistor) LCDs. It receives 3-bit digital data for one dot, selects a level from eight voltage levels, and outputs the level to an LCD.

The HD66310T can drive an LCD panel with an RGBW filter to display a maximum of 4096 colors.

Features

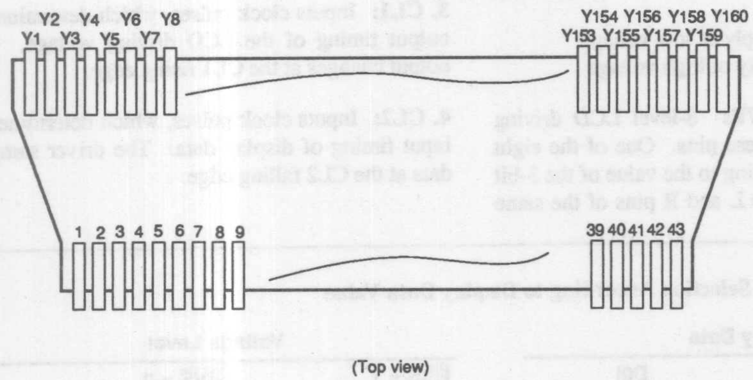
- Full color display: a maximum of 4096 colors
  RGB color filter: 512 colors, 8 gray scales
  RGBW color filter: 4096 colors, 8 gray scales
- High-speed operation
  Number of input data bits: 3 bits × 4
  Maximum operation clock frequency:
  — 12 MHz (HD66310T00)
  — 15 MHz (HD66310T0015)
  Maximum pixels: 480 × 640 dots
- 160 internal driver circuits
- Bidirectional shift
- Internal chip enable signal generator
- Stand-by function
- LCD driving voltage: 15 V to 23 V
- CMOS process

Ordering Information

Type No.	Max. Operating Clock Frequency	Power Supply for Logic Unit	Operating Temperature	Package
HD66310T00	12 MHz	5 V ± 10%	–20 to +75°C	203-pin TCP
HD66310T0015	15 MHz	5 V ± 5%	–20 to +65°C	

Note: The details of TCP pattern are shown in "The Information of TCP."

Pin Arrangement



1	V0L	22	DMY1
2	V1L	23	D20
3	V2L	24	D21
4	V3L	25	D22
5	V4L	26	D23
6	V5L	27	DMY2
7	V6L	28	CL1
8	V7L	29	CL2
9	V_{CC1}	30	BS
10	V_{CC2}	31	SHL
11	EIO1	32	EIO2
12	$\overline{RVS}$	33	TEST
13	D00	34	GND
14	D01	35	V_{EE}
15	D02	36	V7R
16	D03	37	V6R
17	DMY0	38	V5R
18	D10	39	V4R
19	D11	40	V3R
20	D12	41	V2R
21	D13	42	V1R
		43	V0R

Note: This does not apply to TCP dimensions.

Pin Description

Pin List

Pin Name	Number of Pins	Input/Output	Functions (Refer to)
$V_{CC}1$, $V_{CC}2$	2	Power supply	1.
GND	1	Power supply	
V_{EE}	1	Power supply	
V0L–V7L, V0R–V7R	16	Power supply	2.
CL1	1	Input	3.
CL2	1	Input	4.
D00, D10, D20, to D03, D13, D23	12	Input	5.
$\overline{RVS}$	1	Input	6.
SHL	1	Input	7.
EIO1, EIO2	2	Input/output	8.
TEST, BS	2	Input	9.
Y1–Y160	160	Output	10.
DMY0–DMY2	3	—	11.

Pin Functions

1. $V_{CC}1$, $V_{CC}2$, GND, V_{EE}: These pins are used for the power supply.

V_{CC}–GND: Power supply of low voltage
V_{CC}–V_{EE}: Power supply of high voltage

2. V0L–V7L, V0R–V7R: 8-level LCD driving voltage is applied to these pins. One of the eight levels is selected according to the value of the 3-bit input display data. The L and R pins of the same voltage level are connected in the driver.

3. CL1: Inputs clock pulses, which determine the output timing of the LCD driving voltage. The output changes at the CL1 rising edge.

4. CL2: Inputs clock pulses, which determine the input timing of display data. The driver samples data at the CL2 falling edge.

Table 1 Voltage Level Selection According to Display Data Value

Display Data			Voltage Level	
D2j	D1j	D0j	$\overline{\text{RVS}}$ = 1	$\overline{\text{RVS}}$ = 0
0	0	0	V0	V7
0	0	1	V1	V6
0	1	0	V2	V5
0	1	1	V3	V4
1	0	0	V4	V3
1	0	1	V5	V2
1	1	0	V6	V1
1	1	1	V7	V0

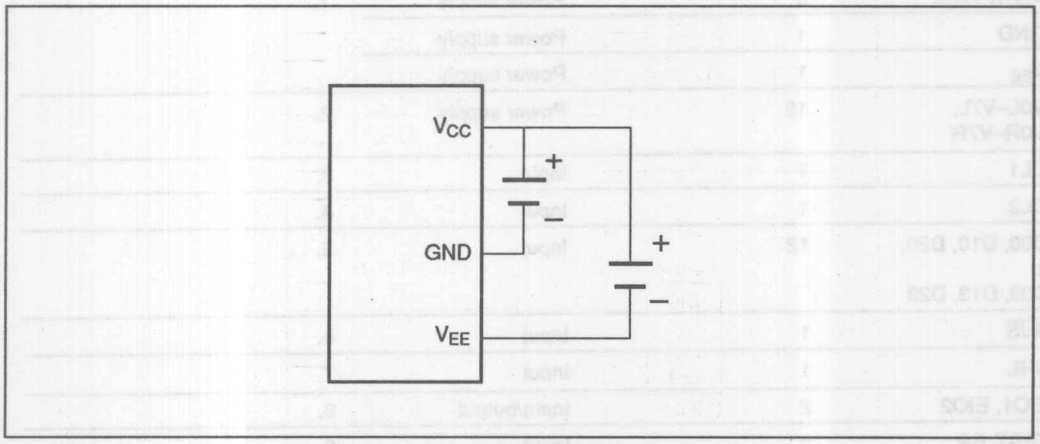


Figure 1 Power Supply for the Device

5. D00–D03, D10–D13, D20–D23: Input display data. See table 1 for the voltage level selection by the display data.

6. $\overline{\text{RVS}}$: Determines if logical I/O display data is reversed. Display data is reversed when $\overline{\text{RVS}}$ is low.

7. SHL: Selects the shift direction of display data.

8. EIO1, EIO2: Inputs/outputs chip enable signals. The SHL signal selects which pin is for input or output. When the chip enable input signal is low, data input starts. When display data corresponding to 160 outputs are input, the chip enable output signal changes from high to low.

9. TEST, BS: Used for test purposes only. Connect to a low level for normal operation.

10. Y1–Y160: Output LCD driving signals.

11. DMY0–DMY2: Reserved pins that should be left open.

Table 2 Input/Output Selection for EIO1 and EIO2

SHL	EIO1	EIO2
GND	Input	Output
V_{CC}	Output	Input

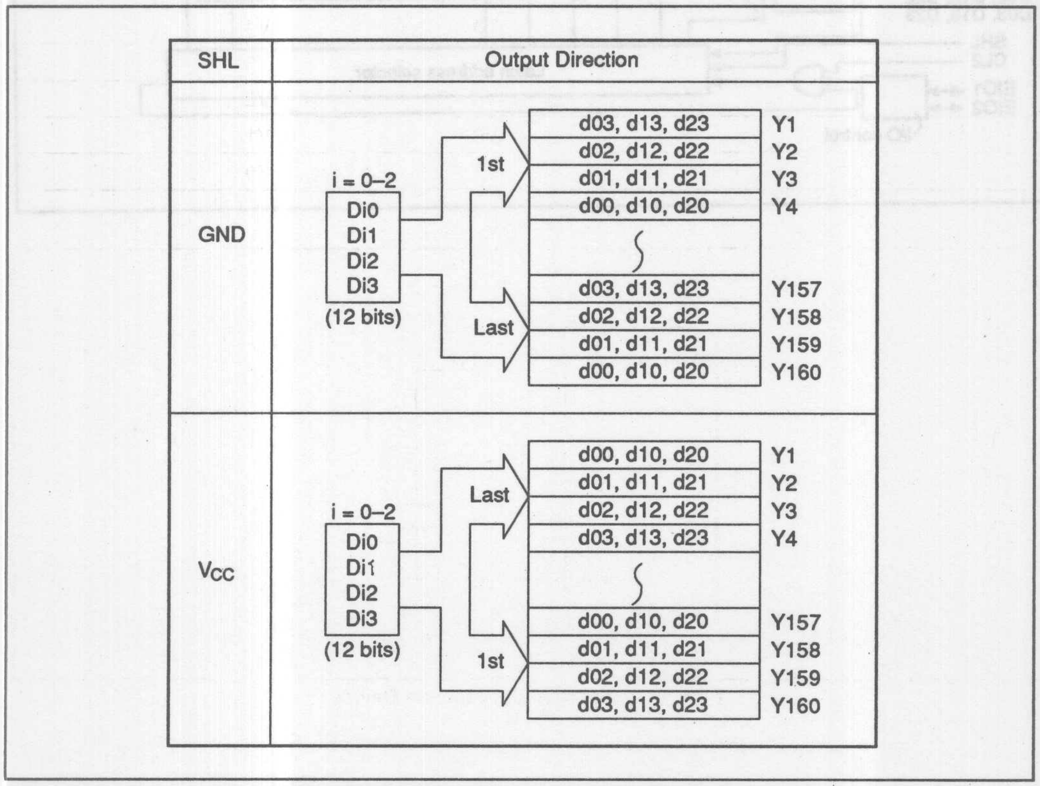
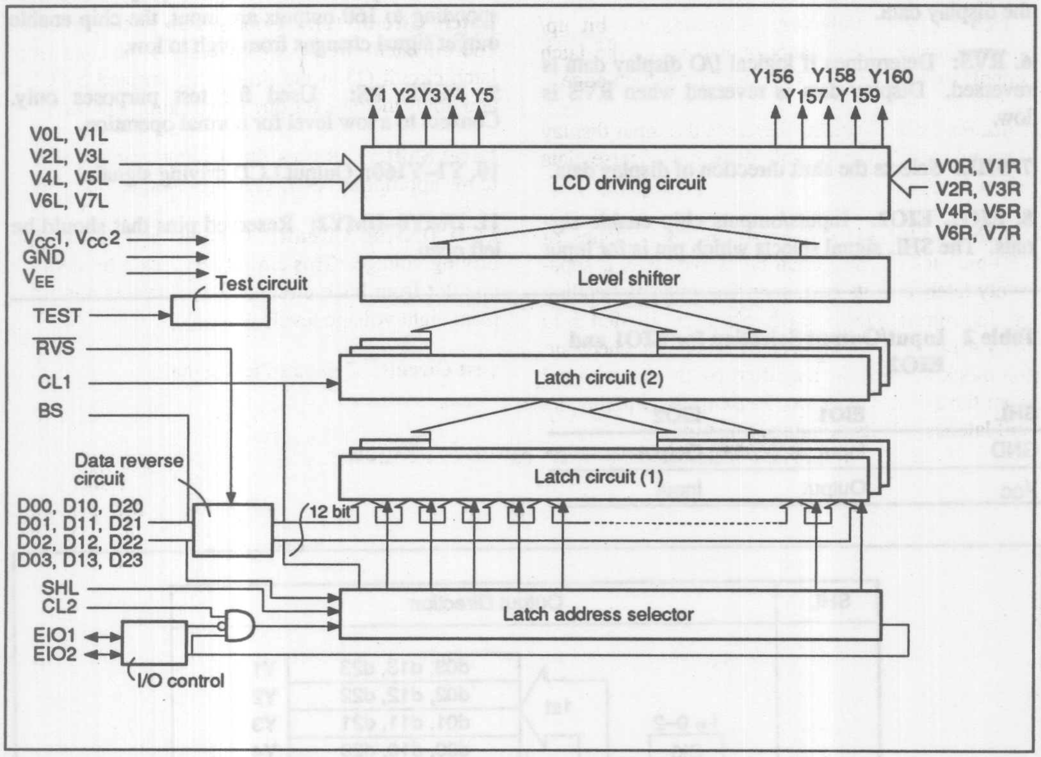


Figure 2 Display Data and Output Direction

Internal Block Diagram



Block Functions

Latch Address Selector: Contains a 6-bit up/down counter and a decoder, and sends the latch signals to latch circuit (1) at the CL2 falling edge.

Data Reverse Circuit: Reverses the input display data when $\overline{RVS}$ = 0, and does not reverse data when $\overline{RVS}$ = 1.

Latch Circuit (1): Consists of three planes of 160-bit latch circuit. Each bit of 3-bit data is separately latched in its corresponding plane depending on its significance. Each plane is divided into forty 4-bit blocks, and all four bits are latched into the block at once, as specified by the latch signal from the address selector. In total, the 3-plane circuit latches 12 bits of data at one time.

Latch Circuit (2): Consists of three planes of 160-bit latch circuit, which latches the data from latch circuit (1) at the timing determined by CL1, and holds the data for one line scanning period.

Level Shifter: Raises the driving voltage of 5 V to the appropriate LCD driving voltage.

LCD Driving Circuit: Outputs an 8-level LCD driving voltage. This circuit receives 3-bit data for one dot from latch circuit (2) and selects one level from eight voltage levels.

Test Circuit: Generates test signals.

System Configuration

A block configuration of the TFT-type color display system using the HD66310 is shown in figure 3.

The HD66310 receives 3-bit data for one pixel and selects one of the eight LCD driving voltage levels to send to the LCD. The LCD driving output circuit, which is produced by the CMOS structure, can use any LCD driving voltage level from V_{CC} to V_{EE}. When the LCD panel uses an RGB color filter (the Triad arrangement), 512 (8^3) colors can be displayed. When using an RGBW color filter (the Quad arrangement), 4096 (8^4) colors can be displayed.

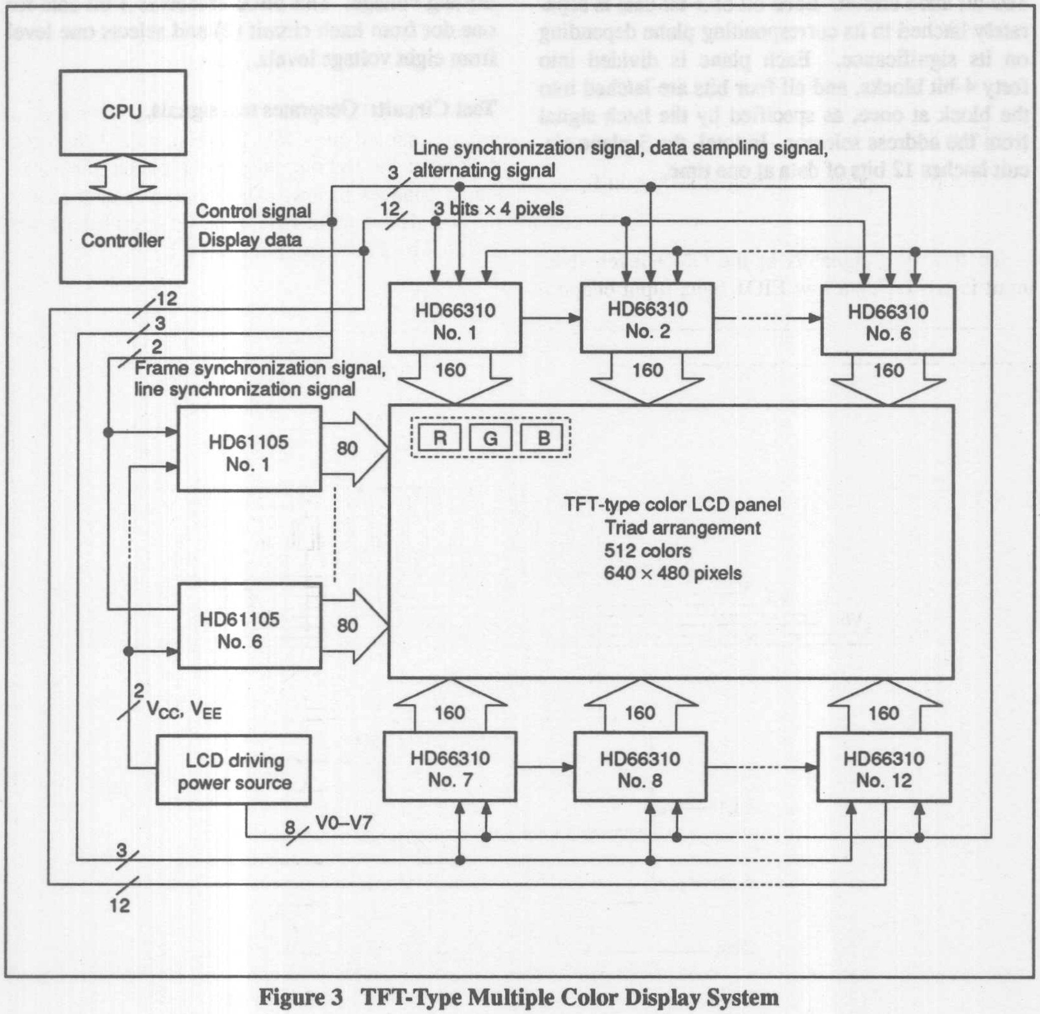


Figure 3 TFT-Type Multiple Color Display System

Internal Operation

8-Level Output

The HD66310 internal circuit unit for one data output is shown in figure 4. The circuit receives 3-bit data (D0j, D1j, D2j) and selects one of eight voltage levels (V0–V7) to output to the LCD.

The transfer gates of the output circuit are produced by the CMOS structure. Therefore, any voltage level between V_{CC} to V_{EE} can be applied to lines V0 to V7.

The HD66310 has 160 of the above circuits.

Operation Timing

The HD66310 operation timing is shown in figure 5.

When the SHL signal is at the GND level, data input is started by a low EIO1 (data input enable) signal. At the CL2 falling edge, 12 bits of data, which are for four outputs (3 bits for gray scales × 4 outputs), are input together. When the data input corresponding to 160 outputs are completed, the HD66310 automatically enters the stand-by mode, and the EIO2 signal changes to low.

The LCD driving output changes at the CL1 rising edge. The voltage level selected by data d1 is output from pin Y1, and the level selected by d160 is output from Y160. See table 1 for the voltage level selection by the input data.

When the SHL signal is at the V_{CC} level, data input is started by a low EIO2 signal. When the data input for 160 outputs are completed, the EIO1 signal changes to low. The voltage level selected by data d1 is output from pin Y160, and the level selected by d160 is output from Y1.

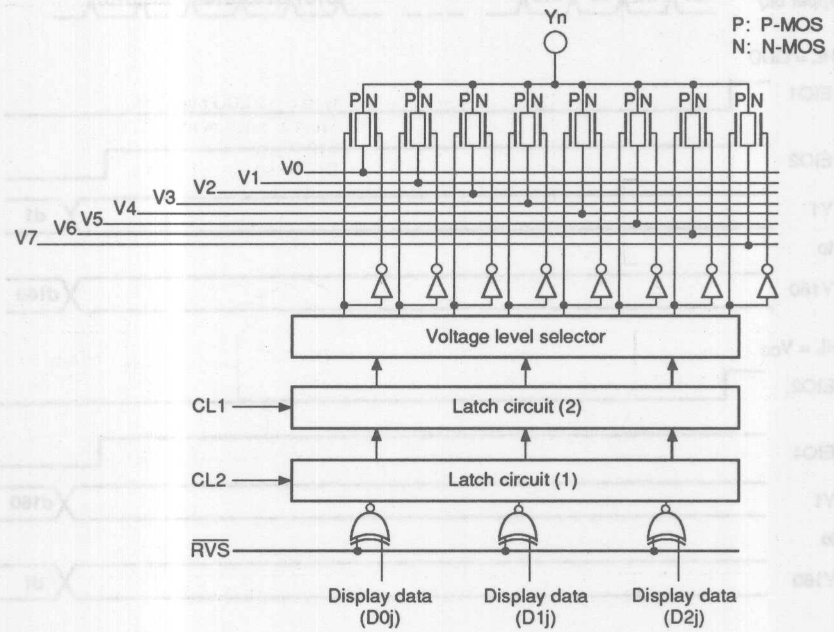


Figure 4 LCD Driving Circuit

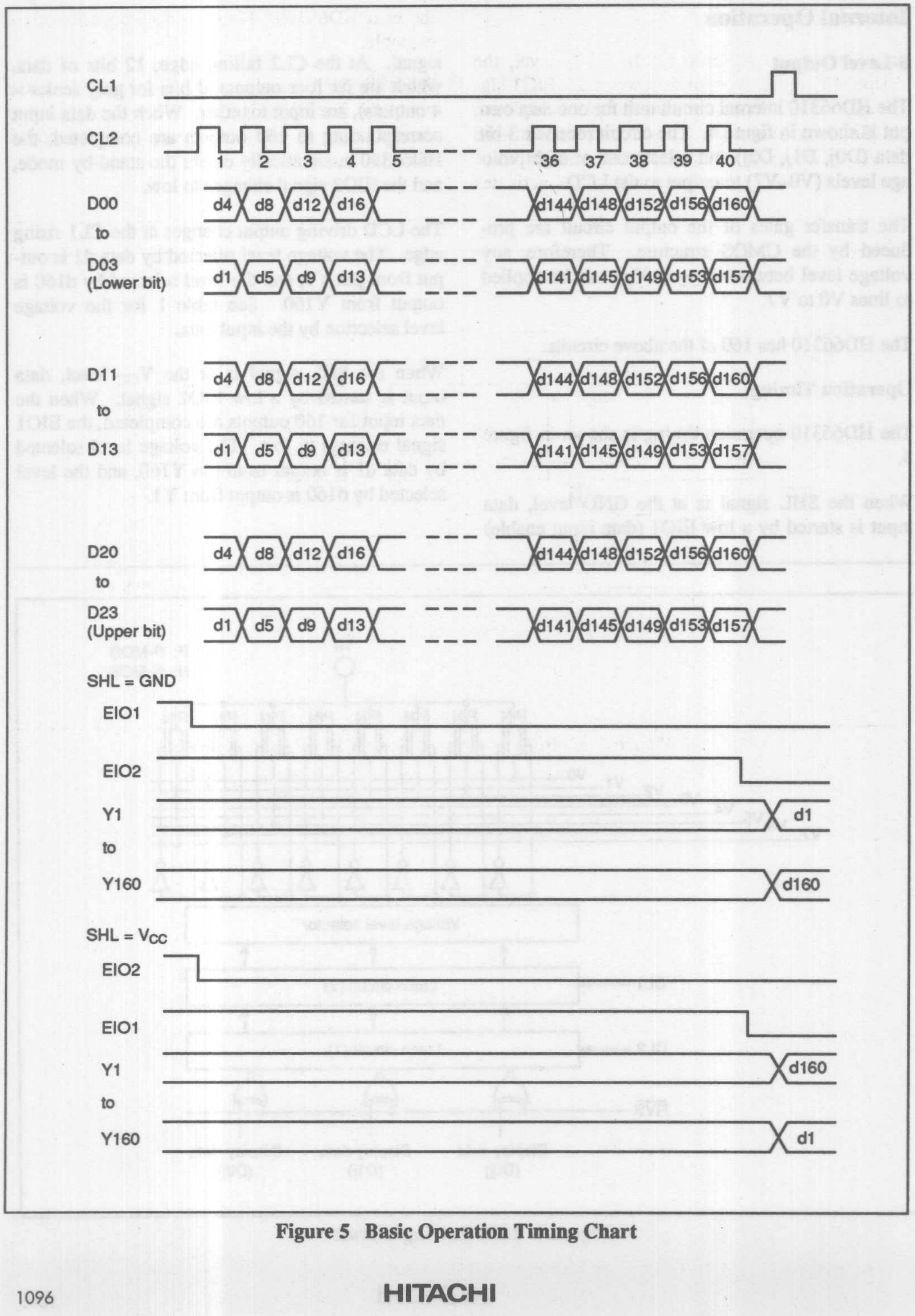


Figure 5 Basic Operation Timing Chart

Cascade Connection

When the SHL signal is at the GND level, the HD66310 begins to input data when the EIO1 signal goes low. When the data input is completed, the EIO2 signal changes to low. By connecting the EIO2 pin of the first HD66310 to the EIO1 pin of the next HD66310, the low EIO2 signal activates the next HD66310. Figure 6 shows a connection example.

When the SHL signal is at the V_{CC} level, the EIO2 pin of the first HD66310 is connected to GND, and the EIO1 pin is connected to the next HD66310 EIO2 pin.

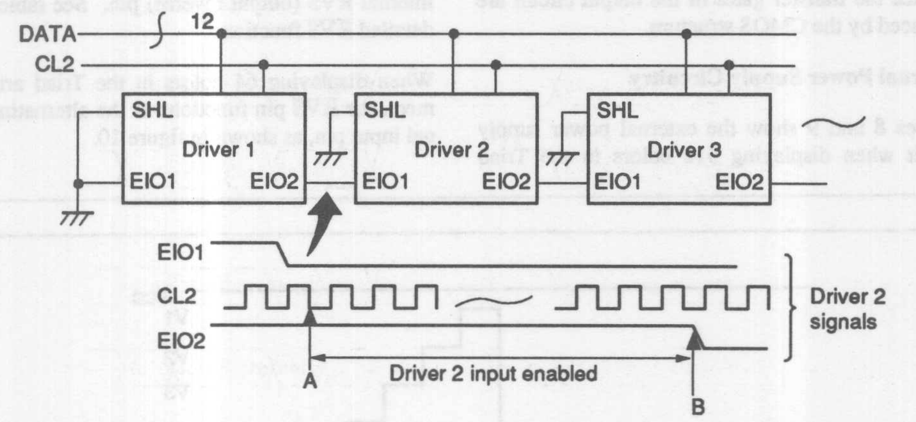


Figure 6 Chip Enable Operation (SHL = GND)

LCD Driving Power Supply Circuitry

Multiple-Level Driving Voltage Method

AC voltage must be applied to the LCD, since DC voltage deteriorates the LCD. To display eight gray scales, 16 voltage levels, shown in figure 7, must be applied.

Although the HD66310 has eight LCD driving voltage input levels, it can output 16 driving voltage levels using the level selector shown in figure 8, since the transfer gates of the output circuit are produced by the CMOS structure.

External Power Supply Circuitry

Figures 8 and 9 show the external power supply circuit when displaying 512 colors in the Triad arrangement, and figure 10 shows the circuit for displaying 64 colors in the Triad arrangement. Table 3 shows the specifications of the LCD panel and the HD66310 pins for each power supply circuit.

The circuit shown in figure 8 is the basic one used when displaying 512 colors in the Triad arrangement. However, the HD66310 can dispense with the level selector, as shown in figure 9, using the internal $\overline{\text{RVS}}$ (output reverse) pin. See table 1 for detailed $\overline{\text{RVS}}$ functions.

When displaying 64 colors in the Triad arrangement, the $\overline{\text{RVS}}$ pin functions as the alternating signal input pin, as shown in figure 10.

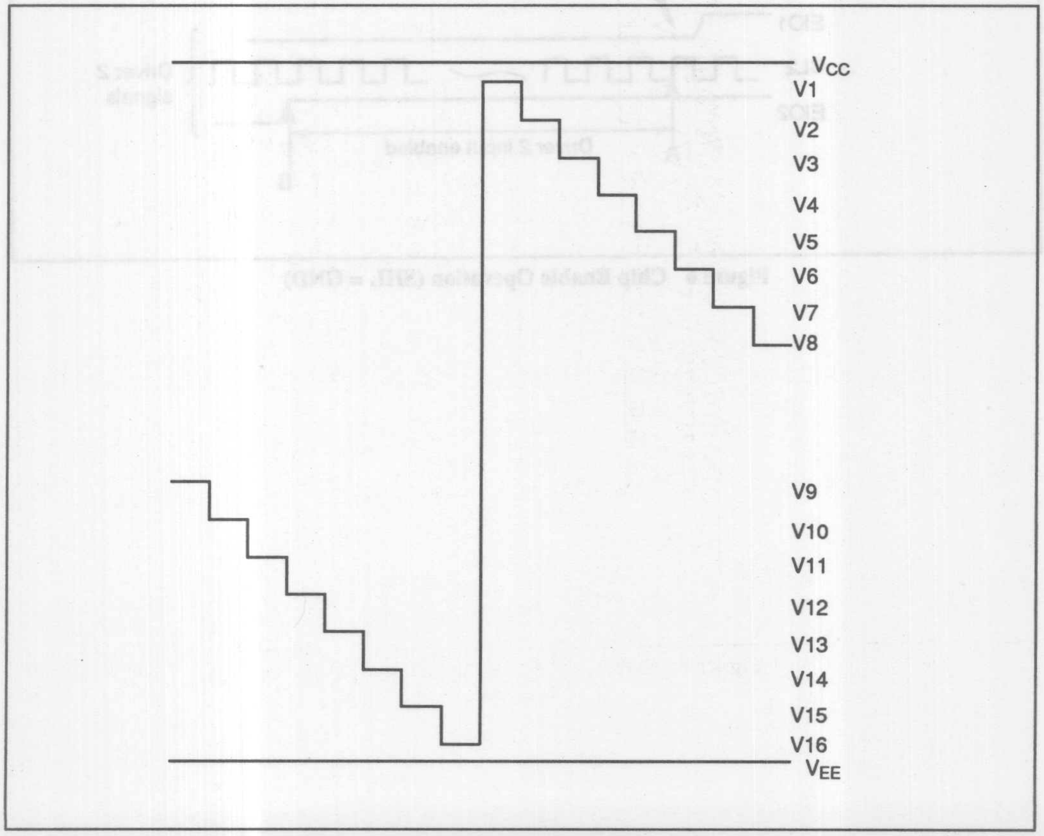


Figure 7 HD66310 Output Waveform

Table 3 Color Display and Pin Specifications

Output Level	Panel Spec.	Display Data Di2	Di1	Di0	$\overline{RVS}$ pin	Power Supply (Refer to)
8 × 2 (AC)	Quad: 4096 colors Triad: 512 colors	1/0 (upper bit)	1/0	1/0 (lower bit)	1	Fig. 8
8 × 2 (AC)	Quad: 4096 colors Triad: 512 colors	1/0 (upper bit)	1/0	1/0 (lower bit)	Alternating signal	Fig. 9
4 × 2 (AC)	Quad: 256 colors Triad: 64 colors	1	1/0 (upper bit)	1/0 (lower bit)	Alternating signal	Fig. 10

1: V_{CC} level voltage
0: GND level voltage

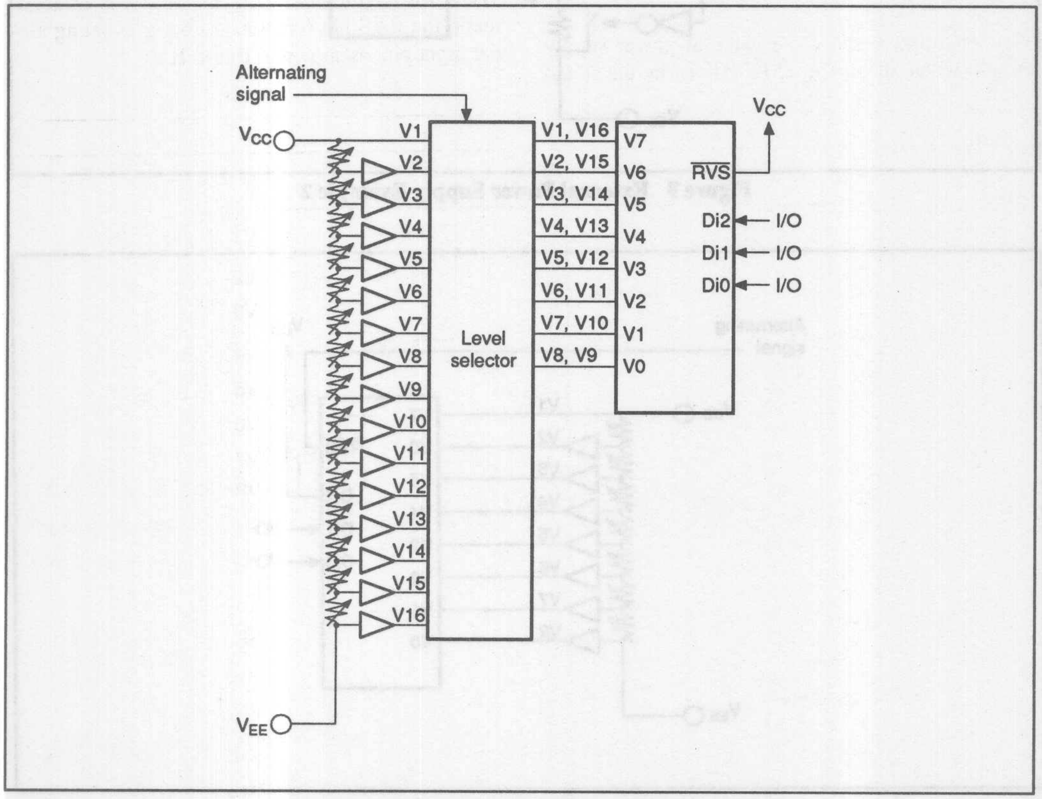


Figure 8 External Power Supply Example 1

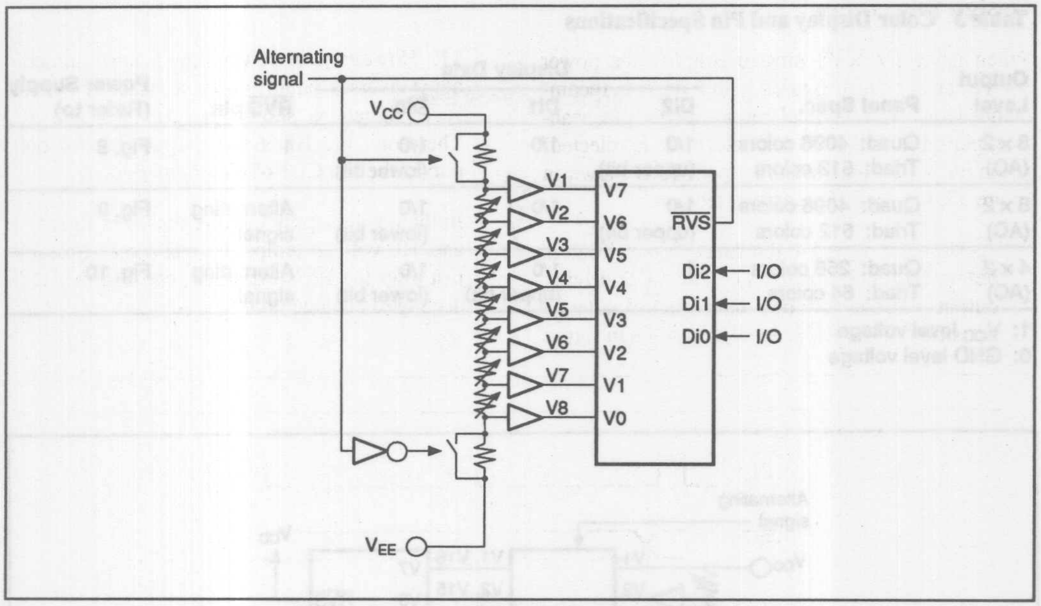


Figure 9 External Power Supply Example 2

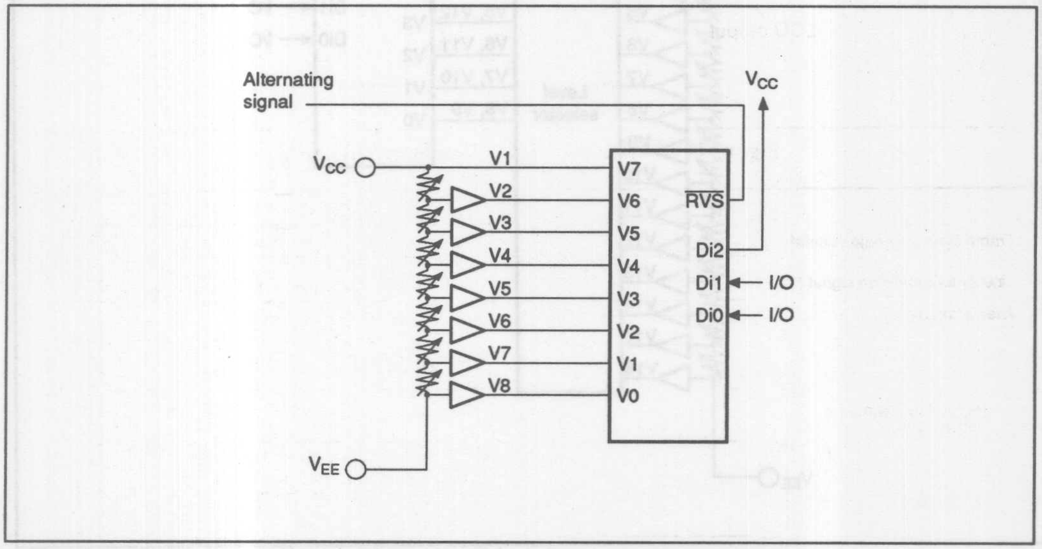


Figure 10 External Power Supply Example 3

Design for Timing

When using the $\overline{RVS}$ pins to simplify the power source, as shown in figures 9 and 10, it is recommended to add a vertical retrace period, (a scanning period in which no scan electrode is selected) at the end of a frame scanning period, as shown in figure 12, for the following two reasons.

- As shown in figure 4, the data reverse circuit is before the latch circuit (1). The LCD driving output is reversed one CL1 period after a transition of the $\overline{RVS}$ signal, as shown in figure 11. However, the power supply lines immediately reverses polarity after a transition of the $\overline{RVS}$ signal, as shown in figures 9 and 10. Therefore, the HD66310 outputs invalid data during the last CL1 of a frame period.
- In the power supply circuits shown in figures 9 and 10, voltage temporarily becomes unstable just after the $\overline{RVS}$ transition, causing the LCD display to become jumbled.

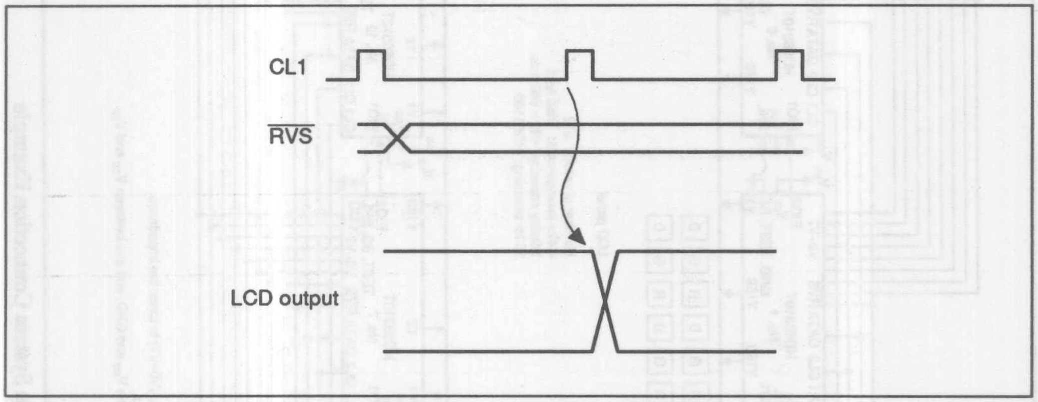


Figure 11 $\overline{RVS}$ and LCD Driving Signals Timing

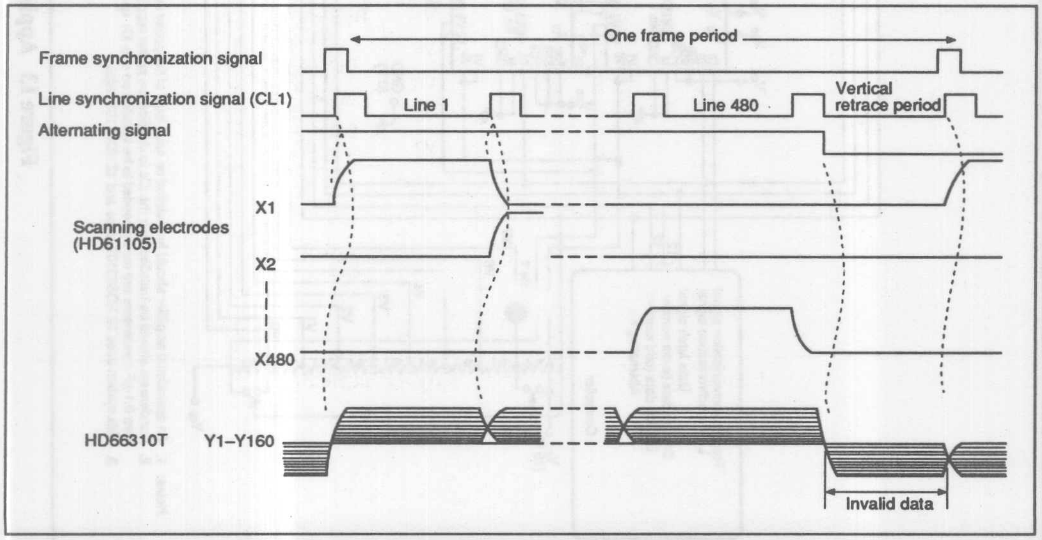
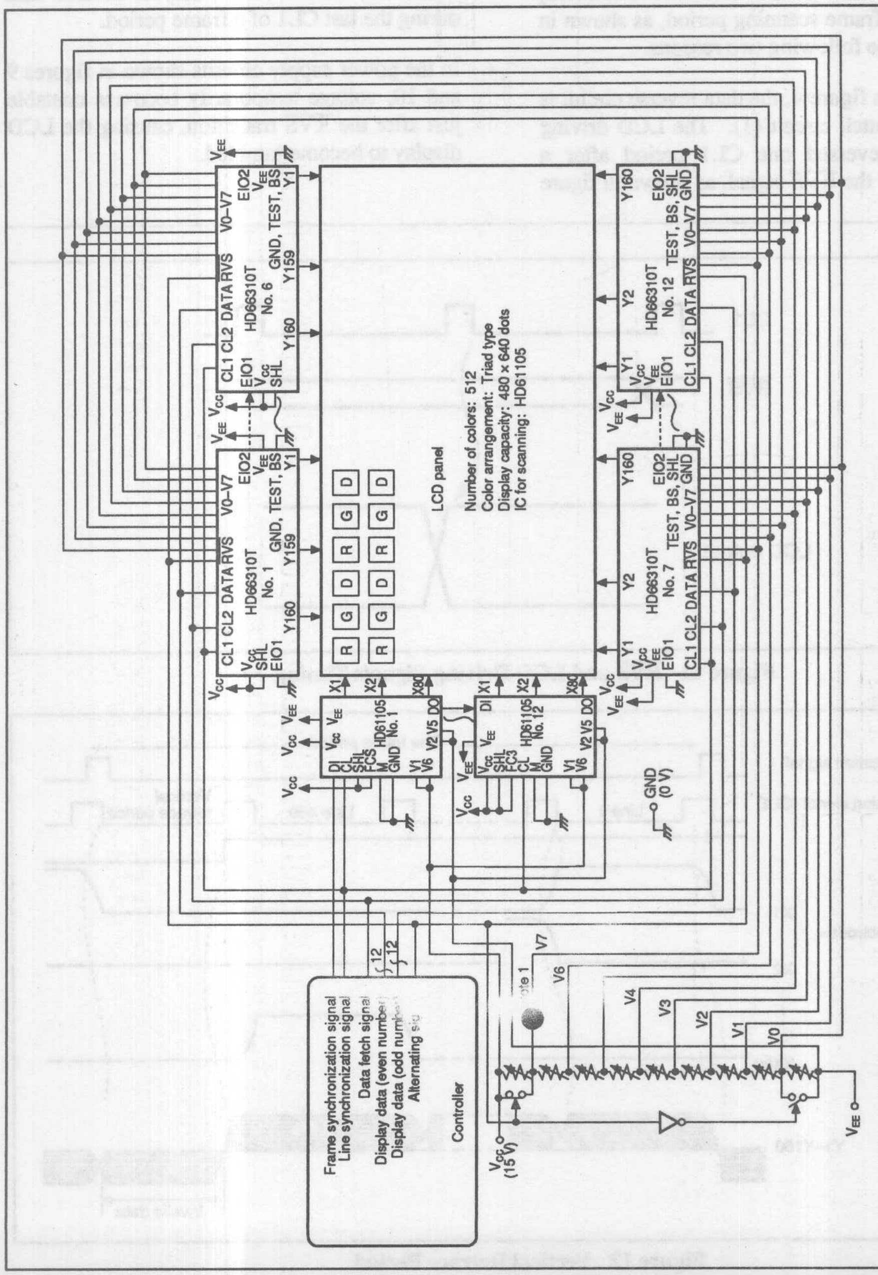


Figure 12 Vertical Retrace Period

Application

Figure 13 shows an HD66310T application for a 480 × 640-dot, 512-color LCD panel. Figure 14 shows the operation timing chart for the system.



Notes: 1. An operational amplifier should be installed on each level of the power supply line (V0–V7) to lower the impedance.
2. Condensers should be installed near the ICs to stabilize the power supply voltage.
Two 0.1-µF condensers are recommended to be installed on one IC: one between V_{CC} and GND, and one between V_{CC} and V_{EE}.
3. This system uses 12 HD66310T chips and 12 HD61105 chips.

Figure 13 Application System Connection Example

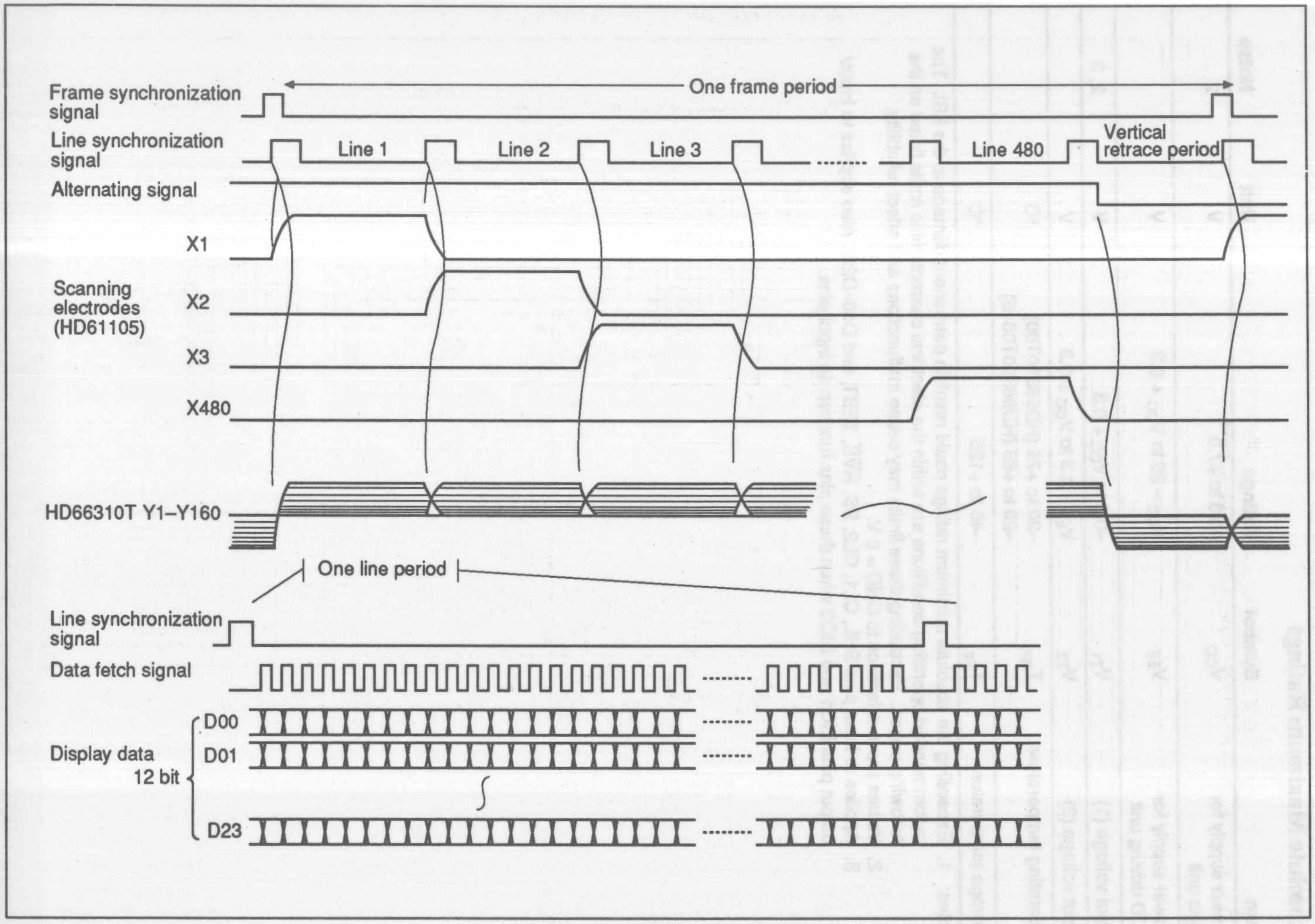


Figure 14 Timing Chart

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Notes
Power supply for logic unit	V_{CC}	–0.3 to +7.0	V	2
Power supply for LCD driving unit	V_{EE}	V_{CC} – 25 to V_{CC} + 0.3	V	
Input voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Input voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	
Operating temperature	T_{opr}	–20 to +75 (HD66310T00) –20 to +65 (HD66310T0015)	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

Notes: 1. Exceeding the absolute maximum ratings could result in permanent damage to the LSI. The recommended operating conditions are within the electrical characteristic limits listed on the following pages. Exceeding these limits may cause malfunctions and affect reliability.

2. Values are in reference to GND = 0 V.
3. Applies to input pins SHL, CL1, CL2, BS, $\overline{RVS}$, TEST, and D00–D23. Also applies to input/output pins EIO1 and EIO2 when these pins function as input pins.

Electrical Characteristics

DC Characteristics
(V_{CC} = +5 V ±10%, GND = 0 V, $V_{CC} - V_{EE}$ = 15 to 23 V, T_a = –20 to +75°C in 12 MHz version)
(V_{CC} = +5 V ±5%, GND = 0 V, $V_{CC} - V_{EE}$ = 15 to 23 V, T_a = –20 to +65°C in 15 MHz version)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Notes
LCD driving power supply voltage	$V_{CC} - V_{EE}$	15		23	V		1
Input high-level voltage (1)	V_{IH1}	$0.8 \times V_{CC}$		V_{CC}	V		2
Input low-level voltage (1)	V_{IL1}	0		$0.2 \times V_{CC}$	V		2
Input high-level voltage (2)	V_{IH2}	$0.75 \times V_{CC}$		V_{CC}	V		3
Input low-level voltage (2)	V_{IL2}	0		$0.25 \times V_{CC}$	V		3
Output high-level voltage	V_{OH}	$V_{CC} - 0.4$			V	I_{OH} = –0.4 mA	4
Output low-level voltage	V_{OL}			0.4	V	I_{OL} = 0.4 mA	4
Input leakage current (1)	I_{L1}	–5.0		+5.0	µA	$V_{IN} = V_{CC}$ to GND	5
Input leakage current (2)	I_{L2}	–10		+10	µA	$V_{IN} = V_{CC}$ to GND	6
Input leakage current (3)	I_{L3}	–100		+100	µA	$V_{IN} = V_{CC}$ to V_{EE}	7
LCD driver on resistance	RON			2.5	kΩ	$V_{CC} - V_{EE}$ = 20 V	8
Current consumption (1)	$-I_{P1}$			25 30	mA mA	Data fetch 12 MHz Data fetch 15 MHz	9, 11
Current consumption (2)	$-I_{P2}$			2 2.5	mA mA	Stand-by 12 MHz Stand-by 15 MHz	9, 11
Current consumption (3)	$-I_{P3}$			3 3.7	mA mA	12 MHz 15 MHz	10, 11

Notes:
1. Voltage between V_{CC} and V_{EE}.
2. Applies to CL1, CL2, SHL, Dij, $\overline{RVS}$, TEST, and BS.
3. Applies to EIO1 (input) and EIO2 (input).
4. Applies to EIO1 (output) and EIO2 (output).
5. Applies to CL1, CL2, SHL, $\overline{RVS}$, Dij, TEST, and BS.
6. Applies to EIO1 (input) and EIO2 (input).
7. Applies to V0L to V7L and V0R to V7R.
8. Applies to Y1 to Y160.
9. Current between V_{CC} and GND under the conditions of $V_{IH} = V_{CC}$, V_{IL} = 0 V, and no load on the output pins.
10. Current between V_{CC} and V_{EE} under the conditions of $V_{IH} = V_{CC}$, V_{IL} = 0 V, and no load on the output pins.
11. f_{CL2} and f_{CL1} are 15 MHz, 37.5 kHz respectively in 15 MHz version.

AC Characteristics

(V_{CC} = +5 V ±10%, GND = 0 V, T_a = –20 to +75°C in 12 MHz version)
(V_{CC} = +5 V ±5%, GND = 0 V, T_a = –20 to +65°C in 15 MHz version)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Notes
Clock period	t_{CYC}	83 (66)			ns		1
Clock high-level pulse width	t_{CWH}	30 (23)			ns		1
Clock low-level pulse width	t_{CWL}	30 (23)			ns		1
Clock rise time	t_R			10 (10)	ns		2
Clock fall time	t_F			10 (10)	ns		2
Clock setup time	t_{SU}	100 (100)			ns		2
Clock hold time	t_H	100 (100)			ns		2
Data setup time	t_{DSU}	20 (10)			ns		3
Data hold time	t_{DH}	30 (25)			ns		3
Enable input setup time	t_{ESU}	20 (10)			ns		4
Enable output delay time	t_{ED}			53 (46)	ns	See figure 16 for test load	4
CL1 high-level pulse width	t_{WH}	100 (100)			ns		5
$\overline{\text{RVS}}$ setup time	t_{RSU}	50 (50)			ns		6
$\overline{\text{RVS}}$ hold time	t_{RH}	50 (50)			ns		6

Data in ( ) is the characteristics in 15 MHz version.

Notes: 1. Applies to CL2.
2. Applies to CL1 and CL2.
3. Applies to Dij and CL2.
4. Applies to EIO1, EIO2, and CL2.
5. Applies to CL1.
6. Applies to $\overline{\text{RVS}}$ and CL2.

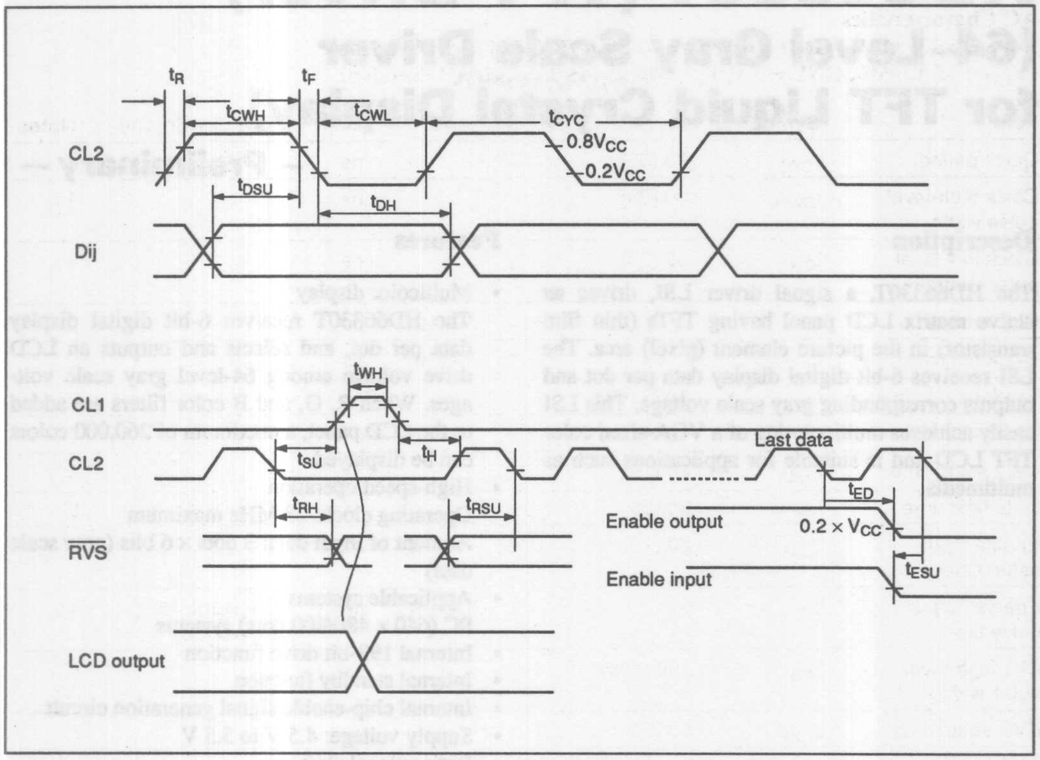


Figure 15 Timing Chart

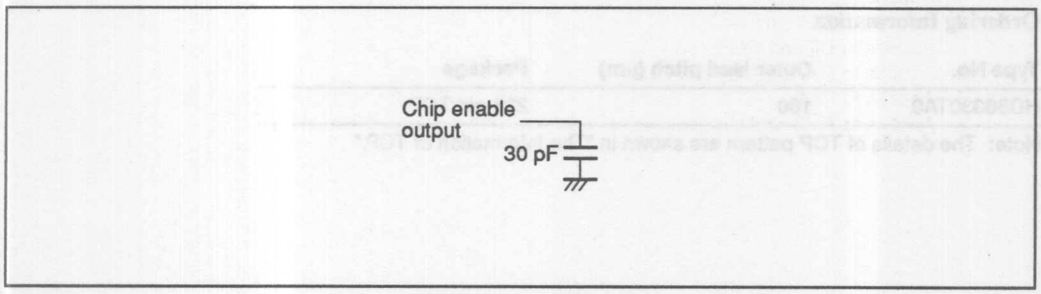


Figure 16 Test Load

HD66330T (TFT Driver)

(64-Level Gray Scale Driver for TFT Liquid Crystal Display)

— Preliminary —

Description

The HD66330T, a signal driver LSI, drives an active matrix LCD panel having TFTs (thin film transistor) in the picture element (pixel) area. The LSI receives 6-bit digital display data per dot and outputs corresponding gray scale voltage. This LSI easily achieves multicoloring of a VGA-sized color TFT LCD and is suitable for applications such as multimedia.

Features

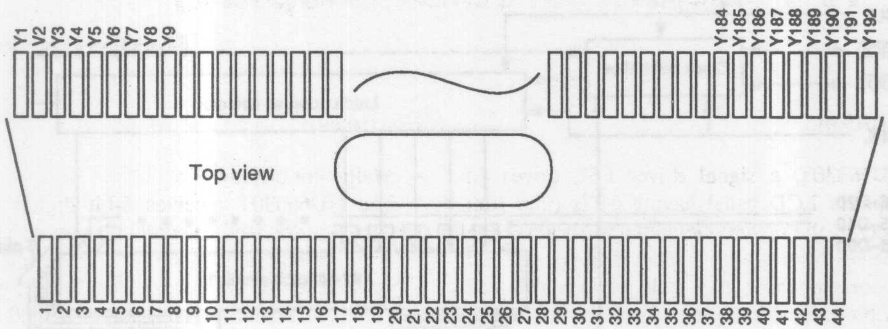
- Multicolor display
  The HD66330T receives 6-bit digital display data per dot, and selects and outputs an LCD drive voltage among 64-level gray scale voltages. When R, G, and B color filters are added to the LCD panel, a maximum of 260,000 colors can be displayed.
- High-speed operation
  Operating clock: 28 MHz maximum
  Amount of input data: 3 dots × 6 bits (gray scale data)
- Applicable systems
  PC (640 × 480/400 dots) systems
- Internal 192-bit drive function
- Internal standby function
- Internal chip-enable signal generation circuit
- Supply voltage: 4.5 V to 5.5 V
- Bidirectional shift

Ordering Information

Type No.	Outer lead pitch (μm)	Package
HD66330TA0	160	236-pin TCP

Note: The details of TCP pattern are shown in "The Information of TCP."

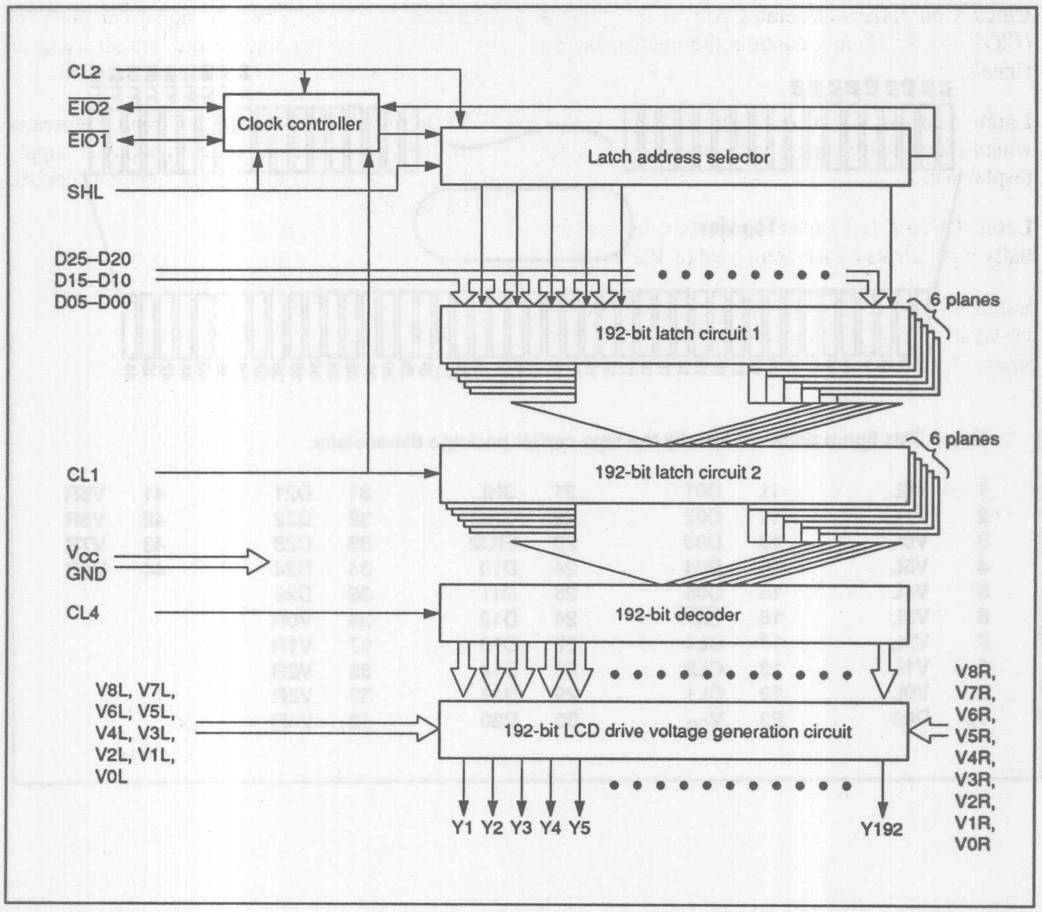
Pin Arrangement



Note: This figure does not specify the tape carrier package dimensions.

1	V8L	11	D01	21	SHL	31	D21	41	V5R
2	V7L	12	D02	22	GND	32	D22	42	V6R
3	V6L	13	D03	23	$\overline{EIO2}$	33	D23	43	V7R
4	V5L	14	D04	24	D10	34	D24	44	V8R
5	V4L	15	D05	25	D11	35	D25		
6	V3L	16	$\overline{EIO1}$	26	D12	36	V0R		
7	V2L	17	CL4	27	D13	37	V1R		
8	V1L	18	CL2	28	D14	38	V2R		
9	V0L	19	CL1	29	D15	39	V3R		
10	D00	20	V_{CC}	30	D20	40	V4R		

Internal Block Diagram



Block Functions

Clock Controller: Generates chip enable signals ($\overline{EIO2}$ and $\overline{EIO1}$) and controls the internal timing signals.

Latch Address Selector: Generates latch signals, which sequentially trigger latch operation of input display data.

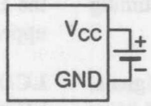
Latch Circuit 1: Latches 3-pixel × 6-bit sequentially input display data; composed of 192 × 6 bits.

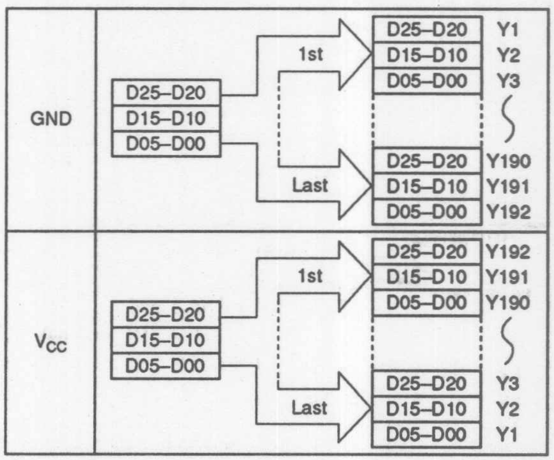
Latch Circuit 2: Latches 192 × 6-bit data latched in latch circuit 1 synchronously with the CL1 signal.

Decoder: Generates a decode signal per pixel for the LCD drive voltage generation circuit using an upper 3-bit decoder and a lower 3-bit decoder.

LCD Drive Voltage Generation Circuit: Generates LCD drive voltages from LCD drive power supply voltages according to the decode signals generated by the decoder.

Pin Functions

Signal Name	Numbers	I/O	Functions
V_{CC}	1	Power supply	 V_{CC}–GND: Supplies power to the LSI.
GND	1	Power supply	
V8L–V0L, V8R–V0R	18	Power supply	Supplies power to the LCD drive voltage generation circuit. The same voltage must be applied to corresponding L- and R-power pins within a range of V_{CC} to GND.
CL1	1	Input	Inputs display data latch pulses for latch circuit 2. At the rising edge of each CL1 pulse, latch circuit 2 latches display data input from latch circuit 1 and outputs LCD drive voltages corresponding to the latched data.
CL2	1	Input	Inputs display data latch pulses for latch circuit 1. At the falling edge of each CL2 pulse, latch circuit 1 latches display data input via D25–D00 and outputs the latched data to latch circuit 2.
D25–D20, D15–D10, D05–D00	18	Input	Inputs 6-bit (gray scale data) × 3-pixel display data.
SHL	1	Input	Selects the shift direction of the display data.



Signal Name	Numbers	I/O	Functions
CL4	1	Input	Controls the 2-phase function. A high level period of this signal specifies the first phase period that performs high output current operation, and a low level specifies the second phase period that outputs the voltage corresponding to the display data.

Pin Functions (cont)

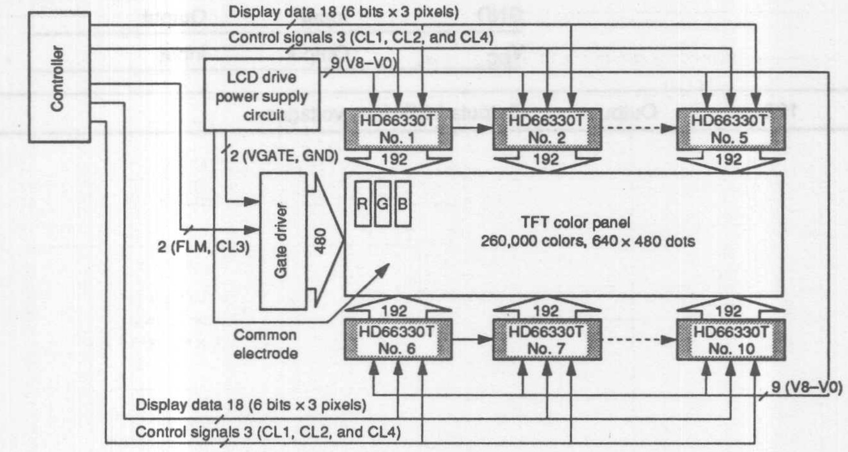
Signal Name	Numbers	I/O	Functions
EIO1, EIO2	2	Input/output	Provides chip-enable signals. Input or output depends on the SHL signal, as shown below. At any one time, the signal being used for input must go low to enable the LSI to latch display data, and the signal being used for output will be driven low after 192 pixels of display data have been read.
Y1–Y192	192	Output	Outputs LCD drive voltages.

SHL Level	EIO1	EIO2
GND	Input	Output
V_{CC}	Output	Input

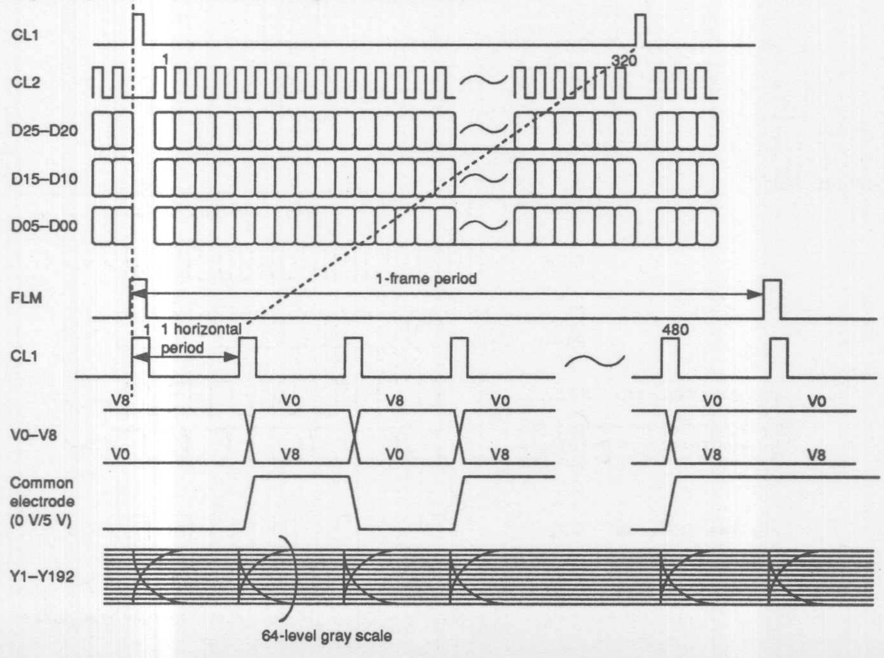
System Overview

The following shows a block diagram of a TFT color LCD system configured with multiple HD66330Ts. The HD66330Ts latch 6-bit data per dot, and selects and outputs one level among 64 internally generated LCD drive voltage levels. When the pixels are structured using R, G, and B color filters, a maximum of 260,000 colors can be displayed.

System block diagram

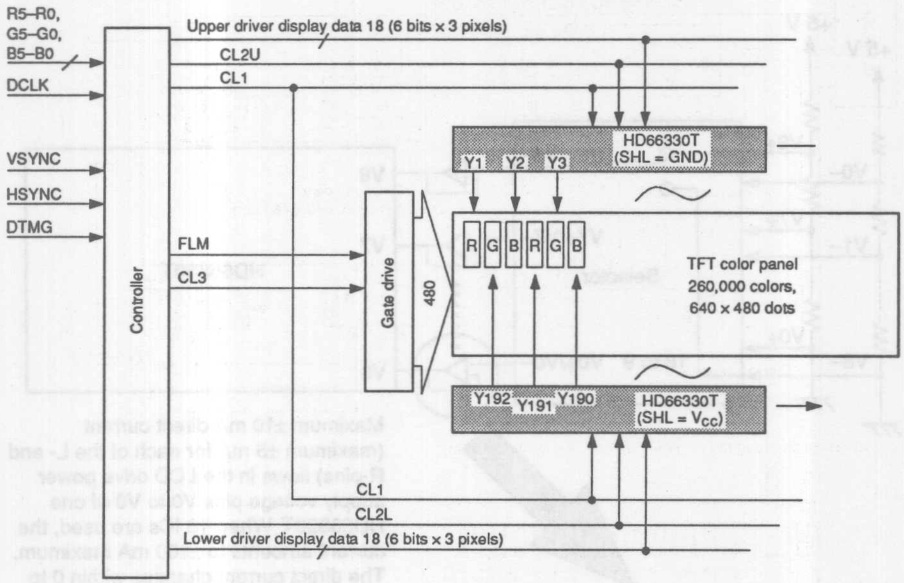


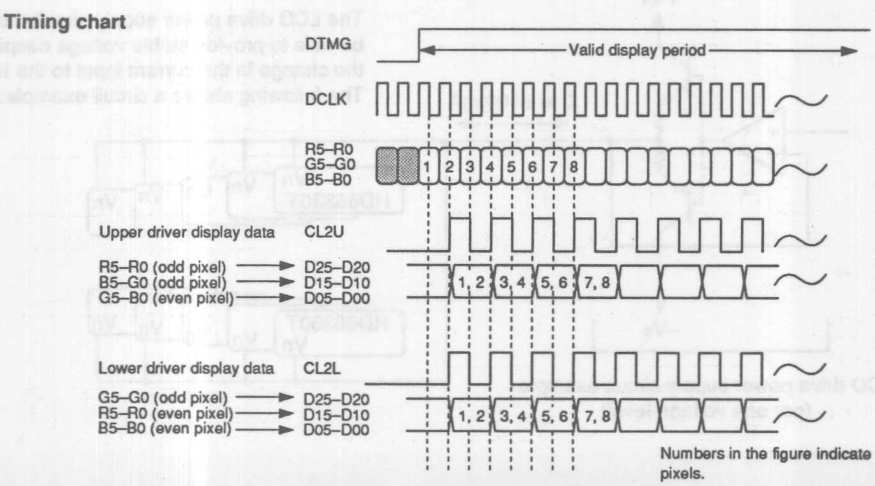
Timing chart (example of the common-voltage AC-drive method)



Timing Chart for Display Data

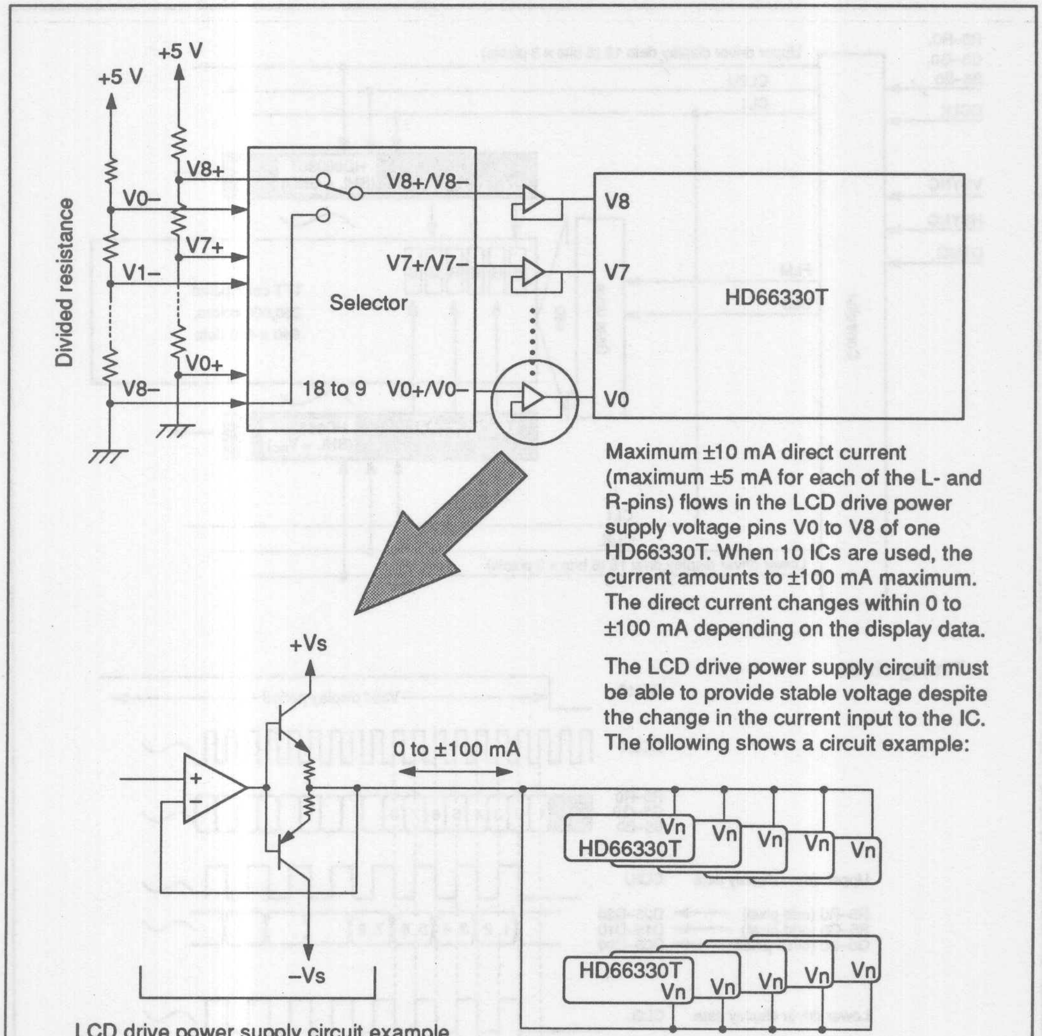
The following figures show the display data timing and hardware configuration for the TFT color LCD system configured with HD66330Ts. Since color panels usually have a narrow connection pitch with driver LSIs, the HD66330Ts should be located above (upper drivers) and below (lower drivers) the panel and alternately connected to the panel pins. In such a configuration, the RGB data and the system dot clock (DCLK) should be divided between the upper and lower drivers. Here, DCLK should be divided into two by the controller.





Power Supply Circuit Example

The figures below show an example of a circuit used to generate LCD drive power supply voltages V0 to V8. In this example, 18 levels of voltage are generated by divided resistance to alternate the current for the LCD panel, and either positive or negative voltages are selected and supplied to the HD66330T. To stabilize voltage, an operational amplifier should be connected to each selector output.



LCD drive power supply circuit example
(per one voltage level)

Power Supply Voltage Examples

Voltage levels to be input to LCD drive power supply pins V0 to V8 should be determined according to panel specifications such as voltage intensity characteristics. The table below lists voltage level examples for reference:

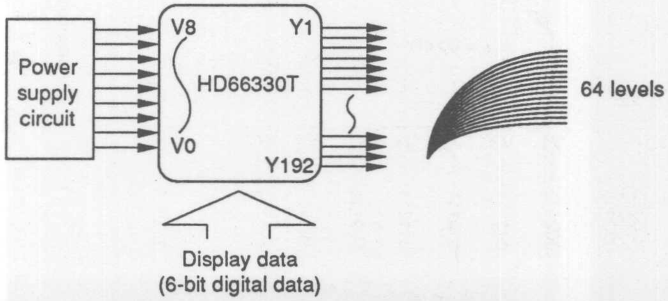
	V0	V1	V2	V3	V4	V5	V6	V7	V8	Counter Electrode
Voltage (V)	0	1.0	1.5	2.0	2.5	3.0	3.5	4.0	5.0	0
	5.0	4.0	3.5	3.0	2.5	2.0	1.5	1.0	0	5.0

Relationship between Display Data and Output Voltage

The HD66330T outputs 64-level gray scale voltage generated by 9 levels of LCD drive power supply voltage and 6-bit digital data. The figure below shows the relationship among the input voltages from the LCD drive power supply circuit, digital codes, and output voltages.

Display Data						Output Voltage		Display Data						Output Voltage	
DI5	DI4	DI3	DI2	DI1	DI0	1st Phase	2nd Phase	DI5	DI4	DI3	DI2	DI1	DI0	1st Phase	2nd Phase
0	0	0	0	0	0	V1	V0 + 1/8 × (V1–V0)	1	0	0	0	0	0	V5	V4 + 1/8 × (V5–V4)
0	0	0	0	0	1	V1	V0 + 2/8 × (V1–V0)	1	0	0	0	0	1	V5	V4 + 2/8 × (V5–V4)
0	0	0	0	1	0	V1	V0 + 3/8 × (V1–V0)	1	0	0	0	1	0	V5	V4 + 3/8 × (V5–V4)
0	0	0	0	1	1	V1	V0 + 4/8 × (V1–V0)	1	0	0	0	1	1	V5	V4 + 4/8 × (V5–V4)
0	0	0	1	0	0	V1	V0 + 5/8 × (V1–V0)	1	0	0	1	0	0	V5	V4 + 5/8 × (V5–V4)
0	0	0	1	0	1	V1	V0 + 6/8 × (V1–V0)	1	0	0	1	0	1	V5	V4 + 6/8 × (V5–V4)
0	0	0	1	1	0	V1	V0 + 7/8 × (V1–V0)	1	0	0	1	1	0	V5	V4 + 7/8 × (V5–V4)
0	0	0	1	1	1	V1	V1	1	0	0	1	1	1	V5	V5
0	0	1	0	0	0	V2	V1 + 1/8 × (V2–V1)	1	0	1	0	0	0	V6	V5 + 1/8 × (V6–V5)
0	0	1	0	0	1	V2	V1 + 2/8 × (V2–V1)	1	0	1	0	0	1	V6	V5 + 2/8 × (V6–V5)
0	0	1	0	1	0	V2	V1 + 3/8 × (V2–V1)	1	0	1	0	1	0	V6	V5 + 3/8 × (V6–V5)
0	0	1	0	1	1	V2	V1 + 4/8 × (V2–V1)	1	0	1	0	1	1	V6	V5 + 4/8 × (V6–V5)
0	0	1	1	0	0	V2	V1 + 5/8 × (V2–V1)	1	0	1	1	0	0	V6	V5 + 5/8 × (V6–V5)
0	0	1	1	0	1	V2	V1 + 6/8 × (V2–V1)	1	0	1	1	0	1	V6	V5 + 6/8 × (V6–V5)
0	0	1	1	1	0	V2	V1 + 7/8 × (V2–V1)	1	0	1	1	1	0	V6	V5 + 7/8 × (V6–V5)
0	0	1	1	1	1	V2	V2	1	0	1	1	1	1	V6	V6
0	1	0	0	0	0	V3	V2 + 1/8 × (V3–V2)	1	1	0	0	0	0	V7	V6 + 1/8 × (V7–V6)
0	1	0	0	0	1	V3	V2 + 2/8 × (V3–V2)	1	1	0	0	0	1	V7	V6 + 2/8 × (V7–V6)
0	1	0	0	1	0	V3	V2 + 3/8 × (V3–V2)	1	1	0	0	1	0	V7	V6 + 3/8 × (V7–V6)
0	1	0	0	1	1	V3	V2 + 4/8 × (V3–V2)	1	1	0	0	1	1	V7	V6 + 4/8 × (V7–V6)
0	1	0	1	0	0	V3	V2 + 5/8 × (V3–V2)	1	1	0	1	0	0	V7	V6 + 5/8 × (V7–V6)
0	1	0	1	0	1	V3	V2 + 6/8 × (V3–V2)	1	1	0	1	0	1	V7	V6 + 6/8 × (V7–V6)
0	1	0	1	1	0	V3	V2 + 7/8 × (V3–V2)	1	1	0	1	1	0	V7	V6 + 7/8 × (V7–V6)
0	1	0	1	1	1	V3	V3	1	1	0	1	1	1	V7	V7
0	1	1	0	0	0	V4	V3 + 1/8 × (V4–V3)	1	1	1	0	0	0	V8	V7 + 1/8 × (V8–V7)
0	1	1	0	0	1	V4	V3 + 2/8 × (V4–V3)	1	1	1	0	0	1	V8	V7 + 2/8 × (V8–V7)
0	1	1	0	1	0	V4	V3 + 3/8 × (V4–V3)	1	1	1	0	1	0	V8	V7 + 3/8 × (V8–V7)
0	1	1	0	1	1	V4	V3 + 4/8 × (V4–V3)	1	1	1	0	1	1	V8	V7 + 4/8 × (V8–V7)
0	1	1	1	0	0	V4	V3 + 5/8 × (V4–V3)	1	1	1	1	0	0	V8	V7 + 5/8 × (V8–V7)
0	1	1	1	0	1	V4	V3 + 6/8 × (V4–V3)	1	1	1	1	0	1	V8	V7 + 6/8 × (V8–V7)
0	1	1	1	1	0	V4	V3 + 7/8 × (V4–V3)	1	1	1	1	1	0	V8	V7 + 7/8 × (V8–V7)
0	1	1	1	1	1	V4	V4	1	1	1	1	1	1	V8	V8

Note: 1st phase: The period in which 2-phase control signal CL4 is high and high output current operation is performed.
2nd phase: The period in which 2-phase control signal CL4 is low and low output current operation is performed (see p. 1199 for details).



Output Offset Voltage

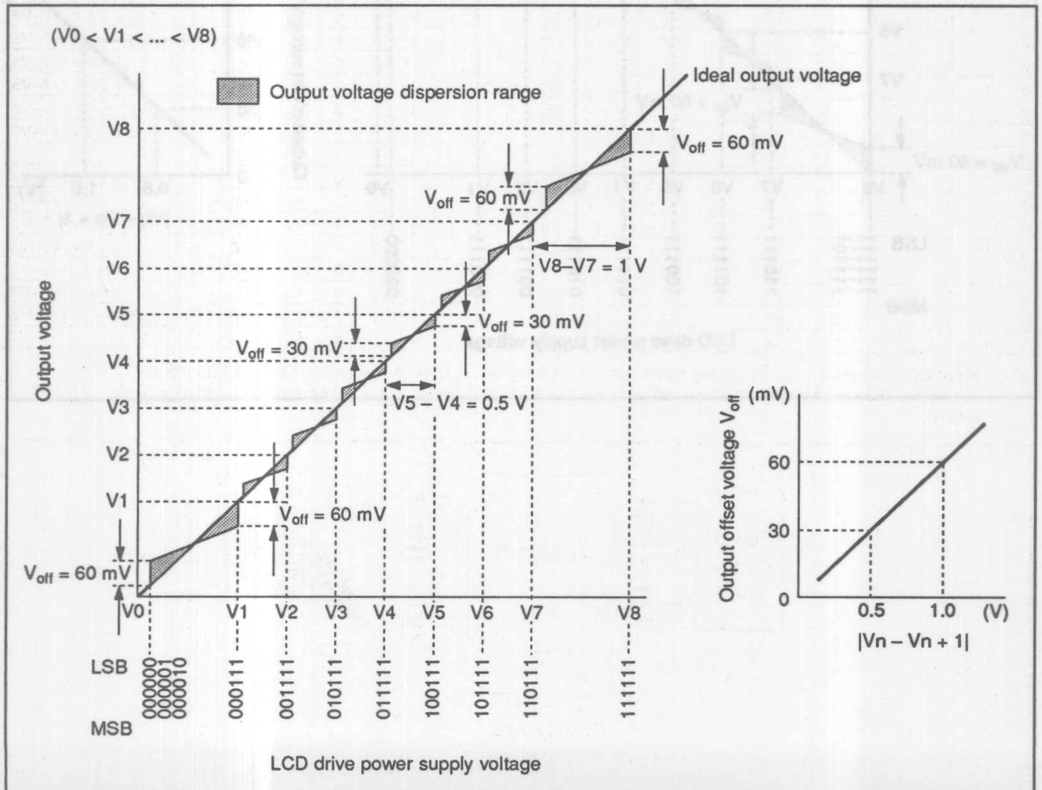
The HD66330T has an internal DA converter per output. The upper three bits of 6-bit display data select and apply the LCD drive power supply voltage level to the DA converter, and the lower three bits select and output one analog voltage level.

Output offset voltage V_{off} is defined as the difference between the actual output voltage and the ideal output voltage expected from the LCD drive power supply voltage and digital display data. The V_{off} can be considered as the total output voltage differences including the differences between LSIs, between different output pins of the same LSI, and that caused by concentrated current in a LSI due to a particular display pattern.

The figure below shows the characteristics of output voltage with respect to LCD drive power supply voltages. Since output offset voltage V_{off} depends on the difference between adjoining LCD drive power supply voltages $|Vn - Vn + 1|$ (n = 0 to 7) output offset voltage will also decrease when the power supply voltage difference $|Vn - Vn + 1|$ is decreased.

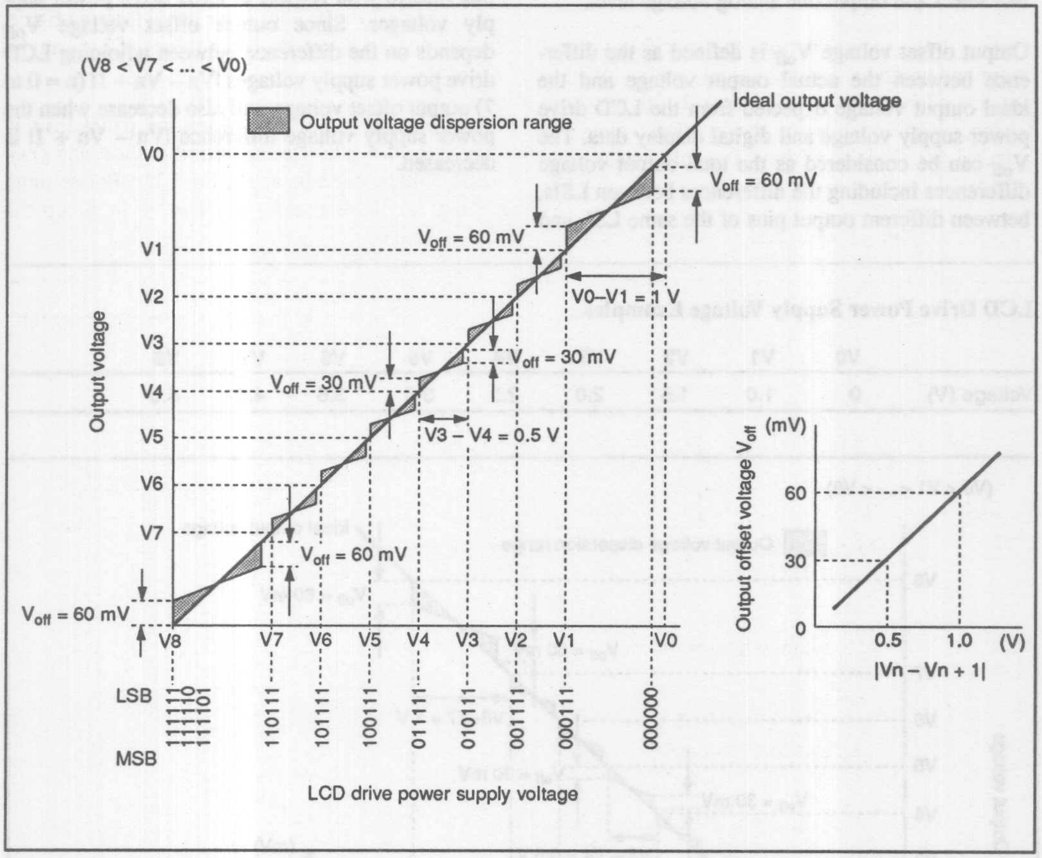
LCD Drive Power Supply Voltage Examples

	V0	V1	V2	V3	V4	V5	V6	V7	V8
Voltage (V)	0	1.0	1.5	2.0	2.5	3.0	3.5	4.0	5.0



LCD Drive Power Supply Voltage Examples

	V8	V7	V6	V5	V4	V3	V2	V1	V0
Voltage (V)	0	1.0	1.5	2.0	2.5	3.0	3.5	4.0	5.0



2-Phase Operation

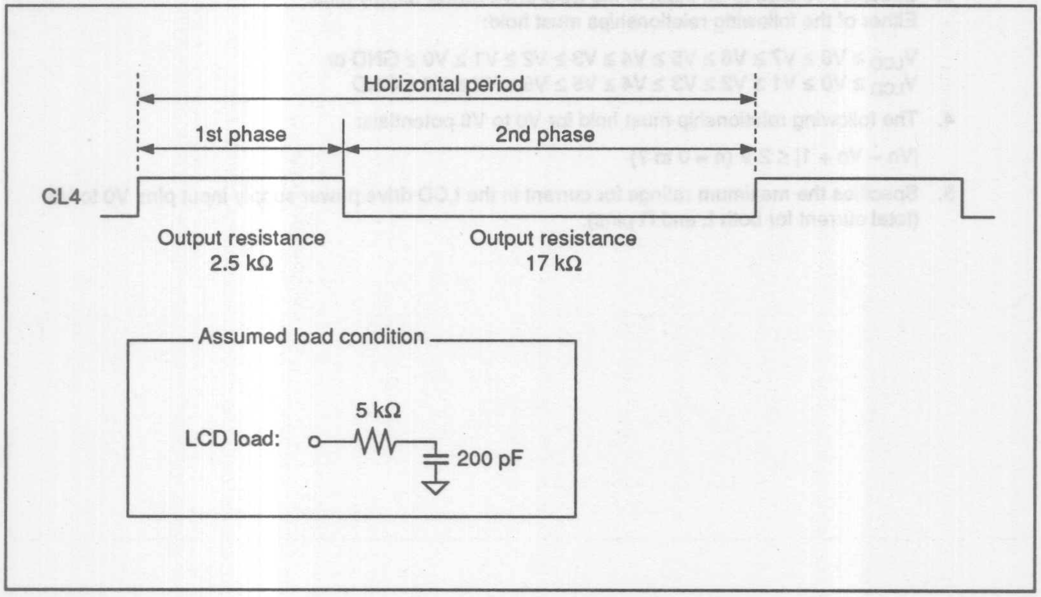
A high-speed low-power output switching function is provided by dividing the horizontal period into 1st-and 2nd-phase periods, where high output current operation and low output current operation are alternately performed.

During the 1st-phase period, the specified voltage is applied to the LCD panel quickly with a low output impedance of about 215 kΩ (high output current operation). Here, the applied voltage is selected by the upper three bits of display data (see p. 1196).

During the 2nd-phase period, a voltage is applied corresponding to the display data with an output impedance of about 17 kΩ (low output current operation).

In general, since it is not required to secure the 1st phase in a 640 × 480-dot color panel (see the figure below for assumed load condition), CL4 can be fixed low.

This function is effective when the panel load is large or when a horizontal period is short and gray scale voltage must be applied quickly. For settings in the 1st-phase period, see note 4 in Electrical Characteristics.



Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage	V_{CC}	–0.3 to +7.0	V	1
Input voltage (1)	V_{t1}	–0.3 to $+V_{CC}$ + 0.3	V	1, 2
Input voltage (2)	V_{t2}	–0.3 to $+V_{CC}$ + 0.3	V	1, 3, 4
LCD power supply input current	I_t	±20	mA	5
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

If the LSI is used beyond the above maximum ratings, it may be permanently damaged. It should always be used within its specified operating range for normal operation to prevent malfunction or degraded reliability.

Notes: 1. Assuming GND = 0 V.

2. Applies to input pins CL1, CL2, CL4, SHL, and Dij, and I/O pins $\overline{\text{EIO1}}$ and $\overline{\text{EIO2}}$ when used as input.
3. Specifies voltage to be input to the LCD drive power supply pins.
   Either of the following relationships must hold:

   $V_{LCD} \geq V8 \geq V7 \geq V6 \geq V5 \geq V4 \geq V3 \geq V2 \geq V1 \geq V0 \geq GND$ or
   $V_{LCD} \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V6 \geq V7 \geq V8 \geq GND$
4. The following relationship must hold for V0 to V8 potentials:

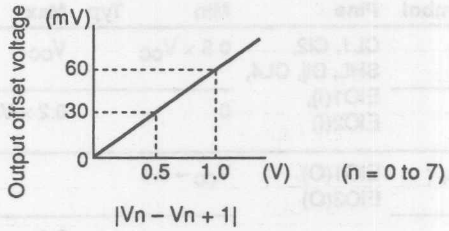
   $|Vn - Vn + 1| \leq 2$ V (n = 0 to 7)
5. Specifies the maximum ratings for current in the LCD drive power supply input pins V0 to V8 (total current for both L and R pins).

Electrical Characteristics

DC Characteristics (V_{CC} – GND = 4.5 to 5.5 V, and T_a = 20 to 75°C, unless otherwise noted)

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Conditions	Notes
Input high-level voltage	V_{IH}	CL1, Cl2, SHL, Dij, CL4, EIO1(I), EIO2(I)	0.8 × V_{CC}		V_{CC}	V		
Input low-level voltage	V_{IL}		0		0.2 × V_{CC}	V		
Output high-level voltage	V_{OH}	EIO1(O), EIO2(O)	V_{CC} – 0.4			V	I_{OH} = –0.4 mA	
Output low-level voltage	V_{OL}				0.4	V	I_{OL} = 0.4 mA	
Input leakage current (1)	I_{L1}	CL1, Cl2, SHL, Dij, CL4	–5		+5	μA		
Input leakage current (2)	I_{L2}	EIO1(I), EIO2(I)	–10		+10	μA		
LCD drive power supply input current	I_t	V0L–V8L, V0R–V8R	–10		+10	mA	Total of L and R pins |Vn – Vn + 1| = 1 V (n = 0 to 7)	
Output offset voltage	V_{off}	Y1–Y192	—		60	mV	V_{CC} – GND = 5 V |Vn – Vn + 1| = 1 V (n = 0 to 7)	1
			—		30	mV	V_{CC} – GND = 5 V |Vn – Vn + 1| = 0.5 V (n = 0 to 7)	
Difference between output pins	V_{ref}	Y1–Y192	—		±30	mV	V_{CC} – GND = 5 V |Vn – Vn + 1| = 1 V (n = 0 to 7)	2
			—		±15	mV	V_{CC} – GND = 5 V |Vn – Vn + 1| = 0.5 V (n = 0 to 7)	
Driver output ON resistance	R_{on1}	Y1–Y192	—		2.5	kΩ	1st phase V_{CC} – GND = 5 V	
	R_{on2}	Y1–Y192	—		17	kΩ	2nd phase V_{CC} – GND = 5 V	
Current consumption (1)	I_{p1}	Between V_{CC} and GND	—		20	mA	Data latch f_{CL2} = 15 MHz, f_{CL1} = 33 kHz	3
Current consumption (2)	I_{p2}	Between V_{CC} and GND	—		4	mA	Standby f_{CL2} = 15 MHz, f_{CL1} = 33 kHz	

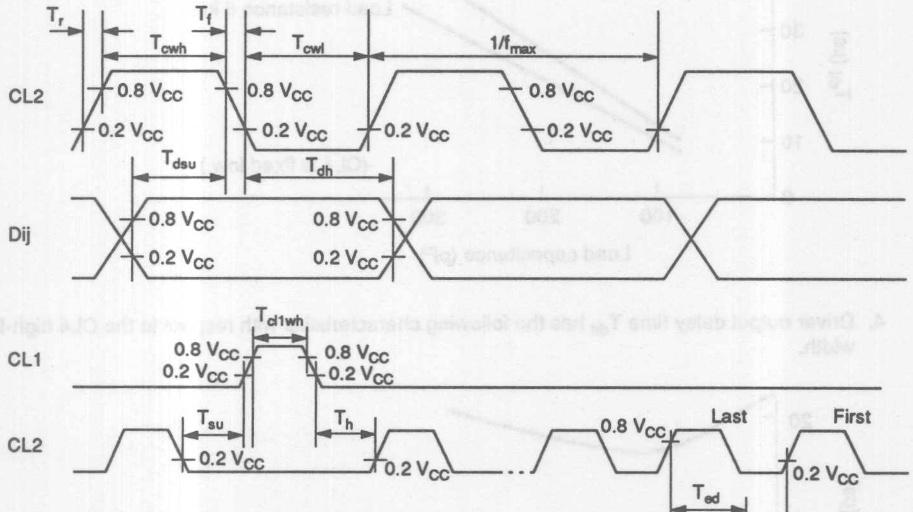
Notes: 1. Output offset voltage V_{off} is defined as difference between the actual output voltage and output voltage expected from the LCD drive power supply voltage and digital display data.
V_{off} shows the following characteristics with respect to voltage difference between adjoining LCD drive power supply pins $|Vn - Vn + 1|$.

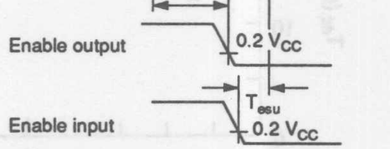


2. V_{ref} can be considered as the maximum total output voltage differences including the differences between LSIs, between output pins of the same LSI, and that caused by concentrated current in an LSI due to a particular display pattern.
3. Except for the current flowing in V0 to V8; outputs are unloaded.

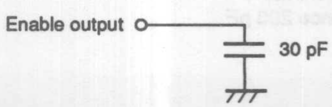
AC Characteristics (V_{CC} – GND = 4.5 to 5.5 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Applicable Pin	Min	Typ	Max	Unit	Test Condition	Notes
Clock cycle time	f_{max}	CL2			28	MHz		
Clock high-level width	T_{cwh}	CL2	10			ns		
Clock high-level width	T_{cwl}	CL2	10			ns		
Clock rise time	T_r	CL1, CL2			6	ns		
Clock fall time	T_f	CL1, CL2			6	ns		
Clock setup time	T_{su}	CL1, CL2	50			ns		
Clock hold time	T_h	CL1, CL2	70			ns		
Data setup time	T_{dsu}	Dij, CL2	10			ns		
Data hold time	T_{dh}	Dij, CL2	10			ns		
Enable setup time	T_{esu}	EIO1, EIO2, CL2	7			ns		
Enable output delay time	T_{ed}	EIO1, EIO2, CL2			20	ns		1
CL1 high-level width	T_{cl1wh}	CL1	56			ns		
Driver output delay time	T_{dd}	CL1, Y1–Y192			22	µs		2, 3, 4

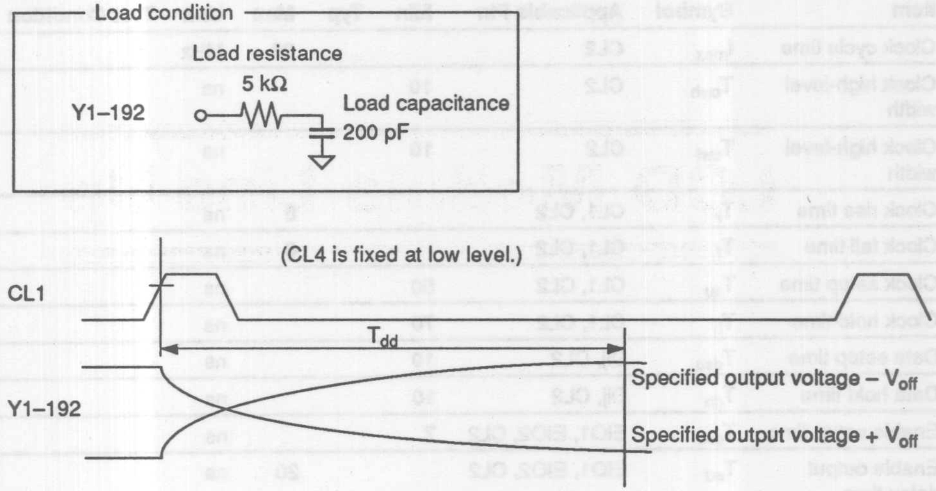




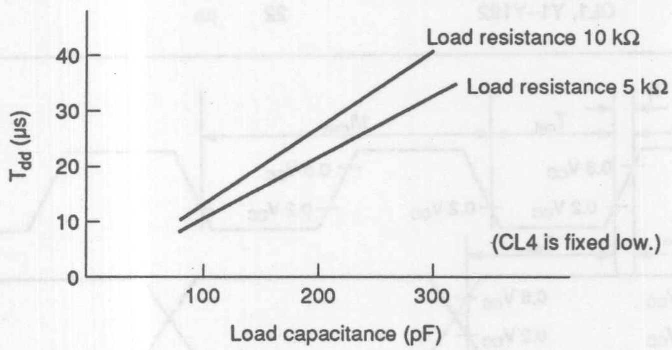
Notes: 1. The figure below shows the load condition for the enable output pins.



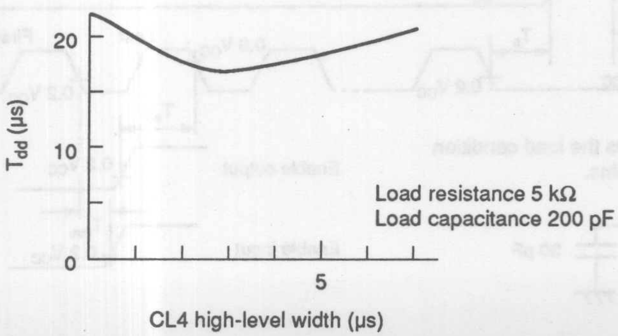
2. Specified by the following load condition and timing.



3. Driver output delay time T_{dd} has the following characteristics with respect to the load condition.

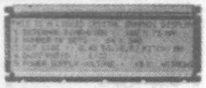


4. Driver output delay time T_{dd} has the following characteristics with respect to the CL4 high-level width.

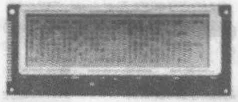


LCD Module Line Up

Graphic Display LCD Module

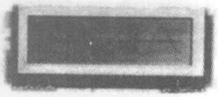


●LM258XB

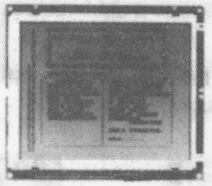


●LM213XB

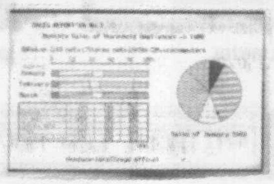
●LM721XBNP



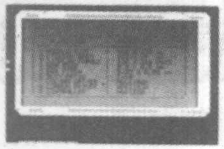
●LMG6390QHGR



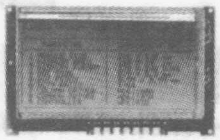
●LM246X



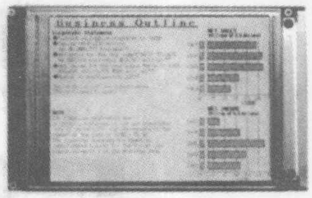
●LMG6471XTFC



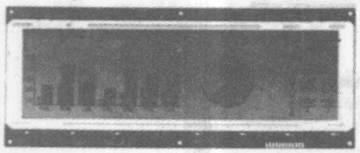
●LM238XB



●LMG6400PLGR

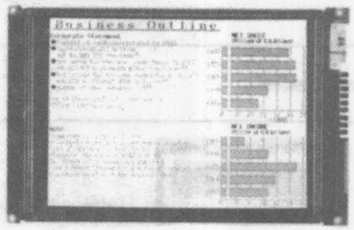


●LMG5040XUFC

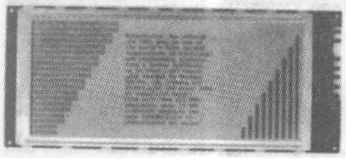


●LM215XB

●LM266XW

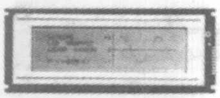


●LMG6151XUFE



●LMG6281XNGE

●LMG9040ZZFC



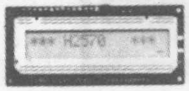
●LM300XM

LCD Module Line Up

Character Display LCD Module

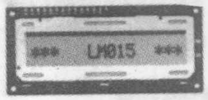
1-line Series

●LM054

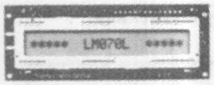


●H2570

●LM020L

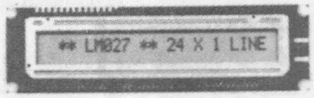


●LM015

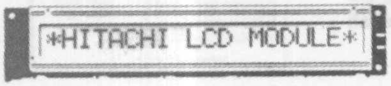


●LM070L

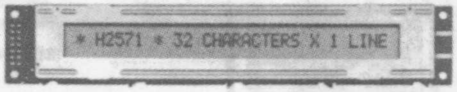
●LM568F



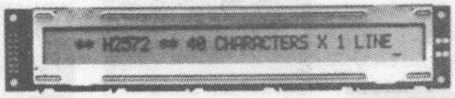
●LM027



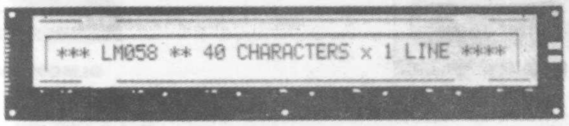
●LM038



●H2571

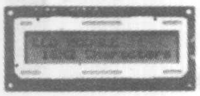


●H2572



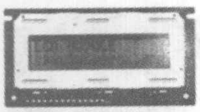
●LM058

2-line Series

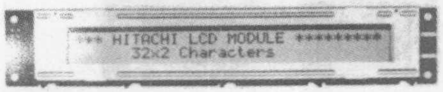


●LM052L

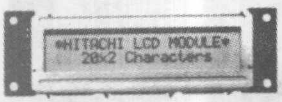
●LM107XML



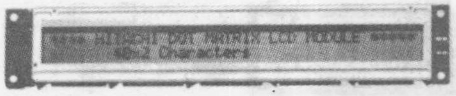
●LM016L, LM016XML



●LM017L

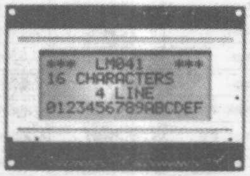


●LM032L, LM032XML

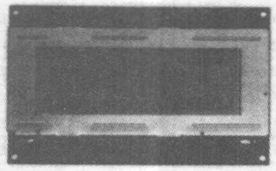


●LM018L

4-line Series

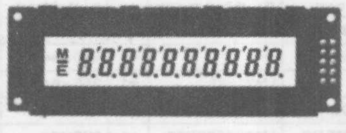


●LM041L



●LM044L

Segment-type LCD module



●LM039

LED with backlight

●LM087LN

●LM091LN

●LM086ALN

●LM092LN

●LM093LN

LCD Module Line Up

Graphic Display LCD Module (Reflection type)

Type		Controller(Note)	Screen Size	Color	Module size	Effective Screen Size	Dot Pitch	Duty
External type	On-thip type		w×h (dots)		w×h×t (mm)	w×h (mm)	w×h (mm)	Cycle
LM258XB	–	*1	240×64	Yellow-green	149×57×13max.	117×41	0.47×0.47	1/64
LM300XM	–	*1	240×64	New gray	180×75×11max.	132×39	0.53×0.53	1/32
–	LM213XB	*1	256×64	Yellow-green	184×75×10max.	149.6×43	0.56×0.56	1/64
LMG6390QHGR	LMG6380QHGR	*1	256×64	New gray	160×68×9.5max. *4	126.3×37	0.47×0.47	1/64
LMG6392QHFR	LMG6382QHFR	*1	256×64	Black & White	160×68×9.5max. *4	126.3×37	0.47×0.47	1/64
LM221XB	LM238XB	*1	240×128	Yellow-green	180×120×13.8max.	148×75	0.55×0.55	1/64
LMG6410PLGR	LMG6400PLGR	*1	240×128	New gray	159.4×101×9.5max. *4	126×71	0.50×0.50	1/128
LMG6412PLFR	LMG6402PLFR	*1	240×128	Black & White	159.4×101×9.5max. *4	126×71	0.50×0.50	1/128
LM246X	–	*2	320×256	Yellow-green	168×150×13.5max.	142×115	0.43×0.43	1/128
LM211XB	–	*1	480×64	New gray	270×82×13max.	240×38	0.49×0.49	1/64
LM211XMC	–	*1	480×64	New gray	270×82×13max.	240×38	0.49×0.49	1/64
LM215XB	–	*1	480×128	Yellow-green	270×110×11.5max.	242×69	0.48×0.48	1/64
LMG6250ULGR	–	*3	480×128	New gray	270×110×11.5max.	242×69	0.48×0.48	1/128
LMG6252ULFR	–	*3	480×128	Black & White	270×110×11.5max.	242×69	0.48×0.48	1/128
LM266XW	–	*2	640×100	New gray	287.5×71.5×11.5max.	243×42	0.36×0.36	1/100
LM280X	–	*3	640×200	Yellow-green	270×104×11max.	236.4×78	0.36×0.36	1/200
LMG6270XNGR	–	*3	640×200	New gray	265×90×8max.	221.2×73	0.33×0.33	1/200
LMG6272XNFR	–	*3	640×200	Black & White	265×90×8max.	221.2×73	0.33×0.33	1/200
LMG6273XNFR	–	*3	640×200	Black & White anti-glare	265×90×8max.	221.2×73	0.33×0.33	1/200
LMG6280XNGR	–	*3	640×200	New gray	270×116×8max.	217.2×96	0.33×0.45	1/200
LMG6282XNFR	–	*3	640×200	Black & White	270×116×8max.	217.2×96	0.33×0.45	1/200
LMG6283XNFR	–	*3	640×200	Black & White anti-glare	270×116×8max.	217.2×96	0.33×0.45	1/200
LMG6111XTFR	–	*3	640×400	Black & White anti-glare	288×173×7.5max.	223.17×143.97	0.33×0.33	1/200
LMG6150XUFR	–	*3	640×480	Black & White anti-glare	272×178×9max.	202.37×152.77	0.31×0.31	1/240

Graphic Display LCD Module (with EL backlight)

LMG6391QHGE	LMG6381QHGE	*1	256×64	New gray	160×68×9.5max. *4	126.3×37	0.47×0.47	1/64
LMG6411PLGE	LMG6401PLGE	*1	240×128	New gray	159.4×101×9.5max. *4	126×71	0.50×0.50	1/128
LMG6251ULGE	–	*3	480×128	New gray	270×110×11.5max.	242×69	0.48×0.48	1/128
LMG6271XNGE	–	*3	640×200	New gray	265×90×9max.	221.2×73	0.33×0.33	1/200
LMG6281XNGE	–	*3	640×200	New gray	270×116×9max.	217.2×96	0.33×0.45	1/200
LMG6171XTBE	–	*3	640×400	Blue anti-glare	256×146×9max.	197×125	0.30×0.30	1/200
LMG6173XTFE	–	*3	640×400	Black & White anti-glare	256×146×9max.	197×125	0.30×0.30	1/200
LMG6151XUFE	–	*3	640×480	Black & White anti-glare	272×178×9max.	202.37×152	0.31×0.31	1/240
LMG6221XUFE	–	*3	640×480	Black & White anti-glare	260×160×9max.	183×138.4	0.28×0.28	1/240

Graphic Display LCD Module (with CFL backlight)

LM721XBNP	–	*3	320×200	Yellow	142×103×30max.	113×77	0.33×0.35	1/200
LMG6160XTFC	–	*3	640×400	Black & White anti-glare	325×191.6×26max.	236×152	0.36×0.36	1/200
LMG6371XTBC	–	*3	640×400	Blue anti-glare	250×145×10.6max.	196×124	0.30×0.30	1/200
LMG6471XTFC	–	*3	640×400	Black & White anti-glare	250×145×10.6max.	196×124	0.30×0.30	1/200
LMG5040XUFC	–	*3	640×480	Black & White anti-glare	256.5×160×10max.	183×137	0.28×0.28	1/242
LMG5060XUFC	–	*3	640×480	Black & White anti-glare	250×172×10.5max.	196×150	0.30×0.30	1/240
LMG9050ZZFC	–	–	1024×768	Black & White anti-glare	300×234×17max.	231×175	0.22×0.22	1/387
LMG9040ZZFC	–	–	1120×780	Black & White anti-glare	316×230×31max.	236×166	0.205×0.205	1/390

Recommended Voltage (Note)								
V_{DD}-V_{SS} (V)	V_{EE}-V_{SS} (V)	Power Consumption	Operating Temperature	Storage Temperature	Weight	Power Supply	Driver (on-chip)	Type
+5	−12	66	0~+40	−20~+60	120	2 Double	LC7940 /7941/7942	LM258XB
+5	−9	33	0~+40	−20~+60	150	2 Double	LC7940 /7941/7942	LM300XM
+5	−10.5	250	0~+40	−20~+60	150	2 Double	MSM5839/5238	LM213XB
+5	−13	90	0~+40	−20~+60	160	2 Double	LC7940/7941/7942	LMG6390QHGR
+5	−13	90	0~+40	−20~+60	160	2 Double	LC7940/7941/7942	LMG6392QHFR
+5	−13.5	210	0~+40	−20~+60	220	2 Double	HD61200/61203	LM238XB
+5	−15	90	0~+40	−20~+60	160	2 Double	LC7940/7942	LMG6410PLGR
+5	−15	90	0~+40	−20~+60	160	2 Double	LC7940/7942	LMG6412PLFR
+5	−20	76	0~+40	−20~+60	265	2 Double	HD61104/61105	LM246X
+5	−10.5	130	0~+40	−20~+60	180	2 Double	MSM5839/5238	LM211XB
+5	−13	90	0~+40	−20~+60	210	2 Double	LC7940/7942	LM211XMC
+5	−13.5	100	0~+40	−20~+60	320.	2 Double	HD61100/61103	LM2115XB
+5	−13	100	0~+40	−20~+60	320	2 Double	LC7940/7942	LMG6250ULGR
+5	−13	100	0~+40	−20~+60	320	2 Double	LC7940/7942	LMG6252ULFR
+5	−19	154	0~+50	−20~+60	200	2 Double	HD61104/61105	LM266XW
+5	−20.5	180	0~+40	−20~+60	290	2 Double	MSM5298/5299	LM280X
+5	−22	115	0~+40	−20~+60	230	2 Double	MSM5298/5299	LMG6270XNGR
+5	−22	115	0~+40	−20~+60	230	2 Double	MSM5298/5299	LMG6272XNFR
+5	−22	115	0~+40	−20~+60	230	2 Double	MSM5298/5299	LMG6273XNFR
+5	−22	115	0~+40	−20~+60	275	2 Double	MSM5298/5299	LMG6280XNGR
+5	−22	115	0~+40	−20~+60	275	2 Double	MSM5298/5299	LMG6282XNFR
+5	−22	115	0~+40	−20~+60	275	2 Double	MSM5298/5299	LMG6283XNFR
+5	−20.5	200	0~+40	−20~+60	420	2 Double	MSM5298/5299	LMG6111XTFR
+5	−21.5	200	0~+40	−20~+60	420	2 Double	MSM5298/5299	LMG6150XUFR
+5	−13	90 1000 *5	0~+40	−20~+60	190	2 Double	LC7940/7942	LMG6391QHGE
+5	−15	90 1000 *5	0~+40	−20~+60	200	2 Double	LC7940/7942	LMG6411PLGE
+5	−13	100 1500 *5	0~+40	−20~+60	380	2 Double	LC7940/7942	LMG6251ULGE
+5	−22	115 1500 *5	0~+40	−20~+60	280	2 Double	MSM5298/5299	LMG6271XNGE
+5	−22	115 1500 *5	0~+40	−20~+60	340	2 Double	MSM5298/5299	LMG6281XNGE
+5	−22	200 2000 *5	0~+40	−20~+60	360	2 Double	MSM5298/5299	LMG6171XTBE
+5	−22	360 2000 *5	0~+40	−20~+60	350	2 Double	MSM5298/5299	LMG6173XTFE
+5	−22	200 2000 *5	0~+40	−20~+60	480	2 Double	MSM5298/5299	LMG6151XUFE
+5	−22	400 2000 *5	0~+40	−20~+60	450	2 Double	MSM5298/5299	LMG6221XUFE
+5	−21.5	230 1000 *6	0~+40	−20~+60	340	2 Double	MSM5298/5299	LM721XBNP
+5	−20.5	360 6000 *6	+10~+40	−20~+60	950	2 Double	MSM5298/5299	LMG6160XTFC
+5	−22	360 2000 *6	+10~+40	−20~+60	400	2 Double	MSM5298/5299	LMG6371XTBC
+5	−22	360 2000 *6	+10~+40	−20~+60	400	2 Double	MSM5298/5299	LMG6471XTFC
+5	−22	400 1800 *6	+5~−40	−10~+60	430	2 Double	MSM5298/5299	LMG5040XUFC
+5	−20.5	360 2500 *6	+10~+40	−20~+60	460	2 Double	MSM5298/5299	LMG5060XUFC
+5	+34	1700 6000 *6	+5~+40	−10~+60	1100	2 Double	HD66107T	LMG9050ZZFC
+5	+38 (+12) *7	1700 6000	+5~+40	−10~+60	1400	3 Double	HD66107T	LMG9040ZZFC

Note: Contoller LSI *1: HD61830 *2: HD63645F/64645F *3: HD66841 *4: External-type contoller maximum thickness is 9.0 mm.
*5: EL power consumption *6: CFL power consumption *7: $V_{FC}-V_{SS}$

LCD Module Line Up

Character Display LCD Module

Type	Screen Size (Char. × Line)	Color	Module Size w×h×t (mm)	Effective Screen Size w×h (mm)	Character Dimensions w×h (mm)	Duty Cycle	Recommended Voltage V_{DD}-V_{SS} (V)
LM054	8×1	Gray	88×44×12max.	61×15.8	6.45×9.4	1/8	+5
LM015	16×1	Gray	80×36×12max.	64.5×13.8	3.15×5.5	1/8	+5
H2570	16×1	Gray	80×36×12max.	64.5×13.8	3.15×7.9	1/11	+5
LM020L	16×1	Gray	80×36×12max.	64.5×13.8	3.07×5.73	1/16	+5
LM020XMBL	16×1	New gray	80×36×12max.	64.5×13.8	3.07×5.73	1/16	+5
LM070L	20×1	Gray	105×39.0×11max.	84.0×13.0	3.2×5.2	1/8	+5
LM038	20×1	Gray	182×35.5×13max.	154.0×15.3	6.7×9.4	1/8	+5
LM027	24×1	Gray	126×36×12max.	100×13.8	3.15×7.9	1/11	+5
H2571	32×1	Gray	174.5×33×13.4max.	132.5×14	3.15×7.9	1/11	+5
H2572	40×1	Gray	182×35.5×13max.	154.0×15.3	3.15×7.9	1/11	+5
LM058	40×1	Gray	290×60×13max.	245×19	4.82×8.18	1/8	+5
LM052L	16×2	Gray	80×36×11max.	64.5×13.8	2.95×3.8	1/16	+5
LM016L	16×2	Gray	84×44×12max.	61×15.8	2.96×4.86	1/16	+5
LM016XMBL	16×2	New gray	84×44×12max.	61×15.8	2.96×4.86	1/16	+5
LM032L	20×2	Gray	116×39×13max.	83×18.6	3.2×4.85	1/16	+5
LM032XMBL	20×2	New gray	116×37×10.5max.	83×18.6	3.2×4.85	1/16	+5
LM060L	24×2	Gray	116×39×13max.	83×18.6	2.7×4.85	1/16	+5
LM017L	32×2	Gray	174.5×33×13.4max.	141.19×16.75	3.45×4.85	1/16	+5
LM018L	40×2	Gray	182×35.5×13max.	154×15.3	3.2×4.85	1/16	+5
LM018XMBL	40×2	New gray	182×35.5×13max.	154×15.5	3.2×4.85	1/16	+5
LM041L	16×4	Gray	87×60×12max.	61.8×25.2	2.95×4.15	1/16	+5
LM044L	20×4	Gray	98×60×12max.	76×25.2	2.95×4.15	1/16	+5

Character Display LCD Module (with LCD backlight)

LM087LN	16×1	Gray	90×36×14max.	64.5×13.8	3.07×6.56	1/16	+5, (+5)
LM086ALN	16×2	Gray	90×36×14max.	64.5×13.8	2.95×3.8	1/16	+5, (−)
LM093LN	16×2	Gray	90×44×13.8max.	61.0×15.3	2.96×4.86	1/16	+5, (+5)
LM091LN	20×2	Gray	126×39×14max.	83×18.6	3.2×4.85	1/16	+5, (+5)
LM092LN	40×2	Gray	192×35.5×14max.	154×15.3	3.2×4.85	1/16	+5, (+5)

Note: Parentheses indicate V_{LED}.

Segment-Type LCD Module

LM039	16×1	Gray	87×27.5×11max.	64.7×13.3	2.2×6.4	1/4	+5

Power Consumption	Operating Temperature	Storage Temperature	Weight	Controller (on-chip)	Type
10	0~+50	−20~+70	35	HD44780	LM054
10	0~+50	−20~+70	25	HD44780	LM015
10	0~+50	−20~+70	25	HD44780	H2570
10	0~+50	−20~+70	25	HD44780	LM020L
10	0~+50	−20~+70	25	HD44780	LM020XMBL
10	0~+50	−20~+70	40	HD44780	LM070L
25	0~+50	−20~+70	65	HD44780	LM038
10	0~+50	−20~+70	40	HD44780	LM027
10	0~+50	−20~+70	60	HD44780	H2571
10	0~+50	−20~+70	65	HD44780	H2572
15	0~+50	−20~+70	150	HD44780	LM058
15	0~+50	−20~+70	25	HD44780	LM052L
15	0~+50	−20~+70	35	HD44780	LM016L
15	0~+40	−20~+60	35	HD44780	LM016XMBL
15	0~+50	−20~+70	50	HD44780	LM032L
15	0~+40	−20~+60	50	HD44780	LM032XMBL
15	0~+50	−20~+70	60	HD44780	LM060L
15	0~+50	−20~+70	60	HD44780	LM017L
15	0~+50	−20~+70	65	HD44780	LM018L
15	0~+50	−20~+70	65	HD44780	LM018XMBL
15	0~+50	−20~+70	60	HD44780	LM041L
17.5	0~+50	−20~+70	65	HD44780	LM044L

155	0~+50	−20~+70	40	HD44780	LM087LN
150	0~+50	−20~+70	40	HD44780	LM086ALN
405	0~+50	−20~+70	50	HD44780	LM093LN
555	0~+50	−20~+70	70	HD44780	LM091LN
855	0~+50	−20~+70	100	HD44780	LM092LN

1.05	0~+50	−20~+70	20	μPD7225G	LM039

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